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Managing Operational Flexibility in Investment Decisions: The Case of Intel

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The importance of actively managing major corporate investment programs has been recognized by both academics and practitioners. Active management in this case means, first of all, identifying (or creating) operating flexibility provided by a company's options to defer, contract, expand, or otherwise alter an investment program during its life cycle. Having identified or created such options, corporate managers should continuously assess their value and "exercise" the options when the circumstances are right. Analysis has focused heavily on how to *value* operational flexibility, and how to combine it with the NPV of direct cash flows to appraise investment programs more accurately.[1] But there has been far less study of how to *manage* such flexibility. In particular, we know very little about how managers exercise operating flexibility when a change to any one investment program can affect a range of other programs, including those outside the firm. Such interrelated investments have become particularly important in our increasingly "connected" economy, where products and technologies are designed by networks of firms and other organizations. In such a context, deferring, accelerating, or otherwise changing any one program is likely to produce positive returns only if there are effective ways of evaluating and coordinating the implications for a much wider system of investments.

The lack of academic attention to investment coordination mechanisms is surprising. The importance of synergies or complementarity relations among diverse investments is widely recognized, and the ability to realize the benefits of such complementarities is often seen as critical to the success of business strategies involving M&A, joint ventures, and other forms of collaboration, as well as the pursuit of comparative advantage.[2] From a recent and extensive survey reported in this journal, we know a great deal about whether and when companies use particular investment valuation techniques such as NPV, IRR, and real options.[3] But that survey did not pose any questions about how managers and chief financial officers coordinate interrelated investment decisions, what practices they use to do so, and how they evaluate investment in the resulting systems of assets. The research reported in this paper is intended to redress this deficit in the study of the actual investment coordination processes of firms.

Our paper is based on a field study carried out at executive office levels in Intel Corporation during a four-year period. Although it is the world's largest microprocessor company, Intel is nevertheless "part of an ecosystem," as one of its executives commented.[4] A decision to defer, accelerate, or otherwise modify any one investment program—for example, a program designed to create a new generation of microprocessors—is almost certain to have a significant effect on the returns to other investments undertaken within the firm *and* on investments by a host of suppliers, OEM customers, operating systems developers, and software companies externally. We had the opportunity to study how the firm seeks to coordinate such interrelated investments, focusing especially on the mechanism that is used—namely, a "technology roadmap." This inherently tentative and revisable agreement sets out the shared expectations of both the sub-units of Intel and the other firms that design components of a system as to when these components are to be available and how they are to inter-operate technically and economically. We describe the technology roadmap, showing how it integrates with traditional DCF analyses and how it facilitates

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1. See, for example, Lenos Trigeorgis, Ed., *Innovation, Organization and Strategy* (Cambridge: Cambridge University Press, forthcoming), and John McCormack, Raoul LeBlanc, and Craig Heiser, "Turning Risk into Shareholder Wealth in the Petroleum Industry," *Journal of Applied Corporate Finance*, Vol. 15, No. 2 (2003), pp. 67-72.

2. See Paul Milgrom and John Roberts, "Economics of Modern Manufacturing," *American Economic Review*, Vol. 80, No. 3 (1990), pp. 511-528; also, Peter Miller and Ted O'Leary, "Capital Budgeting Practices and Complementarity Relations in the Transition to Modern Manufacture," *Journal of Accounting Research*, Vol. 35, No. 2 (1997), pp. 257-271.

3. John Graham and Campbell Harvey, "How Do CFOs Make Capital Budgeting and Capital Structure Decisions?," *Journal of Applied Corporate Finance*, Vol. 15, No. 1 (2002), pp. 8-23.

4. Unless otherwise indicated, all quotes are from first-hand interviews that we held with senior executives and managers at Intel. Those interviewed included the President and CEO, the CFO, the president of Intel Capital, and vice presidents for technology development, manufacturing, product design, and marketing. In addition, we had access to a range of internal, confidential documents and reports relating to the firm's investment processes. For a more complete treatment of our research procedures, see Peter Miller and Ted O'Leary, "Flexibility, Complementarity Relations and Mechanisms of Investment Coordination," in Trigeorgis (forthcoming), cited earlier.

the exercise of operating flexibility when the investment is in systems of complementary assets both inside and outside the firm. The paper also analyzes the roles of technology roadmaps produced at the industry level under the auspices of the SEMATECH consortium in reinforcing and supporting the coordination of firm-level investments and expectations.[5]

Investing in Systems of Complementary Assets

In the early 1980s, Intel's microprocessor was selected as the logic device to power the original IBM PC that came to dominate the microcomputer market during the rest of the decade. By the early 1990s, Intel held over 70% of the market for PC microprocessors. Using the cash flows and the experience provided by this early success, the company began to stimulate and influence the continued growth of the market, while seeking to maintain its share. According to an analyst relations manager at the company,

[*What] we started figuring out and then implemented in the early 1990s was that, in fact, Intel had moved into a position, in terms of our market share and the particular products that we sold, that to try from a concentrated standpoint to take the other guy's market share from him wasn't going to sustain growth for us… So, we started moving to a mentality that went along these lines: if we can do things that stimulate overall market growth, we will assume that we are going to take our fair share of that growth.*

As a means to pursue this strategy profitably, Intel has sought to outperform competitors in the pace at which it introduces improved fabrication processes, new products, and enhanced manufacturing practices.

For almost two decades, the firm has introduced an improved fabrication process (termed a "process generation") at intervals of roughly three years. At comparable intervals, it has launched at least one new family of microprocessor products and commenced production in several new factories, each of them incorporating improvements in layout, operating policies, and other manufacturing procedures. Intel has experienced significant benefits from coordinating such investments closely, so that they form integrated and mutually reinforcing systems of assets.[6]

The company has learned, for example, that it is better to synchronize process-generation and product launches than to introduce them independently. A new process-generation shrinks the sizes of electronic elements, such as transistors, so that more of them fit on an area of silicon. This increase in transistor density enables more microprocessors of a given size to be fabricated on a silicon wafer, improving the yield level. The clock-speed of the microprocessors also improves because elements and circuits are packed together more tightly and distances of electronic travel are reduced. Both these benefits may be magnified if the process introduction is coordinated with that of new microprocessor products. The gain in transistor density provided by a new process partly offsets the increase in the area of silicon that a new product may require to accommodate extra transistors and circuits. The gain in clock-speed from the new process augments that usually achieved from improvements in product architecture. As the company's CFO told us, the benefits of coordination have been so great that Intel will generally incur any incremental cost necessary to align process and product introductions:

[We] work very hard at the timing, making sure that when a manufacturing process is coming up, the product or products are coming at the same time, so they can marry up…We will take a new process as soon as we can get one, and we will put as many [new] products on the new process as we can, and incur any cost necessary. The return is so great on moving to the next generation that it's the technology that's the "preventer." It's the ability to actually be able to engineer the next process that's the limiter.

There are also synergies from aligning new process introductions with improvements in the designs of Intel's high-volume factories. Each new process-generation involves working to finer tolerances across a greater number of manufacturing steps, often using several equipment types that are new to the industry. But the potential improvements in yield-levels become more difficult to realize as successive process-generations are transferred to high-volume factories, whose personnel have to learn the parameters of increasingly complex systems. To facilitate rapid learning, and faster ramping of a new process in high-volume production, Intel seeks to engineer each generation of high-volume factories so that it more closely copies and reflects the exact layouts, equipment sets, operating procedures, and intervention policies of the development site in which the process was originally devised. The trajectory of improved yield-levels attained during the development stage is thus to be continued in each of the high-volume factories, as though the network as a whole comprised a single manufacturing entity.

This sequence of recurrent investment in systems of assets requires substantial levels of both intra-firm and inter-firm coordination. Developers of Intel's proprietary process-generations collaborate closely with a range of suppliers such as Silicon Valley Group and Nikon that are investing concurrently to design more advanced equip-

5. Comprising key semiconductor firms and representatives of the supplier base, SEMATECH was founded in the U.S. in 1987 in response to intense Japanese competition. The aim was to undertake and sponsor pre-competitive research to restore U.S. competitiveness in semiconductors.

6. Peter Miller and Ted O'Leary (forthcoming), cited earlier.

ment sets and materials. Without corresponding advances by those firms occurring at defined moments, Intel would be unable to operationalize its successive generations of process technologies. The value of advances in microprocessor design would thus be substantially reduced. Also, Intel's microprocessor architects seek to coordinate their designs with those of customers and companies that are investing in complementary products. These include computing-devices by Dell, Compaq, Fujitsu, and others, operating systems by developers such as Microsoft and Linux, data-base management systems, internet infrastructures, and extensive sets of application-software programs. Without these complementary investments being made by other firms, and their timing being carefully and accurately synchronized, the price and cost benefits to Intel from product and process advances would be substantially less.

Using Technology Roadmaps to Coordinate Investments

Because of the extensive complementarities between capital spending proposals, Intel's capital budgeting process restricts the right of sub-units to evaluate individual investments independently. To be approved, an investment proposal must not only promise a positive return; it must also be shown to align with a technology roadmap.[7]

A technology roadmap sets out the shared expectations of the various groups that invest to design components as to when the components will be available, and how they will "inter-operate" technically and economically to achieve system-wide innovation. Typically, it will address each of several future coordination points, defined as yearly or quarterly intervals. The groups involved in preparing it may include sub-units of a firm, as well as suppliers, complementors, and OEM customers. A roadmap is an inherently tentative and flexible agreement, one of whose key roles is to enable design groups to assess and manage the system-level implications of advances, delays, or difficulties in bringing investments in new component designs to fruition.[8] Equally, the expectations reflected in a technology roadmap may require fundamental revision if there are indications of insufficient demand for the end-user products the system of component innovations is expected to create. A roadmap thus provides a mechanism for the dynamic coordination of expectations where there is recurrent intra-firm and inter-firm investment.

Ensuring that individual investment decisions are congruent with the relevant roadmap is a task reserved for Intel's most senior executives. As the CEO observed,

We obviously do ROIs on products and things of that sort, but the core decisions the company makes are basically technology roadmap decisions, driven by a fundamental belief that Moore's Law will continue to be valid, that the purchasing community will continue to buy new [computing devices], and that our main charter is to stay ahead of our competition in that space.[9]

In the sections that follow, we examine the preparation of a technology roadmap and the roles it plays in investment coordination. We consider the different stages in the preparation of a technology roadmap, starting with the coordination of Intel's investment decisions with those in its supplier base.

Coordination with Suppliers' Innovations

Intel depends upon innovations by suppliers of equipment sets and materials to make each of its new process-generations operational, and thus to begin its cycles of complementary investment in process, product, and factory designs. Such innovations by suppliers are regarded as benefiting the industry as a whole. As Intel's CEO told us, the firm collaborates with other semiconductor producers to establish collective design needs and timelines:

[It's] much more economical for our industry to work as a whole to create some base technology…[T]he real intellectual property, the real value added, comes not from creating a stand-alone piece of lithographic equipment, or a stand-alone piece of ion implanter [equipment]; it comes from the integration of those into a total process. So our intellectual property, or trade secrets in this case, comes from the integration. We're very able to work with our competitors in creating the stand-alone pieces.

The coordination of investments by semiconductor firms and their suppliers is facilitated by a technology roadmap that is prepared under the auspices of the SEMATECH consortium. Table 1 shows top-level statistics from such a roadmap. It was prepared by delegates from each of the 13 companies that constitute SEMATECH, including Intel, in collaboration with supplier organizations and government and university laboratories. The roadmap indicated the design requirements for equipment sets and materials at each of five future coordination points during the period 1998 to 2010.

The first step in preparing such a roadmap is to establish expectations among semiconductor firms and suppliers as to when investments in component innovation should come to fruition, thus enabling coordinated results at each

7. In general, only routine replacement decisions are exempt from this latter requirement.

8. However, the costs of revision may increase for individual sub-units and firms as a coordination node approaches, because each will have invested in the expectation of system-wide success.

9. "Moore's Law" is named for Intel co-founder and chairman emeritus Gordon Moore, who noted in 1975 that the semiconductor industry seemed capable of doubling the number of electronic elements on a memory device every 18 months. See Gordon Moore, "Progress in Digital Integrated Electronics," in *International Electron Devices Meeting Technical Digest* (Washington DC: IEEE, 1975).

Table 1 **Required Rates and Directions of Change in Individual Design Variables to Achieve Coordinated and System-Wide Innovation As Specified in *National Technology Roadmap for Semiconductors* (1994)**

	Current	Future				
Technology Node	**1995**	**1998**	**2001**	**2004**	**2007**	**2010**
Suppliers' Innovations in Equipment Sets and Materials:						
Lithography						
Minimum feature size (microns)	0.35	0.25	0.18	0.13	0.10	0.07
Scaling factor per generation		*~0.7*	*~0.7*	*~0.7*	*~0.7*	*~0.7*
Silicon wafers						
Wafer diameter (mm)	200	200	300	300	400	400
Increase (mm)			*100*		*100*	
Advances in Semiconductor Product Designs:						
Memories						
Bits per die (millions)	64	256	1,000	4,000	16,000	64,000
Multiple per generation		*4*	*~4*	*4*	*4*	*4*
Microprocessors						
Transistors per die (millions)	12	28	64	150	350	800
Multiple		*~2.3*	*~2.3*	*~2.3*	*~2.3*	*~2.3*

point or node. Without such shared expectations, investment decisions by individual firms could result in significant capital misallocations, as a SEMATECH report explains:

In semiconductor manufacture, progress tends to occur in discrete generations where all the technology elements need to be in place before a transition can be made to the next generation.[10]

Industry practice is to form such expectations by extrapolating from historical performance levels—specifically, by assuming that the conditions under which Moore's Law was achieved in the past can be made to continue. Thus, as shown in Table 1, electronic feature sizes are expected to continue to be reduced at a rate of 0.7 per coordination point due to investments in innovation by lithography suppliers—and such reduction is expected to be accompanied by certain rates of increase in wafer diameter achieved by silicon suppliers. The coordinated availability of these and other newly developed components is expected to permit semiconductor firms to continue introducing new process-generations, each of which increases the density of bits on a memory product by a factor of four[11] and the number of transistors on a microprocessor die by a multiple of about 2.3. These are the goals that semiconductor firms and their suppliers set out to achieve when planning their capital expenditure programs for research and development, commercialization, and capacity installation.

The second step is to specify the key attributes required of components at each node, and to indicate the technologies whose development and commercialization may meet them. Particularly in the case of later coordination points, the SEMATECH roadmap usually seeks to identify a number of alternative component technologies for each critical area. The aim is to encourage competition among suppliers in the development and commercialization of such alternatives to increase the chances that at least one of them will be available when required. The reward for success is often industry-wide demand for the particular technology for several generations. Without an industry-level process to focus the capital spending decisions of suppliers, a firm such as Intel might be unable to realize the benefits of extensive complementarities among its investments.

By indicating when equipment with a particular capability is likely to be demanded, and identifying promising alternatives for providing it, the SEMATECH roadmap enables options on technology development alternatives to be pursued at an industry level. To take the example of lithographic equipment, the 1994 SEMATECH roadmap envisioned that current technologies would not allow for patterning electronic features of 0.1-micron and below; and as a consequence, the synergies available to semiconductor firms from synchronizing product and process introductions might no longer be available. Three potential replacements were identified—proximity x-ray, e-beam projection, and

10. Semiconductor Industry Association, *National Technology Roadmap for Semiconductors* (San Jose, CA: SIA, 1994, p. 27).

11. This is the rate of increase called for by the so-called Moore's Law—a multiple of four per three years, or two per 18-month period. The industry established a different constant—roughly 2.3 per generation—for processes to fabricate microprocessors.

extreme ultraviolet. Each of them had shown promise in laboratory settings, and each had its proponents among semiconductor firms and suppliers. IBM contended that x-ray machines would be superior, whereas Lucent favored e-beam projection. A third group of suppliers and semiconductor firms, including Intel, proposed development and commercialization of extreme ultraviolet machines.

In 1997, Intel's venture capital unit collaborated with two other semiconductor firms, AMD and Motorola, to accelerate the development of extreme ultraviolet (EUV) lithography. The group invested $250 million in EUV projects at three U.S. Department of Defense laboratories. The intent was to leverage the research and development programs of suppliers committed to EUV. They could defer substantial investment in its commercialization until the laboratories, which had pioneered the early stages of EUV technology, had pilot-tested its ability to pattern electronic features reliably. Also valuable, the initiative enabled Intel, AMD, and Motorola to defer investment in a long-term design and supply relationship with the EUV suppliers until after "proof of concept" had been established.

The third and final step in the roadmap process is for the SEMATECH consortium to reassess the feasibility of projections in frequent update meetings. These meetings may consider arguments from members to alter aspects of the roadmap, such as the effects on the profitability of individual firms or groups of firms of changing the frequency of generational shifts. In 1994, for instance, Intel executives concluded that the firm would benefit from two-year rather than the long-established three-year cycles for introducing new process-generations. However, for Intel to benefit from accelerating its investments in process development would require corresponding alterations on the part of an extensive set of other firms. Suppliers would have to find it feasible and profitable to provide new lithography and other equipment sets a year earlier, for instance. Also, if the costs of such provision were not to fall disproportionately on Intel, other large semiconductor firms would have to be persuaded to shift to two-year cycles. The SEMATECH roadmapping process provides a means for negotiating such shifts in expectations at an industry-wide level, so that one or more firms may exercise operational flexibility in investment decision-making. In this particular instance, consortium members and suppliers agreed to a temporary shift to two-year cycles with respect to the 0.25, 0.18, and 0.13-micron nodes, with a reversion to three-year cycles thereafter. The changes were reflected in a revision of the published technology roadmap.

The SEMATECH technology roadmapping process thus provides a mechanism for coordinating expectations and investments among a set of firms and its supplier base in a key sector of the modern economy—one where there is recurrent, system-wide, and interdependent innovation. In addressing design requirements comprehensively for all core types of components, it reflects the dependence of investment returns to any one specialized firm on close coordination with the design plans of others. By establishing the design lags that are most likely to occur at each of several future nodes, the roadmap seeks to focus the attention of venture capitalists and suppliers on developing alternatives in time, thus protecting the core synergies available to a firm like Intel by coordinated process and product introductions. And by providing a means for renegotiating and updating the roadmap, the SEMATECH process acknowledges the inherently high levels of technological and market uncertainty affecting all parties.

Intra-Firm Coordination

In light of the shared expectations formed with suppliers, Intel managers continue the roadmap preparation procedure inside the firm. They plan several future generations of fabrication processes to coincide with the availability of more advanced equipment sets and materials. The intra-firm roadmap shows when each process-generation is expected to be available for test production and high-volume manufacture, and the key technical changes it is expected to introduce, such as additional transistor density.[12] The data is communicated to Intel's factory design group, so that they may extend the intra-firm roadmap to show the benefits of aligning the introduction of each process-generation with that of more advanced manufacturing practices.

Microprocessor architects extend the intra-firm roadmap still further, by planning the investment timelines of several new product families to coincide with the availability of new fabrication processes. Capital spending on a new microprocessor is typically proposed in stages during four or more years. Early investment is aimed at modeling the enhanced capabilities of the new product, without committing to a precise time-frame for execution or to manufacture on a given process-generation. However, as architects begin to form the product on silicon, returns to additional investment come to depend significantly on coordinating product design closely with that of a particular process-generation. As a vice-president for product development explained, such coordination is especially crucial given that much of the investment takes the form of the architects' time:

If I set my [product] design target on the n^{th} technology [i.e., process-generation], and begin my implementation, begin my

12. Estimates are also made of the capital investment to install a unit of capacity utilizing the new process. Such data are communicated only to senior managers who require it to form capital spending proposals.

layout, I might spend on the order of a hundred engineer-years in creating a physical layout only to find that I have to re-do it for the next generation of [process] technology. So, the order of magnitude of investment, once I get to the point where I just want to instantiate transistors, is on the order of a hundred [engineer]-years. And it might be several times that.

A technology roadmap provides a mechanism for evaluating whether and when such irreversible capital spending is likely to be justified, in light of the investment timelines and expected capabilities of complementary components being developed elsewhere in Intel and within an "ecosystem" of upstream and downstream firms.

During the early 1990s, for instance, Intel executives decided to develop 64-bit microprocessors for higher-end workstation and server markets. The Itanium processor, devised jointly with H-P, was planned as the first instantiation of the new architecture. By consulting the technology roadmap, product architects sought to align their investment in the new product with the availability of a suitable new process-generation. Their initial determination was that Itanium should be introduced within the life-cycle of the 0.25-micron process-generation during 1998 or early 1999. They believed that the product timeline could be made to align with that of the process, and that the size of the product would permit an acceptable die-yield per wafer using transistors of 0.25-micron in length.

The product was intended to be shifted quickly to the newer, 0.18-micron process-generation. Not only was that generation expected to offer a further increment of transistor density, it was also anticipated that it would operate on larger, 300mm silicon wafers, which were being developed by suppliers. The relatively large die-size of the Itanium product would thus be offset by process-generation and other advances, so that acceptable yield levels and returns on investment could be achieved.

However, a revision to the process roadmap in October 1997 led to a change in such expectations. As we learned at the time from a senior engineering manager:

The 0.18-micron process [generation] is in development. And, until recently, the plan was that 0.18-micron would become a 300mm generation [i.e., would operate on larger, 300mm wafers]. And we have just decided that it won't; it will stay 200mm. 300mm will shift out a generation. The reason is we were too fast. We have outrun the availability of [materials and] equipment.

A key role of a technology roadmap is to convey such shifts in expectations to relevant parties throughout a network that may extend from suppliers through to various sub-units of a firm and the downstream producers of complementary products. The timing of information exchanges is crucial, so that decisions to defer or otherwise modify an investment program may be taken before large and irreversible capital commitments have been made. Influenced by a mix of factors, including the delayed availability of larger wafers, the large die-size of the product, and difficulties in perfecting its instruction set, Intel's executives decided against building the Itanium product on the 0.25-micron manufacturing process. Originally planned for 1997, the product's launch was deferred to May 2001, and production on 300mm wafers did not begin until February 2002.

Coordination with Customers' and Complementors' Designs

In seeking to align its plans with those of downstream firms, Intel shares elements of its technology roadmap with them, on a reciprocal basis and under non-disclosure agreements, for a period of up to two years prior to the planned product launch dates. As the CEO explained to us:

[About] the time that we are freezing on the product that we want to design, and looking forward to two years of design for its introduction, we have to take that to the software community and say, "Here are the 70 new instructions that this processor has which will make [for example] your multi-media applications better," under a non-disclosure agreement…[We take that data to] the software community, and the hardware community, and you also get the [technical analyst] people who make a living out of following our industry…telling them "this is the direction that Intel's going in"...It's a managing, a partial managing, of the resources of the virtual company, the virtual company being Intel plus a lot of other people bringing product to the market.

The sharing of roadmap data with technical analysts is critical to the coordination of investments at the inter-firm level. Bringing about complementary investments may depend on whether the parties have means of verifying the reliability of each others' claims and promises. In particular, smaller software vendors may be unwilling to invest if they lack confidence in the claims that Intel makes for its future microprocessor generations.

Whereas SEMATECH helps to organize and validate information exchanges between semiconductor firms and suppliers, technical analysts play a similar role with respect to downstream, software development firms. During the early 1990s, Intel began to use the services of a small number of such technical analysts—among them, Micro Design Resources (MDR)—in building the confidence of software developers and other downstream firms. In an interview during 1998, the president of MDR told us:

The view we have come to have is that, in some way, we are the community organizer. We have brought together this community of people who care about microprocessors. And we collect infor-

mation from various members of that community, and then disseminate it to all of them, and then we get them all together for meetings where they can all talk to each other. And so, I think you could say the biggest-picture thing we do is to provide a focal point and opportunities for interaction in that community.

Intel would provide MDR with advance information on next-generation microprocessors, on the condition that certain proprietary data should not be disclosed. The analyst firm would then provide expert appraisals of the product's capability in its newsletters, which are purchased by firms throughout the industry and by stock analysts. The analyst's income stream depends on the perceived objectivity and accuracy of its appraisals. At the same time, Intel's willingness to continue sharing data with the analyst depends on the latter's adherence to evaluations that, while they may be critical, nevertheless conform to non-disclosure provisions with respect to proprietary data.[13]

Implications and Conclusions

We have documented through an intensive field study how a major firm in the microprocessor industry, Intel Corporation, exercises operational flexibility in investment decision-making.

A key finding is that a system of parallel and interacting investments, rather than an individual investment program, may often be the relevant unit of analysis and decision for managers. In the case of Intel, the returns available from accelerating or deferring an individual investment program depend crucially on whether corresponding change can be effected in other, mutually reinforcing sets of investments. This is because of synergies or complementarities between capital spending programs involving, for example, investments in new process-generations, new microprocessor products, and more advanced factory designs. Intel executives seek to identify the relevant set of investments, both within the firm and among an extensive set of external firms and organizations, and to ensure the coordinated development of the resulting system of assets. Our research thus supports the continued extension of theoretical analyses and real-options modeling to incorporate interdependencies among investment programs at intra- and inter-firm levels. This is in contrast to a well-established approach of valuing only the flexibility and the options available *within* an individual investment program, whether this be an R&D project, the extraction of resources from an oil well or a mine, or the installation of novel technologies for supply-chain management.

If there are extensive complementarities among investment programs, it is likely that operational flexibility will need to be managed and negotiated at the level of an overall system of assets to achieve optimal results. To do so requires coordination mechanisms whose significance has been largely overlooked in the literature. As we demonstrate, Intel's ability to exercise flexibility in investment requires a technology roadmap whose preparation and frequent revision depends upon an extensive network of collaborators comprising sub-units of Intel, upstream and downstream firms and organizations, industry consortia, and key firms of technical analysts. However, little is known about how adjustments and shifts in expectations and in investment may be effected in other industrial contexts. For instance, informal evidence suggests that companies have found it difficult to coordinate investments in the development of advanced telecommunications, with negative returns to investment as a consequence.

Survey researchers have provided an extensive overview of the investment appraisal practices that firms claim to use. It is important now to undertake additional surveys and field research on issues of investment coordination and the practices that sustain it. The aim should be to arrive at a broad, inter-industry perspective on whether complementarities are analyzed formally as part of the capital budgeting process, what mechanisms are employed to do so, and how operational flexibility is managed in a variety of contexts.

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13. Peter Miller and Ted O'Leary, *Value Reporting and the Information Ecosystem* (London: PWC, 2000).

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