ID

0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9

Undergraduate Computer Architecture
Quiz Example

Instructions: Fill in your student ID and sign below. All answers must be provided on this page; answers outside the form will be ignored. Questions with ♣ may have zero, one, or more correct answers. The use of calculators and consultation materials is not allowed. This is an individual quiz.

Signature :

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Question 1 If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

- [A] It is not possible to determine the answer with the given information.
- [B] It is not possible to achieve the desired performance by optimizing only the multiplication instructions.
- [C] 3x faster.
- [D] 12x faster.
- [E] 6x faster.

Question 2 How many bits are needed to address a register in the RISC-V register file?

[16]   [8]   [6]   [5]   [32]

Question 3 Convert the number 0xc0980000 from single-precision floating-point representation to decimal.

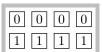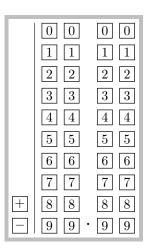|	0	0		0	0
	1	1		1	1
	2	2		2	2
	3	3		3	3
	4	4		4	4
	5	5		5	5
	6	6		6	6
	7	7		7	7
+	8	8		8	8
−	9	9	·	9	9

Question 4 Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 512 bytes capacity. If the cache has blocks of 4 words, how many bits are required for the index field in the address division?

[1] [2] [3] [4] [5] [6] [7] [8] [9]

For the next question, considering a multi-cycle divider, divide 13 by 5, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.

Question 5
Remainder, Cycle 3

0	0	0	0
1	1	1	1

Question 6 Implement the int strlen(const char* str) function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

[0] [1] [2] [3] [4] [5]

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Signature :

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ID

0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9

Question 1 If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

A. 6x faster.

B. 3x faster.

C. It is not possible to determine the answer with the given information.

D. It is not possible to achieve the desired performance by optimizing only the multiplication instructions.

E. 12x faster.

Question 2 How many bits are needed to address a register in the RISC-V register file?

16   6   5   32   8

Question 3 Convert the number 0xc0980000 from single-precision floating-point representation to decimal.

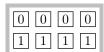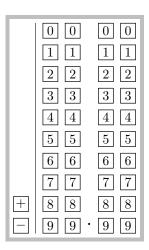|				
	0	0	0	0
	1	1	1	1
	2	2	2	2
	3	3	3	3
	4	4	4	4
	5	5	5	5
	6	6	6	6
	7	7	7	7
+	8	8	8	8
−	9	9 ·	9	9

Question 4 Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 1024 bytes capacity. If the cache has blocks of 16 words, how many bits are required for the index field in the address division?

1 2 3 4 5 6 7 8 9

For the next question, considering a multi-cycle divider, divide 12 by 4, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.

Question 5
Remainder, Cycle 3

0	0	0	0
1	1	1	1

Question 6 Implement the `int strlen(const char* str)` function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

0 1 2 3 4 5

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Undergraduate Computer Architecture
Quiz Example

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Signature :

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ID

0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9

Question 1   If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

- A 3x faster.
- B It is not possible to achieve the desired performance by optimizing only the multiplication instructions.
- C 12x faster.
- D 6x faster.
- E It is not possible to determine the answer with the given information.

Question 2   How many bits are needed to address a register in the RISC-V register file?

| 8 | | 32 | | 5 | | 16 | | 6 |

Question 3   Convert the number 0xc0980000 from single-precision floating-point representation to decimal.

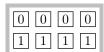| | 0 | 0 | | 0 | 0 |
	1	1		1	1
	2	2		2	2
	3	3		3	3
	4	4		4	4
	5	5		5	5
	6	6		6	6
	7	7		7	7
+	8	8		8	8
−	9	9	·	9	9

Question 4   Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 128 bytes capacity. If the cache has blocks of 8 words, how many bits are required for the index field in the address division?

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

For the next question, considering a multi-cycle divider, divide 14 by 5, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.
Question 5
Remainder, Cycle 3

| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Question 6   Implement the `int strlen(const char* str)` function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

| 0 | 1 | 2 | 3 | 4 | 5 |

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Undergraduate Computer Architecture

Quiz Example

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ID

0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9

Question 1 If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

- [A] 3x faster.
- [B] It is not possible to achieve the desired performance by optimizing only the multiplication instructions.
- [C] It is not possible to determine the answer with the given information.
- [D] 12x faster.
- [E] 6x faster.

Question 2 How many bits are needed to address a register in the RISC-V register file?

| 32 | | 6 | | 5 | | 16 | | 8 |

Question 3 Convert the number 0xc0980000 from single-precision floating-point representation to decimal.

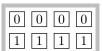| | 0 | 0 | | 0 | 0 |
	1	1		1	1
	2	2		2	2
	3	3		3	3
	4	4		4	4
	5	5		5	5
	6	6		6	6
	7	7		7	7
+	8	8		8	8
−	9	9	·	9	9

Question 4 Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 64 bytes capacity. If the cache has blocks of 4 words, how many bits are required for the index field in the address division?
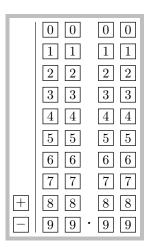
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

For the next question, considering a multi-cycle divider, divide 13 by 4, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.

Question 5
Remainder, Cycle 3

| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Question 6 Implement the `int strlen(const char* str)` function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

| 0 | 1 | 2 | 3 | 4 | 5 |

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Undergraduate Computer Architecture
Quiz Example

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Signature :

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ID

0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9

Question 1   If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

- A   3x faster.
- B   It is not possible to determine the answer with the given information.
- C   It is not possible to achieve the desired performance by optimizing only the multiplication instructions.
- D   6x faster.
- E   12x faster.

Question 2   How many bits are needed to address a register in the RISC-V register file?

| 6 | | 8 | | 16 | | 5 | | 32 |

Question 3   Convert the number 0xc0980000 from single-precision floating-point representation to decimal.

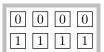| | 0 | 0 | | 0 | 0 |
	1	1		1	1
	2	2		2	2
	3	3		3	3
	4	4		4	4
	5	5		5	5
	6	6		6	6
	7	7		7	7
+	8	8		8	8
−	9	9	·	9	9

Question 4   Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 128 bytes capacity. If the cache has blocks of 2 words, how many bits are required for the index field in the address division?
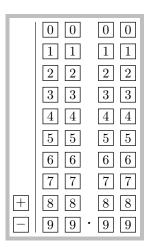
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

For the next question, considering a multi-cycle divider, divide 14 by 5, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.

Question 5
Remainder, Cycle 3

| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Question 6   Implement the `int strlen(const char* str)` function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

| 0 | 1 | 2 | 3 | 4 | 5 |

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ID

0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9

Question 1   If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

- [A] It is not possible to determine the answer with the given information.
- [B] 3x faster.
- [C] It is not possible to achieve the desired performance by optimizing only the multiplication instructions.
- [D] 6x faster.
- [E] 12x faster.

Question 2   How many bits are needed to address a register in the RISC-V register file?

| 6 | | 16 | | 32 | | 8 | | 5 |

Question 3   Convert the number 0xc0980000 from single-precision floating-point representation to decimal.

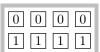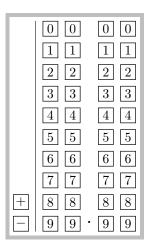| | 0 | 0 | | 0 | 0 |
	1	1		1	1
	2	2		2	2
	3	3		3	3
	4	4		4	4
	5	5		5	5
	6	6		6	6
	7	7		7	7
+	8	8		8	8
−	9	9	·	9	9

Question 4   Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 64 bytes capacity. If the cache has blocks of 2 words, how many bits are required for the index field in the address division?

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

For the next question, considering a multi-cycle divider, divide 12 by 5, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.

Question 5
Remainder, Cycle 3

| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Question 6   Implement the `int strlen(const char* str)` function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

| 0 | 1 | 2 | 3 | 4 | 5 |

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ID

Quiz Example

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Question 1   If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

- A 12x faster.
- B It is not possible to determine the answer with the given information.
- C 6x faster.
- D 3x faster.
- E It is not possible to achieve the desired performance by optimizing only the multiplication instructions.

Question 2   How many bits are needed to address a register in the RISC-V register file?

5   6   16   32   8

Question 3   Convert the number 0xc0980000 from single-precision floating-point representation to decimal.
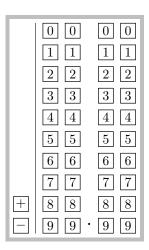
Question 4   Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 1024 bytes capacity. If the cache has blocks of 8 words, how many bits are required for the index field in the address division?

1 2 3 4 5 6 7 8 9

For the next question, considering a multi-cycle divider, divide 13 by 3, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.

Question 5
Remainder, Cycle 3

| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Question 6   Implement the `int strlen(const char* str)` function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

0 1 2 3 4 5

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ID

0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9

Question 1   If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

A 6x faster.

B 12x faster.

C It is not possible to determine the answer with the given information.

D It is not possible to achieve the desired performance by optimizing only the multiplication instructions.

E 3x faster.

Question 2   How many bits are needed to address a register in the RISC-V register file?

6   16   5   32   8

Question 3   Convert the number 0xc0980000 from single-precision floating-point representation to decimal.

	0	0		0	0
	1	1		1	1
	2	2		2	2
	3	3		3	3
	4	4		4	4
	5	5		5	5
	6	6		6	6
	7	7		7	7
+	8	8		8	8
−	9	9	·	9	9

Question 4   Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 256 bytes capacity. If the cache has blocks of 16 words, how many bits are required for the index field in the address division?

1 2 3 4 5 6 7 8 9

For the next question, considering a multi-cycle divider, divide 14 by 5, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.
Question 5
Remainder, Cycle 3

| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Question 6   Implement the `int strlen(const char* str)` function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

0 1 2 3 4 5

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Quiz Example

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ID

0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9

Question 1   If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

- A 6x faster.
- B 3x faster.
- C 12x faster.
- D It is not possible to achieve the desired performance by optimizing only the multiplication instructions.
- E It is not possible to determine the answer with the given information.

Question 2   How many bits are needed to address a register in the RISC-V register file?

| 8 | | 32 | | 6 | | 5 | | 16 |

Question 3   Convert the number 0xc0980000 from single-precision floating-point representation to decimal.

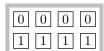| | 0 | 0 | | 0 | 0 |
	1	1		1	1
	2	2		2	2
	3	3		3	3
	4	4		4	4
	5	5		5	5
	6	6		6	6
	7	7		7	7
+	8	8		8	8
−	9	9	·	9	9

Question 4   Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 1024 bytes capacity. If the cache has blocks of 32 words, how many bits are required for the index field in the address division?

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

For the next question, considering a multi-cycle divider, divide 14 by 3, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.

Question 5

Remainder, Cycle 3

| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Question 6   Implement the `int strlen(const char* str)` function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

| 0 | 1 | 2 | 3 | 4 | 5 |

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ID

0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9

Question 1   If a program spends 60% of its time executing multiplication instructions, how much faster do the multiplication instructions need to be for the program to run 2 times faster?

- [A] It is not possible to achieve the desired performance by optimizing only the multiplication instructions.
- [B] 3x faster.
- [C] 6x faster.
- [D] 12x faster.
- [E] It is not possible to determine the answer with the given information.

Question 2   How many bits are needed to address a register in the RISC-V register file?

| 6 | | 8 | | 32 | | 16 | | 5 |

Question 3   Convert the number 0xc0980000 from single-precision floating-point representation to decimal.

	0	0		0	0
	1	1		1	1
	2	2		2	2
	3	3		3	3
	4	4		4	4
	5	5		5	5
	6	6		6	6
	7	7		7	7
+	8	8		8	8
−	9	9	·	9	9

Question 4   Consider an architecture with 32-bit words and a direct-mapped L1 data cache with 32 bytes capacity. If the cache has blocks of 2 words, how many bits are required for the index field in the address division?

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

For the next question, considering a multi-cycle divider, divide 13 by 4, indicating the value of the specified register at the end of the clock cycle. Assume that the inputs and results are represented with 4 bits, and give your answer in binary.

Question 5
Remainder, Cycle 3

| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Question 6   Implement the `int strlen(const char* str)` function in RISC-V assembly, following all necessary ABI conventions and without using pseudo-instructions. The function should return the length of the string.

| 0 | 1 | 2 | 3 | 4 | 5 |

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