A Carrier-Based PWM Method for Three-Phase Four-Leg Voltage Source Converters

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***Abstract*—In this paper a voltage modulation method based on a triangular carrier wave for the three-phase four-leg voltage source converter is described. The four-leg converter can produce three output voltages independently with one additional leg. The proposed modulation method for the four-leg converter can be implemented with a single carrier by a simple but useful "offset voltage" concept. The method is equivalent to the so called three-dimensional space vector PWM method, but its implementation is much easier. The maximum magnitude of the balanced three-phase voltage and the maximum magnitude of zero sequence voltage, which can be synthesized simultaneously, are derived. The feasibility of the proposed modulation technique is verified by computer simulation and experimental results. These results show that a proposed carrier-based pulsewidth modulation (PWM) technique can be easily implemented without conventional computational burden.**

***Index Terms*—Carrier-based PWM, offset voltage, three-dimensional space vector PWM, three-phase four-leg converter, zero sequence voltage.**

I. Introduction

A ZERO sequence voltage and current appears due to an unbalanced load or source in three-phase four-wire systems. Several topologies for providing a neutral connection and controlling the zero sequence voltage have been presented [1]–[3]. A three-phase voltage source converter(VSC) with a neutral leg, that is, a four-leg converter which is able to provide zero sequence voltage, so as to handle the neutral current caused by the unbalanced load or source was proposed [1], [4]–[6]. Also, several modulation methods for the four-leg converter have been suggested [4]–[7]. In [4] feed-forward sinusoidal pulse width modulation (PWM) and three-level hysteresis current controlled PWM schemes were proposed, but none of them optimally exploits zero sequence voltages provided by the extra leg. In [5]–[7], the sixteen voltage vectors generated by the four-leg converter were considered in three-dimensional (3-D) space. By extending the two-dimensional space vector PWM (2-D SVPWM) concept, the so called 3-D SVPWM (3-D SVPWM) achieved the full utilization of converter capability such as maximum output voltage at given dc link voltage and minimum output harmonics current at given switching frequency. But the implementation method needs quite a bit of digital logic and computational power, and it might be a software and hardware burden even for recent digital signal processor (DSP) systems.

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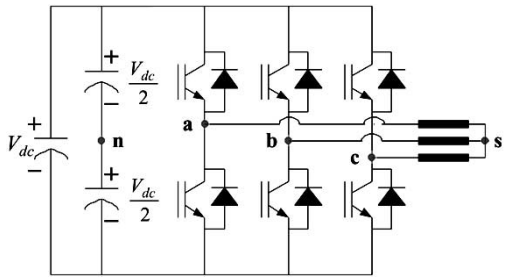

Fig. 1. Three-phase three-leg converter.

Another attempt was made to extend the 2-D SVPWM to a four-leg converter described in [8], where the 16 voltage vectors are decomposed to two groups according to the polarity of the zero sequence voltage. At each group the 2-D SVPWM was applied to synthesize the line to neutral voltages. However it does not guarantee the full utilization of converter capability.

It has been shown that the 2-D SVPWM can be easily implemented by properly manipulating the offset voltage, which is a kind of zero sequence voltage and does not appear in output phase voltage in the three-phase three-leg converter with an isolated neutral point [9]–[12]. The pole voltage references, which have been generated by adding an appropriate offset voltage to the phase voltage references of the three-phase three-leg converter, are compared with a triangular carrier wave like the sine-triangular PWM method. It is equivalent to the 2-D SVPWM but is simple to implement. In [12] it has been shown that various 2-D SVPWM methods such as continuous and discontinuous SVPWM can be implemented by simply changing offset voltages. This paper presents a simple three-phase four-leg PWM method based on the triangular carrier wave PWM method by extending offset voltage concepts to the four-leg converter. It is proved that the proposed method is equivalent to the symmetrically aligned-class I 3-D SVPWM of [7]. In this paper the magnitude of simultaneously available maximum d-q-o voltages (α, β, γ voltages in [7]) is also derived at the given dc link voltage, and the proposed method is verified by simulation and experimental results.

II. Space Vector PWM Method Using Offset Voltage in Three-Phase Three-LEG Voltage Source Converter

Fig. 1 shows a well-known three-phase three-leg voltage source converter with an isolated neutral point. Numerous studies about the PWM scheme for this traditional converter have been published [9]–[14]. From their results, it is widely

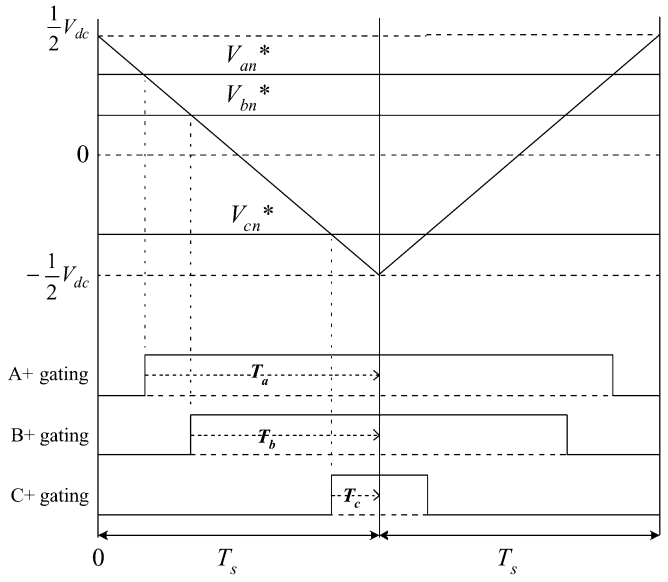

Fig. 2. Actual implementation of the SVPWM in a three-phase three-leg VSC.

known that the addition of a common offset voltage (which is a kind of zero sequence voltage), V_{sn} selected as (1) to the three-phase voltage reference in (2) locates the nonzero voltage vectors(effective voltage vector) in the center of a sampling period [9]–[12]. It provides an optimum switching sequence by which it has some advantages, such as lower harmonic currents and higher available modulation index, compared with the sinusoidal PWM (SPWM) method

$$V_{sn}^* = -\frac{\max(V_{as}^*, V_{bs}^*, V_{cs}^*) + \min(V_{as}^*, V_{bs}^*, V_{cs}^*)}{2} \quad (1)$$

where the three-phase voltage references are given as V_{as}^*, V_{bs}^*, and V_{cs}^*, respectively

$$\begin{aligned} V_{an}^* &= V_{as}^* + V_{sn}^* \\ V_{bn}^* &= V_{bs}^* + V_{sn}^* \\ V_{cn}^* &= V_{cs}^* + V_{sn}^*. \end{aligned} \quad (2)$$

The practical implementation method of the space vector PWM (SVPWM) with a triangular carrier wave was proposed using the offset voltage concept [12]. The switch states of each leg are determined by comparison between the determined pole voltages $(V_{an}^*, V_{bn}^*, V_{cn}^*)$ in (2) and a triangular carrier wave, and then naturally the optimum switching sequence is obtained as shown in Fig. 2.

III. Space Vector PWM Method Using Offset Voltage in Four-Leg VSC

A three-phase four-leg voltage source converter was presented and a 3-D SVPWM method for the four-leg voltage source converter was proposed [6], [7]. The analysis and comparison with switching sequences such as rising edge, falling edge, symmetrically aligned and alternative sequence has been done as was done for the three-leg VSC. From the results, the symmetrically aligned switching sequence is selected to be a good compromise between the switching losses and harmonic contents. However, the 3-D SVPWM of the three-phase four-leg system requires some complicated procedures such as a sector decision based on the projections of the reference vector on the dq plane, adjacent voltage vectors selection based on the polarities of line to neutral voltage references, a duty-ratio calculation of the voltage vectors using the predetermined 24 matrices, and finally the on-time calculation of each switch based on the arrangements of nonzero vectors [7]. Hence the implementation of the 3-D SVPWM needs quite a bit of digital logic and computational power, and it might be a software and hardware burden even for recent digital signal processor (DSP) systems.

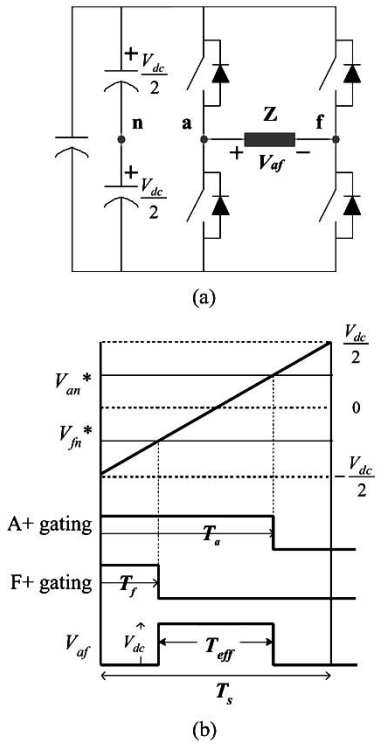

Fig. 3. Full bridge converter and PWM implementation: (a) full bridge converter (two-leg VSC) and (b) relationship between output voltage and pole voltages.

The additional leg of the four-leg converter in the three-phase four-wire system provides a system not only a neutral connection but also the controllability of a zero sequence voltage. By using an offset voltage concept, a zero switching vector can be located at desired timing, so that the symmetrically aligned sequencing scheme can be achieved. Therefore, the PWM strategy using an offset voltage concept could be applied to the three-phase four-leg VSC. For an extension of an offset voltage concept in a three-leg VSC to a four-leg VSC, a full-bridge type VSC, which is a two-leg VSC, is initially selected as a platform for the explanation of the concept of the offset voltage.

A. Single Phase Two-Leg Voltage Source Converter (Full Bridge Type VSC)

A full-bridge type PWM converter in Fig. 3(a) has two legs for generating a single phase output voltage, V_{af}, that ranges from $-V_{\rm dc}$ to $V_{\rm dc}$. The output voltage can be expressed as (3) using the pole voltages (V_{fn}, V_{an})

$$V_{af} = V_{an} - V_{fn}. \quad (3)$$

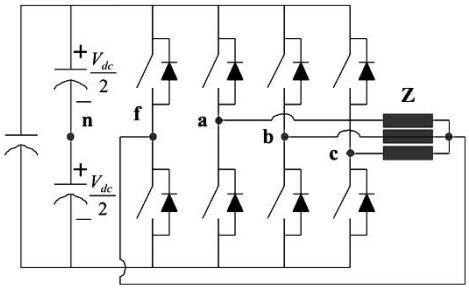

Fig. 4. Four-leg voltage source converter.

The pole voltages are physically limited by the dc bus voltage, $V_{\rm dc}$ as

$$-V_{\rm dc}/2 \le V_{an} \le V_{\rm dc}/2 \tag{4}$$
$$-V_{\rm dc}/2 \le V_{fn} \le V_{\rm dc}/2. \tag{5}$$

There exist various pole voltage ordered pairs, (V_{fn}, V_{an}), satisfying the conditions by (3)–(5). If the pole voltage pairs are selected as (V_{fn}, V_{an}), the ON time of the upper switch can be expressed as (6)–(7) as shown in Fig. 3(b), when a fixed frequency carrier-based PWM is employed with carrier frequency being $1/(2{\rm T_s})$

$$T_a = \frac{T_s}{2} + \frac{V_{an}}{V_{\rm dc}} T_s \tag{6}$$
$$T_f = \frac{T_s}{2} + \frac{V_{fn}}{V_{\rm dc}} T_s. \tag{7}$$

As shown in Fig. 3(b), there exists an additional degree of freedom by which "$T_{\rm eff}$" can be relocated anywhere within the sampling interval by varying V_{fn} while keeping the difference of the pole voltages same, and the output voltage, V_{af}, is always same. In this paper, V_{fn} is referred to as the "offset voltage" in the four-leg VSC system, by which a nonzero voltage vector can be located at desired timing in a sampling period.

B. Three-Phase Four-Leg Voltage Source Converter

Fig. 4 shows a three-phase four-leg VSC, which makes three line to neutral output voltages, that is, V_{af}, V_{bf} and V_{cf}, independently with a constraint by (8), where "f" is the neutral point of load in the three-phase four wire system and is connected to the middle point of an additional leg of the three-phase four-leg VSC. The respective output line to the neutral voltage can be rewritten as (9) by using the respective pole voltage and the common offset voltage "V_{fn}" such as a single phase two-leg or three-phase three-leg VSC

$$-V_{\rm dc} \le V_{af}, V_{bf}, V_{cf} \le V_{dc} \tag{8}$$
$$\begin{aligned} V_{af} &= V_{an} - V_{fn} \\ V_{bf} &= V_{bn} - V_{fn}. \\ V_{cf} &= V_{cn} - V_{fn} \end{aligned} \tag{9}$$

The offset voltage "V_{fn}" can be manipulated actively by control of the gating signal of the additional leg of the three-phase four-leg VSC, which is quite different from three-phase three-leg VSC. If the offset voltage is fixed as a certain value, the respective pole voltages can be calculated as

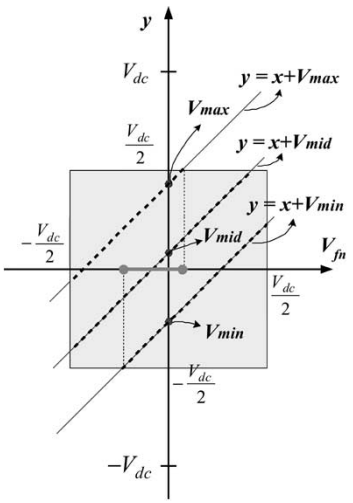

Fig. 5. Available region of the offset voltage, V_{fn}.

$$\begin{aligned} V_{an} &= V_{af} + V_{fn} \\ V_{bn} &= V_{bf} + V_{fn} \\ V_{cn} &= V_{cf} + V_{fn}. \end{aligned} \tag{10}$$

The available combinations of the respective pole voltage and offset voltage can be represented as three ordered pairs $(V_{fn}, V_{an}), (V_{fn}, V_{bn})$, and (V_{fn}, V_{cn}) in rectangular coordinates, and they must also exist within a square, which is centered at origin and has four sides of length $V_{\rm dc}$ as shown in Fig.5, since all pole voltages and offset voltage have constraints as (11)–(12) caused by the dc bus voltage

$$-V_{\rm dc}/2 \le V_{an}, V_{bn}, V_{cn} \le V_{\rm dc}/2 \tag{11}$$
$$-V_{\rm dc}/2 \le V_{fn} \le V_{\rm dc}/2. \tag{12}$$

The respective pole voltage can be substituted by y_1, y_2, and y_3, as can the offset voltage by x. Also, the pole voltage equations in (10) can be rewritten as (13), where they correspond to equations of straight lines with unity slope in x-y coordinates

$$\begin{aligned} y_1 &= x + V_{af} \\ y_2 &= x + V_{bf} \\ y_3 &= x + V_{cf}. \end{aligned} \tag{13}$$

The line to neutral voltages become y-intercepts of respective straight lines, and the ordered pairs should be selected on the dotted line within the square, as shown in Fig. 5. However, the region where the offset voltage is commonly available, is restricted by condition (14), so that this region can be indicated as a solid line on the x-axis, as shown in Fig. 5

$$-\frac{V_{\rm dc}}{2} - V_{\rm min} \le V_{fn} \le \frac{V_{\rm dc}}{2} - V_{\rm max} \tag{14}$$

where $V_{\rm min} = \min(V_{af}, V_{bf}, V_{cf}), V_{\rm mid} = {\rm mid}(V_{af}, V_{bf}, V_{cf}), V_{\rm max} = \max(V_{af}, V_{bf}, V_{cf})$. '$\min(V_{af}, V_{bf}, V_{cf})$' stands for a function which selects the minimum value among $V_{af}, V_{bf}, V_{cf}, {\rm mid}(V_{af}, V_{bf}, V_{cf})$

for the medium value among V_{af}, V_{bf}, V_{cf}, and $\max(V_{af}, V_{bf}, V_{cf})$ for the maximum value among V_{af}, V_{bf}, V_{cf}.

If the difference between a maximum and a minimum value of the line to neutral voltage becomes larger and equals the dc bus voltage, then the available offset voltage is fixed onto one point. Hence the independently achievable output line to neutral voltages of the four-leg VSC would be limited by

$$V_{\max} - V_{\min} \le V_{dc}. \tag{15}$$

The optimum switching sequence, which is equivalent to the symmetrically aligned-class I 3-D SVPWM in [7], can be achieved by selecting the offset voltage as given in

$$V_{fn} = \begin{cases} -\frac{V_{\max}}{2}, & V_{\min} > 0 \\ -\frac{V_{\min}}{2}, & V_{\max} < 0 \\ -\frac{V_{\max}+V_{\min}}{2}, & \text{Otherwise} \end{cases}, \quad \text{that is}$$

$$V_{fn} = \operatorname{mid}\left(-\frac{V_{\max}}{2}, -\frac{V_{\min}}{2}, -\frac{V_{\max}+V_{\min}}{2}\right) \tag{16}$$

and the respective pole voltages are naturally determined by (10). Therefore, ON-times of the upper switch of respective legs can be obtained as (17), and can be simply implemented with a triangular carrier and the offset voltage calculation as shown in the block diagram of Fig. 6

$$\begin{aligned} T_a &= \frac{T_s}{2} + \frac{V_{an}}{V_{\rm dc}} T_s \\ T_b &= \frac{T_s}{2} + \frac{V_{bn}}{V_{\rm dc}} T_s \\ T_c &= \frac{T_s}{2} + \frac{V_{cn}}{V_{\rm dc}} T_s \\ T_f &= \frac{T_s}{2} + \frac{V_{fn}}{V_{\rm dc}} T_s. \end{aligned} \tag{17}$$

By this proposed simple triangular carrier based PWM method, the nonzero voltage vector can be centered during the sampling period identically to the symmetrically aligned-class I 3-D SVPWM, which reveals the lowest harmonics at a given switching frequency [7]. The equivalence of the proposed carrier based PWM to the symmetrically aligned-class I 3-D SVPWM is proved analytically in the Appendix.

IV. Maximum Achievable Voltage in Three-Phase Four-Leg VSC

The available range of the line to line voltage in a four-leg converter is determined by (15). In this section, the range of available zero sequence voltage, $V_o(t)$, of the three-phase four-leg VSC, simultaneously producing the maximum balanced voltages in the d-q reference frame is derived. Balanced three-phase voltages can be expressed as

$$\begin{aligned} V_a &= A\cos(\omega t) \\ V_b &= A\cos\left(\omega t - \frac{2\pi}{3}\right) \\ V_c &= A\cos\left(\omega t + \frac{2\pi}{3}\right). \end{aligned} \tag{18}$$

The line to neutral voltage including the zero sequence voltage can be written as

$$\begin{aligned} V_{af} &= A\cos(\omega t) + V_o(t) \\ V_{bf} &= A\cos\left(\omega t - \frac{2\pi}{3}\right) + V_o(t) \\ V_{cf} &= A\cos\left(\omega t + \frac{2\pi}{3}\right) + V_o(t) \end{aligned} \tag{19}$$

where the zero sequence voltage, $V_o(t)$, can be a constant or an arbitrary function of time.

Due to the constraint given by (15), the maximum value of the magnitude of the balanced voltage, $A_{\max}$, can be derived as

$$A_{\max} = \frac{V_{\rm dc}}{\sqrt{3}}. \tag{20}$$

The maximum magnitude of the zero sequence voltage can be derived by the following procedures. First, the maximum magnitude of the offset voltage, V_{fno}, with no zero sequence voltage and maximum magnitude of balanced voltage given by (21) would be calculated

$$\begin{aligned} V_{af}^* &= A_{\max}\cos(\omega t) \\ V_{bf}^* &= A_{\max}\cos\left(\omega t - \frac{2\pi}{3}\right) \\ V_{cf}^* &= A_{\max}\cos\left(\omega t + \frac{2\pi}{3}\right) \\ V_o &= 0. \end{aligned} \tag{21}$$

In this case the offset voltage satisfies

$$-\frac{A_{\max}}{4} \le V_{fno} \le \frac{A_{\max}}{4} \tag{22}$$

where

$$\frac{A_{\max}}{4} = \frac{V_{\rm dc}}{4\sqrt{3}}.$$

The available range of the offset voltage, which is controlled by an additional leg of the three-phase four-leg VSC, is given in (12). Hence, the available margin of the offset voltage for zero sequence voltage is the difference between the region by (22) and the region by (12). The zero sequence voltage with the simultaneous generation of maximum magnitude of the balanced three-phase voltage should always satisfy

$$|V_o| \le \frac{V_{\rm dc}}{2} - \frac{V_{\rm dc}}{4\sqrt{3}} = V_{o\max} \approx 0.3557 V_{\rm dc}. \tag{23}$$

In the three-phase four-leg VSC, if the balanced three-phase voltages, whose magnitude is A less than $A_{\max}$, are synthesized, then the larger V_o can be generated as

$$|V_o| \le \frac{V_{\rm dc}}{2} - \frac{A}{4}. \tag{24}$$

Therefore, without overmodulation, the maximum magnitude of the line to neutral voltage can be synthesized by the proposed

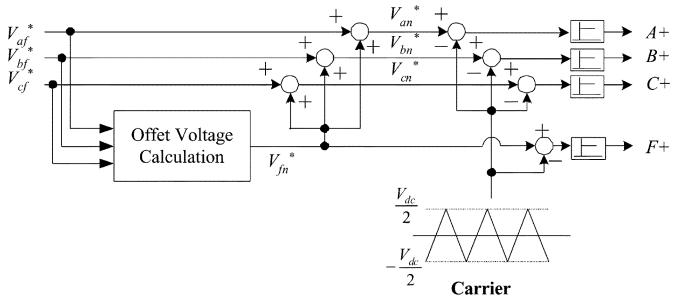

Fig. 6. Proposed PWM scheme for three-phase four-leg VSC.

TABLE I
PARAMETERS OF THE SYSTEM USED IN SIMULATION AND EXPERIMENT

Resistance; R	40 O
Inductance; L	50 mH
Carrier frequency; $(2T_s)^{-1}$	5kHz
DC bus voltage; V_{dc}	300V

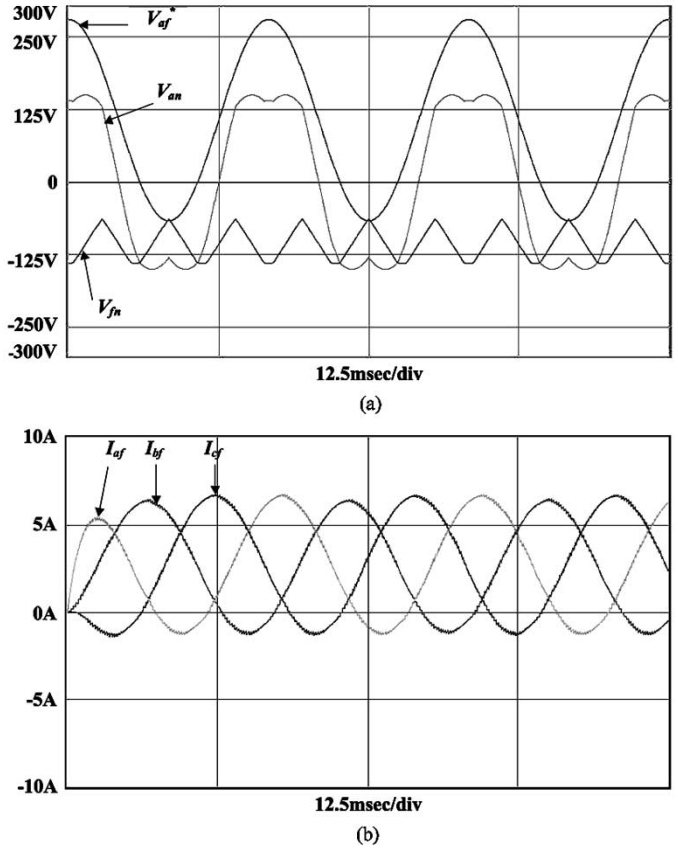

Fig. 7. Simulation results with voltage references in (26): (a) voltage references and (b) three-phase load currents.

PWM method up to the value given by (25) including zero sequence voltage and balanced three-phase voltage

$$V^*_{\text{peak of af, bf, cf}} = \frac{V_{\text{dc}}}{2} + \frac{\sqrt{3}V_{\text{dc}}}{4} \approx 0.933V_{\text{dc}}. \qquad (25)$$

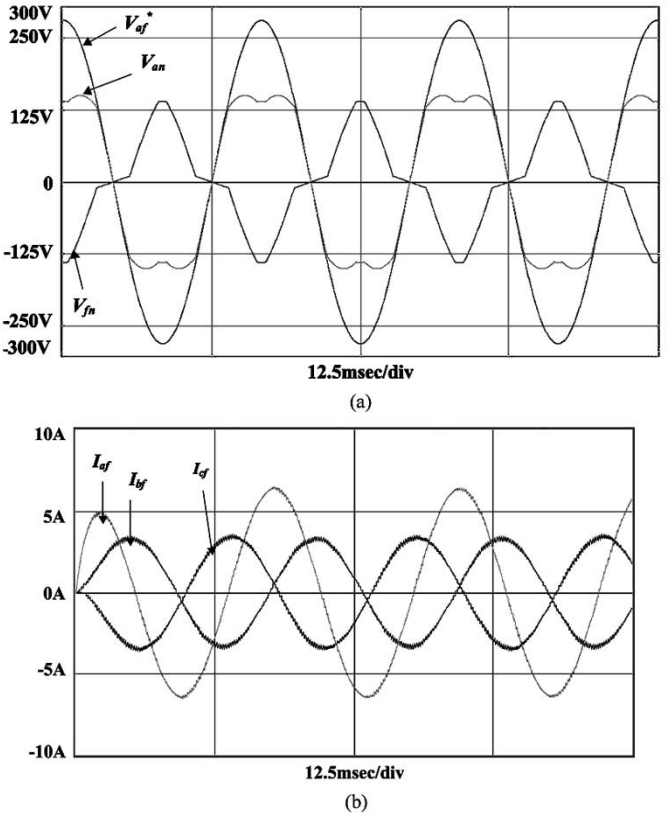

Fig. 8. Simulation results with voltage references in (27): (a) voltage references and (b) three-phase load currents.

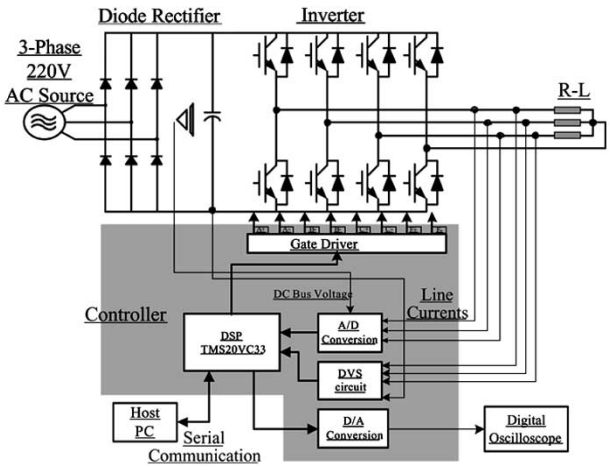

Fig. 9. Experimental setup.

V. SIMULATION AND EXPERIMENTAL RESULTS

The feasibility of the proposed PWM strategy has been investigated and verified through computer simulations and experimental results for the three-phase four-leg VSC system as shown in Fig. 4. The three-phase loads are composed of resistors and inductors whose parameters are summarized in Table I. For the measurement of the PWM voltage in experiments, direct voltage sensing (DVS) circuits are used, which consists of differential amplifiers to reject the common-mode voltage of PWM

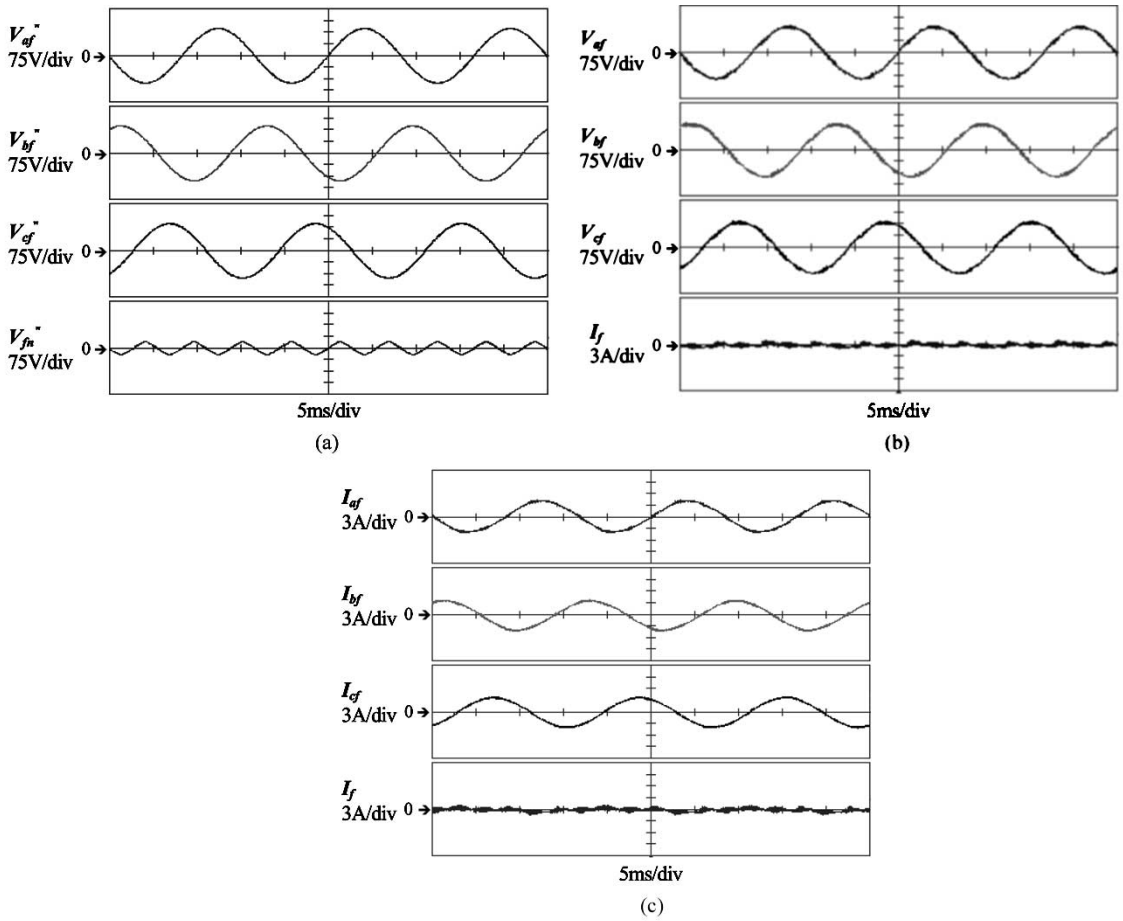

Fig. 10. Balanced voltage generation with no zero sequence voltage.

output voltages and switched integrators to integrate the voltages [15]. By using DVS circuit, the averaged output voltage during a sampling period can be measured precisely.

A. Simulation Results

The first simulation results are shown in Fig. 7 on the condition that the three line to neutral voltage references are given as (26).

Simulation I Condition:

$$\begin{aligned} V_{af}^* &= A_{\max}\cos(\omega t) + V_{o\max} \\ V_{bf}^* &= A_{\max}\cos(\omega t - 2\pi/3) + V_{o\max} \\ V_{cf}^* &= A_{\max}\cos(\omega t + 2\pi/3) + V_{o\max} \end{aligned} \tag{26}$$

where $\omega = 120\pi$, $A_{\max} = V_{\rm dc}/\sqrt{3} \approx 173.2$ [V], $V_{o\max} = V_{\rm dc}/2 - V_{\rm dc}/4\sqrt{3} \approx 106.7$ [V].

In Fig. 7, the offset voltage reference, V_{fn}, and the a-phase pole voltage reference, V_{an}, are shown along with the a-phase line to neutral voltage reference, V_{af}^*. Due to the constant zero sequence voltage there is the constant offset current in each phase current waveform. The magnitude of offset at steady state equals $V_{o\max}/R \approx 0.3557 V_{\rm dc}/R \approx 2.67$ [A].

The second simulation results are shown in Fig. 8 on the condition that the zero sequence voltage exists synchronized with the a-phase balanced voltage reference. Hence, the three voltage references are given as (27).

Simulation II Condition:

$$\begin{aligned} V_{af}^* &= A_{\max}\cos(\omega t) + V_{o\max}\cos(\omega t) \\ V_{bf}^* &= A_{\max}\cos(\omega t - 2\pi/3) + V_{o\max}\cos(\omega t) \\ V_{cf}^* &= A_{\max}\cos(\omega t + 2\pi/3) + V_{o\max}\cos(\omega t) \end{aligned} \tag{27}$$

where $\omega = 120\pi$, $A_{\max} = V_{\rm dc}/\sqrt{3} \approx 173.2$ [V], $V_{o\max} = V_{\rm dc}/2 - V_{\rm dc}/4\sqrt{3} \approx 106.7$ [V].

In Fig. 8 due to the zero sequence voltage, the phase currents are unbalanced and the sum of all phase currents, which flows through the additional leg, is not zero and the sum in a steady state equals $3V_{o\max}\cos(\omega t - \phi)/Z \approx 7.24\cos(120\pi t - 0.4404)$ [A], where $Z = \sqrt{(\omega L)^2 + R^2}$, and $\phi = \tan^{-1}(\omega L/R)$.

B. Experimental Results

The prototype three-phase four-leg PWM converter using two power modules (PM150RSA060, 600 V/150 A) was built as shown in Fig. 9. Fig. 10 shows some results on the condition that the balanced line to neutral voltage references have a magnitude of $V_{\rm dc}/\sqrt{3}$ and a frequency of 60 Hz, with no zero sequence voltage. Figs. 11 and 12 present experimental results on the same condition with those of simulation I and II, respectively. In all figures I_{af} stands for the a-phase current, I_{bf} for the b-phase current, I_{cf} for the c-phase current, and I_f for the neutral component current flowing through the additional leg. As expected in the simulation results, the output voltages measured by the DVS circuit are well synthesized by the four-leg

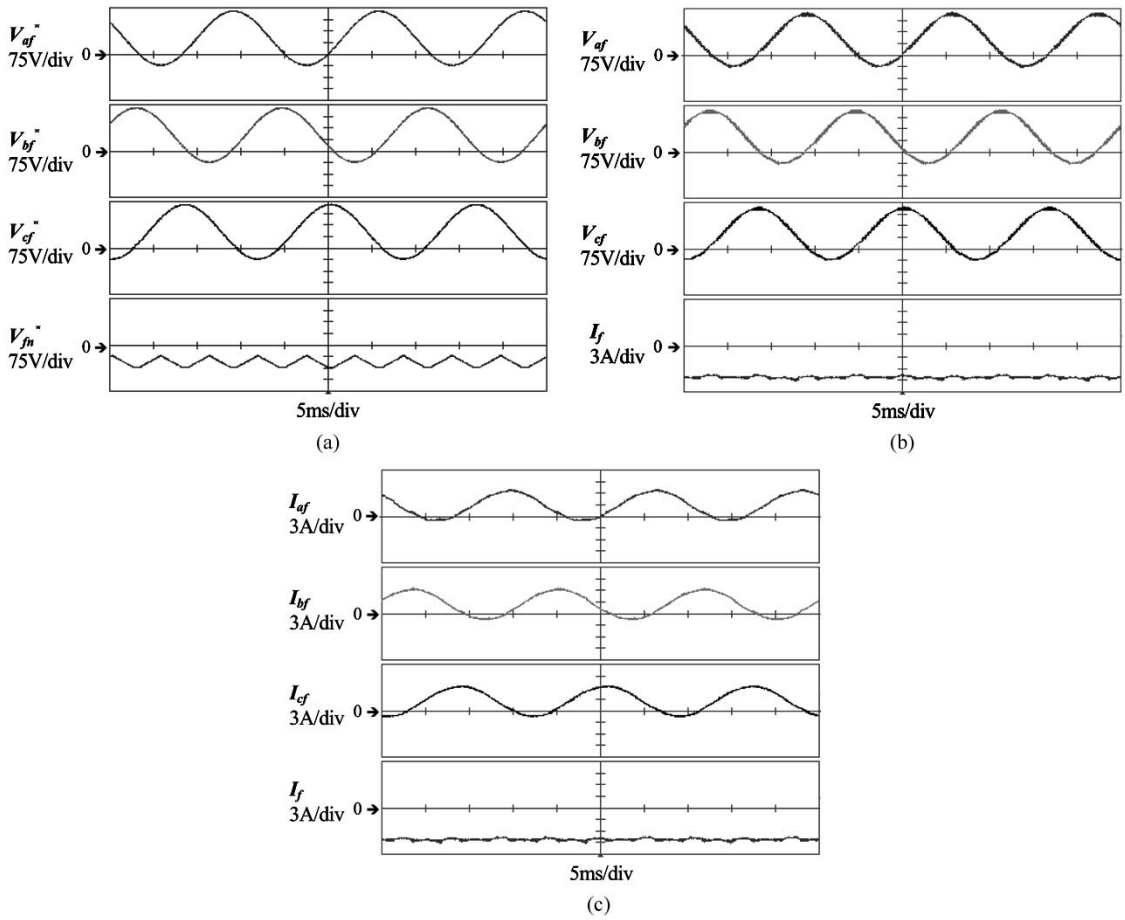

Fig. 11. Maximum zero sequence voltage, which is a constant, added with maximum balanced phase voltages.

converter in Figs. 10–12. The zero sequence current appears in Figs. 11, 12 in contrast to the case of Fig. 10, where only balanced voltages are generated.

VI. Conclusion

In this paper, a novel voltage modulation strategy for the three-phase four-leg voltage source converter based on a triangular carrier has been proposed using an offset voltage concept. It is proved that the proposed method is equivalent to the symmetrically aligned-class I 3-D space vector PWM [7]. The proposed method is so simple that it can be implemented even with a few analog circuits, such as several comparators and operational amplifiers. Alternatively the algorithm for the method can be executed in a simple microprocessor, without complex digital hardware. The magnitude of the maximum line to neutral voltage including the zero sequence voltage and the balanced phase voltage has been derived. It has been shown that the maximum magnitude of the zero sequence voltage is $V_{\rm dc}/2 - V_{\rm dc}/4\sqrt{3}$, while the four-leg VSC simultaneously produces maximum balanced phase voltage whose magnitude is $V_{\rm dc}/\sqrt{3}$. The feasibility of the proposed PWM method has been verified by the computer simulations and experimental results.

Appendix

In this section, it is proved that the proposed PWM technique is equivalent to the symmetrically aligned-class I 3-D SVPWM [7]. The calculation sequence for ON-time of the upper switch of a leg with respective node "a," "b," "c," and "f" has four steps based on 3-D SVM as follows.

Step 1) **Prism Identification among Prism I-VI**
A Prism can be decided based on the projections of the reference voltage vector on the $\alpha\beta$ plane.

Step 2) **Tetrahedron selection among four per each Prism**
Adjacent voltage vectors can be selected based on the polarities of line to neutral voltage references.

Step 3) **Duty-ratio calculation of each nonzero voltage vectors**
The 24-sector has a respective transposing matrix from selected voltage vector to duty ratio, therefore the pre-calculated 24-matrix table is required in practical implementation.

Step 4) **ON time calculation of each switches**
ON time calculation of each switch based on arrangements of nonzero voltage vectors.

The 2^4 switching vectors can be displayed on the dqo reference frame ($\alpha\beta\gamma$ 3-D space in [7]) as shown in Fig.13. The region of Prism I is indicated as a bold triangular prism in Fig.13. The region of Prism I can be divided into four Tetrahedrons based on the polarity of V_{af}, V_{bf} and V_{cf}. Each Tetrahedron has three nonzero switching vectors and two zero switching vectors. In the particular case of Prism I, the nonzero switching vectors (NZSV's) are determined according to Table II, and for the purpose of calculating the duty ratio of NZSV's, the respective ma-

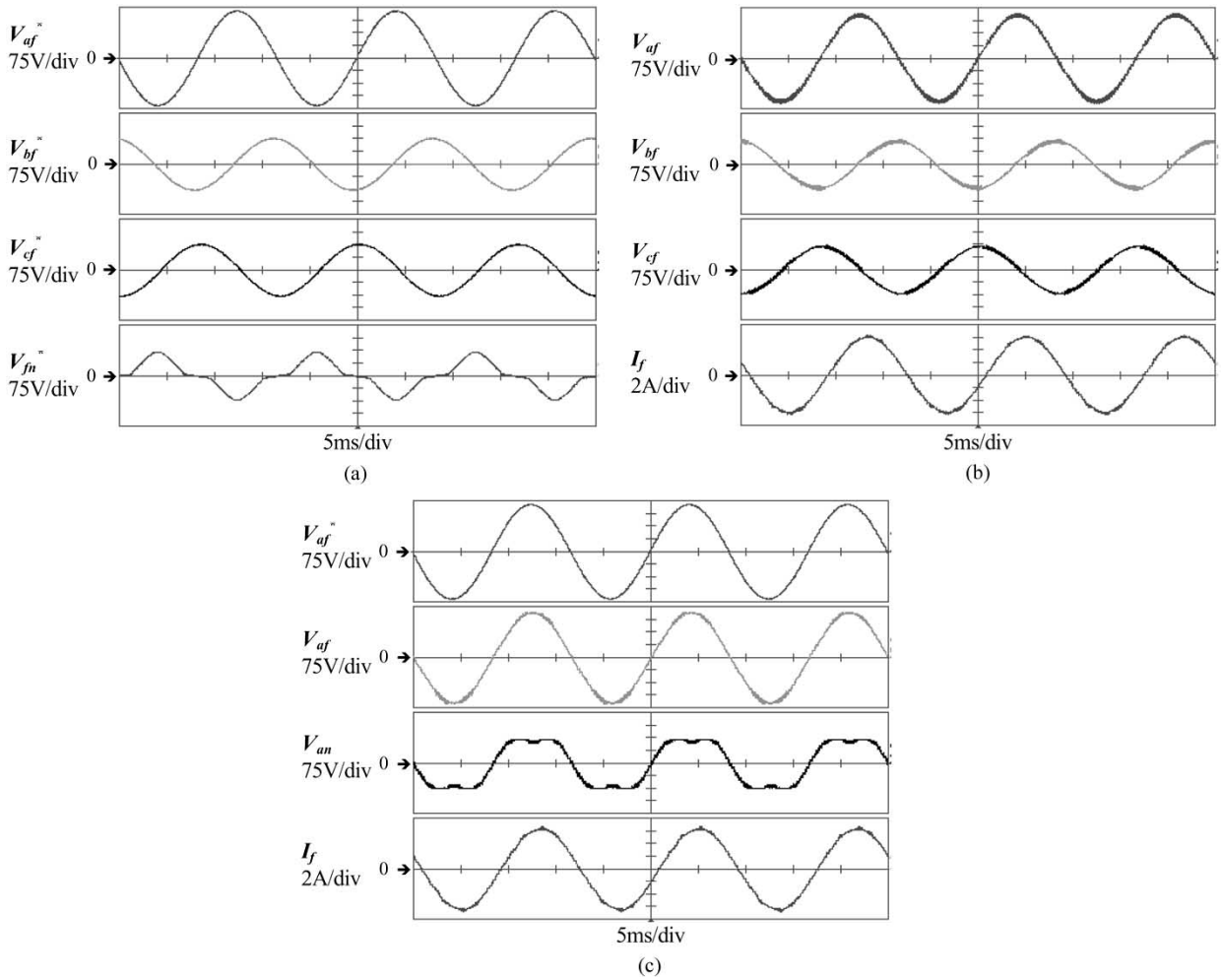

Fig. 12. Sinusoidal zero sequence voltage, synchronized with a-phase, added with maximum balanced phase voltages.

trix for each Tetrahedron is also given as Table II, [7]. Finally, the ON time of the upper switch can be calculated by the arrangement of NZSVs as Fig. 14.

The voltage reference vector $\boldsymbol{V}$ is given as (A1) in the stationary dqo reference frame

$$\boldsymbol{V}_{\boldsymbol{dqo}} = (V_d, V_q, V_o) \tag{A1}$$

V_d, V_q, and V_o can be related to the three line to neutral voltages as (A2), and they can be expressed as (A3) using the spherical coordinate values R, ϕ, and θ as shown in Fig. 15

$$\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_{af} \\ V_{bf} \\ V_{cf} \end{bmatrix} \tag{A2}$$

$$\begin{aligned} V_d &= R\cos\theta\cos\phi \\ V_q &= R\cos\theta\sin\phi \\ V_0 &= R\sin\theta \end{aligned} \tag{A3}$$

hence the line to neutral voltage can be expressed by R, ϕ, and θ as

$$\begin{aligned} V_{af} &= R(\cos\phi\cos\theta + \sin\theta) \\ V_{bf} &= R\frac{1}{2}(-\cos\phi\cos\theta + \sqrt{3}\cos\theta\sin\phi + 2\sin\theta) \\ V_{cf} &= -R\frac{1}{2}(\cos\phi\cos\theta + \sqrt{3}\cos\theta\sin\phi - 2\sin\theta). \end{aligned} \tag{A4}$$

If the voltage reference vector exists in Prism I, the three line to neutral voltages satisfy the inequality (A5) for $0 \le \phi \le \pi/3$ and $-\pi/2 \le \theta \le \pi/2$

$$V_{af} \ge V_{bf} \ge V_{cf} \tag{A5}$$

and similar conditions would exist in each respective Prism as shown in Table III. Therefore, each Prism can be divided into four regions which correspond to the Tetrahedrons in [7], since three line to neutral voltages should be compared with zero. The respective region called Tetrahedron can be divided with the condition of θ as shown in Table IV.

If the offset voltage is selected as proposed in (16), the offset voltage can be rewritten as (A5) in the case of the voltage reference vector being in Tetrahedron 3 of Prism I

$$V_{fn} = -R\frac{(\cos\phi\cos\theta + \sin\theta)}{2}. \tag{A5}$$

Then by (A4) and (A5) the pole voltage references are determined as

$$\begin{aligned} V_{an} &= R\frac{(\cos\phi\cos\theta + \sin\theta)}{2} \\ V_{bn} &= R\frac{1}{2}(-2\cos\phi\cos\theta + \sqrt{3}\cos\theta\sin\phi + \sin\theta) \\ V_{cn} &= R\frac{1}{2}(-2\cos\phi\cos\theta - \sqrt{3}\cos\theta\sin\phi + \sin\theta). \end{aligned} \tag{A6}$$

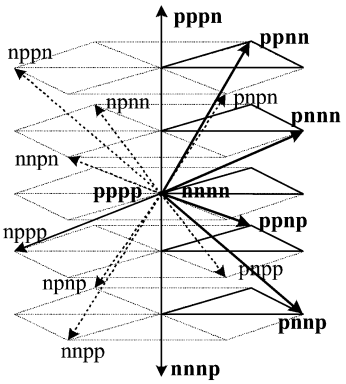

Fig. 13. Sixteen switching vectors in dqo reference frame.

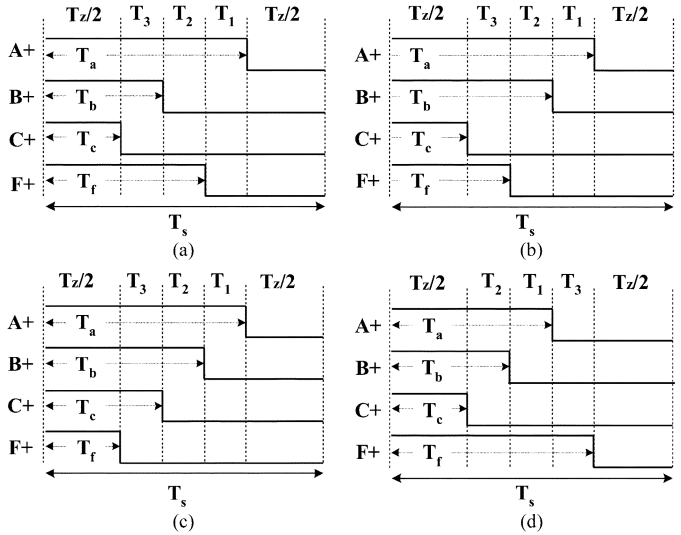

Fig. 14. Conceptual switching sequence with respect to Tetrahedron in Prism I in case of symmetrically aligned-class I: (a) tetrahedron 1, (b) tetrahedron 2, (c) tetrahedron 3, and (d) tetrahedron 4.

TABLE II
CONVENTIONAL METHOD IN PRISM I [7]

	Nonzero Switching Vectors	Zero Switching Vectors	Polarity of V_{af}, V_{bf} and V_{cf}	Calculation Matrix
Tetrahedron 1	(P,N,N,N)	(P,P,P,P) (N,N,N,N)	$V_{af} \geq 0$	$\begin{bmatrix} 1 & 0 & 1 \\ 1/2 & -\sqrt{3}/2 & -1 \\ 0 & \sqrt{3} & 0 \end{bmatrix}$
	(P,N,N,P)		$V_{bf} \leq 0$	
	(P,P,N,P)		$V_{cf} \leq 0$	
Tetrahedron 2	(P,N,N,N)		$V_{af} \geq 0$	$\begin{bmatrix} 3/2 & -\sqrt{3}/2 & 0 \\ -1/2 & \sqrt{3}/2 & 1 \\ 1/2 & \sqrt{3}/2 & -1 \end{bmatrix}$
	(P,P,N,N)		$V_{bf} \geq 0$	
	(P,P,N,P)		$V_{cf} \leq 0$	
Tetrahedron 3	(P,N,N,N)		$V_{af} \geq 0$	$\begin{bmatrix} 3/2 & -\sqrt{3}/2 & 0 \\ 0 & \sqrt{3} & 0 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix}$
	(P,P,N,N)		$V_{bf} \geq 0$	
	(P,P,P,N)		$V_{cf} \geq 0$	
Tetrahedron 4	(P,N,N,P)		$V_{af} \leq 0$	$\begin{bmatrix} 3/2 & -\sqrt{3}/2 & 0 \\ 0 & \sqrt{3} & 0 \\ -1 & 0 & -1 \end{bmatrix}$
	(P,P,N,P)		$V_{bf} \leq 0$	
	(N,N,N,P)		$V_{cf} \leq 0$	

Therefore ON time of the upper switches can be calculated as

$$T_a = \frac{T_s}{2} + \frac{T_s}{V_{\rm dc}}\frac{R}{2}(\cos\phi\cos\theta + \sin\theta)$$
$$T_b = \frac{T_s}{2} + \frac{T_s}{V_{\rm dc}}\frac{R}{2}(-2\cos\phi\cos\theta + \sqrt{3}\cos\theta\sin\phi + \sin\theta)$$
$$T_c = \frac{T_s}{2} + \frac{T_s}{V_{\rm dc}}\frac{R}{2}(-2\cos\phi\cos\theta - \sqrt{3}\cos\theta\sin\phi + \sin\theta)$$
$$T_f = \frac{T_s}{2} - \frac{T_s}{V_{\rm dc}}\frac{R}{2}(\cos\phi\cos\theta + \sin\theta). \quad \text{(A7)}$$

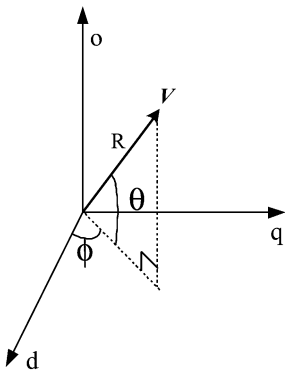

Fig. 15. Voltage reference vector in dqo reference frame.

TABLE III
MAGNITUDE CONDITION ACCORDING TO EACH PRISM

Prism I	Prism II	Prism III	Prism IV	Prism V	Prism VI
$0 \leq \phi \leq \pi/3$	$\pi/3 \leq \phi \leq 2\pi/3$	$2\pi/3 \leq \phi \leq \pi$	$\pi \leq \phi \leq 4\pi/3$	$4\pi/3 \leq \phi \leq 5\pi/3$	$5\pi/3 \leq \phi \leq 0$
$V_{af} \geq V_{bf} \geq V_{cf}$	$V_{bf} \geq V_{af} \geq V_{cf}$	$V_{bf} \geq V_{cf} \geq V_{af}$	$V_{cf} \geq V_{bf} \geq V_{af}$	$V_{cf} \geq V_{af} \geq V_{bf}$	$V_{af} \geq V_{cf} \geq V_{bf}$

TABLE IV
θ CONDITIONS ACCORDING TO TETRAHEDRONS IN PRISM I WHERE $0 \leq \phi \leq \pi/3$

Tetrahedron 1	Tetrahedron 2	Tetrahedron 3	Tetrahedron 4
$\tan\theta \geq -\cos\phi$	$\tan\theta \geq -\cos\phi$	$\tan\theta \geq -\cos\phi$	$\tan\theta \leq -\cos\phi$
$\tan\theta \leq \cos(\phi + \pi/3)$	$\tan\theta \geq \cos(\phi + \pi/3)$	$\tan\theta \geq \cos(\phi + \pi/3)$	$\tan\theta \leq \cos(\phi + \pi/3)$
$\tan\theta \leq \cos(\phi - \pi/3)$	$\tan\theta \leq \cos(\phi - \pi/3)$	$\tan\theta \geq \cos(\phi - \pi/3)$	$\tan\theta \leq \cos(\phi - \pi/3)$

TABLE V
POLE VOLTAGE REFERENCE IN PRISM I

Tetrahedron 1	Tetrahedron 2	Tetrahedron 3	Tetrahedron 4
$V_{an} = V_{af} - \frac{V_{af} + V_{cf}}{2}$	$V_{an} = V_{af} - \frac{V_{af} + V_{cf}}{2}$	$V_{an} = \frac{V_{af}}{2}$	$V_{an} = V_{af} - \frac{V_{cf}}{2}$
$V_{bn} = V_{bf} - \frac{V_{af} + V_{cf}}{2}$	$V_{bn} = V_{bf} - \frac{V_{af} + V_{cf}}{2}$	$V_{bn} = V_{bf} - \frac{V_{af}}{2}$	$V_{bn} = V_{bf} - \frac{V_{cf}}{2}$
$V_{cn} = V_{cf} - \frac{V_{af} + V_{cf}}{2}$	$V_{cn} = V_{cf} - \frac{V_{af} + V_{cf}}{2}$	$V_{cn} = V_{cf} - \frac{V_{af}}{2}$	$V_{cn} = \frac{V_{cf}}{2}$
$V_{fn} = -\frac{V_{af} + V_{cf}}{2}$	$V_{fn} = -\frac{V_{af} + V_{cf}}{2}$	$V_{fn} = -\frac{V_{af}}{2}$	$V_{fn} = -\frac{V_{cf}}{2}$

The pole voltage references and the offset voltage in Prism I are summarized in Table V. With this Table, the ON time of the upper switches in the other Tetrahedrons can be similarly induced. However, the duty ratios of the selected switching vectors for the 3-D SVPWM in Prism I and Tetrahedron 3 are given by (A8), [7]. As shown in Fig. 14(c), ON time of upper switches and the duty ratios of the selected switching vectors have the relationship given by

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \frac{1}{V_{\rm dc}} \begin{bmatrix} 3/2 & -\sqrt{3}/2 & 0 \\ 0 & \sqrt{3} & 0 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix} \begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} \quad \text{and}$$
$$D_z = 1 - D_1 - D_2 - D_3. \quad \text{(A8)}$$
$$T_a = \frac{T_z}{2} + T_3 + T_2 + T_1 = T_s\left(\frac{D_z}{2} + D_3 + D_2 + D_1\right)$$
$$T_b = \frac{T_z}{2} + T_3 + T_2 = T_s\left(\frac{D_z}{2} + D_3 + D_2\right)$$
$$T_c = \frac{T_z}{2} + T_3 = T_s\left(\frac{D_z}{2} + D_3\right)$$
$$T_f = \frac{T_z}{2} = T_s\frac{D_z}{2}. \quad \text{(A9)}$$

If the Vd, Vq, and Vo are substituted by (A3) in (A8), the duty ratios can be expressed in terms of R, ϕ, and θ, and the results can be substituted to (A9). Then ON time of upper switches can be expressed in terms of R, ϕ, and θ. These results of the ON-time of upper switches are exactly the same as (A7), which have been calculated by the proposed carrier based PWM. In other Prisms and Tetrahedrons, the equivalence between the symmetrically aligned-class I 3-D SVPWM and the proposed carrier based PWM could be similarly proved. Furthermore other gating sequences such as the class II 3-D SVPWM in [7] can be implemented by simply changing the rule to define offset voltage from (16) to proper ones like the method in [12] in the case of the 2-D SVPWM.

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