CSE125 Lab2: Finite State Machines

Due Date: Wednesday 4/22/2020 11:59pm

I. Regular Expression Checker (14 Points)

Implement a Moore finite state machine (FSM) that checks the following regular expression:

(AB*C(A|(D(B|C|D))))*D, where the set of symbols S={A,B,C,D}. If you are not familiar with regular expressions, review them first.

The symbols are encoded in binary as follows:

Symbol	Binary
A	00
B	01
C	10
D	11

```
module regex(input clk, input res_n, input [1:0] symbol_in,
             input last_symbol, output result, output done);
           /* Your code here */
endmodule
```

The FSM should be implemented as part of the module shown above. The FSM is provided with one symbol per clock cycle. In the same cycle where the last symbol of a sequence is provided to the FSM, the `last_symbol` signal goes high for one cycle. The `result` should be 1 in the case of a match and 0 in the case the input does not match the regex. The validity of the result should be signaled by `done`=1 one cycle after `last_symbol`=1.

A testbench for evaluation can be found here https://git.ucsc.edu/cse125/spring20/lab2

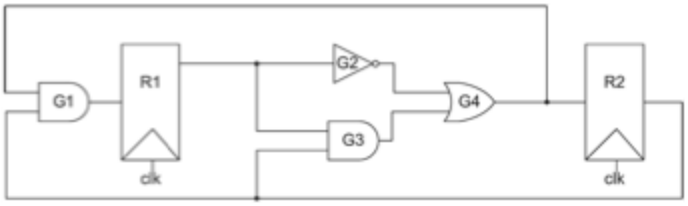
Submit via Canvas the following files

a) A drawing of the FSM. Make sure to mark the start and end state(s). There is a nice open tool to draw FSMs at http://madebyevan.com/fsm/
b) A Verilog file named regex.v that implements the Moore FSM in behavioral Verilog.
c) A testbench that instantiates the modules. The testbench should check the following inputs: ABCDD, ABBBCAABD, ABCDDD, ABBCAAD
d) A screenshot of a waveform stored as waveform.png showing all inputs and outputs over the duration of 7 clock cycles (in addition to reset time etc.) for the input ABCDD.
e) A write up that lists the synthesis results (resources and Fmax).

II. Timing (6 Points)

Consider the circuit below with the following timing parameters:

Setup Time	40ps
Hold Time	35ps
Clk-to-Q Delay	30ps (min), 50ps (max)
Propagation delay for each gate	70ps (min), 90ps (max)



Submit via Canvas a document with the file name timing.pdf that provides answers to the following question:

a) Identify the critical path or paths in this circuit. You may make use of register names (R1 and R2) and the gate names (g1,g2,g3,g4) to describe the critical paths.
b) Calculate the maximum clock rate the circuit can be operated at
c) Can the register hold times ever be violated? Why?