

ZYNQ7 Processing System (5.2)

Documentation IP Location Presets

Page Navigator

Zynq Block Design

Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

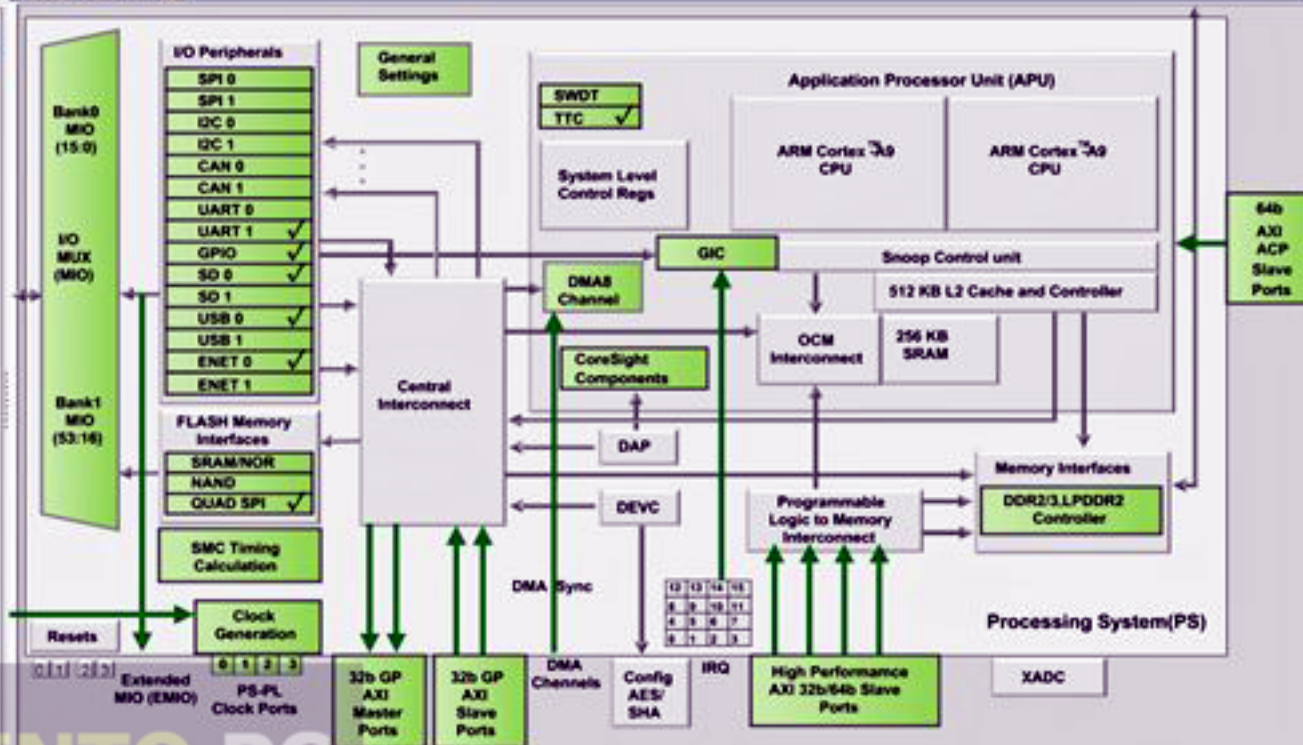
MIO Configuration

Clock Configuration

DDR Configuration

SMC Timing Calculation

Interrupts



GET INTO PC

Programmable Logic(PL)