

Component Name	design_1_fir_compiler_0_0
Filter Type	Single Rate
Number of Interleaved Channels	16
Number of Parallel Channels	2
Clock Frequency	N/A
Input Sampling Frequency	N/A
Sample Period	1
Number of Parallel Input Samples	1
Number of Parallel Output Samples	1
Input Data Width	16
Input Data Fractional Bits	15
Number of Coefficients	29
Calculated Coefficients	29
Number of Coefficient Sets	16
Reloadable Coefficients	No
Coefficient Structure	Non Symmetric
Coefficient Width	25
Coefficient Fractional Bits	27
Quantization Mode	Quantize_Only
Filter gain due to quantization mode	N/A
Rounding Mode	Convergent Rounding to Even
Output Width	19 (full precision = 41 bits)
Output Fractional Bits	20
Cycle Latency	39
Filter Architecture	Systolic Multiply Accumulate