```vhdl
library ieee;
use ieee.std_logic_1164.ALL;
use ieee.numeric_std.all;
--
entity baseline_control is
  generic(
    W                   : natural; --:=5;      -- numero de bits de direcciones. 2**W = 32 direcciones para W=5
    ADCBITS             : natural; -- := 10;   -- numero de bits en los datos
    RBITS               : natural; -- := 12;   -- numero de bits de los registros
    REFRESH_RATE        : natural; -- := 80000; -- 80000 clk implican un refresh rate de 2ms (80000 * 25 ns = 2ms)
    NCH                 : natural  --:= 3      -- numero de canales de la electronica
  );

  port(
    clk_40mhz           : in std_logic;
    reset               : in std_logic;
    ptick_2ms           : out std_logic;
    data_adc1           : in   std_logic_vector(ADCBITS-1 downto 0);
    data_adc2           : in   std_logic_vector(ADCBITS-1 downto 0);
    data_adc3           : in   std_logic_vector(ADCBITS-1 downto 0);
    baseline1           : out   std_logic_vector(RBITS-1 downto 0);
    baseline2           : out   std_logic_vector(RBITS-1 downto 0);
    baseline3           : out   std_logic_vector(RBITS-1 downto 0)
  );
end baseline_control;

architecture rtl of baseline_control is

  signal cont_promedio_reg, cont_promedio_next : unsigned((2**W-1) downto 0);
  signal adc1_sum_reg, adc1_sum_next : unsigned((2**W-1) downto 0);
  signal adc2_sum_reg, adc2_sum_next : unsigned((2**W-1) downto 0);
  signal adc3_sum_reg, adc3_sum_next : unsigned((2**W-1) downto 0);
```