

Interconnect

Master 0

Slave 0

Conversion  
and/or  
Pipelining

```
graph LR; M0[Master 0] --> IC[Interconnect]; subgraph IC; CP[Conversion and/or Pipelining]; end; IC --> S0[Slave 0];
```

The diagram illustrates a data path from Master 0 to Slave 0. Master 0 is represented by a white rectangle on the left. An arrow points from Master 0 to a large light-gray rectangle labeled 'Interconnect' at the top. Inside the 'Interconnect' rectangle is a smaller dark-gray rectangle labeled 'Conversion and/or Pipelining'. An arrow points from this inner rectangle to Slave 0, which is a white rectangle on the right.