```
arnaldi@kornephoros:~/work/lago/lago-fpga-vhdl$ ls
baseline_control.prj  dcm_200mhz.v          interfaz_spi.prj  kcuart_tx.vhd          lago_fpga_vhdl.xise  spi_dac.vhd
baseline_control.xst  GPSNFIFO.FMT          interfaz_spi.vhd  lago_fpga_vhdl_1200.ucf  lago_fpga_vhdl.xst   trigger.vhd
baseline.vhd          GPS_n_fifo.vhd        interfaz_spi.xst  lago_fpga_vhdl.prj     Makefile             uart_rx.vhd
bbfifo_16x8.vhd       GPSNFIFO.VHD          ipcore_dir        lago_fpga_vhdl.ucf     nexys2_1200.batch    uart_tx.vhd
clk_40mhz.v           HP03_par_control.vhd  kcpsm3.vhd        lago_fpga_vhdl.vhd     nexys2_500.batch     usb_if_ctrl.vhd
clock_divider.v       HP_LAGO.VHD           kcuart_rx.vhd     lago_fpga_vhdl.vhd_orig  rampa_hv.vhd
arnaldi@kornephoros:~/work/lago/lago-fpga-vhdl$
```