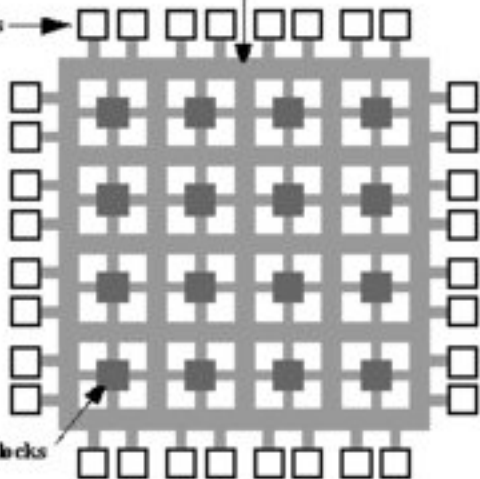


Interconnect Resources

I/O Cells



Logic Blocks