

1. Description

1.1. Project

Project Name	LineTrackingCarV2
Board Name	custom
Generated with:	STM32CubeMX 6.8.1
Date	05/16/2023

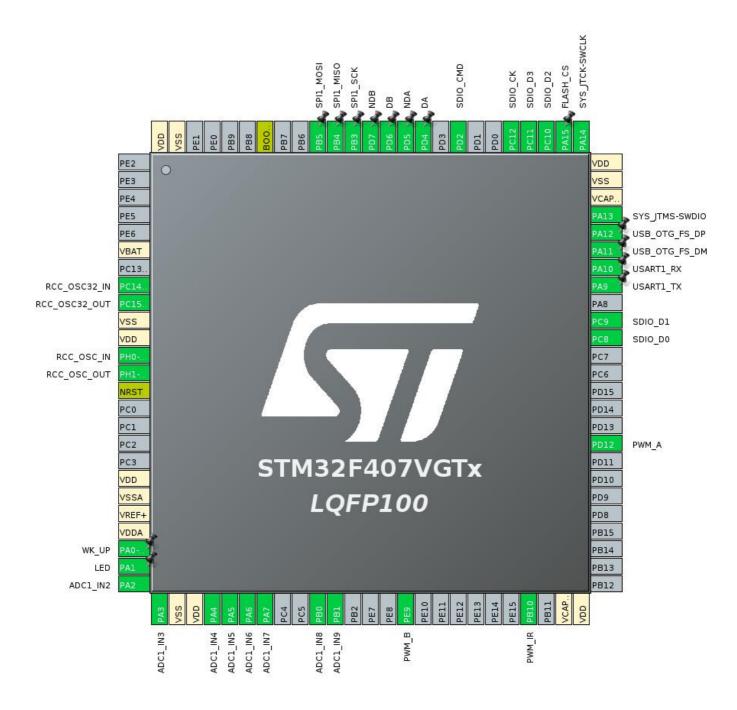
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



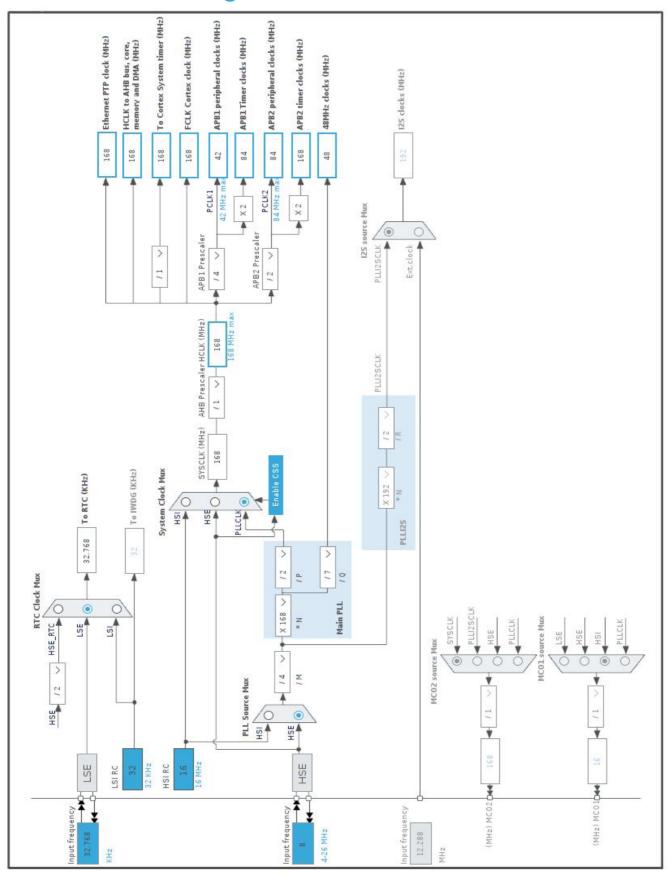
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP100	(function after		Function(s)	
	reset)			
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP *	I/O	GPIO_Input	WK_UP
24	PA1 *	I/O	GPIO_Output	LED
25	PA2	I/O	ADC1_IN2	
26	PA3	I/O	ADC1_IN3	
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN4	
30	PA5	I/O	ADC1_IN5	
31	PA6	I/O	ADC1_IN6	
32	PA7	I/O	ADC1_IN7	
35	PB0	I/O	ADC1_IN8	
36	PB1	I/O	ADC1_IN9	
40	PE9	I/O	TIM1_CH1	PWM_B
47	PB10	I/O	TIM2_CH3	PWM_IR
49	VCAP_1	Power		
50	VDD	Power		
59	PD12	I/O	TIM4_CH1	PWM_A
65	PC8	I/O	SDIO_D0	SDIO_D0
66	PC9	I/O	SDIO_D1	SDIO_D1
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15 *	I/O	GPIO_Output	FLASH_CS
78	PC10	I/O	SDIO_D2	SDIO_D2
79	PC11	I/O	SDIO_D3	SDIO_D3
80	PC12	I/O	SDIO_CK	SDIO_CK
83	PD2	I/O	SDIO_CMD	SDIO_CMD
85	PD4 *	I/O	GPIO_Output	DA
86	PD5 *	I/O	GPIO_Output	NDA
87	PD6 *	I/O	GPIO_Output	DB
88	PD7 *	I/O	GPIO_Output	NDB
89	PB3	I/O	SPI1_SCK	
90	PB4	I/O	SPI1_MISO	
91	PB5	I/O	SPI1_MOSI	
94	воото	Boot		
99	VSS	Power		
100	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	LineTrackingCarV2
Project Folder	/work/14-LHC/LineTrackingCarV2
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_RTC_Init	RTC
5	MX_SDIO_SD_Init	SDIO
6	MX_FATFS_Init	FATFS
7	MX_SPI1_Init	SPI1
8	MX_ADC1_Init	ADC1
9	MX_TIM8_Init	TIM8
10	MX_USB_DEVICE_Init	USB_DEVICE
11	MX_USART1_UART_Init	USART1

Rank	Function Name	Peripheral Instance Name
12	MX_TIM1_Init	TIM1
13	MX_TIM2_Init	TIM2
14	MX_TIM4_Init	TIM4

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
мси	STM32F407VGTx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

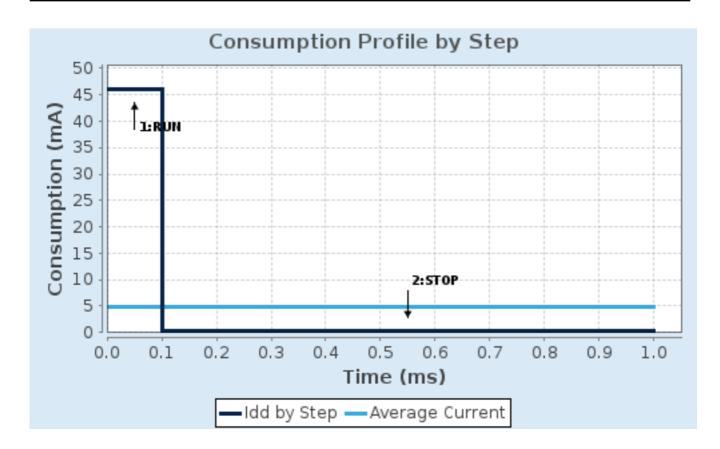
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.47	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1
mode: IN2
mode: IN3
mode: IN4
mode: IN5
mode: IN6
mode: IN7
mode: IN8
mode: IN9

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Discontinuous Conversion Mode

Right alignment

Enabled

Enabled

Disabled

DMA Continuous Requests Enabled *

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 8 *

External Trigger Conversion Source Timer 8 Trigger Out event *

External Trigger Conversion Edge Trigger detection on the rising edge

Rank 1

Channel Channel 2
Sampling Time 144 Cycles *

Rank 2 *

Channel 3 *
Sampling Time Channel 3 *

<u>Rank</u> 3 *

Channel 4 *
Sampling Time Channel 4 *

<u>Rank</u> **4** *

Channel 5 *

Sampling Time 144 Cycles *

<u>Rank</u> 5 *

Channel 6 *

Sampling Time 144 Cycles *

<u>Rank</u> 6 *

Channel 7 *
Sampling Time Channel 7 *
144 Cycles *

<u>Rank</u> 7 *

Channel 8 *
Sampling Time Channel 8 *

<u>Rank</u> 8 *

Channel 9 *
Sampling Time Channel 9 *

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.3. RTC

mode: Activate Clock Source

7.3.1. Parameter Settings:

General:

Hour Format Hourformat 24

Asynchronous Predivider value 127
Synchronous Predivider value 255

7.4. SDIO

Mode: SD 4 bits Wide bus

7.4.1. Parameter Settings:

SDIO parameters:

Clock transition on which the bit capture is made Rising transition

SDIO Clock divider bypass Disable

SDIO Clock output enable when the bus is idle

Disable the power save for the clock

SDIO hardware flow control

The hardware control flow is disabled

SDIOCLK clock divide factor 0

7.5. SPI1

Mode: Full-Duplex Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate)

Baud Rate 42.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled
NSS Signal Type Software

7.6. SYS

Debug: Serial Wire

Timebase Source: TIM14

7.7. TIM1

Clock Source: Internal Clock
Channel1: PWM Generation CH1

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 168-1 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 1000-1 *

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

7.8. TIM2

Clock Source: Internal Clock
Channel3: PWM Generation CH3

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 336-1 *

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 1000-1 *

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.9. TIM4

Clock Source: Internal Clock
Channel1: PWM Generation CH1

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 84-1 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 1000-1 *

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.10. TIM8

Clock Source : Internal Clock

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 84-1 *
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 100-1 *
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Enable (Trigger delayed for master/slaves simultaneous start)

*

Trigger Event Selection Update Event *

7.11. USART1

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

7.12. USB_OTG_FS

Mode: Device_Only

7.12.1. Parameter Settings:

Speed Device Full Speed 12MBit/s

Low powerDisabledLink Power ManagementDisabledVBUS sensingDisabledSignal start of frameDisabled

7.13. FATFS

mode: SD Card

7.13.1. Set Defines:

Version:

FATFS version R0.12c

Function Parameters:

FS_READONLY (Read-only mode) Disabled
FS_MINIMIZE (Minimization level) Disabled

USE_STRFUNC (String functions) Enabled with LF -> CRLF conversion

USE_FIND (Find functions) Enabled *

USE_MKFS (Make filesystem function) Enabled
USE_FASTSEEK (Fast seek function) Enabled
USE_EXPAND (Use f_expand function) Disabled
USE_CHMOD (Change attributes function) Disabled
USE_LABEL (Volume label functions) Disabled
USE_FORWARD (Forward function) Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target) Latin 1

USE_LFN (Use Long Filename) Enabled with dynamic working buffer on the STACK *

MAX_LFN (Max Long Filename) 255

LFN_UNICODE (Enable Unicode)

STRF_ENCODE (Character encoding)

FS_RPATH (Relative Path)

ANSI/OEM

UTF-8

Disabled

Physical Drive Parameters:

VOLUMES (Logical drives) 1

MAX_SS (Maximum Sector Size) 512

MIN_SS (Minimum Sector Size) 512

MULTI_PARTITION (Volume partitions feature) Disabled

USE_TRIM (Erase feature) Disabled

FS_NOFSINFO (Force full FAT scan) 0

System Parameters:

FS_TINY (Tiny mode) Disabled
FS_EXFAT (Support of exFAT file system) Disabled

FS_NORTC (Timestamp feature) Dynamic timestamp

FS_REENTRANT (Re-Entrancy) Enabled
FS_TIMEOUT (Timeout ticks) 1000
USE_MUTEX Disabled

SYNC_t (O/S sync object) osSemaphoreld

FS_LOCK (Number of files opened simultaneously) 2

7.13.2. Advanced Settings:

SDIO/SDMMC:

SDIO instance SDIO
Use dma template Enabled
BSP code for SD Generic

7.14. FREERTOS

Interface: CMSIS_V1

7.14.1. Config parameters:

API:

FreeRTOS API CMSIS v1

Versions:

FreeRTOS version 10.3.1 CMSIS-RTOS version 1.02

MPU/FPU:

ENABLE_MPU Disabled ENABLE_FPU Disabled

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000 MAX_PRIORITIES 7

MINIMAL_STACK_SIZE 128

MAX_TASK_NAME_LEN 16

USE_16_BIT_TICKS Disabled

IDLE_SHOULD_YIELD Enabled

USE_MUTEXES Enabled

USE_RECURSIVE_MUTEXES Disabled

USE_COUNTING_SEMAPHORES Enabled **

QUEUE_REGISTRY_SIZE 8

USE_APPLICATION_TASK_TAG Disabled
ENABLE_BACKWARD_COMPATIBILITY Enabled
USE_PORT_OPTIMISED_TASK_SELECTION Enabled
USE_TICKLESS_IDLE Disabled
USE_TASK_NOTIFICATIONS Enabled
RECORD_STACK_HIGH_ADDRESS Disabled

Memory management settings:

Memory Allocation
Dynamic *

TOTAL_HEAP_SIZE
40960 *

Memory Management scheme
heap_4

Hook function related definitions:

USE_IDLE_HOOK

USE_TICK_HOOK

Disabled

USE_MALLOC_FAILED_HOOK

USE_DAEMON_TASK_STARTUP_HOOK

CHECK_FOR_STACK_OVERFLOW

Disabled

Option2 *

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS

USE_TRACE_FACILITY

USE_STATS_FORMATTING_FUNCTIONS

Enabled *

Co-routine related definitions:

USE_CO_ROUTINES Disabled MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Enabled
TIMER_TASK_PRIORITY 2
TIMER_QUEUE_LENGTH 10
TIMER_TASK_STACK_DEPTH 256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE size_t
USE_POSIX_ERRNO Disabled

7.14.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled Enabled uxTaskPriorityGet Enabled vTaskDelete Disabled vTaskCleanUpResources Enabled vTaskSuspend vTaskDelayUntil Enabled * Enabled vTaskDelay xTaskGetSchedulerState Enabled xTaskResumeFromISR Disabled * Disabled xQueueGetMutexHolder xSemaphoreGetMutexHolder Disabled Disabled pcTaskGetTaskName Disabled uxTaskGetStackHighWaterMark xTaskGetCurrentTaskHandle Disabled eTaskGetState Disabled xEventGroupSetBitFromISR Enabled * xTimerPendFunctionCall Enabled * Disabled xTaskAbortDelay xTaskGetHandle Disabled ux Task Get Stack High Water Mark 2Enabled *

7.14.3. Advanced settings:

Newlib settings (see parameter description first):

Project settings (see parameter description first):

Use FW pack heap file Enabled

7.15. USB DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.15.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)

1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)

1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)

512
USBD_SELF_POWERED (Enabled self power)

Enabled

USBD_DEBUG_LEVEL (USBD Debug Level) 0: No debug message

Class Parameters:

USB CDC Rx Buffer Size 2048
USB CDC Tx Buffer Size 2048

7.15.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier) 1155

LANGID_STRING (Language Identifier) English(United States)

MANUFACTURER_STRING (Manufacturer Identifier) STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier) 22336

PRODUCT_STRING (Product Identifier) STM32 Virtual ComPort

CONFIGURATION_STRING (Configuration Identifier)

CDC Config

INTERFACE_STRING (Interface Identifier)

CDC Interface

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	Pull-up *	Very High	SDIO_D0
	PC9	SDIO_D1	Alternate Function Push Pull	Pull-up *	Very High	SDIO_D1
	PC10	SDIO_D2	Alternate Function Push Pull	Pull-up *	Very High	SDIO_D2
	PC11	SDIO_D3	Alternate Function Push Pull	Pull-up *	Very High	SDIO_D3
	PC12	SDIO_CK	Alternate Function Push Pull	Pull-up *	Very High	SDIO_CK
	PD2	SDIO_CMD	Alternate Function Push Pull	Pull-up *	Very High	SDIO_CMD
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PWM_B
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down		PWM_IR

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed Very High	User Label
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	PWM_A
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USB_OTG_ FS	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PA0-WKUP	GPIO_Input	Input mode	Pull-down *	n/a	WK_UP
	PA1	GPIO_Output	Output Push Pull	Pull-up *	Low	LED
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	FLASH_CS
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	DA
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	NDA
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	DB
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	NDB

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SDIO_RX	DMA2_Stream6	Peripheral To Memory	Medium *
SDIO_TX	DMA2_Stream3	Memory To Peripheral	Medium *
ADC1	DMA2_Stream0	Peripheral To Memory	High *
USART1_TX	DMA2_Stream7	Memory To Peripheral	Medium *

SDIO_RX: DMA2_Stream6 DMA request Settings:

Mode: Peripheral Flow Control *

Use fifo: Enable *

FIFO Threshold:

Peripheral Increment:

Memory Increment:

Peripheral Data Width:

Word *

Memory Data Width: Word

Peripheral Burst Size: 4 Increme

Peripheral Burst Size: 4 Increment *

Memory Burst Size: 4 Increment

SDIO_TX: DMA2_Stream3 DMA request Settings:

Mode: Peripheral Flow Control *

Use fifo: Enable *

FIFO Threshold: Full
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Word *

Peripheral Burst Size: 4 Increment *
Memory Burst Size: 4 Increment

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable

Memory Increment:

Enable *

Peripheral Data Width: Half Word
Memory Data Width: Half Word

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
		15	0	
Pendable request for system service	true			
System tick timer	true	15	0	
ADC1, ADC2 and ADC3 global interrupts	true	5	0	
USART1 global interrupt	true	5	0	
TIM8 break interrupt and TIM12 global interrupt	true	5	0	
TIM8 update interrupt and TIM13 global interrupt	true	5	0	
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	15	0	
SDIO global interrupt	true	5	0	
DMA2 stream0 global interrupt	true	6	0	
DMA2 stream3 global interrupt	true	5	0	
USB On The Go FS global interrupt	true	5	0	
DMA2 stream6 global interrupt	true	5	0	
DMA2 stream7 global interrupt	true	5	0	
PVD interrupt through EXTI line 16		unused		
Flash global interrupt		unused		
RCC global interrupt		unused		
TIM1 break interrupt and TIM9 global interrupt		unused		
TIM1 update interrupt and TIM10 global interrupt	unused			
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused			
TIM1 capture compare interrupt	unused			
TIM2 global interrupt	unused			
TIM4 global interrupt	unused			
SPI1 global interrupt	unused			
TIM8 capture compare interrupt	unused			
FPU global interrupt	unused			

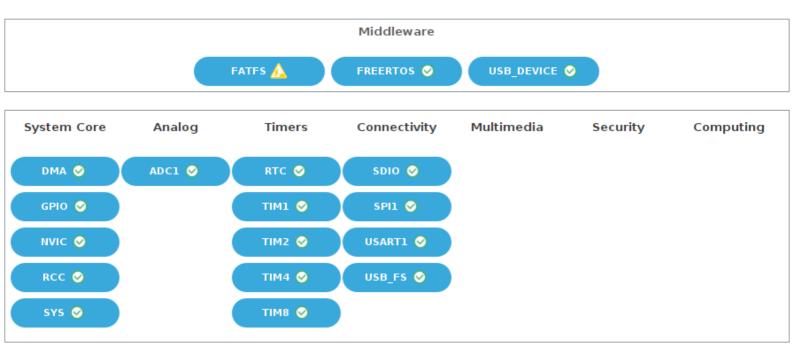
8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
ADC1, ADC2 and ADC3 global interrupts	false	true	true
USART1 global interrupt	false	true	true
TIM8 break interrupt and TIM12 global interrupt	false	true	true
TIM8 update interrupt and TIM13 global interrupt	false	true	true
TIM8 trigger and commutation interrupts and TIM14 global interrupt	false	true	true
SDIO global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream3 global interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true
DMA2 stream6 global interrupt	false	true	true
DMA2 stream7 global interrupt	false	true	true

^{*} User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Docs & Resources

Type Link

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417_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f405-415_407-

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System View https://www.st.com/resource/en/svd/stm32f4_svd.zip

Description

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417_bsdl.zip

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