1. Description

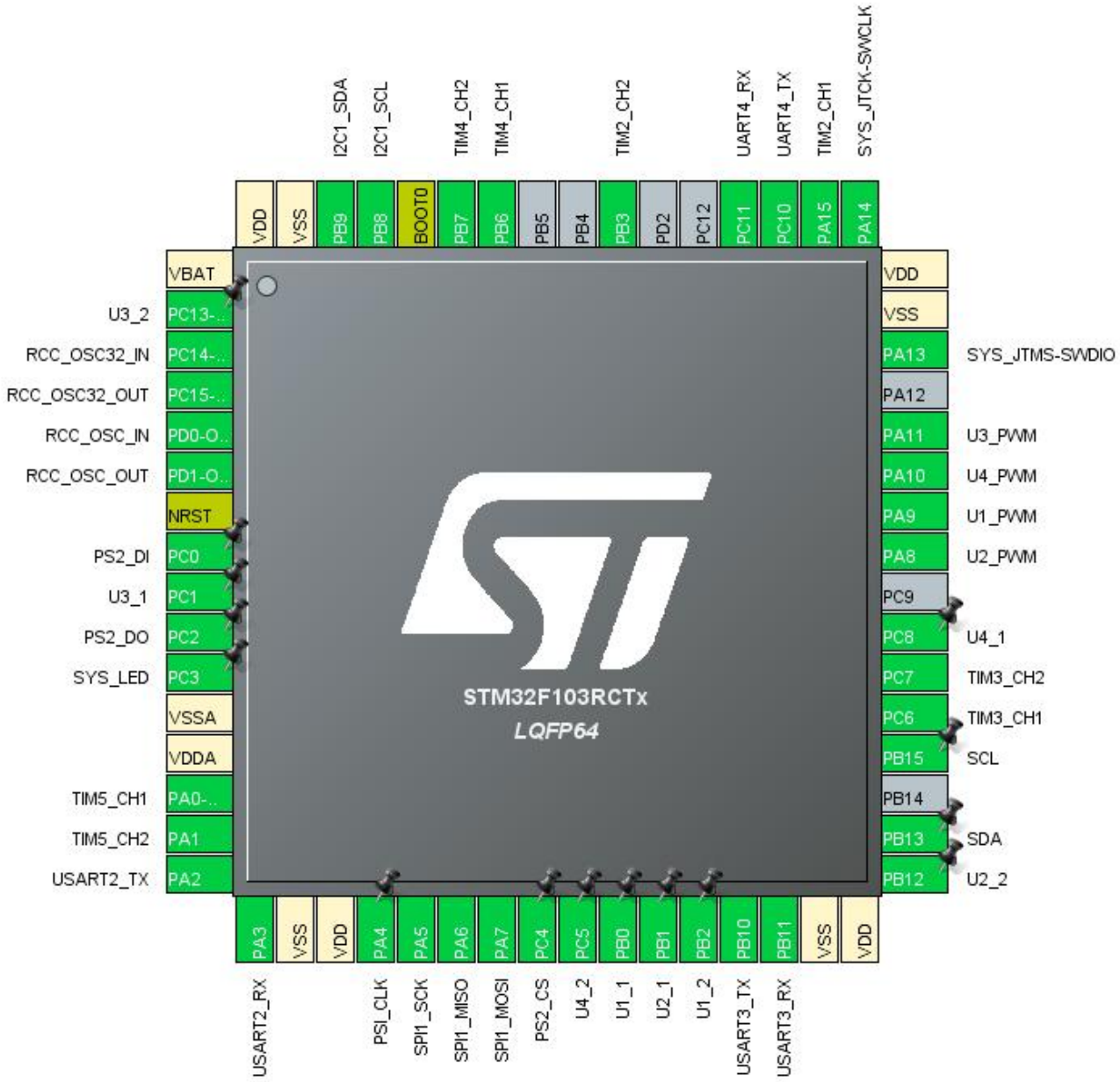
1.1. Project

Project Name	code_DIY
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	10/21/2019

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RCTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



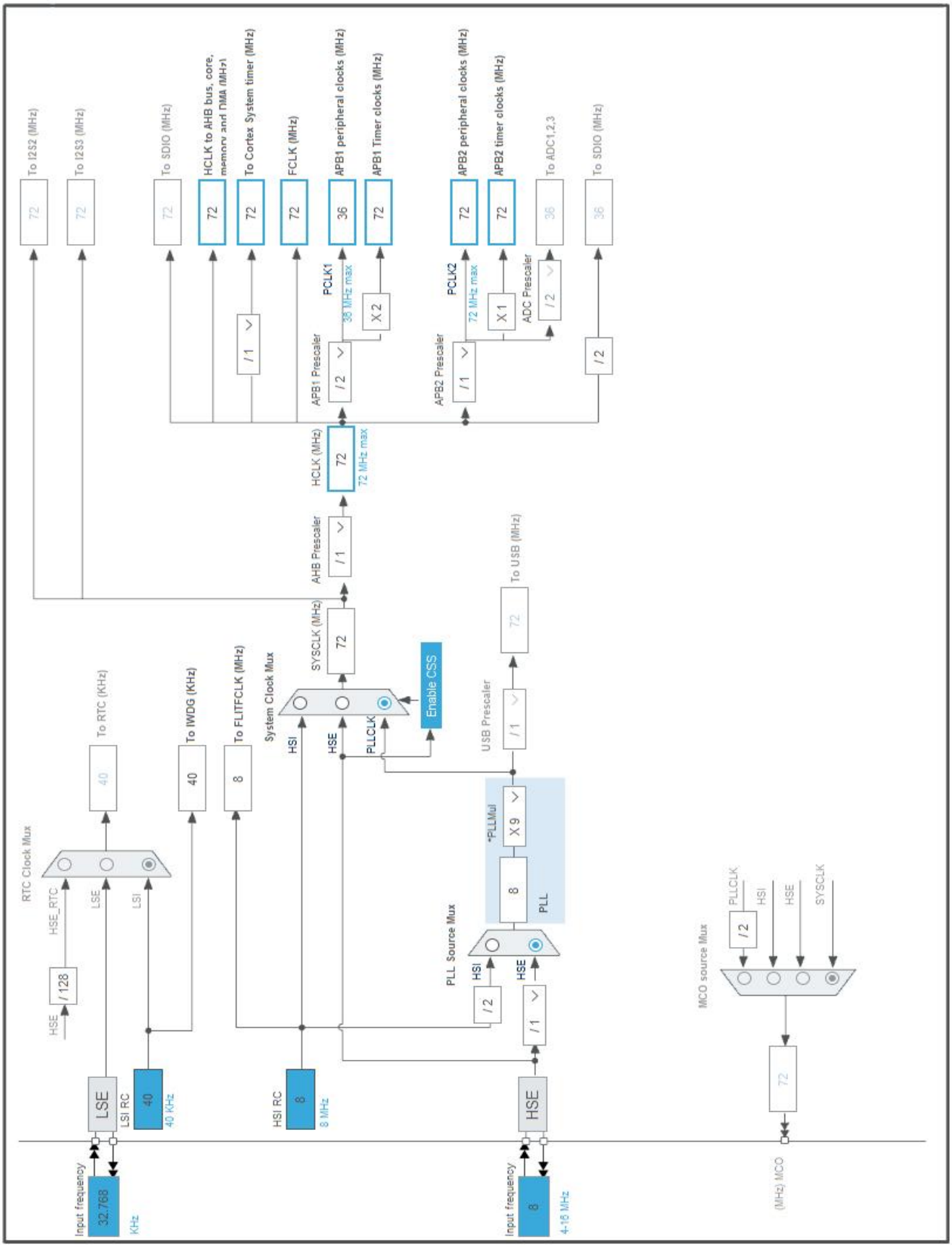
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	U3_2
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Input	PS2_DI
9	PC1 *	I/O	GPIO_Output	U3_1
10	PC2 *	I/O	GPIO_Output	PS2_DO
11	PC3 *	I/O	GPIO_Output	SYS_LED
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM5_CH1	
15	PA1	I/O	TIM5_CH2	
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	PSI_CLK
21	PA5	I/O	SPI1_SCK	
22	PA6	I/O	SPI1_MISO	
23	PA7	I/O	SPI1_MOSI	
24	PC4 *	I/O	GPIO_Output	PS2_CS
25	PC5 *	I/O	GPIO_Output	U4_2
26	PB0 *	I/O	GPIO_Output	U1_1
27	PB1 *	I/O	GPIO_Output	U2_1
28	PB2 *	I/O	GPIO_Output	U1_2
29	PB10	I/O	USART3_TX	
30	PB11	I/O	USART3_RX	
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	U2_2
34	PB13 *	I/O	GPIO_Output	SDA
36	PB15 *	I/O	GPIO_Output	SCL
37	PC6	I/O	TIM3_CH1	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
38	PC7	I/O	TIM3_CH2	
39	PC8 *	I/O	GPIO_Input	U4_1
41	PA8	I/O	TIM1_CH1	U2_PWM
42	PA9	I/O	TIM1_CH2	U1_PWM
43	PA10	I/O	TIM1_CH3	U4_PWM
44	PA11	I/O	TIM1_CH4	U3_PWM
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15	I/O	TIM2_CH1	
51	PC10	I/O	UART4_TX	
52	PC11	I/O	UART4_RX	
55	PB3	I/O	TIM2_CH2	
58	PB6	I/O	TIM4_CH1	
59	PB7	I/O	TIM4_CH2	
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	code_DIY
Project Folder	E:\\\\\\VSLAM_Car\STM32programe\code_DIY
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RCTx
Datasheet	14611_Rev12

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. I2C1

I2C: I2C

7.1.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.2. IWDG

mode: Activated

7.2.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	**64 ***
IWDG down-counter reload value	**1025 ***

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100

LSE Startup Timout Value (ms)	5000

7.4. SPI1

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.5. SYS

Debug: Serial Wire

Timebase Source: TIM7

7.6. TIM1

Clock Source : Internal Clock

Channel1: Output Compare CH1

Channel2: Output Compare CH2

Channel3: Output Compare CH3

Channel4: Output Compare CH4

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**18-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***

Internal Clock Division (CKD)	**Division by 4 ***
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 3:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 4:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

7.7. TIM2

Combined Channels: Encoder Mode

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.8. TIM3

Combined Channels: Encoder Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.9. TIM4

Combined Channels: Encoder Mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.10. TIM5

Combined Channels: Encoder Mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.11. TIM6

mode: Activated

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**720-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000-1 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.12. UART4

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.13. USART2

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.14. USART3

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	n/a	**High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	n/a	**High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	n/a	**High ***	
	PA6	SPI1_MISO	Input mode	No pull-up and no pull-down	**n/a**	
	PA7	SPI1_MOSI	Alternate Function Push Pull	n/a	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	U2_PWM
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	U1_PWM
	PA10	TIM1_CH3	Alternate Function Push Pull	n/a	Low	U4_PWM
	PA11	TIM1_CH4	Alternate Function Push Pull	n/a	Low	U3_PWM
TIM2	PA15	TIM2_CH1	Input mode	No pull-up and no pull-down	n/a	
	PB3	TIM2_CH2	Input mode	No pull-up and no pull-down	n/a	
TIM3	PC6	TIM3_CH1	Input mode	No pull-up and no pull-down	n/a	
	PC7	TIM3_CH2	Input mode	No pull-up and no pull-down	n/a	
TIM4	PB6	TIM4_CH1	Input mode	No pull-up and no pull-down	n/a	
	PB7	TIM4_CH2	Input mode	No pull-up and no pull-down	n/a	
TIM5	PA0-WKUP	TIM5_CH1	Input mode	No pull-up and no pull-down	n/a	
	PA1	TIM5_CH2	Input mode	No pull-up and no pull-down	n/a	
UART4	PC10	UART4_TX	Alternate Function Push Pull	n/a	**High ***	
	PC11	UART4_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	**High ***	
	PA3	USART2_RX	Input mode	No pull-up and no pull-down	**n/a**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USART3	PB10	USART3_TX	Alternate Function Push Pull	n/a	**High ***	
	PB11	USART3_RX	Input mode	No pull-up and no pull-down	**n/a**	
GPIO	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	U3_2
	PC0	GPIO_Input	Input mode	**Pull-down ***	n/a	PS2_DI
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	U3_1
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PS2_DO
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SYS_LED
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PSI_CLK
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PS2_CS
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	U4_2
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	U1_1
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	U2_1
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	U1_2
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	U2_2
	PB13	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	SDA
	PB15	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	SCL
	PC8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	U4_1

8.2. DMA configuration

DMA request	Stream	Direction	Priority
UART4_RX	DMA2_Channel3	Peripheral To Memory	Low
UART4_TX	DMA2_Channel5	Memory To Peripheral	Low
I2C1_RX	DMA1_Channel7	Peripheral To Memory	Low
I2C1_TX	DMA1_Channel6	Memory To Peripheral	Low
USART3_TX	DMA1_Channel2	Memory To Peripheral	Low

UART4_RX: DMA2_Channel3 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_TX: DMA2_Channel5 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C1_RX: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C1_TX: DMA1_Channel6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte

Memory Data Width:	Byte

USART3_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
TIM6 global interrupt	true	0	0
TIM7 global interrupt	true	0	0
DMA2 channel3 global interrupt	true	0	0
DMA2 channel4 and channel5 global interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
TIM5 global interrupt	unused		
UART4 global interrupt	unused		

*** User modified value**

9. Software Pack Report