1. Description

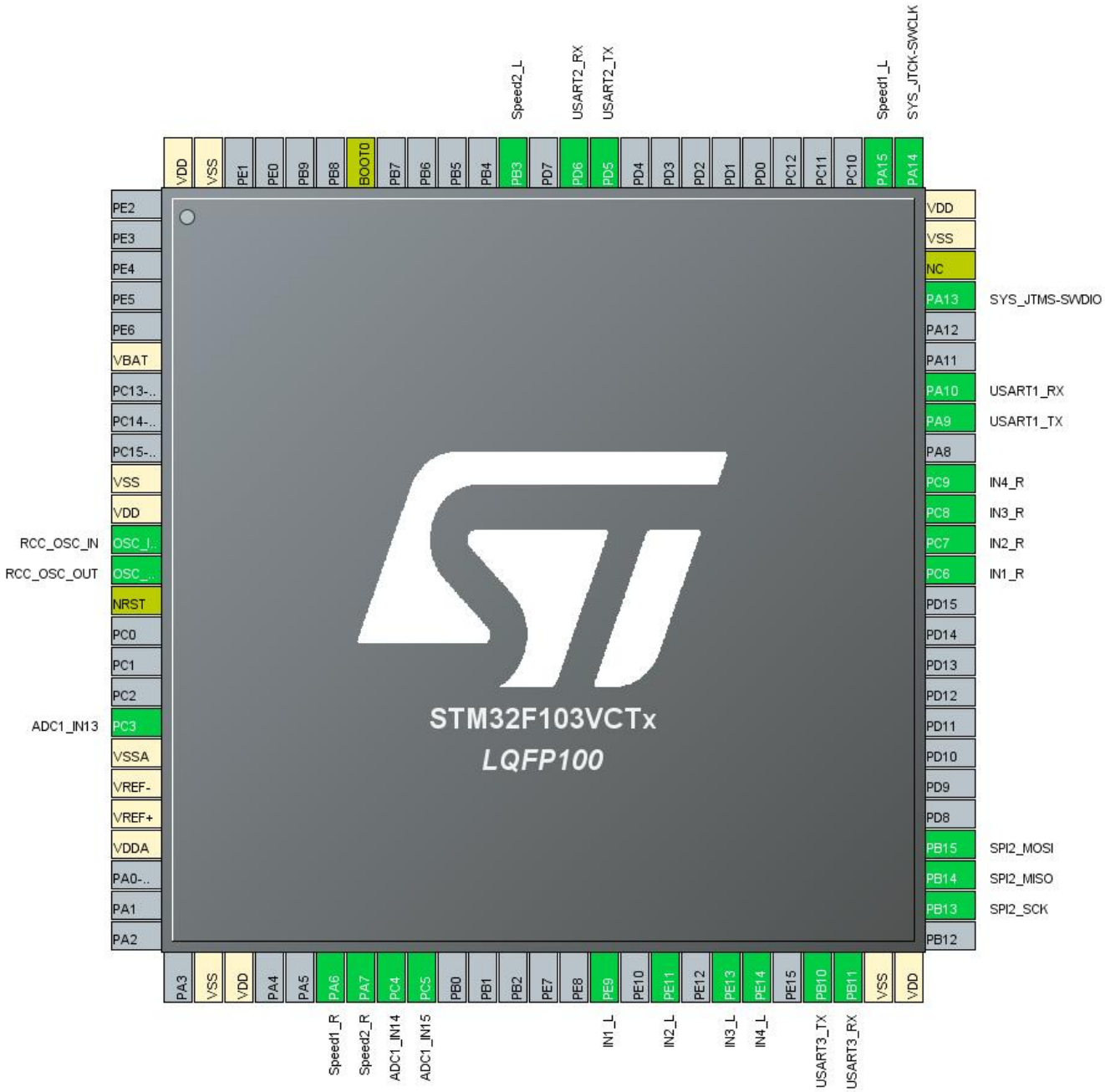
1.1. Project

Project Name	STM32Cube
Board Name	custom
Generated with:	STM32CubeMX 5.2.1
Date	10/04/2019

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103VCTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration

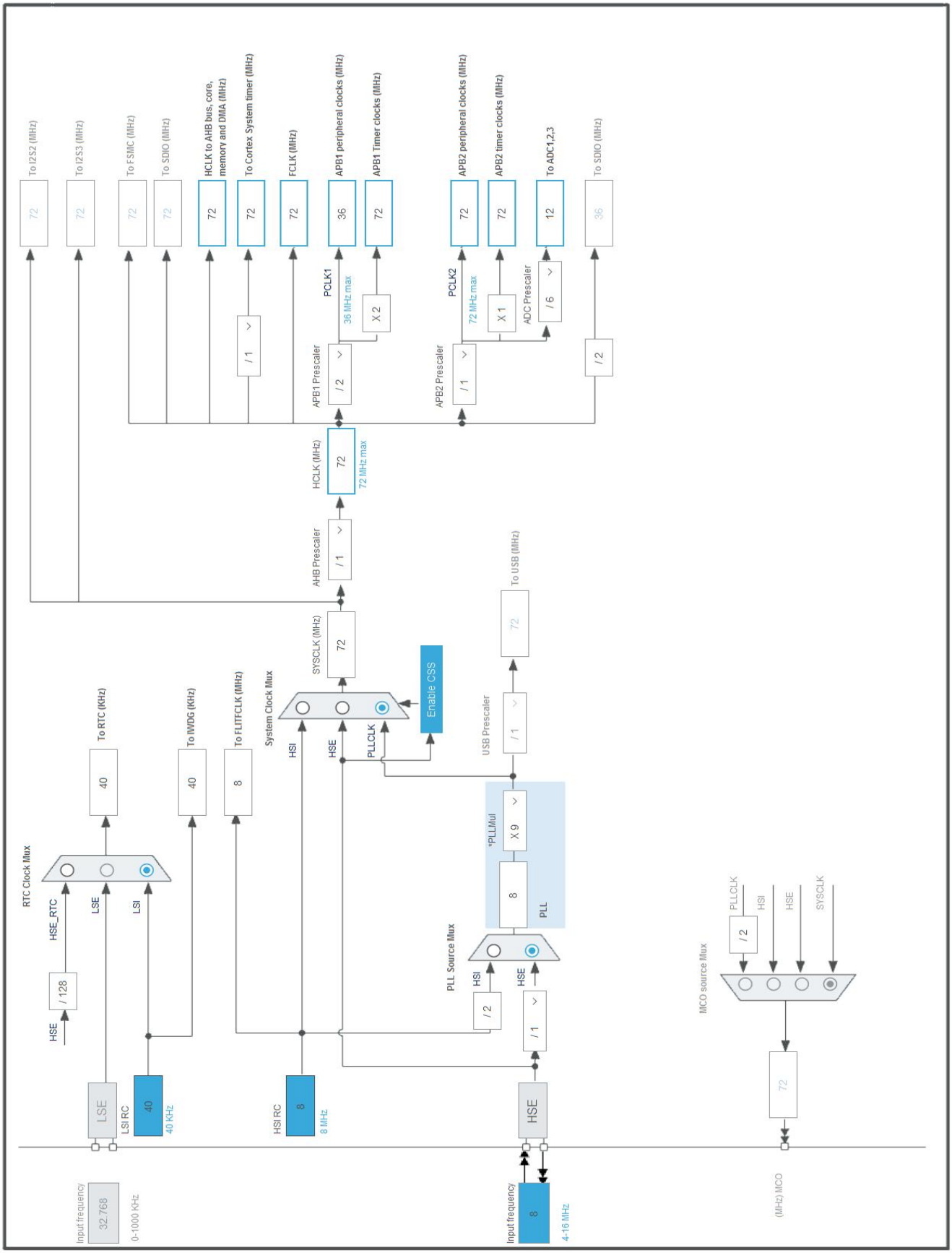


3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	OSC_IN	I/O	RCC_OSC_IN	
13	OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
18	PC3	I/O	ADC1_IN13	
19	VSSA	Power		
20	VREF-	Power		
21	VREF+	Power		
22	VDDA	Power		
27	VSS	Power		
28	VDD	Power		
31	PA6	I/O	TIM3_CH1	Speed1_R
32	PA7	I/O	TIM3_CH2	Speed2_R
33	PC4	I/O	ADC1_IN14	
34	PC5	I/O	ADC1_IN15	
40	PE9	I/O	TIM1_CH1	IN1_L
42	PE11	I/O	TIM1_CH2	IN2_L
44	PE13	I/O	TIM1_CH3	IN3_L
45	PE14	I/O	TIM1_CH4	IN4_L
47	PB10	I/O	USART3_TX	
48	PB11	I/O	USART3_RX	
49	VSS	Power		
50	VDD	Power		
52	PB13	I/O	SPI2_SCK	
53	PB14	I/O	SPI2_MISO	
54	PB15	I/O	SPI2_MOSI	
63	PC6	I/O	TIM8_CH1	IN1_R
64	PC7	I/O	TIM8_CH2	IN2_R
65	PC8	I/O	TIM8_CH3	IN3_R
66	PC9	I/O	TIM8_CH4	IN4_R
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	NC	NC		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15	I/O	TIM2_CH1	Speed1_L
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
89	PB3	I/O	TIM2_CH2	Speed2_L
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32Cube
Project Folder	E:\Myprograme\VSLAM_Car\STM32Cube
Toolchain / IDE	EWARM V8
Firmware Package Name and Version	STM32Cube FW_F1 V1.7.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103VCTx
Datasheet	14611_Rev12

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN13

mode: IN14

mode: IN15

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	**Channel 15 ***
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. IWDG

mode: Activated

7.2.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.4. RTC

mode: Activate Clock Source

7.4.1. Parameter Settings:

Calendar Time:

Data Format	BCD data format

General:

Auto Predivider Calculation	Enabled
Asynchronous Predivider value	Automatic Predivider Calculation Enabled
Output	Alarm pulse signal on the TAMPER pin

7.5. SPI2

Mode: Full-Duplex Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	Low

Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.6. SYS

Debug: Serial Wire

Timebase Source: TIM7

7.7. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**17 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	**Division by 4 ***
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1

Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.8. TIM2

Combined Channels: Encoder Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xffff-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***

____ Parameters for Channel 1 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.9. TIM3

Combined Channels: Encoder Mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xffff-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.10. TIM6

mode: Activated

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**720-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000-1 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.11. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: Output Compare CH4

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**17 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	**Division by 4 ***
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable

Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 4:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

7.12. USART1

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.13. USART2

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.14. USART3

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.15. WWDG

mode: Activated

7.15.1. Parameter Settings:

Watchdog Clocking:

WWDG counter clock prescaler	**8 ***
WWDG window value	**127 ***
WWDG free-running downcounter value	**127 ***

Watchdog Interrupt:

Early wakeup interrupt	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC3	ADC1_IN13	Analog mode	n/a	n/a	
	PC4	ADC1_IN14	Analog mode	n/a	n/a	
	PC5	ADC1_IN15	Analog mode	n/a	n/a	
RCC	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	n/a	**High ***	
	PB14	SPI2_MISO	Input mode	No pull-up and no pull-down	**n/a**	
	PB15	SPI2_MOSI	Alternate Function Push Pull	n/a	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	n/a	Low	IN1_L
	PE11	TIM1_CH2	Alternate Function Push Pull	n/a	Low	IN2_L
	PE13	TIM1_CH3	Alternate Function Push Pull	n/a	Low	IN3_L
	PE14	TIM1_CH4	Alternate Function Push Pull	n/a	Low	IN4_L
TIM2	PA15	TIM2_CH1	Input mode	No pull-up and no pull-down	n/a	Speed1_L
	PB3	TIM2_CH2	Input mode	No pull-up and no pull-down	n/a	Speed2_L
TIM3	PA6	TIM3_CH1	Input mode	No pull-up and no pull-down	n/a	Speed1_R
	PA7	TIM3_CH2	Input mode	No pull-up and no pull-down	n/a	Speed2_R
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	n/a	Low	IN1_R
	PC7	TIM8_CH2	Alternate Function Push Pull	n/a	Low	IN2_R
	PC8	TIM8_CH3	Alternate Function Push Pull	n/a	Low	IN3_R
	PC9	TIM8_CH4	Alternate Function Push Pull	n/a	Low	IN4_R
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART2	PD5	USART2_TX	Alternate Function Push Pull	n/a	**High ***	
	PD6	USART2_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART3	PB10	USART3_TX	Alternate Function Push Pull	n/a	**High ***	
	PB11	USART3_RX	Input mode	No pull-up and no pull-down	**n/a**	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low
USART3_TX	DMA1_Channel2	Memory To Peripheral	Low

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel2 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
USART3 global interrupt	true	0	0
TIM6 global interrupt	true	0	0
TIM7 global interrupt	true	0	0
Window watchdog interrupt	unused		
PVD interrupt through EXTI line 16	unused		
RTC global interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
SPI2 global interrupt	unused		
TIM8 break interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger and commutation interrupts	unused		
TIM8 capture compare interrupt	unused		

*** User modified value**

9. Software Pack Report