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Class	Document	Message
		Successful Compile for
	·	

Design Rules Verification ReportFilename : C:\Users\leona\OneDrive\Documents\Perso\projets_persos\Switch HP\Altium\A

Warnings 0 Rule Violations 4

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.4mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	4
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=15mm) (Preferred=1mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.5mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=1mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	4

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Via (13mm,66mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned
Un-Routed Net Constraint: Via (13mm,73mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned
Un-Routed Net Constraint: Via (4mm,66mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned
Un-Routed Net Constraint: Via (4mm,73mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned

Line #	Name	Description	Designator Quanti	ty	Manufacturer 1	Manufacturer Part Number 1	Manufacturer Lifecycle 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Subtotal 1
4 pins	EC481508		J1	1							
8 pins speaker connector			J4, J5	2							
ESP32	ESP32-DEVKITC-32D	Eval Board For Esp-Wroom- 32	U1	1							
ESP32 protectio n for inductive loads	ULN2003A	Integrated Circuit	IC1	1							
Relay (Speaker level)	G2RL-24-DC5	Relay or Contactor	K1, K2, K3, K4	4							
Relay (line level)	G6K-2P-Y-DC5	Relay or Contactor	K5, K6, K7	3							
Jack connector	734101	Undefined or Miscellaneous	U2, U3, U4, U5	4							