PLL calc		BCK Divider (RBCK)	SCK (MHz)	J.D (R = 1) (PLL K Factor)	DACCLK (16x FS)	DACDivider (DDAC)	DSPCK (MHz)	DSPDivider (DDSP)	IDAC	Charge Pump Divider (CPCK)	CPCK (MHz)	OSR Divider	OSRCLK (MHz)
Clock IN (P = 1) (MHz)	12												
Number of channels	2												
Bits résolution (LRCLK)(FS)	32												
44.1	2.8224	32	90.3168	7.52640	0.7056	128	45.1584	2	1024	1	0.7056	1	0.7056
48	3.072	32	98.304	8.19200	0.768	128	49.152	2	1024	1	0.768	1	0.768
88.2	5.6448	16	90.3168	7.52640	1.4112	64	45.1584	2	512	1	1.4112	1	1.4112
96	6.144	16	98.304	8.19200	1.536	64	49.152	2	512	1	1.536	1	1.536
176.4	11.2896	8	90.3168	7.52640	2.8224	32	45.1584	2	256	1	2.8224	1	2.8224
192	12.288	8	98.304	8.19200	3.072	32	49.152	2	256	1	3.072	1	3.072
352.8	22.5792	4	90.3168	7.52640	5.6448	16	45.1584	2	128	1	5.6448	1	5.6448
384	24.576	4	98.304	8.19200	6.144	16	49.152	2	128	1	6.144	1	6.144
Number of channels	2												
Bits résolution (LRCLK)	24												
44.1	2.1168	32	67.7376	5.64480	0.7056	96	67.7376	1	1536	1	0.7056	1	0.7056
48	2.304	32	73.728	6.14400	0.768	96	73.728	1	1536	1	0.768	1	0.768
88.2	4.2336	16	67.7376	5.64480	1.4112	48	67.7376	1	768	1	1.4112	1	1.4112
96	4.608	16	73.728	6.14400	1.536	48	73.728	1	768	1	1.536	1	1.536
176.4	8.4672	8	67.7376	5.64480	2.8224	24	67.7376	1	384	1	2.8224	1	2.8224
192	9.216	8	73.728	6.14400	3.072	24	73.728	1	384	1	3.072	1	3.072
352.8	16.9344	4	67.7376	5.64480	5.6448	12	67.7376	1	192	1	5.6448	1	5.6448
384	18.432	4	73.728	6.14400	6.144	12	73.728	1	192	1	6.144	1	6.144
Number of channels	2												
Bits résolution (LRCLK)	16												
44.1	1.4112	64	90.3168	7.52640	0.7056	128	45.1584	2	1024	1	0.7056	1	0.7056
48	1.536	64	98.304	8.19200	0.768	128	49.152	2	1024	1	0.768	1	0.768
88.2	2.8224	32	90.3168	7.52640	1.4112	64	45.1584	2	512	1	1.4112	1	1.4112
96	3.072	32	98.304	8.19200	1.536	64	49.152	2	512	1	1.536	1	1.536
176.4	5.6448	16	90.3168	7.52640	2.8224	32	45.1584	2	256	1	2.8224	1	2.8224
192	6.144	16	98.304	8.19200	3.072	32	49.152	2	256	1	3.072	1	3.072
352.8	11.2896	8	90.3168	7.52640	5.6448	16	45.1584	2	128	1	5.6448	1	5.6448
384	12.288	8	98.304	8.19200	6.144	16	49.152	2	128	1	6.144	1	6.144

PLL calc (Clock is a bit TOO fast)						BCK Divider (RBCK)	SCK (MHz)	J.D (R = 1) (PLL K Factor)	DACCLK (16x FS)	DACDivider (DDAC)	DSPCK (MHz)	DSPDivider (DDSP)	IDAC	Charge Pump Divider (CPCK)	CPCK (MHz)	OSR Divider	OSRCLK (MHz)
Clock IN) (MHz)	12.004 MHz		P = 1		12.004												
Number of channels				2													
Bits résolution (LRCLK)(FS)				32													
				LRLCK	BCK												
LRCLK	BCK	LRLCK	BCK	% ERR	% ERR												
44.1	2.8224	44.1147	2.8233408	0.033%	0.033%	32	90.34691	7.52640	0.705835	128	45.17345	2	1024	1	0.705835	1	0.705835
48	3.072	48.016	3.073024	0.033%	0.033%	32	98.33677	8.19200	0.768256	128	49.16838	2	1024	1	0.768256	1	0.768256
88.2	5.6448	88.2294	5.6466816	0.033%	0.033%	16	90.34691	7.52640	1.41167	64	45.17345	2	512	1	1.41167	1	1.41167
96	6.144	96.032	6.146048	0.033%	0.033%	16	98.33677	8.19200	1.536512	64	49.16838	2	512	1	1.536512	1	1.536512
176.4	11.2896	176.4588	11.2933632	0.033%	0.033%	8	90.34691	7.52640	2.823341	32	45.17345	2	256	1	2.823341	1	2.823341
192	12.288	192.064	12.292096	0.033%	0.033%	8	98.33677	8.19200	3.073024	32	49.16838	2	256	1	3.073024	1	3.073024
352.8	22.5792	352.9176	22.5867264	0.033%	0.033%	4	90.34691	7.52640	5.646682	16	45.17345	2	128	1	5.646682	1	5.646682
384	24.576	384.128	24.584192	0.033%	0.033%	4	98.33677	8.19200	6.146048	16	49.16838	2	128	1	6.146048	1	6.146048
Number of channels				2													
Bits résolution (LRCLK)				24													
				LRLCK	BCK												
		LRLCK	BCK	% ERR	% ERR												
44.1	2.1168	44.1147	2.1175056	0.033%	0.033%	32	67.76018	5.64480	0.705835	96	67.76018	1	1536	1	0.705835	1	0.705835
48	2.304	48.016	2.304768	0.033%	0.033%	32	73.75258	6.14400	0.768256	96	73.75258	1	1536	1	0.768256	1	0.768256
88.2	4.2336	88.2294	4.2350112	0.033%	0.033%	16	67.76018	5.64480	1.41167	48	67.76018	1	768	1	1.41167	1	1.41167
96	4.608	96.032	4.609536	0.033%	0.033%	16	73.75258	6.14400	1.536512	48	73.75258	1	768	1	1.536512	1	1.536512
176.4	8.4672	176.4588	8.4700224	0.033%	0.033%	8	67.76018	5.64480	2.823341	24	67.76018	1	384	1	2.823341	1	2.823341
192	9.216	192.064	9.219072	0.033%	0.033%	8	73.75258	6.14400	3.073024	24	73.75258	1	384	1	3.073024	1	3.073024
352.8	16.9344	352.9176	16.9400448	0.033%	0.033%	4	67.76018	5.64480	5.646682	12	67.76018	1	192	1	5.646682	1	5.646682
384	18.432	384.128	18.438144	0.033%	0.033%	4	73.75258	6.14400	6.146048	12	73.75258	1	192	1	6.146048	1	6.146048
Number of channels				2													
Bits résolution (LRCLK)				16													
				LRLCK	BCK												
		LRLCK	BCK	% ERR	% ERR												
44.1	1.4112	44.1147	1.4116704	0.033%	0.033%	64	90.34691	7.52640	0.705835	128	45.17345	2	1024	1	0.705835	1	0.705835
48	1.536	48.016	1.536512	0.033%	0.033%	64	98.33677	8.19200	0.768256	128	49.16838	2	1024	1	0.768256	1	0.768256
88.2	2.8224	88.2294	2.8233408	0.033%	0.033%	32	90.34691	7.52640	1.41167	64	45.17345	2	512	1	1.41167	1	1.41167
96	3.072	96.032	3.073024	0.033%	0.033%	32	98.33677	8.19200	1.536512	64	49.16838	2	512	1	1.536512	1	1.536512
176.4	5.6448	176.4588	5.6466816	0.033%	0.033%	16	90.34691	7.52640	2.823341	32	45.17345	2	256	1	2.823341	1	2.823341
192	6.144	192.064	6.146048	0.033%	0.033%	16	98.33677	8.19200	3.073024	32	49.16838	2	256	1	3.073024	1	3.073024
352.8	11.2896	352.9176	11.2933632	0.033%	0.033%	8	90.34691	7.52640	5.646682	16	45.17345	2	128	1	5.646682	1	5.646682
384	12.288	384.128	12.292096	0.033%	0.033%	8	98.33677	8.19200	6.146048	16	49.16838	2	128	1	6.146048	1	6.146048

PLL calc (Clock is a bit TOO Slow)						BCK Divider (RBCK)	SCK (MHz)	J.D (R = 1) (PLL K Factor)	DACCLK (16x FS)	DACDivider (DDAC)	DSPCK (MHz)	DSPDivider (DDSP)	IDAC	Charge Pump Divider (CPCK)	CPCK (MHz)	OSR Divider	OSRCLK (MHz)
Clock IN) (MHz)	11.995 MHz		P = 1		11.995												
Number of channels				2													
Bits résolution (LRCLK)(FS)				32													
				LRLCK	BCK												
LRCLK	BCK	LRLCK	BCK	% ERR	% ERR												
44.1	2.8224	44.081625	2.821224	0.04%	0.04%	32	90.27917	7.52640	0.705306	128	45.13958	2	1024	1	0.705306	1	0.705306
48	3.072	47.98	3.07072	0.04%	0.04%	32	98.26304	8.19200	0.76768	128	49.13152	2	1024	1	0.76768	1	0.76768
88.2	5.6448	88.16325	5.642448	0.04%	0.04%	16	90.27917	7.52640	1.410612	64	45.13958	2	512	1	1.410612	1	1.410612
96	6.144	95.96	6.14144	0.04%	0.04%	16	98.26304	8.19200	1.53536	64	49.13152	2	512	1	1.53536	1	1.53536
176.4	11.2896	176.3265	11.284896	0.04%	0.04%	8	90.27917	7.52640	2.821224	32	45.13958	2	256	1	2.821224	1	2.821224
192	12.288	191.92	12.28288	0.04%	0.04%	8	98.26304	8.19200	3.07072	32	49.13152	2	256	1	3.07072	1	3.07072
352.8	22.5792	352.653	22.569792	0.04%	0.04%	4	90.27917	7.52640	5.642448	16	45.13958	2	128	1	5.642448	1	5.642448
384	24.576	383.84	24.56576	0.04%	0.04%	4	98.26304	8.19200	6.14144	16	49.13152	2	128	1	6.14144	1	6.14144
Number of channels				2													
Bits résolution (LRCLK)				24													
				LRLCK	BCK												
		LRLCK	BCK	% ERR	% ERR												
44.1	2.1168	44.081625	2.115918	0.04%	0.04%	32	67.70938	5.64480	0.705306	96	67.70938	1	1536	1	0.705306	1	0.705306
48	2.304	47.98	2.30304	0.04%	0.04%	32	73.69728	6.14400	0.76768	96	73.69728	1	1536	1	0.76768	1	0.76768
88.2	4.2336	88.16325	4.231836	0.04%	0.04%	16	67.70938	5.64480	1.410612	48	67.70938	1	768	1	1.410612	1	1.410612
96	4.608	95.96	4.60608	0.04%	0.04%	16	73.69728	6.14400	1.53536	48	73.69728	1	768	1	1.53536	1	1.53536
176.4	8.4672	176.3265	8.463672	0.04%	0.04%	8	67.70938	5.64480	2.821224	24	67.70938	1	384	1	2.821224	1	2.821224
192	9.216	191.92	9.21216	0.04%	0.04%	8	73.69728	6.14400	3.07072	24	73.69728	1	384	1	3.07072	1	3.07072
352.8	16.9344	352.653	16.927344	0.04%	0.04%	4	67.70938	5.64480	5.642448	12	67.70938	1	192	1	5.642448	1	5.642448
384	18.432	383.84	18.42432	0.04%	0.04%	4	73.69728	6.14400	6.14144	12	73.69728	1	192	1	6.14144	1	6.14144
Number of channels				2													
Bits résolution (LRCLK)				16													
				LRLCK	BCK												
		LRLCK	BCK	% ERR	% ERR												
44.1	1.4112	44.081625	1.410612	0.04%	0.04%	64	90.27917	7.52640	0.705306	128	45.13958	2	1024	1	0.705306	1	0.705306
48	1.536	47.98	1.53536	0.04%	0.04%	64	98.26304	8.19200	0.76768	128	49.13152	2	1024	1	0.76768	1	0.76768
88.2	2.8224	88.16325	2.821224	0.04%	0.04%	32	90.27917	7.52640	1.410612	64	45.13958	2	512	1	1.410612	1	1.410612
96	3.072	95.96	3.07072	0.04%	0.04%	32	98.26304	8.19200	1.53536	64	49.13152	2	512	1	1.53536	1	1.53536
176.4	5.6448	176.3265	5.642448	0.04%	0.04%	16	90.27917	7.52640	2.821224	32	45.13958	2	256	1	2.821224	1	2.821224
192	6.144	191.92	6.14144	0.04%	0.04%	16	98.26304	8.19200	3.07072	32	49.13152	2	256	1	3.07072	1	3.07072
352.8	11.2896	352.653	11.284896	0.04%	0.04%	8	90.27917	7.52640	5.642448	16	45.13958	2	128	1	5.642448	1	5.642448
384	12.288	383.84	12.28288	0.04%	0.04%	8	98.26304	8.19200	6.14144	16	49.13152	2	128	1	6.14144	1	6.14144