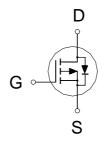
P-Channel Logic Level Enhancement Mode Field Effect Transistor

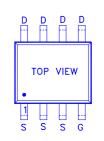
P2003EVG

Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	R _{DS(ON)}	I _D		
-30	20m	-9A		





4 :GATE 5,6,7,8 :DRAIN 1,2,3 :SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST	SYMBOL	LIMITS	UNITS	
Drain-Source Voltage	V_{DS}	-30	V	
Gate-Source Voltage	V_{GS}	±20	V	
Continuous Drain Current	T _C = 25 °C		-9	
	T _C = 70 °C	- I _D	-8	Α
Pulsed Drain Current ¹	I _{DM}	-50		
Dower Dissipation	T _C = 25 °C	Б.	2.5	W
Power Dissipation	T _C = 70 °C	$ P_D$	1.3	VV
Operating Junction & Storage Tem	T_j, T_{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{ heta JC}$		25	°C / W
Junction-to-Ambient	$R_{ hetaJA}$		50	°C/W

¹Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	CVMPOL	TEST CONDITIONS	LIMITS			UNIT	
PARAMETER	SYMBOL TEST CONDITIONS		MIN	TYP	MAX	ONI	
		STATIC					
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1	-1.5	-3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1		
		$V_{DS} = -20V, V_{GS} = 0V, T_{J} = 125 \text{ °C}$			-10	μΑ	
On-State Drain Current ¹	I _{D(ON)}	$V_{DS} = -5V, V_{GS} = -10V$	-50			Α	
Drain-Source On-State	D	$V_{GS} = -4.5V, I_D = -7A$		25	35	~	
Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -9A$		15	20	m	
Forward Transconductance ¹	g fs	$V_{DS} = -10V, I_{D} = -9A$		24		S	

²Duty cycle ≤ 1%

P-Channel Logic Level Enhancement Mode Field Effect Transistor

P2003EVG SOP-8 Lead-Free

DYNAMIC							
Input Capacitance	C _{iss}		1610				
Output Capacitance	C _{oss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$	410		pF		
Reverse Transfer Capacitance	C _{rss}] [200				
Total Gate Charge ²	Q_g		17	24			
Gate-Source Charge ²	Q_{gs}	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = -10V,$	5		nC		
Gate-Drain Charge ²	Q_{gd}	I _D = -9A	6				
Turn-On Delay Time ²	t _{d(on)}		5.7				
Rise Time ²	t _r	$V_{DS} = -15V, R_{L} = 1$	10		nS		
Turn-Off Delay Time ²	t _{d(off)}	$I_D \cong -1A, V_{GS} = -10V, R_{GS} = 6$	18		113		
Fall Time ²	t _f		5				
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)							
Continuous Current	Is			-2.1	Α		
Pulsed Current ³	I _{SM}			-4	A		
Forward Voltage ¹	V _{SD}	$I_F = -1A$, $V_{GS} = 0V$		-1.2	V		

¹Pulse test : Pulse Width ≤ 300 μ sec, Duty Cycle ≤ 2%.

REMARK: THE PRODUCT MARKED WITH "P2003EVG", DATE CODE or LOT #

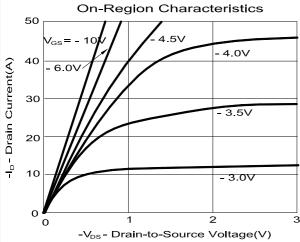
Orders for parts with Lead-Free plating can be placed using the PXXXXXXG parts name.

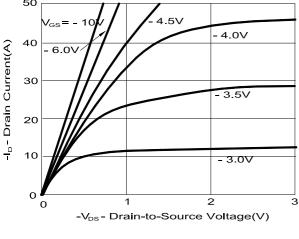
²Independent of operating temperature.

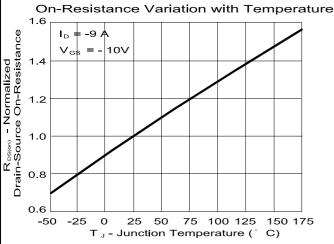
³Pulse width limited by maximum junction temperature.

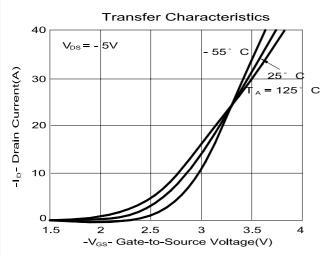
P-Channel Logic Level Enhancement Mode Field Effect Transistor

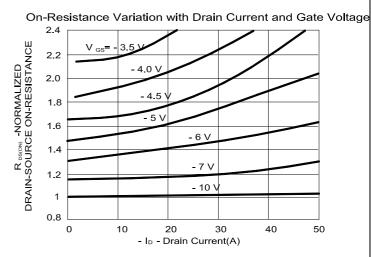
P2003EVG

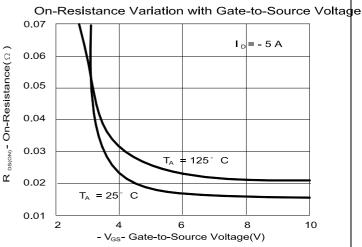


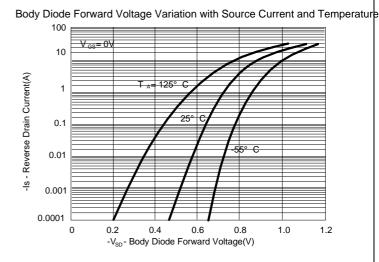






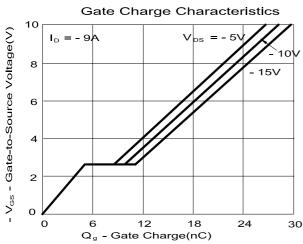


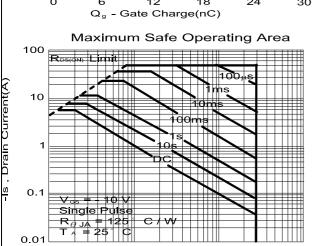




P-Channel Logic Level Enhancement Mode Field Effect Transistor

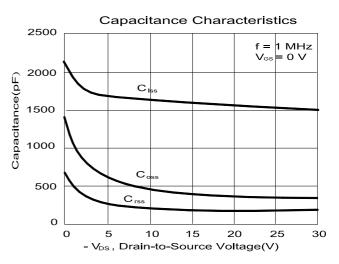
P2003EVG SOP-8 Lead-Free

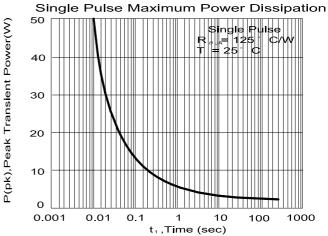


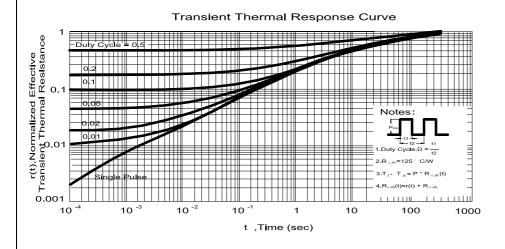


-V_{SD}, Drain - Source Voltage(V)

0.1







P-Channel Logic Level Enhancement Mode Field Effect Transistor

P2003EVG SOP-8 Lead-Free

SOIC-8(D) MECHANICAL DATA

Dimension	mm			Diagramaia	mm		
	Min.	Тур.	Max.	Dimension	Min.	Тур.	Max.
А	4.8	4.9	5.0	Н	0.5	0.715	0.83
В	3.8	3.9	4.0	I	0.18	0.254	0.25
С	5.8	6.0	6.2	J		0.22	
D	0.38	0.445	0.51	К	0°	4°	8°
Е		1.27		L			
F	1.35	1.55	1.75	М			
G	0.1	0.175	0.25	N			

