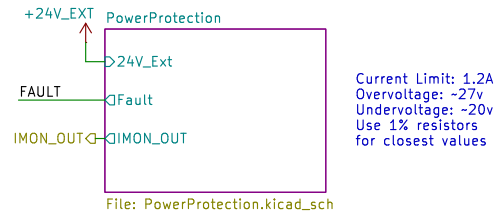
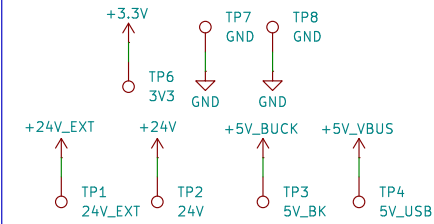


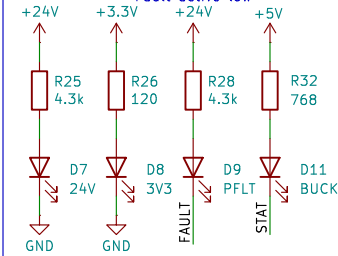
## Power Protection



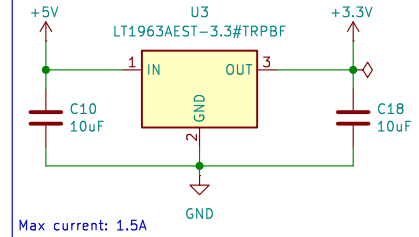
## Testpoints



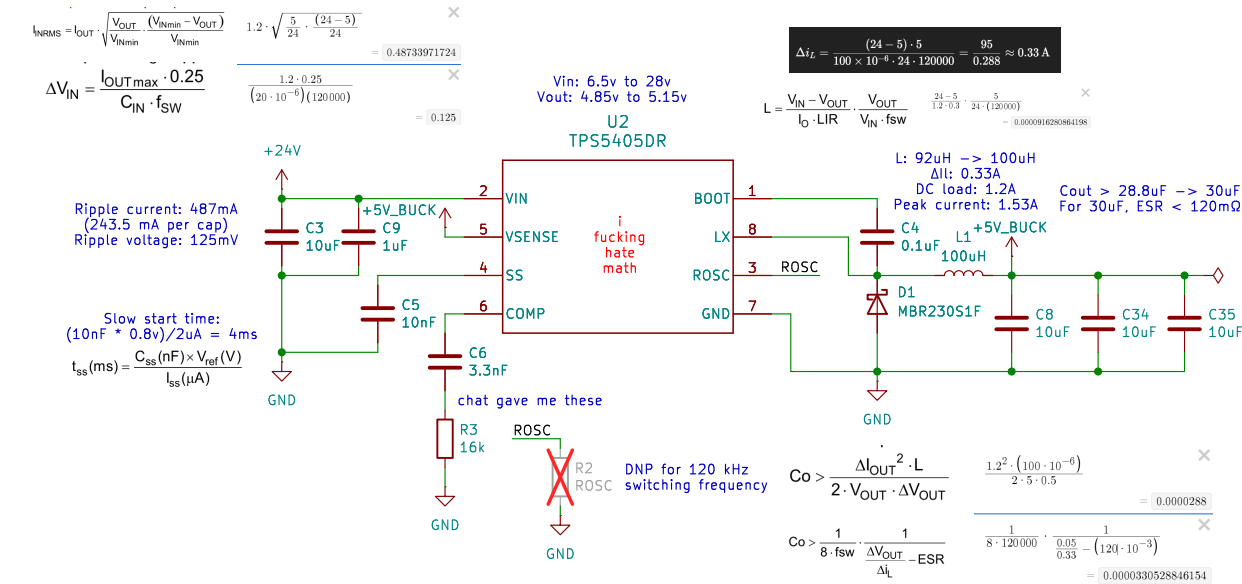
## Indicators



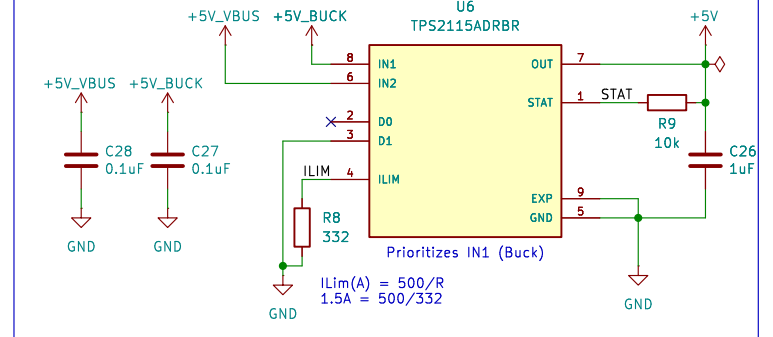
## 5->3.3v LDO



## 24->5v Buck Converter



## 5v Power Mux



Sheet: /PowerDist/  
File: PowerDist.kicad\_sch

## Title: Power Distribution

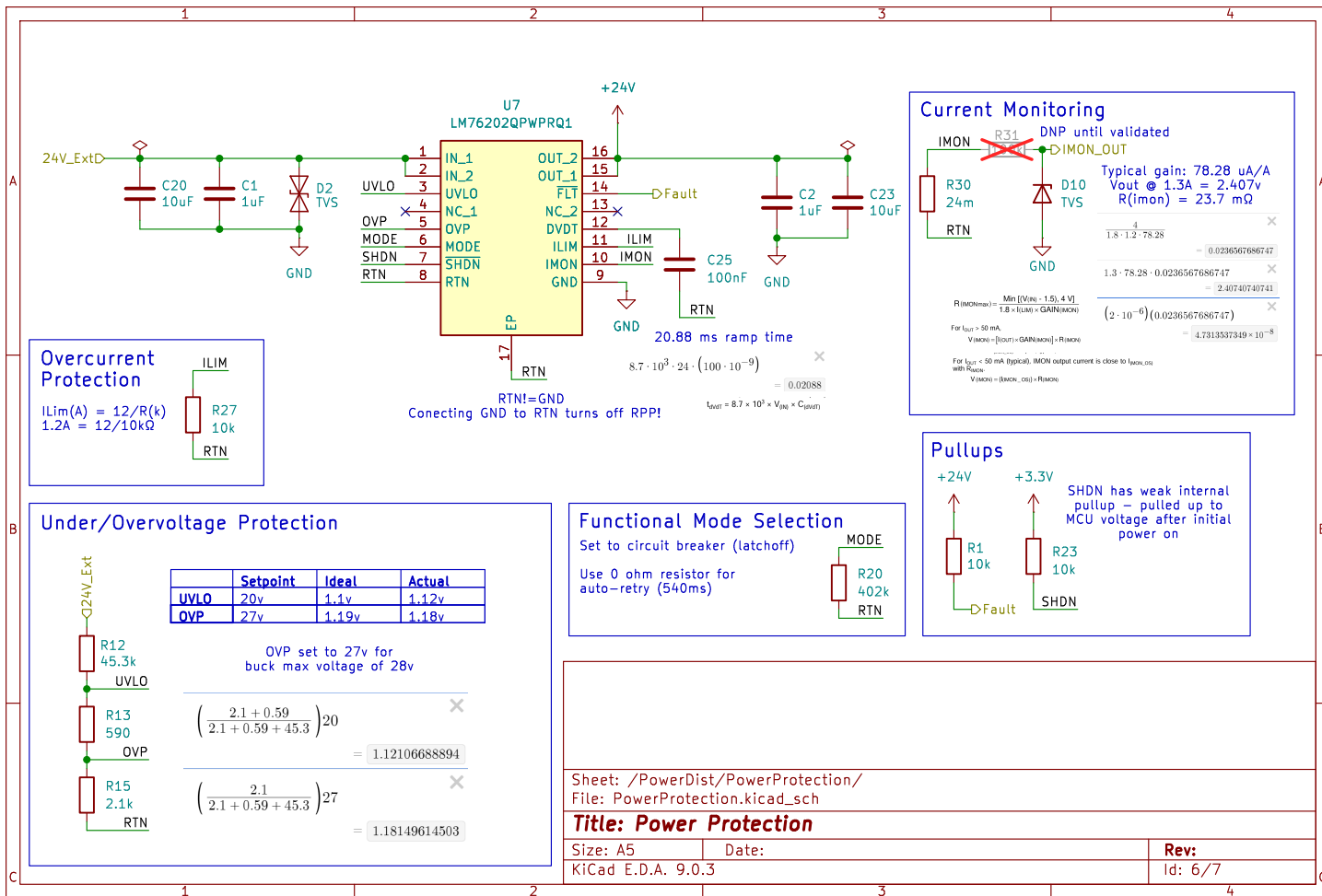
Size: A4

Date:

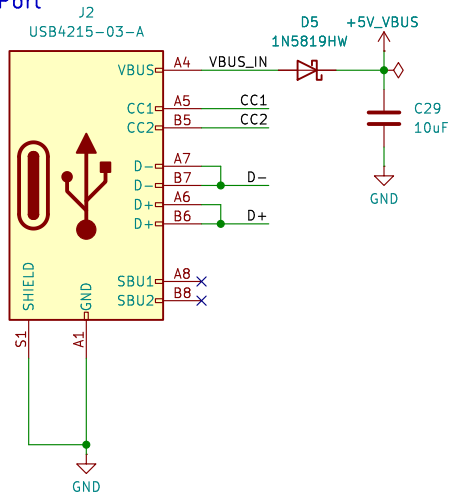
KiCad E.D.A. 9.0.3

Rev:

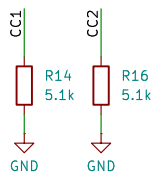
Id: 4/7



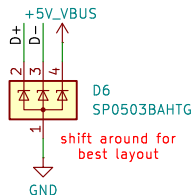
## USB-C Port



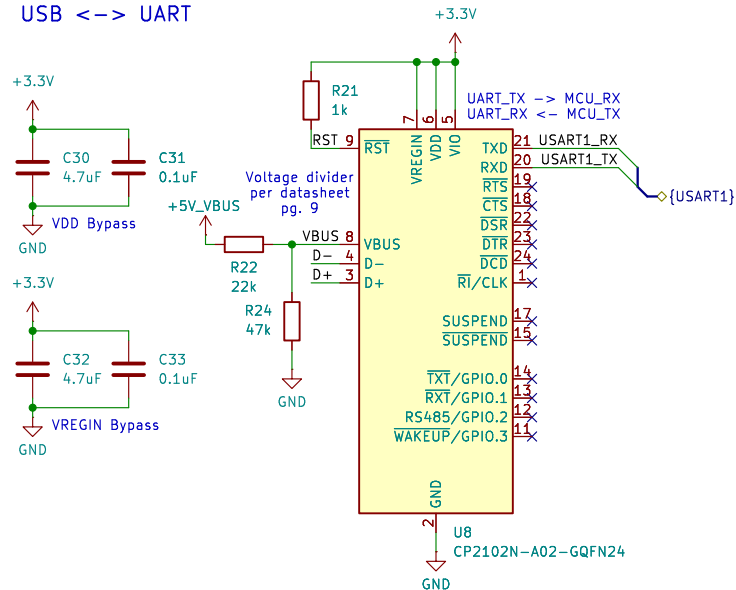
## CCx Pulldown



## USB Protection



## USB <--> UART



Sheet: /USB/  
File: USB.kicad\_sch

**Title: USB**

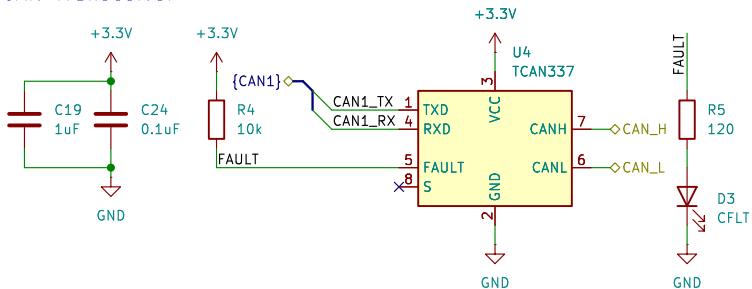
Size: A5  
KiCad E.D.A. 9.0.3

Date:

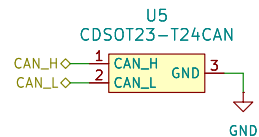
Rev:

Id: 3/7

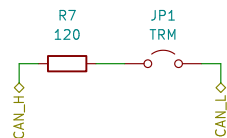
## CAN Transceiver



## CAN Bus Protection



## CAN Bus Termination



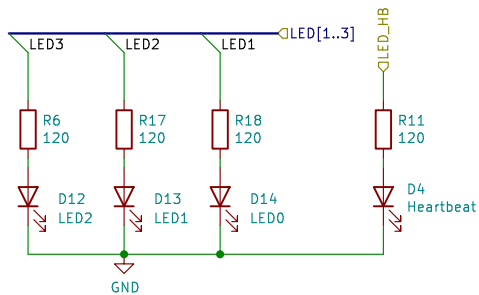
Sheet: /CAN/  
File: CAN.kicad\_sch

**Title: CAN**

Size: A5  
KiCad E.D.A. 9.0.3

Date:

Rev:  
Id: 2/7



Sheet: /LEDs/  
File: Leds.kicad\_sch

**Title: LEDs**

Size: A5  
KiCad E.D.A. 9.0.3

Date:

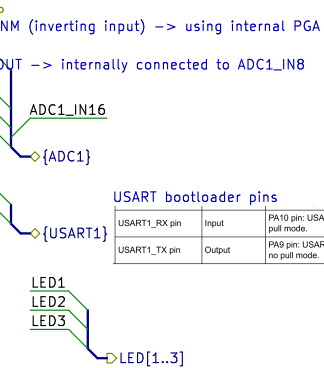
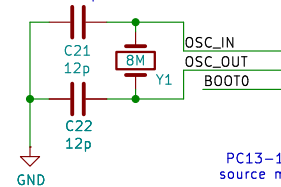
Rev:

Id: 5/7

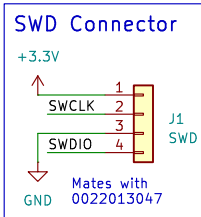
## Bypass/Separation

The diagram illustrates the bypass and separation capacitors for VDD and VDDA. It shows two main sections:

- VDD Bypass Caps:** A series of capacitors (C13, C14, C16, C17) connected between VDD and GND. C13 is 4.7uF, C14 is 100nF, C16 is 100nF, and C17 is 100nF.
- VDDA Bypass Caps:** A series of capacitors (C12, C15) connected between VDDA and GND. C12 is 100nF and C15 is 100nF.
- VDDA Separation:** A FerriteBead (FB4) is connected between VDD and VDDA. A capacitor (C7, 100nF) is connected between VDDA and GND.



USART1_RX pin	Input	PA10 pin: USART1 in reception mode. Used in input no pull mode.
USART1_TX pin	Output	PA9 pin: USART1 in transmission mode. Used in input no pull mode.



## SPI Protection

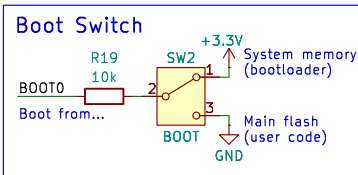
The diagrams illustrate the SPI protection circuit for two components, CR2 and CR1, both identified as D5V0P4UR6S0-7. Each component is represented by a rectangular box containing a 3x3 grid of diodes, indicating bidirectional protection for the SPI lines.

**CR2 D5V0P4UR6S0-7:**

- Inputs:** SPI1\_NSS (pin 1), SPI1\_SCK (pin 3), and GND (pin 4).
- Outputs:** SPI1\_MISO (pin 6) and SPI1\_MOSI (pin 5).
- Power:** +3.3V is connected to pin 6.

**CR1 D5V0P4UR6S0-7:**

- Inputs:** SPI2\_MISO (pin 1), SPI2\_NSS (pin 3), and GND (pin 4).
- Outputs:** SPI2\_MOSI (pin 6) and SPI2\_SCK (pin 5).
- Power:** +3.3V is connected to pin 6.



# Primary Pin Functions

add list of alternate functions

STM32L431CBTx  
LQFP48

Pinout details:

- Top Edge:** VDD, VSS, CAN1\_TX, CAN1\_RX, I2C1\_BDA, I2C1\_SCL, I2C1\_SDA, SPI1\_SCK, GPIO\_Output, SYS\_JTDO-SWCLK
- Right Edge:** VDD, VSS, SYS\_JTMS-SWDIO, PA13, PA12, SPI1\_MOSI, PA11, SPI1\_MISO, PA10, USART1\_RX, PA9, USART1\_TX, PA8, GPIO\_Output, PA7, SPI2\_MOSI, PA6, SPI2\_MISO, PA5, SPI2\_NSS, PA4, VDD
- Bottom Edge:** VSS, SPI2\_SCK, GPIO\_Output, SPI1\_SCK, SPI1\_MISO, ADC1\_IN16, ADC1\_IN15, ADC1\_IN14, ADC1\_IN13, ADC1\_IN12, ADC1\_IN11, ADC1\_IN10, ADC1\_IN9, SPI1\_VOUT
- Left Edge:** VBAT, PC13, PC14, PC15, PA15, PA14, PA13, PA12, PA11, PA10, PA9, PA8, PA7, PA6, PA5, PA4, PA3, PA2, PA1, PA0

Additional labels on the left:

- RCC\_OSC\_IN
- RCC\_OSC\_OUT
- OPAMP1\_VINP
- OPAMP1\_VBIM
- ADC1\_IN7

Rev: 7/7