

# COMS10015 quick(ish) reference hand-out: transistors and logic gates

## Definition: informal

$$\begin{aligned}
 \text{N-MOSFET} : & \left. \begin{array}{c} d \\ | \\ g \\ | \\ s \end{array} \right\} \rightsquigarrow \left\{ \begin{array}{ll} g = V_{dd} = 5V & \Rightarrow \text{transistor is activated, } s \text{ and } d \text{ connected} \\ g = V_{ss} \approx GND = 0V & \Rightarrow \text{transistor is deactivated, } s \text{ and } d \text{ disconnected} \end{array} \right. \\
 \\
 \text{P-MOSFET} : & \left. \begin{array}{c} s \\ | \\ g \\ | \\ d \end{array} \right\} \rightsquigarrow \left\{ \begin{array}{ll} g = V_{ss} \approx GND = 0V & \Rightarrow \text{transistor is activated, } s \text{ and } d \text{ connected} \\ g = V_{dd} = 5V & \Rightarrow \text{transistor is deactivated, } s \text{ and } d \text{ disconnected} \end{array} \right.
 \end{aligned}$$

## Definition: formal

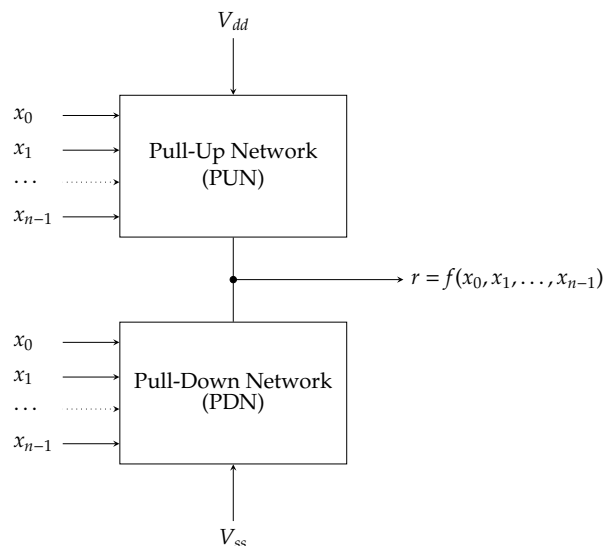
**Definition 1.** An **N-MOSFET** (or **N-type MOSFET**, or **N-channel MOSFET**, or **NPN MOSFET**) is constructed from *N-type* semi-conductor terminals and a *P-type* body:

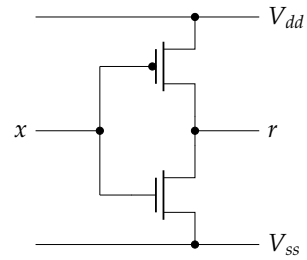
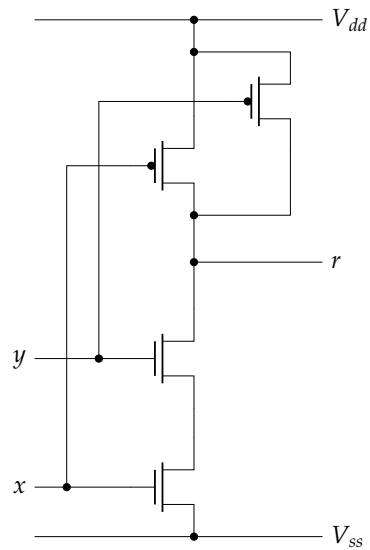
- applying a potential difference to the gate widens the conductive channel, meaning source and drain are connected (i.e., act like a conductor); the transistor is activated.
- removing the potential difference from the gate narrows the conductive channel, meaning source and drain are disconnected (i.e., act like an insulator); the transistor is deactivated.

**Definition 2.** A **P-MOSFET** (or **P-type MOSFET**, or **P-channel MOSFET**, or **PNP MOSFET**) is constructed from *P-type* semi-conductor terminals and an *N-type* body:

- applying a potential difference to the gate narrows the conductive channel, meaning source and drain are disconnected (i.e., act like an insulator); the transistor is deactivated.
- removing the potential difference from the gate widens the conductive channel, meaning source and drain are connected (i.e., act like a conductor); the transistor is activated.

## Design framework



**Logic gates: NOT****Logic gates: NAND****Logic gates: NOR**