Problem 1.

1. The critical path: I-Mem, Regs, Regs, ALU, Regs. First fetch instruction-I-Mem. Then, fetch two operands, which corresponds to two Regs. After that, calculate the result-ALU. Finally, store the result back to register-Regs. 400+200+200+100+200 = 1100ps
2. The new critical path: I-Mem, Regs, ALU, Regs. 400+250+100+250 = 1000ps

Problem 2.

1. The cycle time = 300+400+350+550+100 = 1700ps. The latency = 1700ps. The throughput = 1/1700.
2. The cycle time = 550+20 = 570ps. The latency = 570*5 = 2850ps. The throughput = 1/570.
3. Memory. The cycle time = 400+20 = 420ps. The latency = 420*6 = 2520ps. The throughput = 1/420.
4. Data memory: 15%+10% = 25%. Write port: 50%+15% = 65%.

Problem 3.

1. Cycle time = 10ns. After pipelining, the best cycle time = 2ns. The overall speedup = 10/2 = 5.
2. The new cycle time is 4ns and the speedup = 10/4 = 2.5.
3. The new cycle time is 4ns+20ps = 4.02ns and the new speedup = 10/4.02 = 2.49.
4. The new CPI= 1.4+0.2*1+0.05*2 = 1.7. The original time = 1.4*10ns. The new time = 1.7*4.02=6.834ns. The speed up = 14/6.834 = 2.05.

Problem 4.

1. 102 depends on 100; 102 depends on 101; 103 depends on 100; 104 depends on 103; 105 depends on 101; 105 depends on 103.
2. 2. Each stall takes 3 cycles. The execution time is 16 cycles.
3. 1 stall can happen. 100 LDR, 101 LDR, 102 NOP, 103 ADD, 104 ADD, 105 OR, 105 STR.

Problem 5.

1. The total execution time = 4+14+2+12+2 = 34ms. The new execution time = (4+2+2)*0.85+14+12 = 32.8ms. The speedup = 34/32.8 = 1.037
2. The new execution time = 4+14*0.9+2+12+2 = 32.6ms. The speedup = 1.043.
3. The new execution time = 4+14+2+12*0.9+2 = 32.8ms. The speedup = 1.037.

Problem 6.

1. P1: $\frac{3\times10^9}{1.5} = 2\times10^9$; P2: $\frac{2.5\times10^9}{1.0} = 2.5\times10^9$; P3: $\frac{4.0\times10^9}{2.2} = 1.8\times10^9$. Therefore, P2 has the highest performance.
2. P1: cycles = $3GHz\times10 = 3\times10^{10}$, Instructions = $3\times10^{10}/1.5 = 2\times10^{10}$; P2: cycles = 2.5×10^{10}, Instructions = 2.5×10^{10}. P3: cycles = 4.0×10^{10}, Instructions = $4.0\times10^{10}/2.2 = 1.8\times10^{10}$.
3. We need to reduce CPI/clock rate by 30%. CPI*1.2/(clock rate * a) = 0.7*CPI/clock rate. a = 1.7. Therefore, the new clock rate for each processers should be: P1 = 3*1.7 = 5.1GHz. P2 = 2.5*1.7 = 4.25GHz. P3 = 4*1.7 = 6.8GHz.