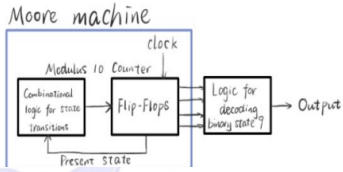
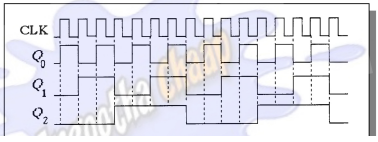
Chapter 9

1.



4. See Figure 8-2.



6. See Figure 8-3.

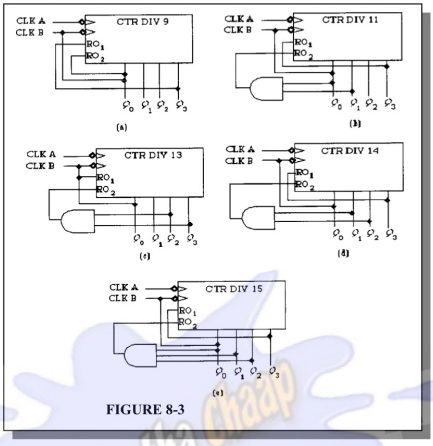


FIGURE 8-3

8. See Figure 8-4.

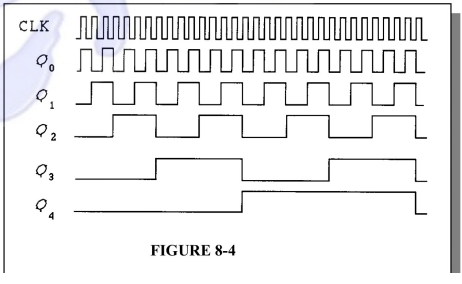


FIGURE 8-4

9. Each flip-flop is initially reset.

CLK	J_0K_0	J_1K_1	J_2K_2	J_3K_3	Q_0	Q_1	Q_2	Q_3
1	1	0	0	0	1	0	0	0
2	1	1	0	0	0	1	0	0
3	1	0	0	0	1	1	0	0
4	1	1	1	0	0	0	1	0
5	1	0	0	0	1	0	1	0
6	1	1	0	0	0	1	1	0
7	1	0	0	0	1	1	1	0
8	1	1	1	1	0	0	0	1
9	1	0	0	0	1	0	0	1
10	1	0	0	1	0	0	0	0

11. See Figure 8-6.

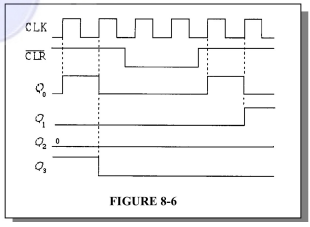


FIGURE 8-6

12. See Figure 8-7.

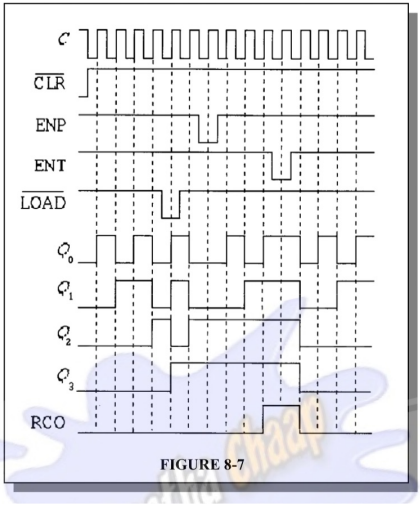


FIGURE 8-7

14. See Figure 8-9.

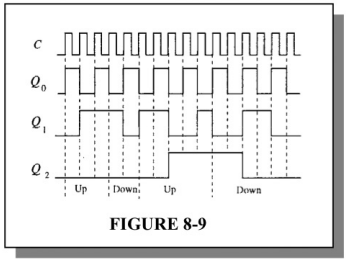


FIGURE 8-9

15 See Figure 8-10.

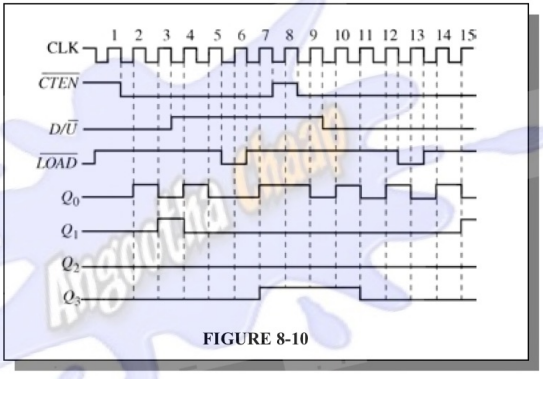


FIGURE 8-10

18.

	Q_2	Q_1	Q_0	D_2	D_1	D_0
Initially	0	0	0	0	0	1
At CLK 1	0	0	1	0	1	1
At CLK 2	0	1	1	1	1	1
At CLK 3	1	1	1	1	1	0
At CLK 4	1	1	0	1	0	0
At CLK 5	1	0	0	0	0	1
At CLK 6	0	0	1	0	1	1

The sequence is 000 to 001 to 011 to 111 to 110 to 100 and back to 001, etc.

19.

	FF3	FF2	FF1	FF0	Q_3	Q_2	Q_1	Q_0
Initially	Tog	Tog	Tog	Tog	0	0	0	0
After CLK 1	NC	NC	NC	Tog	1	1	1	1
After CLK 2	NC	NC	Tog	Tog	1	1	1	0
After CLK 3	NC	Tog	Tog	Tog	1	1	0	1
After CLK 4	Tog	Tog	Tog	Tog	1	0	1	0
After CLK 5	Tog	Tog	Tog	Tog	0	1	0	1

Tog = toggle, NC = no change

The counter locks up in the 1010 and 0101 states, alternating between them.

20.

18. NEXT-STATE TABLE

Present State		Next State	
Q_1	Q_0	Q_1	Q_0
0	0	1	0
1	0	0	1
0	1	1	1
1	1	0	0

TRANSITION TABLE

Output State Transitions (Present state to next state)		Flip-Flop Inputs			
Q_1	Q_0	J_1	K_1	J_0	K_0
0 to 1	0 to 0	1	X	0	X
1 to 0	0 to 1	X	1	1	X
0 to 1	1 to 1	1	X	X	0
1 to 0	1 to 0	X	1	X	1

See Figure 8-13.

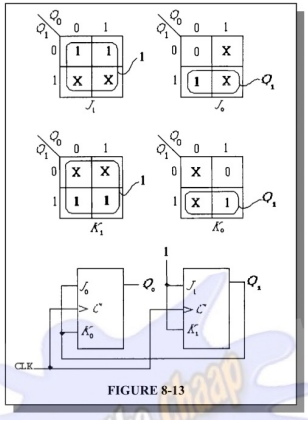


FIGURE 8-13

21.

NEXT-STATE TABLE

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	1	1	0	0
1	0	0	0	1	1
0	1	1	1	0	1
1	0	1	1	1	1
1	1	1	1	1	0
1	1	0	0	1	0
0	1	0	0	0	1

TRANSITION TABLE

Output State Transitions (Present state to next state)			Flip-flop Inputs					
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0 to 1	0 to 0	1 to 0	1	X	0	X	X	1
1 to 0	0 to 1	0 to 1	X	1	1	X	1	X
0 to 1	1 to 0	1 to 1	1	X	X	1	X	0
1 to 1	0 to 1	1 to 1	X	0	1	X	X	0
1 to 1	1 to 1	1 to 0	X	0	X	0	X	1
0 to 0	1 to 0	0 to 1	0	X	X	1	1	X
1 to 0	1 to 1	0 to 0	X	1	X	0	0	X

See Figure 8-14.

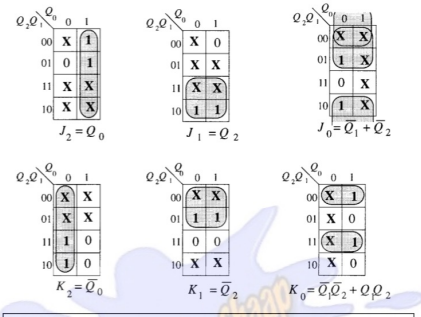


FIGURE 8-14

2. NEXT-STATE TABLE

Present State				Next State			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	1	0	0	1
1	0	0	1	0	0	0	1
0	0	0	1	1	0	0	0
1	0	0	0	0	0	1	0
0	0	1	0	0	1	1	1
0	1	1	1	0	0	1	1
0	0	1	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	0	0	0

TRANSITION TABLE

Output State Transition (Present State to next state)				Flip-flop Inputs							
Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0 to 1	0 to 0	0 to 0	0 to 1	1	X	0	X	0	X	1	X
1 to 0	0 to 0	0 to 0	0 to 1	X	1	0	X	0	X	X	0
0 to 1	0 to 0	0 to 0	1 to 0	1	X	0	X	0	X	X	1
1 to 0	0 to 0	0 to 1	0 to 0	X	1	0	X	1	X	0	X
0 to 0	0 to 1	1 to 1	0 to 1	0	X	1	X	X	0	1	X
0 to 0	1 to 0	1 to 1	1 to 1	0	X	X	1	X	0	X	0
0 to 0	0 to 1	1 to 1	1 to 0	0	X	1	X	X	0	X	1
0 to 0	1 to 1	1 to 0	0 to 0	0	X	X	0	X	1	0	X
0 to 0	1 to 1	0 to 0	0 to 1	0	X	X	0	0	X	1	X
0 to 0	1 to 0	0 to 0	1 to 0	0	X	X	1	0	X	X	1

Binary states for 10, 11, 12, 13, 14, and 15 are unallowed and can be represented by don't cares.

See Figure 8-15. Counter implementation is straightforward from input expressions.

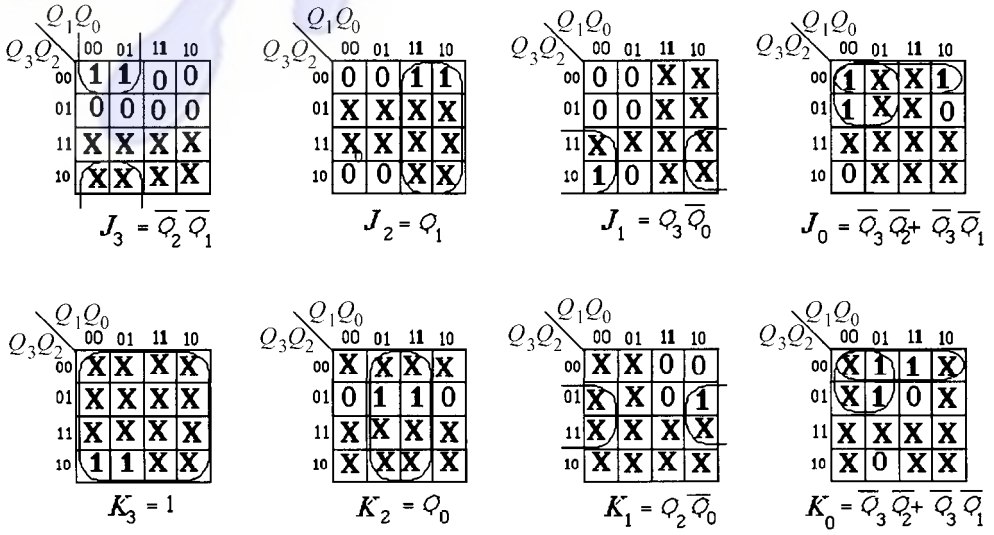


FIGURE 8-15

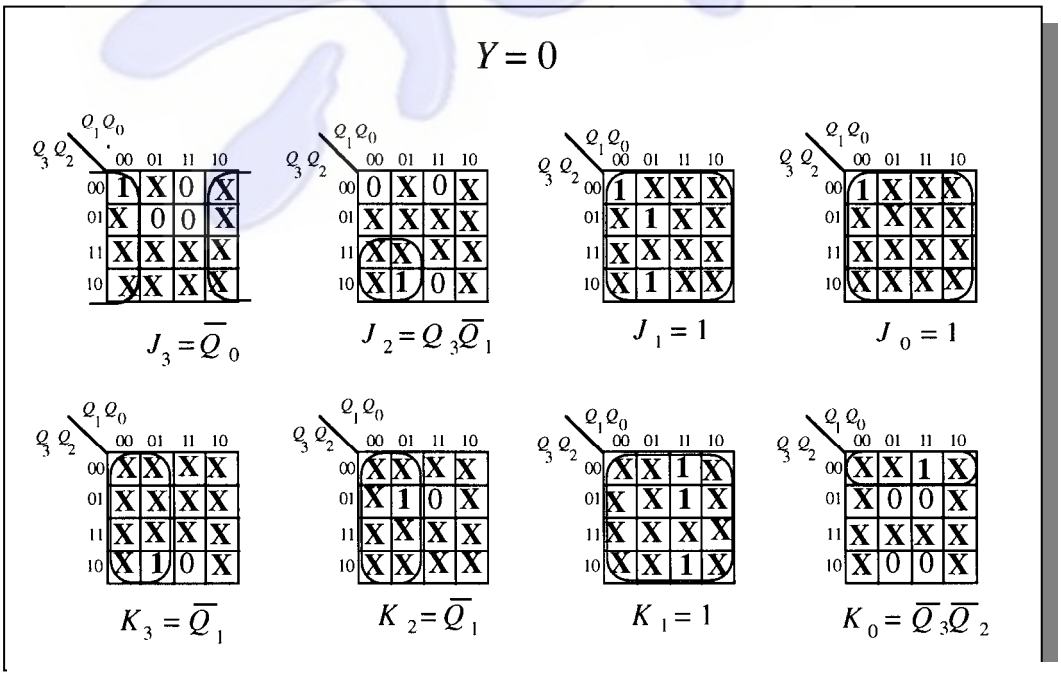
23. NEXT-STATE TABLE

Present State				Next State							
				$Y = 1$ (Up)				$Y = 0$ (Down)			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	1	1	1	0	1	1
0	0	1	1	0	1	0	1	0	0	0	0
0	1	0	1	0	1	1	1	0	0	1	1
0	1	1	1	1	0	0	1	0	1	0	1
1	0	0	1	1	0	1	1	0	1	1	1
1	0	1	1	0	0	0	0	1	0	0	1

TRANSITION TABLE

Output State Transitions (Present State to next state)				Y	Flip-flop Inputs			
Q_3	Q_2	Q_1	Q_0		J_3K_3	J_2K_2	J_1K_1	J_0K_0
0 to 1	0 to 0	0 to 1	0 to 1	0	1X	0X	1X	1X
0 to 0	0 to 0	0 to 1	0 to 1	1	0X	0X	1X	1X
0 to 0	0 to 0	1 to 0	1 to 0	0	0X	0X	X1	X1
0 to 0	0 to 1	1 to 0	1 to 1	1	0X	1X	X1	X0
0 to 0	1 to 0	0 to 1	1 to 1	0	0X	X1	1X	X0
0 to 0	1 to 1	0 to 1	1 to 1	1	0X	X0	1X	X0
0 to 0	1 to 1	1 to 0	1 to 1	0	0X	X0	X1	X0
0 to 1	1 to 0	1 to 0	1 to 1	1	1X	X1	X1	X0
1 to 0	0 to 1	0 to 1	1 to 1	0	X1	1X	1X	X0
1 to 1	0 to 0	0 to 1	1 to 1	1	X0	0X	1X	X0
1 to 1	0 to 0	1 to 0	1 to 1	0	X0	0X	X1	X0
1 to 0	0 to 0	1 to 0	1 to 0	1	X1	0X	X1	X1

See Figure 8-16.



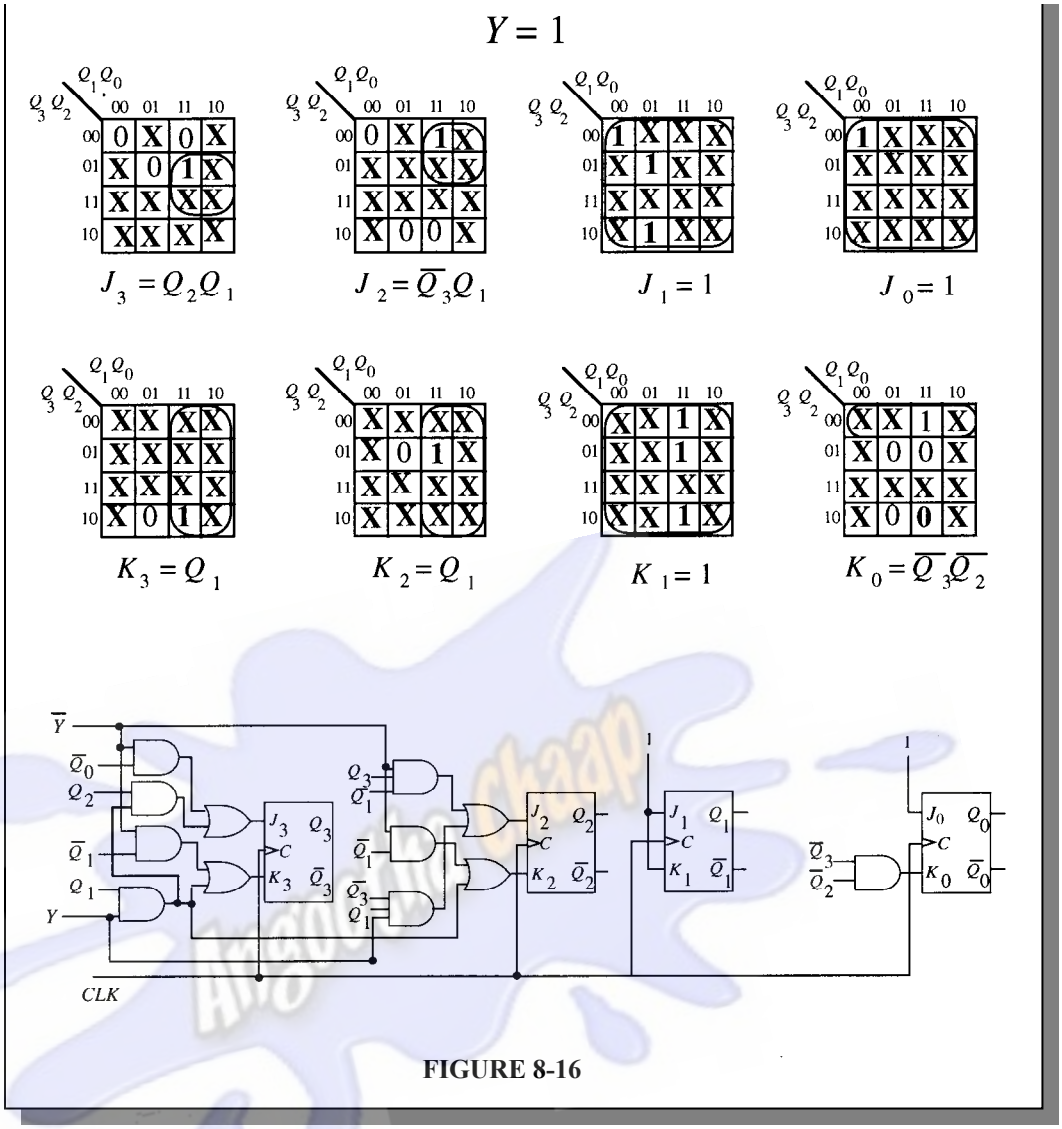


FIGURE 8-16

Section 8-5 Cascaded Counters

24 (a) Modulus = 4 × 8 × 2 = **64**

$$f_1 = \frac{1\,\text{kHz}}{4} = \mathbf{250\ Hz}$$

$$f_2 = \frac{250\,\text{Hz}}{8} = \mathbf{31.25\ Hz}$$

$$f_3 = \frac{31.25\,\text{Hz}}{2} = \mathbf{15.625\ Hz}$$

(b) Modulus = $10 \times 10 \times 10 \times 2 = \mathbf{2000}$

$$f_1 = \frac{100\,\text{kHz}}{10} = \mathbf{10\ kHz}$$

$$f_2 = \frac{10\,\text{kHz}}{10} = \mathbf{1\ kHz}$$

$$f_3 = \frac{1\,\text{kHz}}{10} = \mathbf{100\ Hz}$$

$$f_4 = \frac{100\,\text{Hz}}{2} = \mathbf{50\ Hz}$$

(c) Modulus = $3 \times 6 \times 8 \times 10 \times 10 = \mathbf{14400}$

$$f_1 = \frac{21\,\text{MHz}}{3} = \mathbf{7\ MHz}$$

$$f_2 = \frac{7\,\text{MHz}}{6} = \mathbf{1.167\ MHz}$$

$$f_3 = \frac{1.167\,\text{MHz}}{8} = \mathbf{145.875\ kHz}$$

$$f_4 = \frac{145.875\,\text{kHz}}{10} = \mathbf{14.588\ kHz}$$

$$f_5 = \frac{14.588\,\text{kHz}}{10} = \mathbf{1.459\ kHz}$$

(d) Modulus = $2 \times 4 \times 6 \times 8 \times 16 = \mathbf{6144}$

$$f_1 = \frac{39.4\,\text{kHz}}{2} = \mathbf{19.7\ kHz}$$

$$f_2 = \frac{19.7\,\text{kHz}}{4} = \mathbf{4.925\ kHz}$$

$$f_3 = \frac{4.925\,\text{kHz}}{6} = \mathbf{820.83\ Hz}$$

$$f_4 = \frac{820.683}{8} = \mathbf{102.6\ Hz}$$

$$f_5 = \frac{102.6\,\text{Hz}}{16} = \mathbf{6.41\ Hz}$$

28. See Figure 8-20.

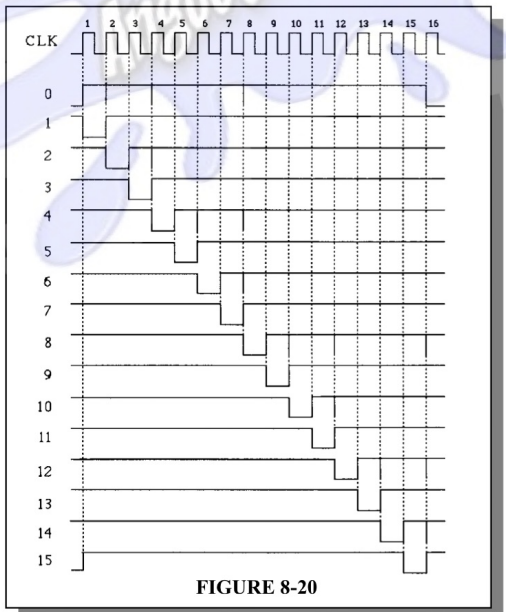


FIGURE 8-20

31. See Figure 8-22.

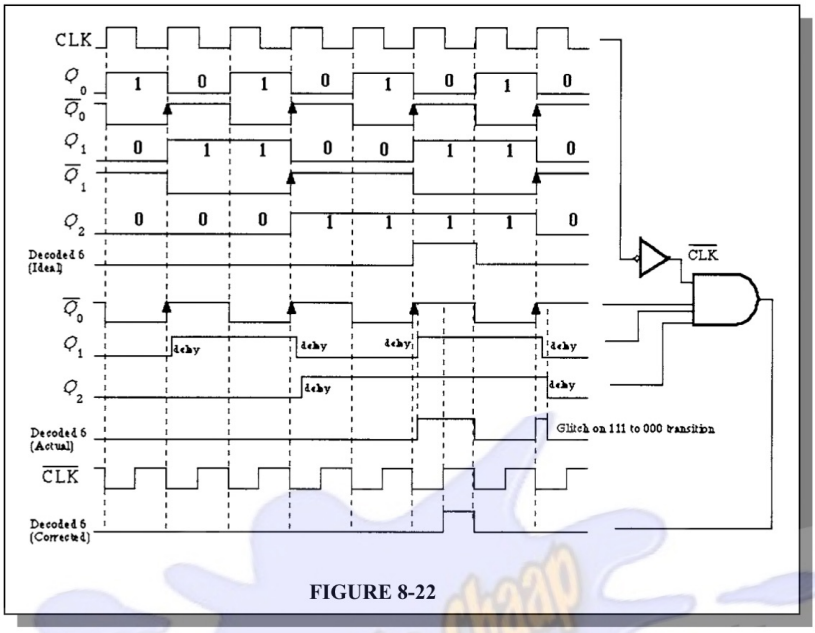


FIGURE 8-22

34. For the digital clock, the counter output frequencies are:
Divide-by-60 input counter:

$$\frac{60\text{ Hz}}{60} = 1\text{ Hz}$$

Seconds counter:

$$\frac{1\text{ Hz}}{60} = 16.7\text{ mHz}$$

Minutes counter:

$$\frac{16.7\text{ mHz}}{60} = 278\ \mu\text{Hz}$$

Hours counter:

$$\frac{278\ \mu\text{Hz}}{12} = 23.1\ \mu\text{Hz}$$

35. $53 + 37 - 22 = \mathbf{68}$