1. The critical path latencies (maximum delay in a stage) for the major blocks in a simple processor (unpipelined) are given below.

I-Mem	ALU	Regs	D-Mem
400ps	100ps	200ps	350ps

Answer the following questions:

1) What is the critical path for a LC3 ADD instruction? Explain your break-up. Assume the register file is single-ported.
2) If we add another read and write port to the register file, the Regs increase to 250 ps. What is the new critical path for an ADD instruction?

2. The 5 stages of the processor have the following latencies:

Fetch	Decode	Execute	Memory	Writeback
300ps	400ps	350ps	550ps	100ps

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages.

1) Non-pipelined processor: what is the cycle time? What is the latency of an instruction? What is the throughput?
2) Pipelined processor: What is the cycle time? What is the latency of an instruction? What is the throughput?
3) If you could split one of the pipeline stages into 2 equal halves, which one would you choose? What is the new cycle time? What is the new latency? What is the new throughput?
4) Assume the distribution of instructions that run on the processor is:

   50%: ALU
   25%: BR
   15%: LOAD
   10%: STORE

   Assuming there are no stalls or hazards, what is the utilization of the data memory? What is the utilization of the register file's write port? (Utilization in percentage of clock cycles used)

3. You are given a non-pipelined processor design which has a cycle time of 10ns and average CPI of 1.4. Calculate the latency speedup in the following questions.

1) What is the best speedup you can get by pipelining it into 5 stages?
2) If the 5 stages are 1ns, 1.5ns, 4ns, 3ns, and 0.5ns, what is the best speedup you can get compared to the original processor?
3) If each pipeline stage added also adds 20ps due to register setup delay, what is the best speedup you can get compared to the original processor?
4) The pipeline from 3.3 stalls 20% of the time for 1 cycle and 5% of the time for 2 cycles (these occurrences are disjoint). What is the new CPI? What is the speedup compared to the original processor?

4. Sequence of instructions:

```
100 LDR R2, R1, #0
101 LDR R1, R3, #4
102 ADD R3, R1, R2
103 ADD R3, R2, R2
104 OR  R4, R3, #0
104 STR R3, R1, #5
```

1) List the Read-After-Write data dependencies.
2) Assume the 5-stage IF/ID/EX/MEM/WB pipeline with no bypassing/forwarding, and each stage takes 1 cycle. Instead of inserting NOPs, you let the processor stall on hazards. How many times does the processor stall? How long is each stall (in cycles)? What is the execution time (in cycles) for the whole program?
3) Assume the 5-stage pipeline with full bypassing/forwarding. During the course, we showed an example with forwarding the result of EX stage to the ID stage. It's also possible to forward the result of MEM stage to the ID stage. The full forwarding means the processor implement both kinds. In this case, how many stalls can happen? Rewrite the program with NOP instructions to eliminate the hazards. [NOTE: In computer science, a NOP, no-op, or NOOP (pronounced "no op"; short for no operation) is an assembly language instruction, programming language statement, or computer protocol command that does nothing.

5. The following table shows the execution time of five routines of a program running on 16 processors.

# Processors	Routine A (ms)	Routine B (ms)	Routine C (ms)	Routine D (ms)	Routine E (ms)
16	4	14	2	12	2

1) Find the total execution time, and how much it is reduced if the time of routines A, C, & E is improved by 15%.
2) By how much is the total time reduced if routine B is improved by 10%?
3) By how much is the total time reduced if routine D is improved by 10%?

6. Consider three different processors, P1 P2 and P3, executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and a CPI of 2.2.

1) Which processor has the highest performance expressed in instructions per second?
2) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
3) We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?