JOINT INSTITUTE
交大密西根学院

ECE3700J Introduction to Computer Organization

Homework 6

Assigned: July 4, 2023

Due: 4:00pm on July 11, 2023

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1. (10 points) Which levels and concepts of a memory hierarchy are analogous to these frozen food storage mechanisms and events?
   a. The refrigerator in the kitchen
   b. Frozen food freezers at a grocery store
   c. Suppliers of frozen food for the grocery store
   d. Getting food from the refrigerator to cook
   e. Time it takes to get food from the refrigerator
   f. Chances of not finding the desired food in the refrigerator
   g. Putting cooked food into the refrigerator
   h. Getting new food from the grocery store to put in the refrigerator
   i. Time taken to get new food from the grocery store
   j. Finding a short cut to the grocery store to get new food
2. (40 points) Below is a list of memory address references, given as word addresses:
   0x03, 0x04, 0x05, 0x03, 0xBE, 0xBF, 0x58, 0x5C, 0xB0, 0x2C, 0xBA, 0xED
   (1) For each of these references, identify the tag and the cache index given a direct-mapped cache with 8 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. (10 points)
   (2) For each of these references, identify the tag and the cache index given a direct-mapped cache with two-word blocks and a total size of 4 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. (10 pints)
   (3) You are asked to optimize a cache design for the given references. There are three direct-mapped cache designs possible, all with a total of 8 words of data: design C1 has 1-word blocks, design C2 has 2-word blocks, and design C3 has 4-word blocks. In terms of miss rate, which cache design is the best? If the miss stall time is 45 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design? (20 points)

3. (50 points) For a direct-mapped cache design with a 32-bit byte address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31 – 9	8 – 5	4 – 0

(1) What is the cache block size (in words)? (5 points)

(2) How many blocks does the cache have? (5 points)

(3) What is the ratio between total bits required for such a cache implementation over the data storage bits? (5 points)

Beginning from power on, the following byte addresses for cache references are recorded.

Address											
0x10	0x04	0x20	0x74	0xEC	0x0A	0x711	0x1D	0x9C	0xD1C	0xF6	0x878

(4) (20 points) For each reference, list

a) its tag, index, and offset

b) whether it is a hit or a miss, and

c) How many blocks were replaced (if any)?

(5) What is the hit ratio? (5 points)

(6) Show the final state of the cache, with each valid line represented as <index, tag, data>. (10 points)