National Tsing Hua University
Department of Electrical Engineering
Capstone Project Research Report

IoT Sensor Interface Circuit Chip Design

Research Field: Integrated Circuits and Systems

Team: B371

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ABSTRACT

While humans possess the ability to discern various gases through their sense of smell, the detection of toxic gases proves challenging. Additionally, individual variations in olfactory perception hinder the quantification of gas concentrations and the establishment of unified standards. The necessity of an electronic nose becomes evident, offering assistance in detecting toxic gases with a quantified olfactory outcome for high-precision gas detection. Notably, electronic noses exhibit advantages such as small size, low cost, rapid response, and high resolution, ensuring convenient portability.

In our implementation, the electronic nose undergoes a gas sensing process, inducing physical property changes. The sensing mechanism employs resistors, with variations in resistance values reflecting alterations in physical properties. Subsequently, these resistance values are converted into analog signals and transmitted to the interface circuit for further conversion into digital signals. The digital signals can then be sent to an information recognition system for analysis, ultimately leading to the identification of the gas type.

Given the lack of specificity in individual gas sensors for gas analysis, our project focuses on an array of gas sensors to enhance accuracy in identifying specific gases. Among the myriad gas sensor types, we employ resistive sensors, specifically conductive polymer gas sensors, chosen for their high sensitivity and straightforward signal retrieval.

The objective of the designed interface circuit is to accurately recognize a broad range of resistance values (at least 500 ohms to 5M ohms), ensuring a dynamic range exceeding 4 decades. Simultaneously, the overall power consumption should be below 8mW, and accuracy should surpass 3%. Therefore, we adopt the architecture of an oscillator-based resistance readout circuit for implementation due to its digital output, high stability, and the potential for direct integration into the recognition system in real electronic nose applications, eliminating the need for additional ADC processing and saving circuit area.

Furthermore, the circuit architecture boasts multiple adjustable parameters (see Section 2-2 for parameter details), including reference voltage (Vref), comparator upper and lower limit voltages, current mirror path ratios, and the capacitor value above the integrator. These parameters determine the triangular wave period formed under various resistor values. Consequently, by configuring diverse parameter values, the circuit can precisely control the triangular wave period within a considerable range for a broad spectrum of resistor values. Thus, this architecture enables accurate measurement of high dynamic range resistances.

Through improvements inspired by the referenced circuit [4], our project achieves a sensor resistance range with a relative error of less than 1%, spanning from 2000 ohms to 300M ohms. The dynamic range of resistances with a relative error of 1% exceeds 5 decades, and for resistance values between 500 ohms and 900M ohms, the measurement error does not surpass 3%. With a relative error of 3%, the dynamic range reaches beyond 6 decades, maintaining a resolution above the target level while allowing precise measurement of high dynamic range resistances. The post-simulation power consumption of our circuit is 6.228mW, controlled within the initially set 8mW boundary. In point 3, we conduct a detailed analysis of the primary energy-consuming circuit modules, anticipating future modifications to parameters or structures for high-power circuits to achieve the same or even higher precision with low power optimization.

CONTENTS

In everyday life, there are numerous situations that require gas identification. Although humans can discern different gases through their sense of smell, the detection of toxic gases poses challenges. Moreover, individual variations in olfactory perception prevent the detection of gas concentrations and the establishment of unified standards.

The electronic nose, consisting of a gas sensor array, signal acquisition circuitry, and data recognition system, serves as a quantifiable and standardizing alternative to human olfaction. It offers advantages such as small size, low cost, rapid response, and high resolution. Notably, an electronic nose can be placed in a gas environment for extended periods without causing olfactory fatigue. Additionally, it can detect toxic gases, making it suitable for portable devices. Consequently, electronic noses find widespread applications in various gas sensing domains.

In the application of gas sensors in electronic noses, individual sensors lack specificity for particular gases. Hence, gas sensor arrays are commonly employed to enhance the accuracy of gas identification. Given the diverse types of gas sensors, this project focuses on resistive sensors, specifically conductive polymer gas sensors. These sensors exhibit varying resistance values based on different gas types, with the rate of resistance change proportional to gas concentration. However, these sensors are susceptible to external factors such as ambient temperature, humidity, and background odors. Moreover, sensors coated with different sensing materials may not have identical initial resistance values.

Therefore, the purpose of the designed interface circuit in this project is to convert changes in sensor resistance values into digital signals for facilitating gas identification and concentration analysis. With a focus on reducing power consumption, maintaining accuracy, minimizing the impact of external environmental factors, and expanding the applicable dynamic range of resistances, the interface circuit aims to ensure that a broader range of sensor resistance values can be accurately recognized by the electronic nose system.

2. Thesis Reviewing

(1) Refer to the two sensing interface circuit forms of digital and semi-digital through [4]

Half-Digital – In the semi-digital architecture [4], the circuit is composed of a comparator, inverter, positive-edged triggered D-flip-flop (DFF), 8-bit up counter, and an 8-bit DAC, with Rs representing the gas sensor's resistance. The gas sensor is biased by the DAC output current.

The circuit operates in two modes:

(a) Adaptation Mode

i. At the beginning of gas sensing, the sensor is pre-biased to Vref in the adaptation mode.
ii. The DFF and counter are reset, setting the counter's output to 0 and making the DAC output current 0A.
iii. The voltage across Rs (Vs) is 0V, which is less than Vref, causing the comparator to output high, enabling the counter to count up.
iv. As the counter counts up, the DAC output current increases, causing Vs to rise.
v. When Vs rises to Vref, the comparator output switches from high to low, putting the counter in a stop-counting state.
vi. At this point, Vs is maintained at the default Vref, and the loop is open.

(b) Sensing Mode

- Gas sensing begins in this mode, and due to the open loop, the gas sensor is biased by a constant DAC output current. The sensor signal is then converted into a voltage signal.

This dual-mode operation allows the circuit to adapt the gas sensor to Vref initially and then seamlessly transition to gas sensing while maintaining a stable bias. The circuit's design ensures precise control of the sensor's biasing and enables the conversion of the sensor signal into a voltage signal during gas sensing.

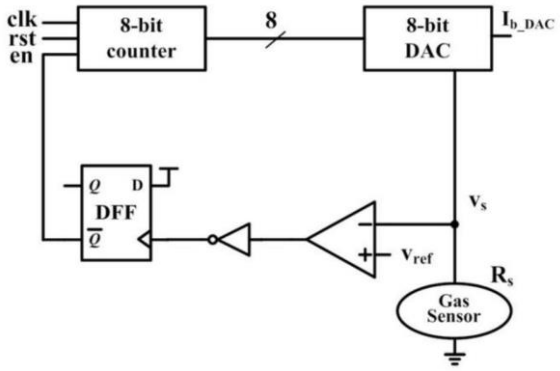

Figure 1.1: Half-Digital gas sensing Circuit [4]

- Digital – In the digital architecture [4], the circuit consists of a hysteresis comparator, inverter, 8-bit UP/$\overline{\overline{DN}}$ counter, and an 8-bit DAC, with Rs representing the gas sensor. The gas sensor is biased by the DAC output current, resulting in voltage Vs. Vs and the reference voltage Vref are compared in the hysteresis comparator, and the comparator's output controls whether the counter counts up or down through an inverter. The counter's output regulates the DAC's output current. When the counter counts up or down, the DAC's output current increases or decreases.

The circuit operates in two modes:

(a) Adaptation Mode

i. At the beginning of gas sensing, the sensor is adapted to Vref.
ii. The counter is reset, setting the counter's output to 0, making the DAC output current 0A.
iii. The comparator outputs low, enabling the counter to count up, causing the DAC output current to increase and Vs to rise.
iv. The circuit enters the adaptation mode when Vs rises to Vref.

(b) Sensing Mode

Gas sensing begins in this mode, and the sensor signal is converted into a digital signal.

The circuit's operation is as follows:

i. Reset the counter, setting the counter's output to 0, making the DAC output current 0A. The comparator outputs low, enabling the counter to count up, causing the DAC output current to increase, and Vs to rise. The circuit enters the adaptation mode.
ii. When Vs rises to Vref, the comparator output switches from low to high, and the counter starts counting down.

iii. When Vs is less than Vref, the comparator output switches from high to low, and the counter counts up, entering the sensing mode.

The circuit repeats steps ii. and iii., and the feedback mechanism ensures that, as the gas sensor reacts, its resistance changes. The feedback controls different DAC output currents to maintain Vs at Vref, converting the sensor signal into a current signal whose magnitude is proportional to the counter's digital output signal.

In summary, the advantages of the semi-digital architecture lie in its stable biasing controlled by a digital signal, resulting in high stability and low power consumption. However, its drawbacks include the significant impact of bias size on linearity between voltage and resistance, as well as output resolution. On the other hand, the digital architecture's advantages include the direct conversion of analog resistance signals into digital signals, enabling direct signal transmission to the recognition system without the need for ADC architecture and ensuring high stability. However, its drawback is that resolution is influenced by the number of output bits.

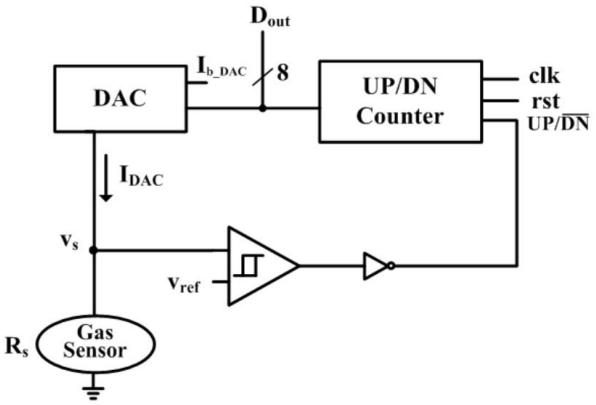

Figure 1.2: Digital Gas Sensing Circuit Operation [4]

(2) Reference circuit architecture through [2]

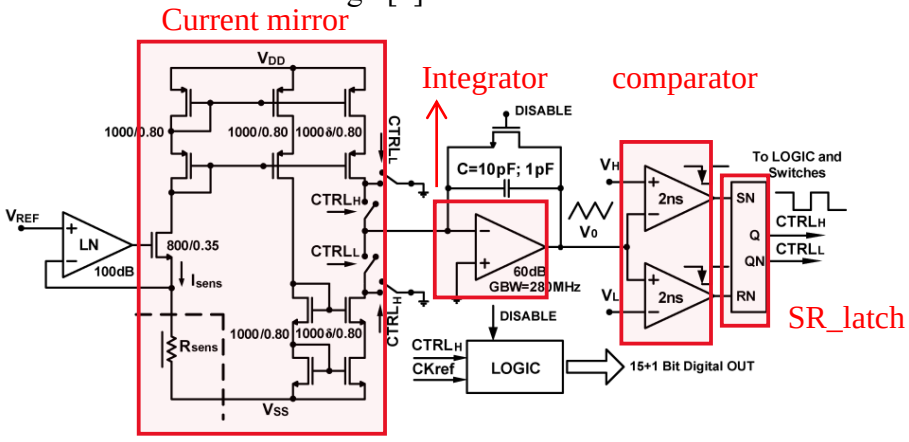

Figure1.3: Oscillator-Based Gas Sensing Circuit Operation [2]

The IEEE oscillator-based gas sensing circuit employs an LN OP to lock the voltage at the Rsens node to Vref, establishing an inverse proportional relationship between Isens and Rsens. After passing through an integrator and comparator, and then through an SR latch for digitalization, the feedback loop returns to the current mirror's switch, generating a triangular wave with the peak controlled between VH and VL. Through the period of the triangular wave, and by comparing it with a designed logic and a reference clock period, the circuit obtains the sensed resistance value (Rsens). As the resistance values (Rsens) change due to different gases, the readout from this architecture is advantageous for subsequent gas identification.

Advantages

i. **Digital Output**: The circuit provides a digital output, offering high stability.
ii. **Direct Integration in Gas Recognition Systems**: In practical applications of electronic nose gas recognition, the digital output can be directly fed into the recognition system without the need for additional ADC processing, saving circuit area.
iii. **Adjustable Parameters**: The circuit architecture features various adjustable parameters, such as Vref, VH and VL of the comparator, current ratios in the current mirror's left and right paths, and the capacitance value above the integrator. These parameters determine the triangular wave period under different resistances. Setting different modes with varying parameter values allows control of the triangular wave period within a considerable range. This flexibility results in a high dynamic range, aligning with the specified goals of the circuit.

This oscillator-based architecture stands as a reference due to its ability to meet the high dynamic range requirements outlined in your project's initial specifications.

3. Revising and Implementing

In the improved design, two additional OPs are added to the current mirror. In Figure 3 (logic block), a counter and DFF have been implemented. The DFF receives a signal (Reset) with a fixed period, serving as the reference clock. The counter takes the output of SR_latch, a digital signal with the same period as the triangular wave. The Reset signal from the DFF, after passing through some buffer delay, acts as the Reset for the counter. This arrangement achieves the periodic comparison necessary for digitizing the resistance signal. The digital output from the logic block is set to 16 bits, enhancing the accuracy of resistance measurement errors. For a detailed description of the improved circuit

architecture, please refer to Section 2 of the report.

In terms of practical implementation, the output from the Integrator accurately measures the triangular wave. The circuit undergoes measurements in 5 corners and 3 temperature conditions, with error calculations. The achieved dynamic range surpasses the 141dB reported in the referenced paper, reaching 155dB. For detailed implementation results, please refer to Section 3 of the report—Experimental Results.

The decision to convert analog resistance signals to digital signals through the circuit was made to ensure stable output. Additionally, to achieve a large dynamic range, meaning a wide range of low-error resistance measurements, the circuit architecture was referenced. Simultaneously, to control the current mirror's current precision, two OPs were added to lock the Vgs of the MOS in the current mirror, stabilizing the current.

II. Research Methodology

1. System Design

After discussing and analyzing the advantages and disadvantages of the above literature, we decided to use the structure of resistance control oscillator to perform resistance read out. The circuit architecture is as follows:

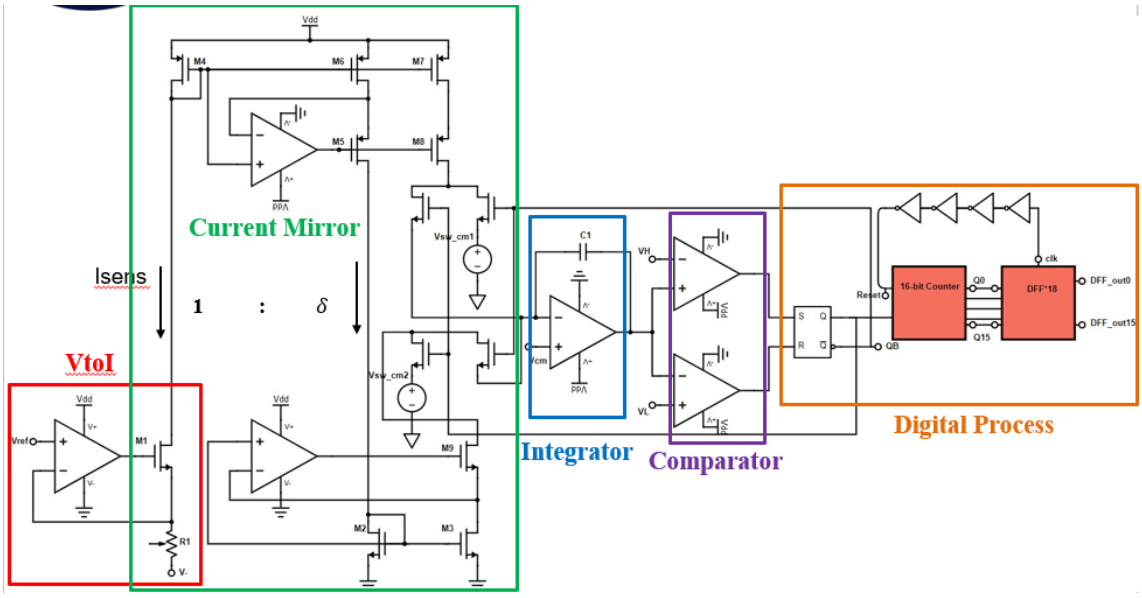

Figure 2.1: System Structure Diagram

In the circuit improvement, NMOS was chosen as the switch, and a D Flip-Flop was added at the output of the counter to facilitate analysis by the backend data recognition system. Additionally, an extra reset signal was introduced, enabling simultaneous resetting of the counter and control of the D Flip-Flop's output. In the design of the counter, a 16-bit

configuration was implemented to cover a broad frequency range. This conversion of signal frequency to digital output expands the range of recognizable sensor resistance values.

To address a wide range of sensor resistance values while minimizing power consumption, two modes were designed. These modes set the sensor bias at different reference voltages, namely 50mV and 500mV. The circuit can adjust the bias voltage based on the external sensor resistance, achieving a reduction in current and power consumption.

In terms of signal frequency, improvements were made to the transistor size and the amplifier, comparator, and counter architectures. These modifications were aimed at achieving the desired precision, reducing errors during frequency analysis in the backend circuit.

These enhancements collectively contribute to a more versatile and efficient circuit, capable of accommodating a broader range of sensor resistance values while maintaining precision and minimizing power consumption.

2. Principle and Structure

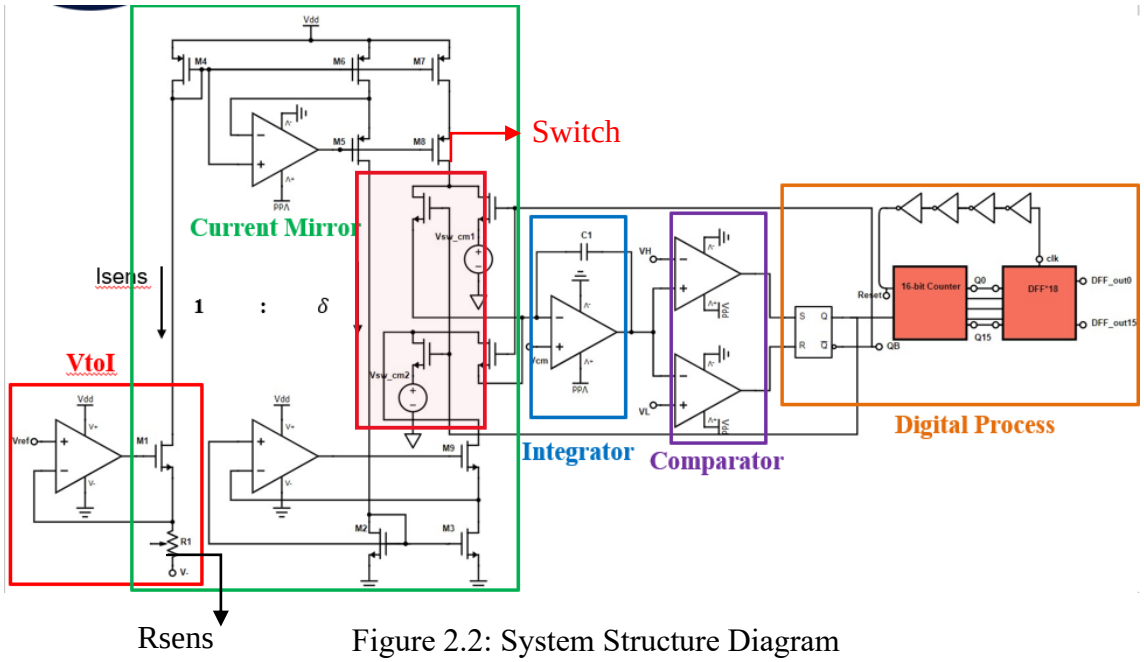

Figure 2.2: System Structure Diagram

Table 2.1: Overall circuit architecture adjustable parameter setting table

input	parameter	
Vref	50mV	500mV
Rsens	500~500k ohm	5k~5M ohm
Isens	100u~100nA	100u~100nA
VH	1.2 V	
VL	0.6 V	
δ	0.1	
C1	3pF	
Tosc	360n ~ 360us	360n ~ 360us
VDD	1.8 V	
Vsw_cm1/Vsw_cm2/Vcm	0.9 V	

The chip comprises six operational amplifiers (Op-Amp), a set of current mirrors (M1~M9), an SR latch, two outputs from the SR latch — Q and $\overline{Q}$, controlling the switches M8 and M9 connected to the negative terminal of the integrator. It also includes 16 counters and 16 D Flip-Flops (DFF).

In the context of gas detection applications, different gases cause varying changes in the resistance of gas detectors. The primary goal of this chip is to convert analog signals into digital signals for gas type identification. The method involves connecting an external resistor and using vtoiop to generate a constant current. The current mirror then replicates this current to the integrator op, adjusting the integration speed based on the different current sizes. This variation in current sizes results in different integration speeds, creating differences in the oscillation period.

The comparator op controls the integration range between 0.6V and 1.2V. The SR latch and counter then digitize the signal. Each time the upper or lower bound is reached, the counter increments. This process achieves the conversion of the analog signal representing changes in resistance to a digital signal.

The integration period is given by the formula:

$$T_{osc} = \frac{2C \cdot \Delta V \cdot R_{sens}}{\delta \cdot V_{ref}}$$

Here, C is the capacitance value between the integrator op's negative terminal and the output terminal, ΔV is the voltage difference set by the comparator op for the upper and lower bounds, Rsens is the resistance value of the external resistor, δ is the ratio by which the current mirror scales the current size, and Vref is the fixed voltage given by vtoiop, representing the voltage across Rsens.

3. Subcircuit and SPEC definition

A. V to I OP

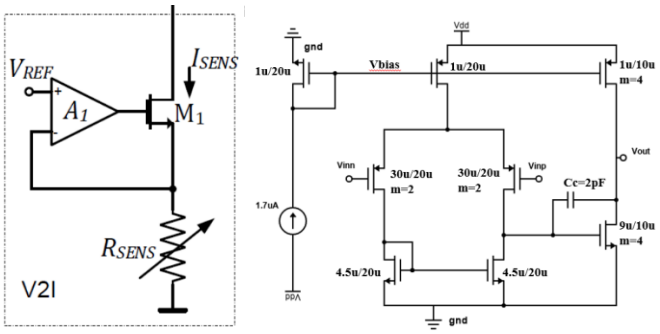

Figure 2.3: The left picture shows the overall architecture of VtoI, and the right picture shows the 2-stage single-ended pmos type op-amp used.

SPEC:

- Gain > 10000: To ensure that the replication of VREF has an error of less than 0.1 %. Achieving a high gain is crucial for minimizing the replication error of V_REF.
- Bandwidth > 0.1Hz: Due to the infrequent changes in V_REF, the bandwidth shou ld be sufficient for the application. A higher bandwidth ensures that the circuit res ponds promptly to changes in V_REF when they occur.
- Phase margin > 65°: To avoid circuit output oscillations. A phase margin greater t han 65° provides stability to the circuit and prevents unwanted oscillations.

VtoI biases the sensor resistor R_SENS at a fixed reference voltage V_REF=50mV or 500mV through a negative feedback mechanism. The resistance dynamic range of this topic is initially set to 500Ω-500kΩ or 5kΩ-5MΩ. The current flowing through M1 will be limited. In 0.1-100uA, Op-amp does not use the Folded-cascode structure because it needs to have enough output swing to cope with changes in the M1 gate terminal voltage, so that the op-amp has sufficient gain and phase under various output voltages. margin, bias the sensing at the accurate reference voltage V_REF.

B. Current Mirror and CM OP

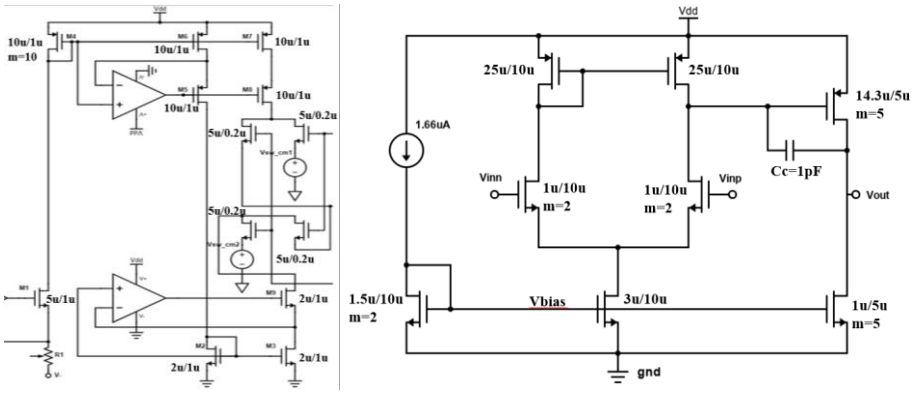

Figure 2.4: The left picture shows the overall architecture of CM, and the right picture shows the 2-stage single-ended nmos type op-amp used by the OP in CM

SPEC:

- Gain > 10000: To ensure that the replication of VREF has an error of less than 0.1 %. Achieving a high gain is crucial for minimizing the replication error of V_REF.
- Bandwidth > 0.1Hz: Due to the infrequent changes in V_REF, the bandwidth shou ld be sufficient for the application. A higher bandwidth ensures that the circuit res ponds promptly to changes in V_REF when they occur.
- Phase margin > 65°: To avoid circuit output oscillations. A phase margin greater t han 65° provides stability to the circuit and prevents unwanted oscillations.

In the VtoI operation with a voltage range of 50mV to 500mV and a working range for Rsens of 500Ω to 5MΩ, the current flowing through M1 ranges from 100nA to 100 μ A. Through the use of M5, M6, M7, M8, four MOS transistors, and M4 with a W/L ratio of 1/10, the right side allows currents in the range of 10nA to 10 μ A. Two CM ops are employed to lock the VDS of M4 and M6, as well as the VDS of M2 and M3 at the same level, enhancing the accuracy of the current mirror. This configuration ensures that M1 allows an appropriate current flow within the specified voltage and resistance ranges.

C. Integrator

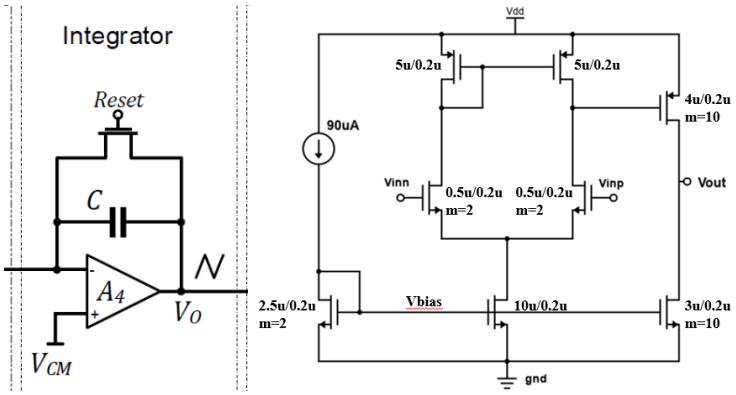

Figure 2.5: The left picture shows the overall architecture of Integrator, and the right picture shows the 2-stage single-ended nmos type op-amp.

SPEC:

- Gain > 40dB: This is to minimize the impact of the input on the output voltage.
- Bandwidth > 2.78MHz ×4 = 11.12MHz: According to the Fourier series of the triangular wave, our bandwidth needs to cover the first two components with the highest energy.

By formula:

$$x_{triangle}(t) = \frac{8}{\pi^2}\sum_{k=0}^{\infty}(-1)^k \frac{\sin((2k+1)t)}{(2k+1)^2} = \frac{8}{\pi^2}\left(\sin(t) - \frac{1}{9}\sin(3t) + \frac{1}{25}\sin(5t) - \cdots\right)$$

After the current mirror replicates the current flowing through the sensing resistor RSENS in proportion, the replicated current will charge and discharge the integrator,

transforming the changes in the sensing resistor's resistance into changes in signal frequency. The output point Vo of the integrator is connected to two comparators. These comparators limit the integration range of the integrator, which, in this project, is set to be 0.6-1.2V. To adapt to a larger voltage variation range, the amplifier in the integrator does not use the Folded-cascode architecture, ensuring it has sufficient output swing. When the replicated current is at its maximum value of 10uA, the charging and discharging frequency of the integrator is approximately 2.77MHz. To ensure the circuit operates normally at any frequency, we designed a high-bandwidth integrator with sufficient gain.

D. Comparator & SR Latch

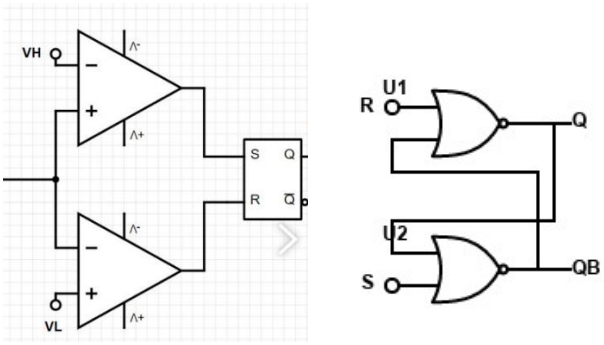

Figure 2.6: The left picture shows the overall architecture of Comparator & SR_latch, the right picture shows the SR_latch structure

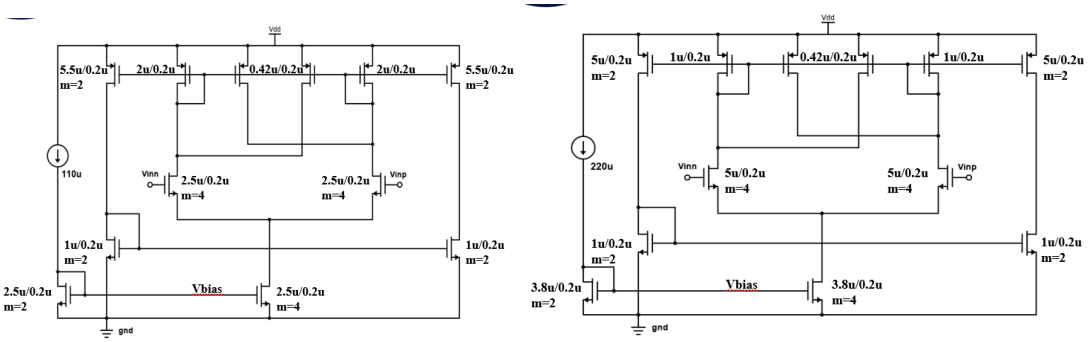

Figure 2.7: The left picture shows the Comparator up structure, the right picture shows the Comparator down structure.

The function of the comparator is to limit the integration range of the integrator. When the output voltage of the integrator is greater than VH = 1.2V or less than VL = 0.6, the comparator changes state. This causes the subsequent SR latch to generate feedback signals Q and !Q, controlling the switch (NMOS) at the input of the integrator. This forces the integrator to switch from charging to discharging or from discharging to charging, thereby restricting the integration range of the integrator to 0.6-1.2V. Additionally, the output Q of the SR latch is connected to the subsequent circuit, the counter. To reduce

the impact of comparator delay on the circuit, we adjusted the parameters of the internal MOSFETs in the comparator, reducing the hysteresis effect of the comparator to minimize the frequency error of the converted signal.

E. Counter & D-Flip Flop

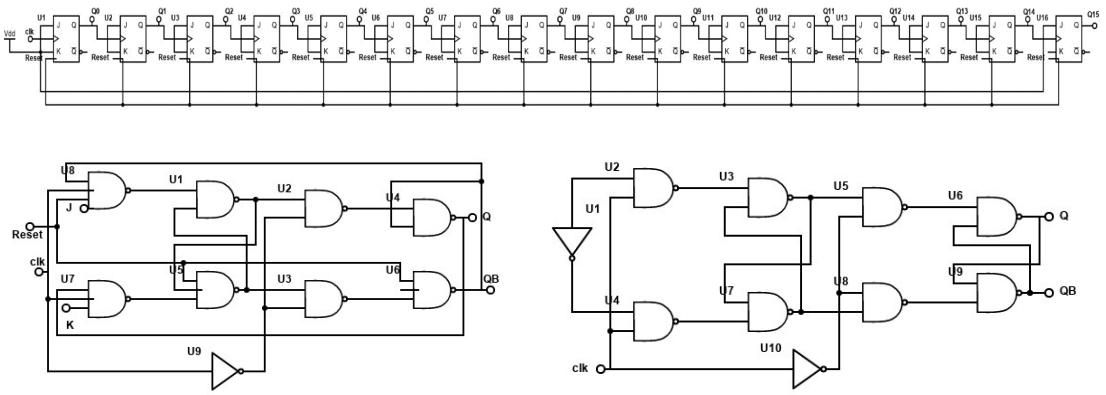

Figure 2.8: The upper picture shows the circuit structure of counter, the lower left picture shows the circuit structure of JKFF, and the lower right picture shows the circuit structure of DFF.

When the integrator undergoes the charging-to-discharging or discharging-to-charging transition, the output Q of the SR latch is also controlled by the comparator to undergo a transition, forming a periodic waveform. Therefore, a counter and a D-Flip-Flop are used to read this periodic waveform and convert the result into a digital output. This facilitates signal frequency analysis by the backend recognition system for the analysis of sensor resistance.

F. Op_Vbias circuit

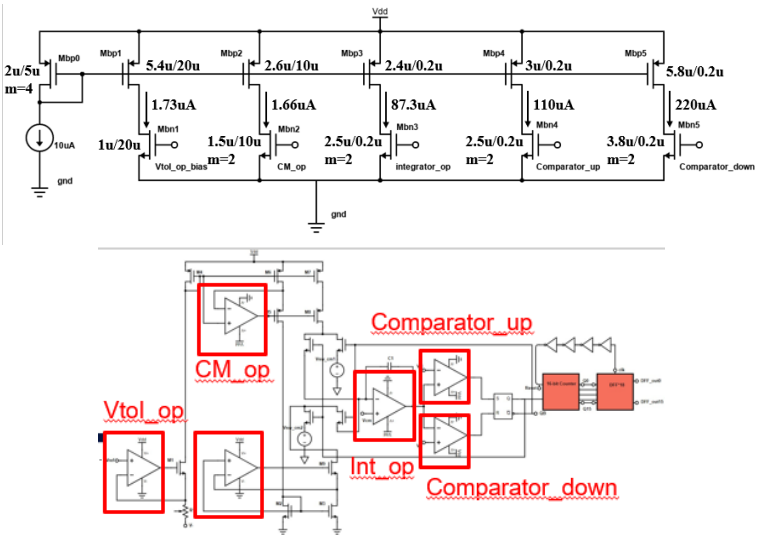

Figure 2.9: The picture above shows the circuit structure of OP_Vbias, and the picture below shows the OP that needs to use Vbias.

From the previous circuit architecture diagram, it is known that each of the six operational amplifiers (OPs) requires a Vbias voltage. Therefore, as shown in the diagram above, a current source (10uA) is designed, and Mbp0 corresponds to the current mirror structure of Mbp1~Mbp5, forming the gate bias for Mbn1~Mbn5 for each OP.

4. SPEC

Table 2.2: Expected SPEC table

Specification	
Power Supply(V)	1.8
Resistance Dynamic range	500Ω-5MΩ
Counter Output bit	16
Total current(mA)	4.5
Total Power(mW)	8
Chip size(mm^2)	1.2mm * 1.2mm
Core Area	0.4mm * 0.4mm
Maximum Relative error	3%
Integrator Range(ΔV)	0.6 - 1.2V

DR = 20*log(Rmax /Rmin * 2^$Nres$), set Rmax = 5M, Rmin = 500, in pursuit of DR=140dB, Nres is set to 16, that is, the digital output has 16 bits, reaching precision from 0.1%~ 0.4%.

III. Experiment Results

1. Pre-Sim

- **Period and VDD current in all corner**

Vref = 50mV Rsens = 500ohm 27 ℃ TT

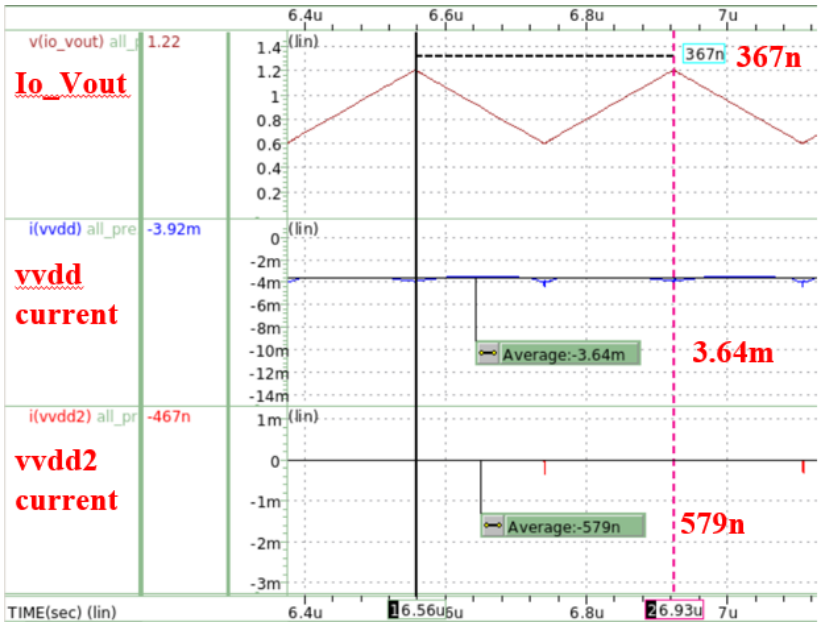

Figure 3.1: Triangular wave period diagram and VDD current (used to calculate power)

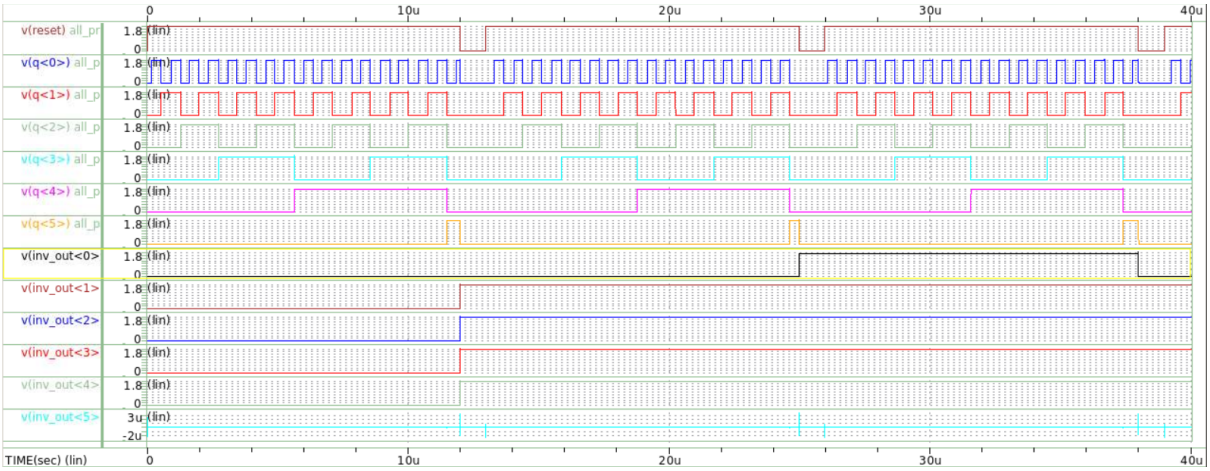

Figure 3.2: Digital waveform diagram

The reset picture above shows the reset signal of the input counter and DFF. q<0>~q<5>are the five bits of the counter LSB. The counter keeps counting up. The frequency of the up counting is the frequency of the triangle wave, inv_out<0> ~inv_out<5> is the result of counting and comparing the output wave of counter q<0>~q<5> into DFF and reference clk.

For simulation results of other Vref, Rsens, temperature, and corner combinations, please refer to Table 3-1 below.

Table 3.1: ALL_ckt Presim in diff. condition

Vref=50mV	500 ohm			500k ohm		
	27 ℃			27 ℃		
Corner	TT	SS	FF	TT	SS	FF
Period	367n	363n	364n	359u	365u	366u
Power	6.55m	5.84m	10.3m	6.34m	5.84m	10.3m

Vref=500mV	5k ohm			5M ohm			50M ohm		
	27 ℃			27 ℃			27 ℃		
Corner	TT	SS	FF	TT	SS	FF	TT	SS	FF
Period	364n	359n	357n	360u	360u	357u	3.59m	3.6m	3.58m
Power	6.55m	5.83m	10.3m	6.34m	5.83m	10.3m	7.85m	6.10m	10.7m

- **All block power comparison**

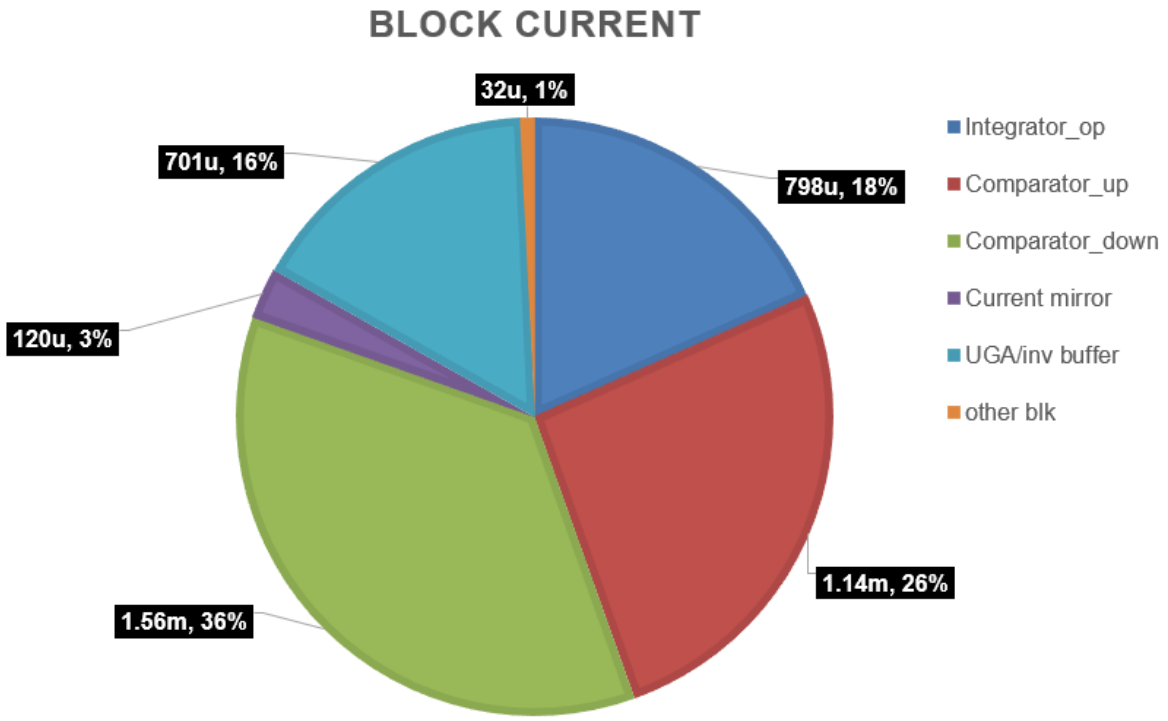

Figure 3.3: Block current pie chart

Analyzing the overall circuit, we can observe the current and power distribution in each subregion. Since the entire architecture uses a 1.8 V VDD, the current relationship also reflects the power relationship. It is evident that the most power-consuming circuits are the two comparators, followed by the integrator. This is due to the high bandwidth requirements of these three operational amplifiers to achieve a linear and stable waveform at high frequencies for the triangular wave. UGA and inv buffer also consume a significant amount of power. Their roles are to buffer the analog and digital signals to the output pad, allowing external measurements of the chip through the PCB board.

Referring to Table 2-1, we find that the current mirror flows 100uA in the leftmost circuit and 1/10 of the current in the other two branches when the minimum resistance is present. Therefore, the total current simulated for the current mirror is indeed 120uA.

- **Period relative error with resistance variation**

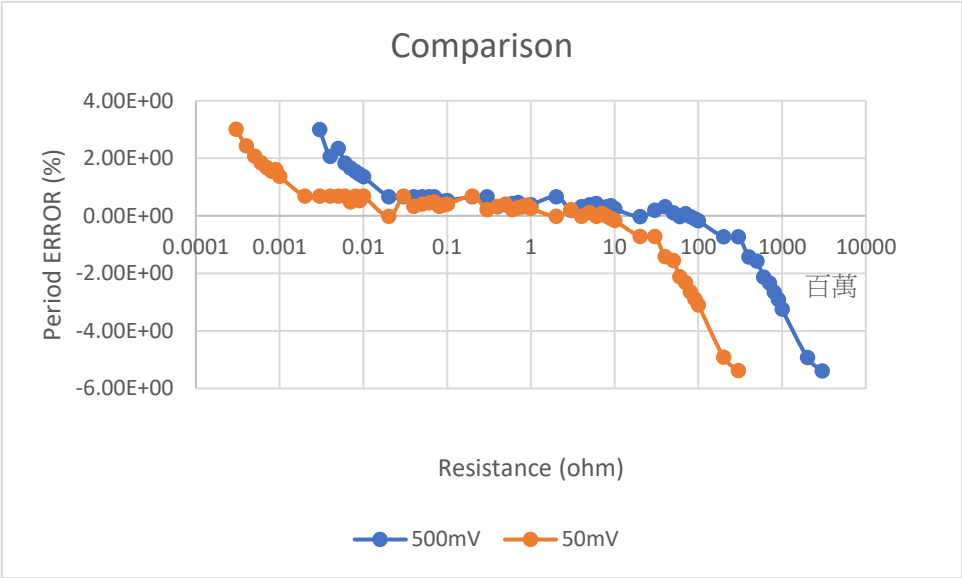

Figure 3.4: Vref = 500mV/50mV period error comparison

In Presim, we finally recorded the periods for Vref = 500mV, 3000 ohms3000M ohms, and Vref = 50mV, 300 ohms300M ohms, respectively. We calculated the arithmetic average of the periods for each case and then calculated the error between each resistance period and its average value, obtaining the graph shown above. Using a ±1% error as a reference, the overall circuit can measure a resistance range covering 2000 ohms to 300M ohms. Therefore, in the dynamic range (DR) formula DR = 20log(Rmax /Rmin * 2^$Nres$), where Nres = 16 bits, the dynamic range is DR = 20log(300M /2000 * 2^16) = 200dB. This exceeds the initial project's expectation of a dynamic range greater than 141dB.

2. Post-Sim

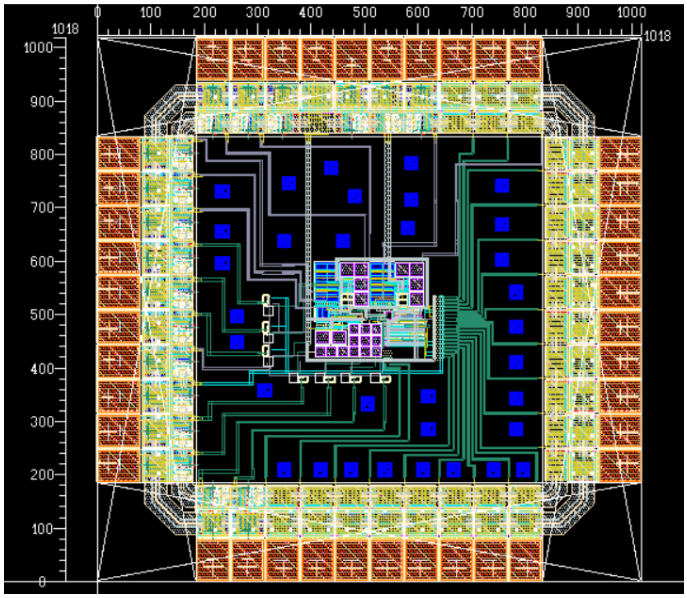

Figure 3.5: Interface circuit layout

- **Postsim with pad Period and VDD current in all corner**

  Vref = 50mV Rsens = 500ohm 27 ℃ TT

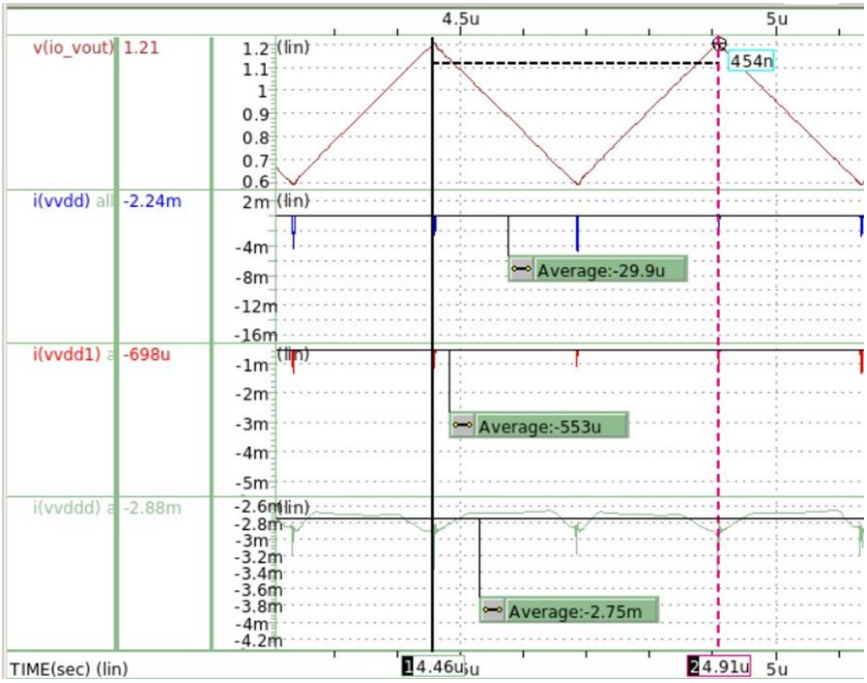

Figure 3.6: Postsim triangle wave period diagram and VDD current (used to calculate power)

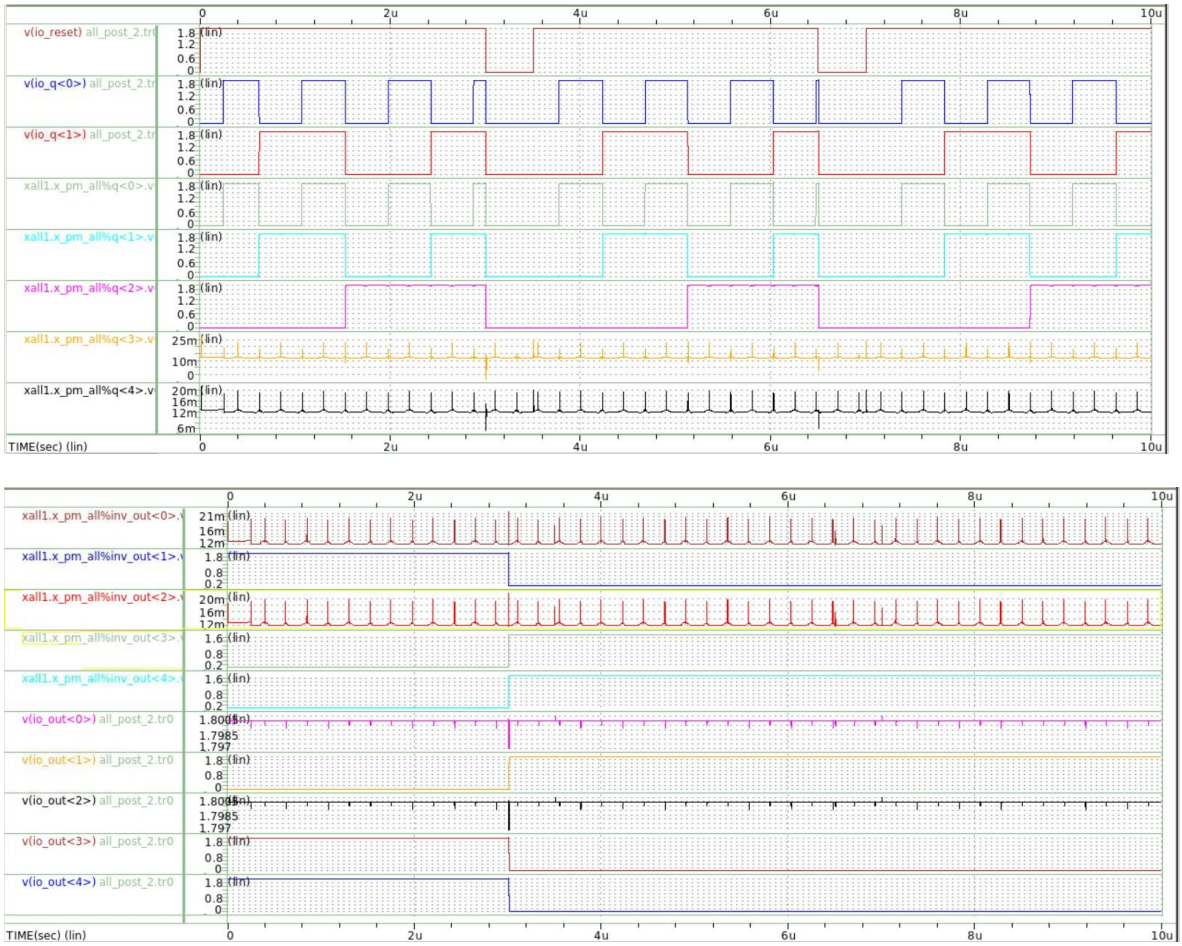

Figure 3.7: Digital part Postsim waveform diagram

The diagram shows that io_reset is an external input for the reset signal to the counter and DFF. q<0> to q<4> represents the 4 least significant bits (LSB) of the counter within the circuit, indicating that the counter is continuously counting upward, and the counting frequency corresponds to the frequency of the triangular wave.

Among them, io_q<0> and io_q<1> represent the measured values of q<0> and q<1> connected to the PAD. inv_out<0> to inv_out<4> take the output waves of counter q<0> to q<4> and feed them into DFF along with the reference clock for counting and comparison. io_out<0> to io_out<4> represent the digital signals, and inv_out<0> to inv_out<4> are their inverted versions. These signals are then sent through inv buffers to the PAD for output. Therefore, the signals are inversely related.

For the results of post-simulation with different combinations of Vref, Rsens, temperature, and corner, please refer to Table 3-2.

Table 3-2: ALL_ckt Postsim in diff. condition

Vref=50mV	500 ohm						500k ohm					
	27 ℃			37 ℃			27 ℃			37 ℃		
Corner	TT	SS	FF	TT	SS	FF	TT	SS	FF	TT	SS	FF
Period	392n	454n	338n	388n	450n	339n	369u	424u	316u	370u	423u	316u
Power	7.56m	6.00m	10.1m	7.60m	6.01m	10.1m	7.26m	5.71m	9.79m	7.31m	5.73m	9.85m

Vref=500mV	5k ohm						5M ohm					
	27 ℃			37 ℃			27 ℃			37 ℃		
Corner	TT	SS	FF	TT	SS	FF	TT	SS	FF	TT	SS	FF
Period	377n	431n	324n	379n	431n	324n	367u	424u	316u	369u	422u	317u
Power	7.56m	6.00m	10.1m	7.61m	6.01m	10.2m	7.26m	5.71m	9.79m	7.31m	5.73m	9.84m

3. Presim and Postsim comparison

SPEC

Table 3.3: SPEC

Specification	SPEC	Pre-sim(TT)	Post-sim(TT)
Power Supply(V)	1.8V(Analog)	1.8V(Analog)	1.8V(Analog)
Dynamic Range	500Ω-5MΩ	500Ω-300MΩ	500Ω-5MΩ
Counter Output bit	16	16	16
Total Current(mA)	4.5	3.52~3.64	3.34~3.46
Total Power(VDD,mW)	8	6.336~6.552	6.012~6.228
Chip size(mm^2)	<1.2 x 1.2		1.018 x 1.018
Integrator Range(ΔV)	0.6-1.2V	0.58 – 1.22V	0.58 – 1.22V

Table 3.4: Presim and Postsim period and power comparison

	500ohm			500kohm				5kohm			5Mohm		
	27℃			27℃				27℃			27℃		
Corner	TT	SS	FF	TT	SS	FF	Corner	TT	SS	FF	TT	SS	FF
Period (post)	392n	454n	338n	369u	424u	316u	Period (post)	377n	431n	324n	367u	424u	316u
Power (post)	7.56m	6.00m	10.1m	7.26m	5.71m	9.79m	Power (post)	7.56m	6.00m	10.1m	7.26m	5.71m	9.79m
Period (pre)	367n	363n	364n	359u	365u	366u	Period (pre)	364n	359n	357n	360u	360u	357u
Power (pre)	6.55m	5.84m	10.3m	6.34m	5.84m	10.3m	Power (pre)	6.55m	5.83m	10.3m	6.34m	5.83m	10.3m

From the above comparison, it can be roughly observed that the power in postsimulation is only slightly larger than in presimulation. The MOS threshold voltage (Vth) follows the order SS > TT > FF, so the FF corner MOS has the maximum current, leading to the highest power consumption. As for the period in postsimulation, there is a significant difference between corners. This is due to the presence of capacitors in the OP and Integrator sections of the architecture. The values of these capacitors are significantly influenced by the corner in the manufacturing process. Therefore, during actual measurements, methods such as adjusting Vref are employed to make the period approach the simulated value in presimulation.

IV. Conclusion

The circuit's objective is to implement a low-power, wide dynamic range gas sensor. Analog resistance signals are converted into digital outputs by the circuit, which are then observed as frequencies. To achieve a wide dynamic range, additional digital output bits are introduced. The circuit incorporates two Vref values (50mV, 500mV) for controlling current levels (100n~100u), optimizing energy consumption. The architecture provides a 200dB dynamic range, covering resistance values from 2000 ohms to 300M ohms, with a maximum

relative error of 1% and 16 bits of digital output. The circuit, implemented in a 180nm process, occupies an area of 1.04M um^2, consumes 3.4mA current, and has a power consumption of 6mW.

As observed in Fig. 3-3, the currents in comparator_up and comparator_down are the highest, followed by the integrator, constituting about eighty to ninety percent of the total power consumption. This is due to the need for stable integration waveforms and comparator functionality, requiring a large number of parallel MOS transistors (m) in both cases. For instance, the second stage of the integrator OP uses m=10. Further improvements in this area could potentially enhance the overall power consumption compared to the referenced paper.

V. Reference

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VI. Acknowledgements

After reviewing multiple papers on IoT sensor interface circuits and considering the specifications outlined in these papers, our objective was to develop a circuit using a smaller 90nm process and a low 1.2VDD. We aimed to achieve lower power consumption than the 6mW specified in the papers while having the capability to measure resistances as low as 500 ohms. The decision was made to adopt an oscillator-based resistance readout circuit. The project timeline included completing the VtoI op and Current mirror designs from April to May,

Integrator, Comparator, and SR_latch designs from May to June, counter and logic design with presim simulations from June to July, and finally, layout + postsim from July to August, leading to the tape-out.

During this period, we faced challenges with the integrator, attempting to balance the bandwidth requirement (above 500kHz for a stable triangular wave) while meeting the specified low current demand. We persevered through discussions and explored various adjustments, such as increasing capacitance to modify the positions and sequence of first and second-order poles. Ultimately, it was suggested to switch to the 180nm process and increase VDD from 1.2V to 1.8V, resulting in a successful implementation.

I would like to express my sincere gratitude to Professor Kea-Tiong (Samuel) Tang for his invaluable guidance and support throughout this project. His expertise and insights were instrumental in navigating the challenges we encountered, particularly during discussions regarding adjustments to the integrator and the decision to switch to the 180nm process. Professor Tang's continuous involvement, encouragement, and provision of resources in the laboratory greatly contributed to the success of our implementation. I am truly appreciative of the opportunity to work under his mentorship and benefit from his wealth of knowledge in the field.