University of California, Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EE140, EE240A Fall 2023
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Final Design Project and *Student Design Competition*

Check In: By Thursday 11/16/2023 or Friday 11/17/2023
Report Due: Sunday, Dec. 3, 2023 on Gradescope

1) Project Introduction

A **liquid-crystal display (LCD)** is a common display technology used in flat panel displays, TVs, computers and mobile devices. LCD screens use the light-modulating properties of liquid crystals, which do not emit light directly; they require external light (backlight) to produce a visible image. Voltage applied across an LCD pixel polarizes the light and determines the amount of light that passes through the pixel. LCDs can require high voltages to fully polarize and maximize contrast. A description of how LCD displays work can be found at https://en.wikipedia.org/wiki/File:Lcd-engineerguy.ogv.

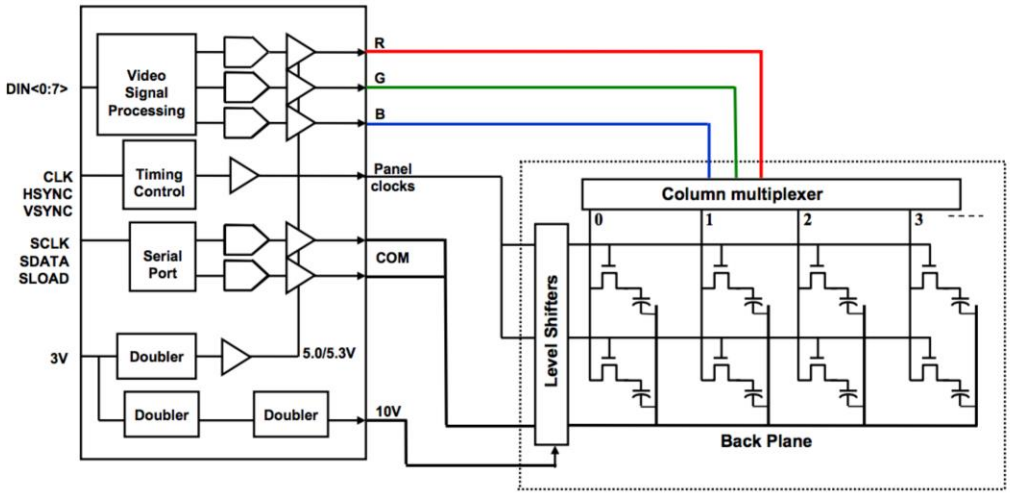


Figure 1: Example LCD driver

LCD pixels are often organized in an active matrix as shown in Figure 1. Each composite LCD pixel is comprised of a red, a green and a blue pixel, each driven by an individual amplifier. These amplifiers scan across all pixels in the array, updating the voltage stored on the pixel capacitance, thus updating the image. This rapid scanning requires the amplifier to set an accurate pixel voltage within a short period of time. LCD displays commonly operate at a refresh rate of 60 Hz. In this project, you will be designing a driver for a 38-mm smartwatch display, which has 272 x 340 pixels. Your driver must drive *all pixels sequentially* in the display in one period of the refresh rate.

Image processing is computed in the digital domain and a display driver includes Digital to Analog converters. Therefore, the amplifier takes it's input from an ideal 0.7V fullscale 10-bit digital to analog converter (DAC). The most difficult transition that the amplifier must make is a full swing of 1.4V, creating a dark to light transition. Each pixel in an LCD display has a capacitance from 10s to 100s of pF. The interconnect and transistors in the array add a large series resistance on the order of hundreds of ohms. In our model, we will use a series resistance of 400 Ohms and a capacitance of 60 pF as shown in Figure 2. You will be designing the amplifier depicted below to the specifications in Table 1.

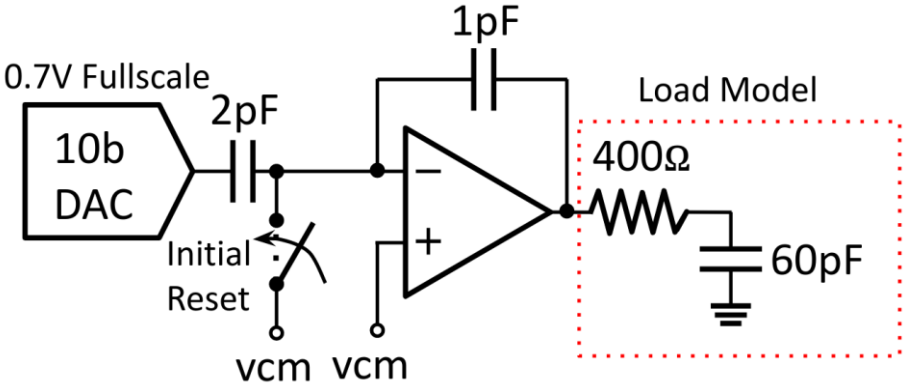


Figure 2: LCD driver amplifier with pixel load model. The output is at the pixel capacitor terminal after the series resistance.

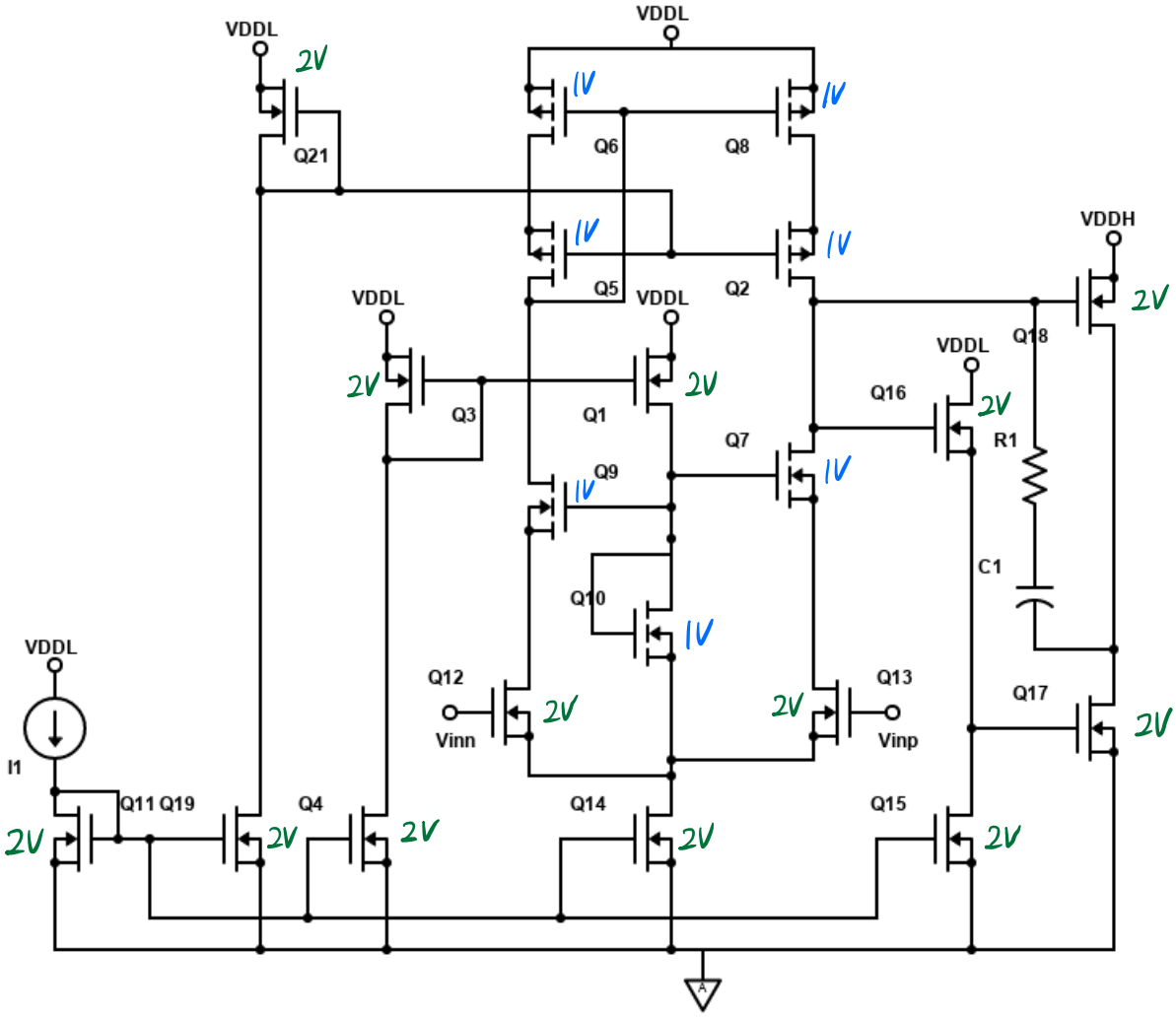
Table 1: Design Specifications

Course	**EE 140**	**EE 240A**
Technology	Gpdk045	
Power Supplies	GND (0V), VDDL (< 1.1V), VDDH (<1.8V)	
Closed Loop DC Gain	2	
Load	400 Ohms, 60pF (output at capacitor)	
Settling Time (T_{settle}) $= \max\{T_{settle,rise}, T_{settle,fall}\}$[1]	***to be calculated*** **for 1.4V output step rising and falling**	
Total Error	≤0.2%	
Power Consumption	**≤ 1.1 mW**	**≤ 0.6 mW**
Output Voltage Swing	≥ 1.4V	
Maximum Current Mirror Ratio	20	
Maximum Total Capacitance[2]	4p F	2p F
Maximum Total Resistance	100M Ohm	10M Ohm
CMRR at DC	≥65dB	
PSRR at DC	≥50dB	
Phase Margin	≥ 45°	
Figure of Merit (FoM) to Maximize	$\frac{10^{-9}}{T_{settle} \times P_{total}}$	

[1]Settling time is defined as the maximum of the rising and falling settling times for a 1.4V output step.
[2]Defined as total capacitance of explicit capacitors added to the design. This excludes the load and the feedback capacitors.

I. Overview

- **Schematic**



- **Comparison with Target Specifications**

Property	Specification	Achieved
Power Supplies	VDDL≤1.1V | VDDH≤1.8V	VDDL=1.1V|VDDH=1.8V
Closed Loop DC Gain	2	2
Load	RL=400Ω | CL=60pF	RL=400Ω | CL=60pF
Max. Settling Time	180ns	174ns
Total Error	≤ 0.2%	0.193%
Power Consumption	≤ 1.1mW	610uW
Output Voltage Swing	≥ 1.4V	≥ 1.4V
Max. Mirror Ratio	20	20
Max. Added Capacitance	4pF	30f
CMRR at DC	≥ 65dB	68.93dB
PSRR at DC	≥ 50dB	50.17dB
Phase Margin	≥ 45°	45.39°
FOM	≥ 5.05	9.43

- **Circuit Operation**
  I aim to design an amplifier tailored for an LCD display, focusing on achieving low error, high swing, and low power consumption. In the first stage, I employ a telescopic cascode to attain the desired gain, complemented by a meticulously designed current mirror to establish optimal biasing points. Acknowledging the limitations in voltage swing associated with the **telescopic cascode**, I introduce a **class AB amplifier** for my second stage to enhance swing capabilities. Additionally, I utilize a common-source configuration to set the DC output bias point, contributing to the overall performance of the amplifier. The subsequent design section will delve into detailed insights regarding these design choices and their impact.

II. Design

- **Stage 1 Design Considerations**
  Objective: The primary objective of the first stage is to achieve a substantial gain that fulfills the specified static error requirement of 0.2%. Additionally, it aims to allocate a significant portion of this gain to contribute effectively to the dynamic transient error.

  Initial Attempt with Differential Pair: In the initial phase of the design process, a conventional differential pair was considered for the first stage. Despite meticulous size optimization, the gain achieved proved insufficient to meet the stringent static error specifications.

  Telescopic Cascode: To overcome the limitations in gain, the design approach was shifted to incorporate a telescopic cascode amplifier. This configuration was selected for its ability to substantially increase the gain from gmro to **gmro^2**. The telescopic structure offered a favorable trade-off between gain and swing, aligning with the project's specific requirements.

  Current Mirror: To enhance stability and ensure predictable operating conditions, a current mirror was incorporated into the design. The current mirror plays a crucial role in maintaining a precise biasing current, contributing to a consistent quiescent point. Leveraging the inherent advantages of the telescopic cascode architecture, which inherently provides higher gain compared to a simple differential pair, the introduction of a current mirror further amplifies the gain by guaranteeing a constant and well-defined bias current.

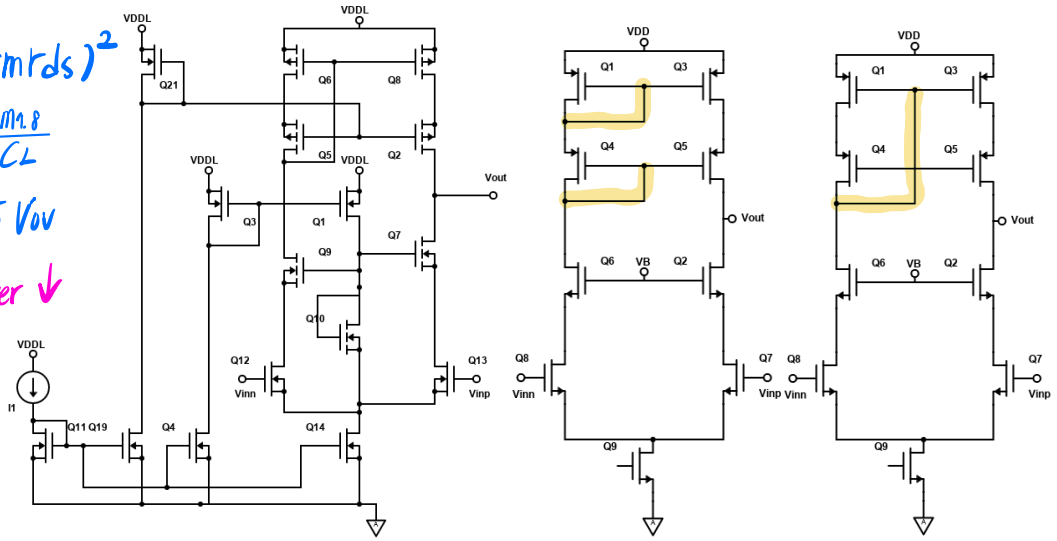
Gain: $A_D = \frac{1}{2}(g_m r_{ds})^2$

Cutoff freq $= \omega_t = \frac{g_{m1,8}}{C_L}$

$V_{out(swing)} = V_{DD} - 5V_{ov}$

So, fast and Power ↓

But $V_{out,swing}$ ↓.



Tied V_{B4} directly to $V_{B(1,3)}$ to prevent waste on V_{th}. (Swing ↑)

$V_X = V_{DD} - V_{SG1} - V_{SG4} \Rightarrow V_{out(max)} = V_{DD} - V_{OV1} - V_{OV4} - |V_{th}|$

But for Y, $V_{out(max)} = V_{DD} - V_{OV1} - V_{OV4}$ larger!

Design Methodology:

1. Sizing

- **Quiescent Current and Voltage Calculation**
  The first step involves calculating the quiescent current and voltage parameters for the telescopic cascode, accounting for the integration of a current mirror. The calculated gm/Id values are then input into a MATLAB analysis using the Lab2 code. This analysis assists in identifying the point of maximum gain per unit current, thereby establishing the optimal range for gm and ro.

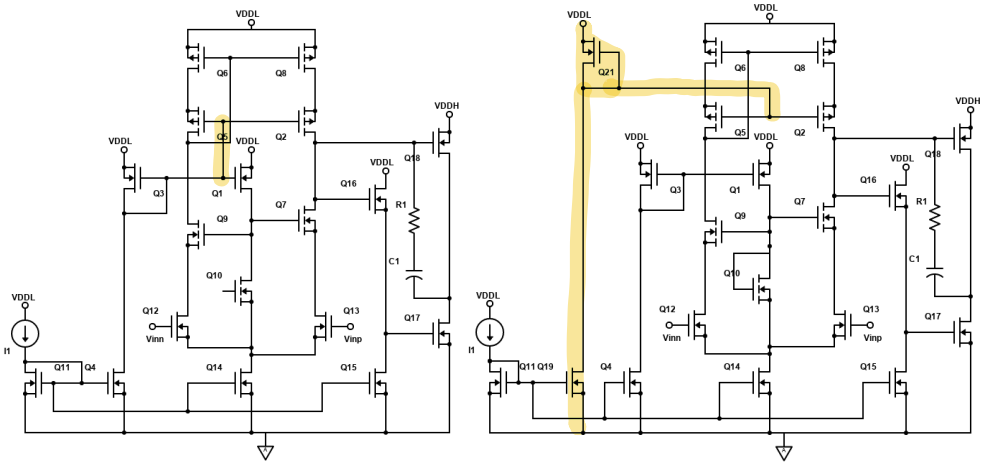
- **Optimal Size Determination**
  While designing the first stage, the focus is on obtaining the range of optimal sizes rather than precise values. Emphasis is placed on biasing as the primary design consideration during this stage.

2. Biasing

- **Current Mirror Implementation**
  A current mirror with a very low current (2uA) is employed to set the DC operating point for the NMOS and PMOS transistors in the telescopic cascode. Initially, attempts were made to use the same current mirror for both the NMOS and PMOS biasing points. However, this approach proved problematic for the PMOS due to its sensitivity to low currents, pushing it into the linear region and compromising DC output.

- **Dual Current Mirror Configuration**
  In response to the PMOS challenges, a valuable insight from Avi led to the implementation of an additional pair of current mirrors. This configuration addressed the low current issue for the PMOS, ensuring stable DC operation and preserving the integrity of the output.

- **MATLAB Look-Up Function**
  The MATLAB look-up function played a pivotal role in sizing, providing a more accurate assessment of device parameters. The look-up table, based on given device parameters, facilitated precise determination of raw Vgs and Vds values. This approach was found to be more reliable than relying on arbitrary cross-ratios. Adjusting the bias voltage as needed enhanced the similarity of gds values in a given **cascode stack.**



3. Important Variables

- **Length**: We know that The length of the transistors is a critical variable that impacts various aspects of the amplifier's performance. Opting for higher length values tends to result in minimal changes in power consumption, a significant increase in voltage gain, and a slower settling error. However, the choice of length is carefully tuned to balance the improvement in static error against the potential trade-off in settling response. In this design, a length of 480nm is chosen, not only for its optimization in static error but also for its facilitation of sizing considerations.
- **Input Common Voltage (Vcm)**: Initially set at the default value of 0.45V, the input common voltage (Vcm) underwent iterative adjustments during the design process. After sizing both stages and meeting CMRR, PSRR, and phase margin specifications, it became apparent that reducing power consumption while maintaining low settling error was challenging. A strategic increase in Vcm from 0.45V to 0.6V proved instrumental, resulting in a considerable reduction in error and a drop in settling time from 0.22us to 0.15us.
- **Vds, sat:** Controlling the saturation voltage (Vds, sat) is achieved by manipulating the width of the transistors, particularly focusing on devices in which the impact of gm is less pronounced. This approach, especially for PMOS devices in the first stage, ensures effective control over saturation voltage and contributes to overall amplifier performance.

Pros:

- **High Gain:** The choice of a telescopic cascode configuration enables a substantial increase in gain, a critical factor in achieving a small static error. The gain is elevated from gmro to gmro^2, contributing significantly to the amplifier's overall performance.

- **Improved Linearity:** The quadratic dependence of gain on ro in the telescopic cascode enhances linearity, ensuring a more accurate and predictable response.

Cons:

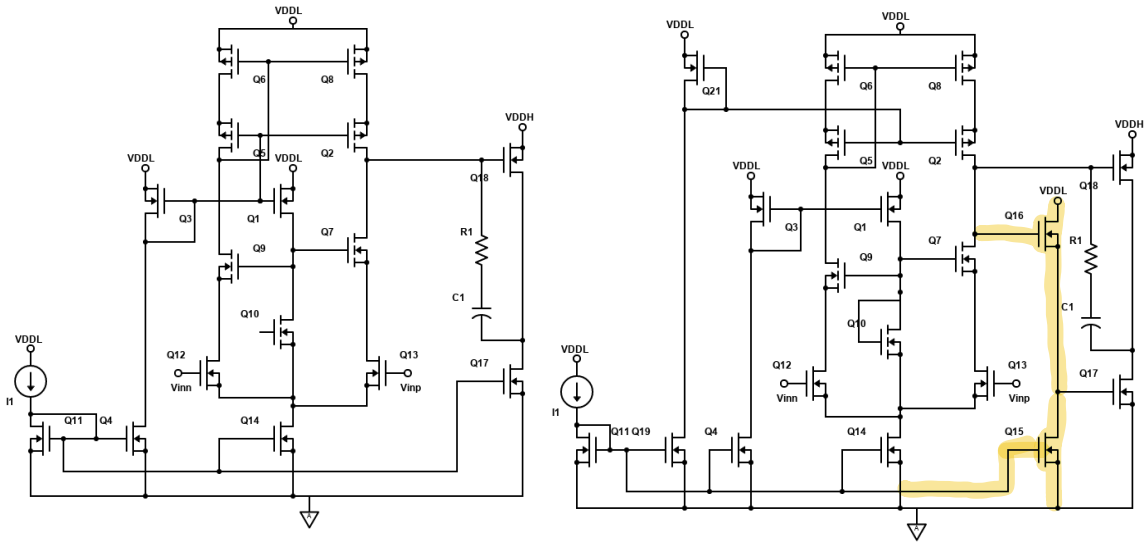
- **Reduced Swing:** A trade-off is introduced by the telescopic circuit, which drives a small capacitance (miller compensation cap), leading to a reduction in swing. However, this trade-off is considered acceptable given the chosen class AB configuration for the second stage. The benefits in terms of gain and linearity outweigh the limitations in swing for the specific design objectives.

- **Stage 2 Design Considerations**

Objective: The primary objective of the second stage is to enhance the output voltage swing while preserving a high gain and improving overall linearity. To achieve these specifications, a combination of a Class AB amplifier and a common-source amplifier with Miller compensation is employed.

Why Class AB Amplifier? The selection of a Class AB amplifier for the second stage is driven by the desire to harness the benefits of both Class A and Class B amplifier configurations. This choice is strategic in minimizing crossover distortion and extending the output swing. Given that the project's ultimate goal is to achieve low error, high voltage swing, and a fast frequency response, the Class AB amplifier aligns with these objectives.

Initial Attempt without Common Source Amplifier: In the initial design phase for the second stage, a Class AB amplifier with RC compensation was considered. However, a significant challenge emerged when attempting to set the biasing point of the NMOS in the Class AB configuration. The conventional approach of creating another current mirror pair proved impractical due to the substantial width required, surpassing a mirror ratio of 20. Recognizing this limitation, a pivotal decision was made to incorporate a common-source amplifier into the design. This addition not only addressed the biasing challenges but also resulted in a substantial increase in gain.



Why Common Source Amplifier? The Common Source Amplifier is an integral component of the second stage, chosen for its ability to provide high voltage gain and suitability for driving loads with low input impedance. Additionally, it functions as an effective DC level shifter, capable of biasing with generally low current (<=3uA). Its unique characteristics, including the ability to use relative widths to set VGS of the NMOS device, make it a valuable addition to the circuit. Moreover, it overcomes the slew-rate limit, which is advantageous for the power-hungry Class AB configuration, leveraging the increased gm,eff.

Design Methodology:

- **Sizing:** The sizing process for the Common Source Amplifier involves a combination of automated tools and manual adjustments. While initial sizing is performed using Matlab scripts, the final tuning is done through hand calculations. This is necessitated by the need to ensure that the DC output_load is maintained at 0.9V to maximize the output swing. The iterative process involves adjusting the width of the PMOS of the Common Source Amplifier, which, in turn, influences gm,p, Wnmos, and Ibias.
- **Current and Bias:** The length of the Common Source Amplifier is selected based on the unity-gain frequency calculated, with consideration given to avoiding violations of the unity-gain frequency threshold. A balance is struck between achieving higher gain and preventing excessive power consumption. The size of the PMOS in the Class AB amplifier is crucial in determining the overall power consumption of the circuit. Larger widths result in increased power consumption, requiring careful optimization.

- **RC Miller Compensation**

  Objective: The primary objective of integrating RC Miller compensation in the telescopic cascode amplifier, serving as the first stage, is to enhance bandwidth and stability while preserving the voltage gain. This compensation technique plays a pivotal role in mitigating the challenges associated with multiple dominant poles in the two-stage operational amplifier. Without compensation, the telescopic cascode amplifier might exhibit insufficient phase margin, introducing the risk of instability and oscillatory behavior.

  Design Methodology:

  - **Tuning Parameters**

  The design methodology for RC Miller compensation involves a reliance on Virtuoso sweep due to Matlab's limitations in predicting slew-rate. The key parameters tuned are Rm (resistance) and Cm (capacitance), which have a significant impact on phase margin. The tuning process focuses on optimizing these parameters to ensure stability and adequate bandwidth.

  - **Slew-Rate Considerations**

  Given Matlab's limitations in predicting slew-rate, the Virtuoso sweep becomes crucial for obtaining accurate values of Cm and Rm. While these parameters might not significantly affect settling error, their influence on phase margin is crucial for maintaining stability. Therefore, the tuning of Rm and Cm becomes a critical step in achieving the desired performance.

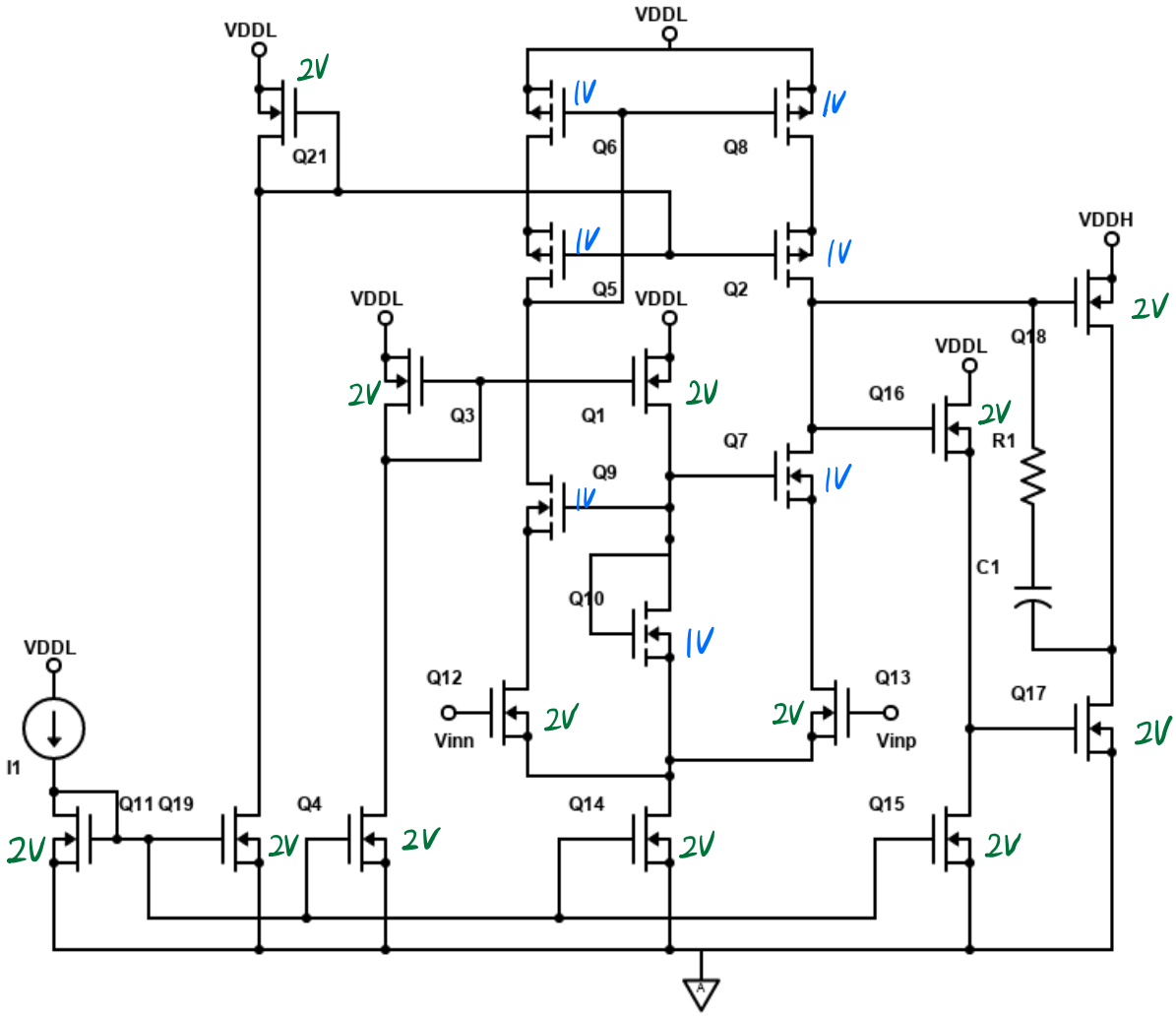
  Pros:

  - **Enhanced Bandwidth:** RC Miller compensation contributes to an overall enhancement in bandwidth, crucial for meeting dynamic performance requirements.
  - **Improved Linearity:** The quadratic dependence of gain on ro in the telescopic cascode enhances linearity, ensuring a more accurate and predictable response.
  - **Improved Stability:** By addressing multiple dominant poles, RC Miller compensation significantly improves the stability of the telescopic cascode amplifier, reducing the risk of instability and oscillations.

  Cons:

  - **Parameter Tuning Complexity:** The tuning of Rm and Cm, particularly in the absence of accurate slew-rate predictions from Matlab, introduces an element of complexity. However, this trade-off is deemed acceptable for the benefits gained in stability and bandwidth.

III. Transistor and Bias Summary

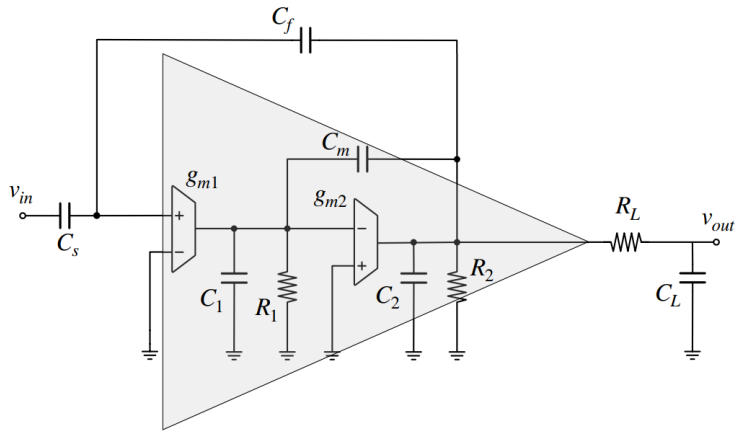


#Transistor	W/L (um)	|ID| (uA)	|Vgs| (V)	Gm (uA/V)	Gds (1u/Ω)
Q11	1.5/0.48	1.999	0.497	34.16	//NA(2V)
Q19	20/0.48	24.35	0.497	425.7	//NA(2V)
Q21	1/0.48	24.35	0.655	145	4.8
Q4	6.5/0.48	7.41	0.497	130	//NA(2V)
Q1、Q3	1/0.48	7.41、6.79	0.616	70	//NA(2V)
Q6、Q8	5.8/0.48	10.63	0.441	219	6.46、6.39
Q2、Q5	10/0.48	10.63	0.418	219	5.5、7.6
Q7、Q9	35/0.48	10.63	0.36	244	18.5、11.68
Q10	0.4/0.48	6.79	0.649	45.5	1.1
Q12、Q13	100/0.48	10.63	0.379	255	//NA(2V)
Q14	30/0.48	28	0.497	507	//NA(2V)
Q16	150/0.48	6.85	0.265	193.3	3.04
Q15	2/0.48	6.85	0.497	100	5.065
Q18	6.5/0.48	2.38	1.28	1.43	//NA(2V)
Q17	300/0.48	2.38	0.251	69.1	//NA(2V)

IV. Discussion

Matlab Script Analysis:

At week2, we assume the ideal behavior simulation to design the two stage amplifier. By letting gmro = 100(V/V), f_T = 10GHz, Cm = 1pF, CL = 60pF, and $C_{DD} = \frac{C_{GG}}{10}$ for calculation. After putting C1, C2, R1(ro1), R2(ro2), gm1, gm2 into the script, we can do the iteration to get the optmized miller capacitance.



Closed loop 3dB frequency = Loop Gain's unity gain = 100MHz

For Phase Margin = 45°, the Non-Dominant Pole = 100MHz = $\frac{gm2}{C1+C2+CL} \approx \frac{gm2}{CL}$

gm2 = 100M*CL = 100M*(60p) = 6m (A/V)

$\frac{Non-Dominate\ Pole}{Loop\ Gain} = \frac{100M}{\frac{gmro}{2}*\frac{gmro}{2}*\beta}$ = 80kHz

80kHz = $\frac{1}{gm2*R1*R2*Cm}$ => R1*R2 = $\frac{1}{80k*6m*1p}$ = 2083.3MΩ

R2 = ro2 = $\frac{100}{gm2}$ = 16.67kΩ => R1 = $\frac{2083.3M}{16.67k}$ = 124.973k

gm1 = $\frac{100}{124.973k}$ = 0.8m(A/V)

$C_{GG}1 = \frac{gm1}{2\pi f_T} = \frac{0.8m}{2\pi*10G}$ = 12.7fF

$C_{GG}2 = \frac{gm1}{2\pi f_T} = \frac{6m}{2\pi*10G}$ = 95.54fF

$C_{DD}1 = \frac{C_{GG}1}{10} = \frac{6m}{2\pi*10G}$ = 1.27fF

$C_{DD}2 = \frac{C_{GG}1}{10} = \frac{0.8m}{2\pi*10G}$ = 9.554fF

C1 = $C_{DD}1 + C_{GG}2$ = 96.81fF

C2 = $C_{DD}2$ = 9.554fF

Return Ratio = $\frac{V_o}{V_{in}} * \beta = \frac{gm1(gm2-Gc)}{G1+Gc} \frac{1}{G2+Gc+\frac{gm2-Gc}{G1+Gc}Gc} * \frac{1}{3}$

Z1 = R1 // C1 = $\frac{ro1}{1+ro1*C1*S}$

ZL = RL + $\frac{1}{CL*S}$

Zfb = $\frac{1}{Cs*S} + \frac{1}{Cf*S}$

Z2 = R2 // C2 = $\frac{ro2}{1+ro2*C2*S}$

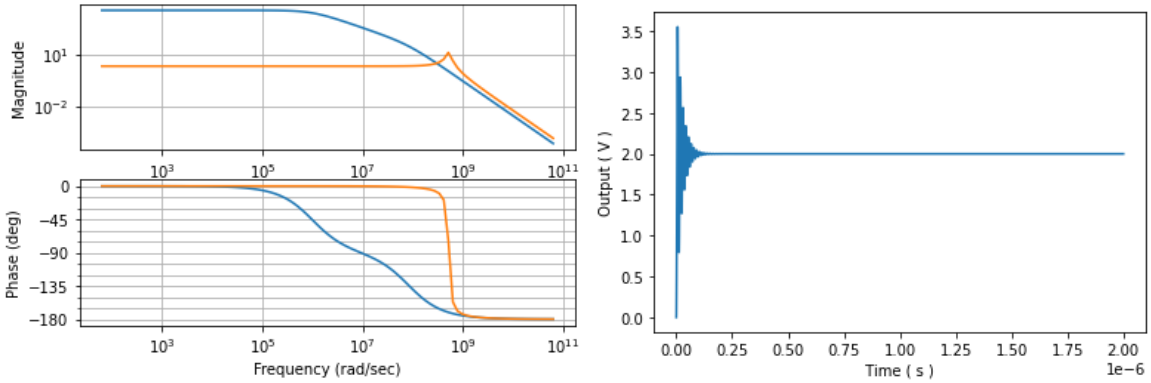
Zmiller = $\frac{1}{Cm*S}$

A-inf = Cs * S * ($\frac{1}{Cf*S} + RL$)

A-closed loop = A-inf * $\frac{RR}{1+RR}$

Before adding the Compensation Capacitance and Resistance?

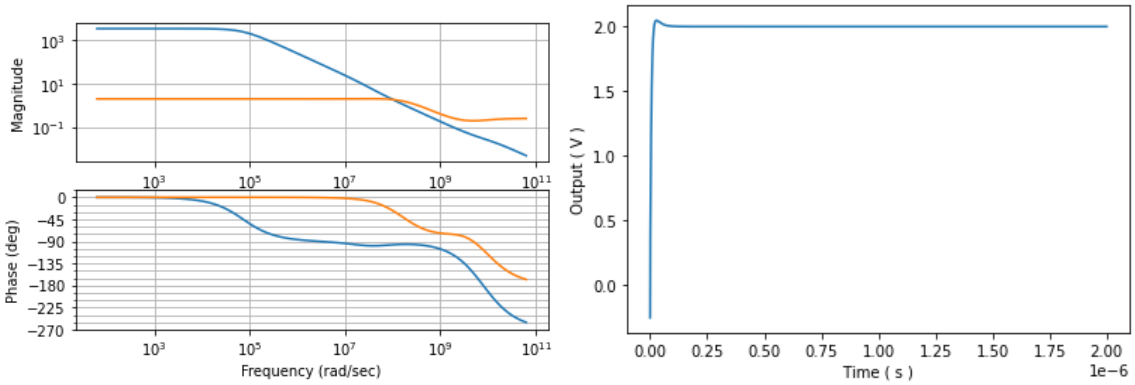
- **Initial Phase Margin:** Without compensation, the telescopic cascode amplifier may exhibit a lower initial phase margin.
- **Dominant Poles:** The open-loop gain of the amplifier will have dominant poles, and the phase response might not provide sufficient stability.
- **Risk of Instability:** In the absence of compensation, the amplifier may be prone to instability, leading to potential oscillations.




```
Open Loop Phase Margin = (inf, 9.164089907235706, nan, 518641363.5082205)
Closed Loop Phase Margin = (inf, 7.952628306980785, nan, 901107048.3696125)
```

After adding the Compensation Capacitance and Resistance?

- **Introduction of Zero:** The compensation network introduces a zero in the transfer function, strategically placed to counteract the effect of dominant poles.
- **Increased Phase Margin:** Properly designed compensation, with the addition of Cm and Rm, leads to an increase in phase margin.
- **Improved Stability:** The compensation circuit actively contributes to stabilizing the amplifier by providing additional phase lead.
- **Reduced Risk of Oscillations:** The phase margin improvement significantly reduces the risk of instability and oscillatory behavior in the amplifier.




```
 Open Loop Phase Margin = (33.07939043285198, 84.04784009907837, 7937857818.408965,
183286716.03893992)
Closed Loop Phase Margin = (inf, 120.35784443372074, nan, 341687850.41657364)
```

Impact of Cm and Rm Values:

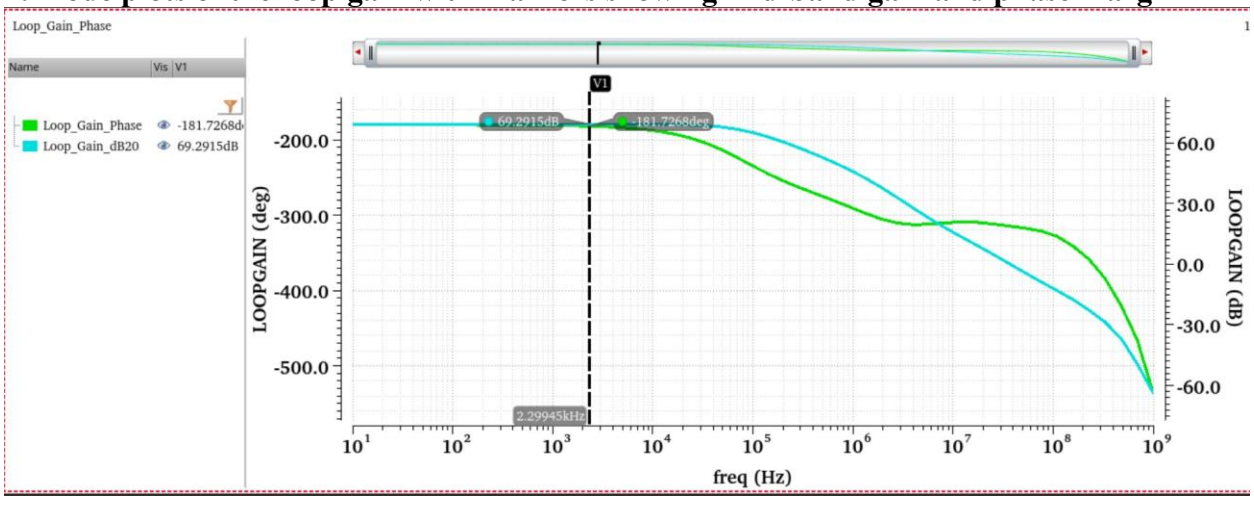
- **Tuning for Stability:** The specific values of Cm and Rm play a crucial role in determining the effectiveness of compensation.
- **Increased Cm:** A higher compensation capacitance (Cm) tends to introduce more phase lead, potentially increasing the phase margin.
- **Optimal Rm:** Proper selection of the compensation resistance (Rm) is necessary for achieving the desired stability without compromising bandwidth excessively.

Trade-offs in Compensation:

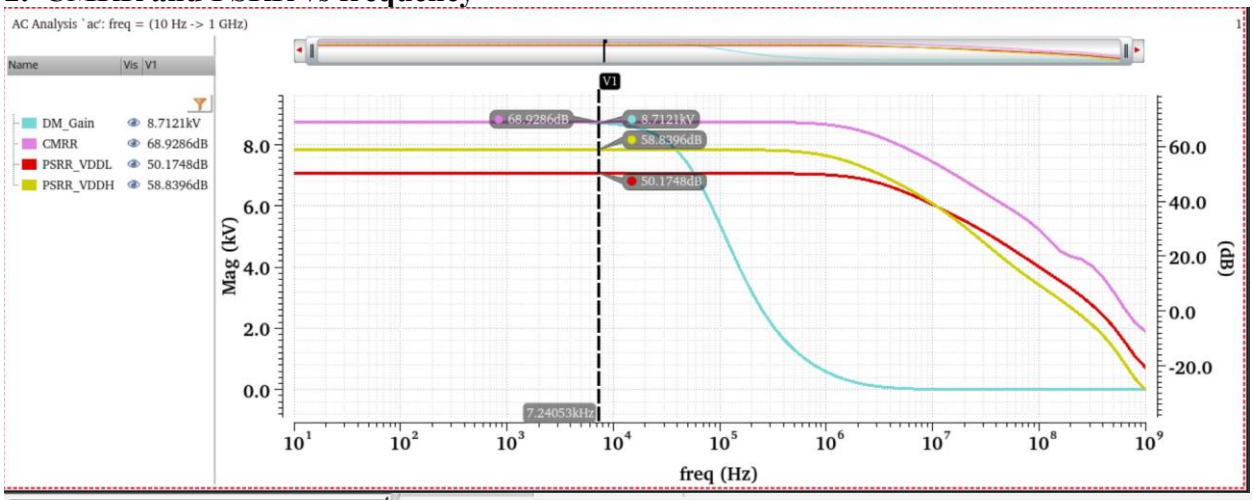
- Bandwidth Considerations: While compensation enhances stability, there is a trade-off with bandwidth. Excessive compensation may reduce the bandwidth of the amplifier.
- Optimization Process: Designers engage in an optimization process to find the right balance, ensuring that stability requirements are met without sacrificing essential performance metrics.

AC Analysis

1. Bode plots of the loop gain with markers showing mid-band gain and phase margin



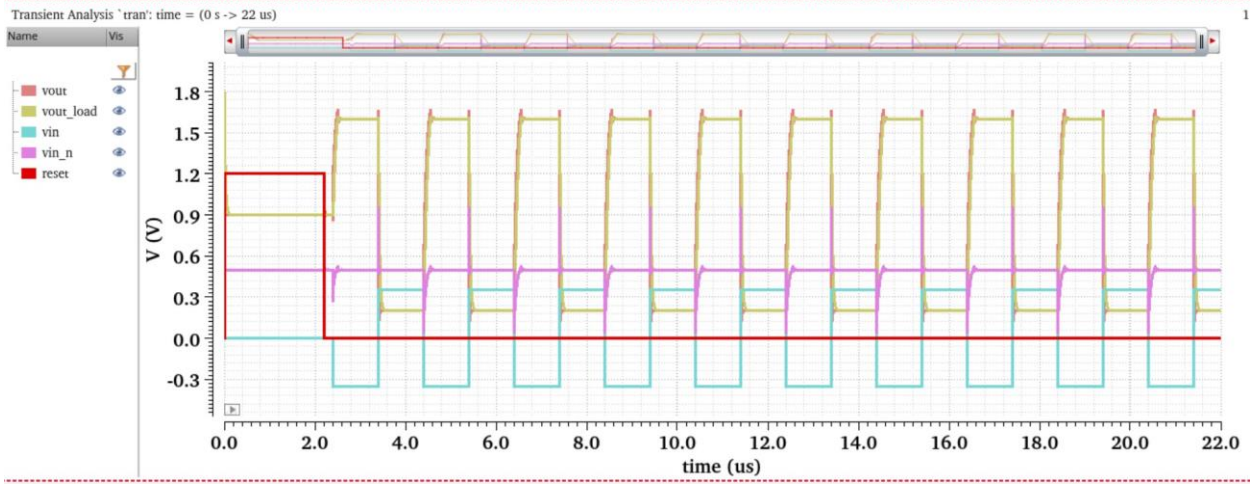
2. CMRR and PSRR vs frequency



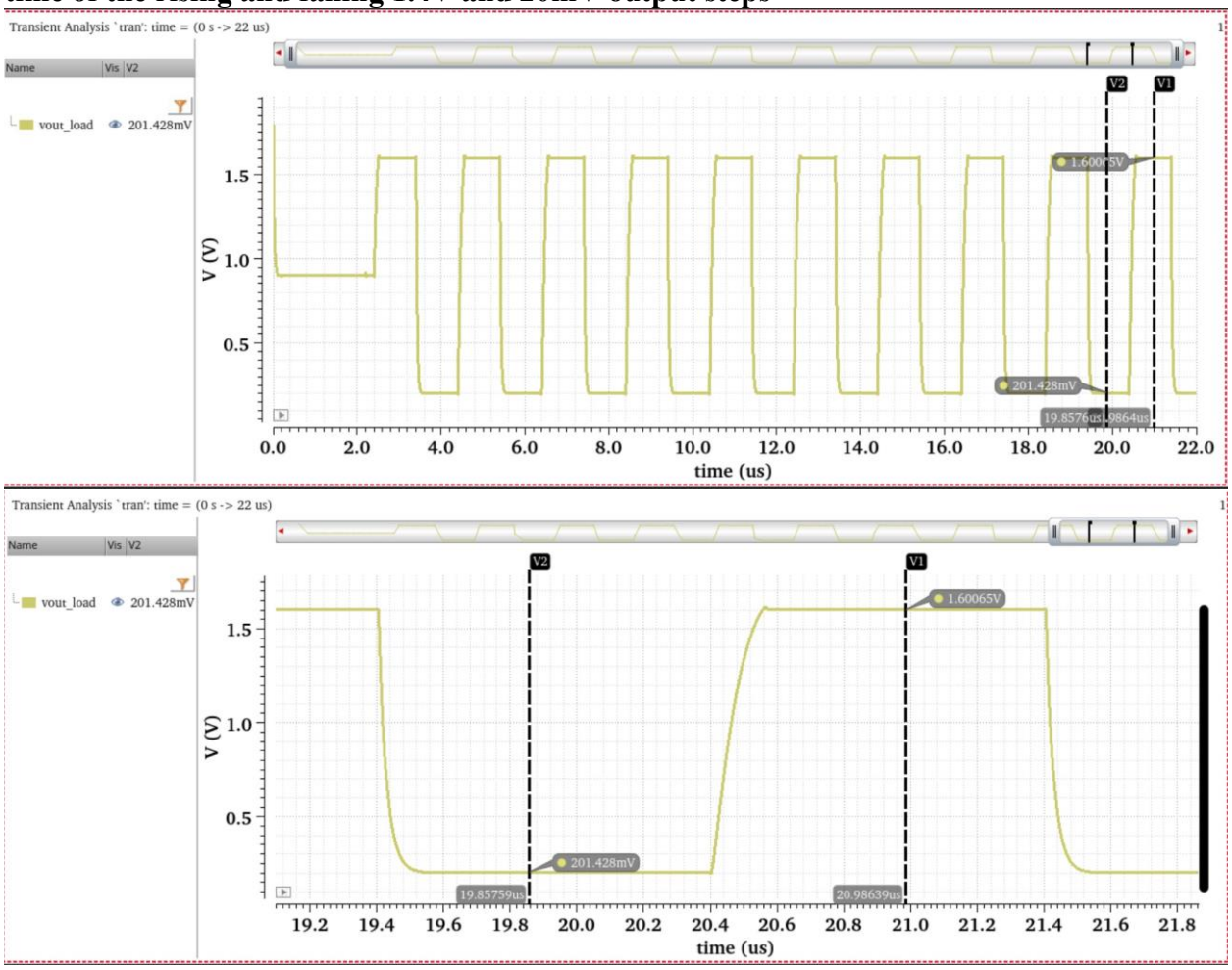
Name	Type	Details	Value
CM_Gain	expr	vfreq('ac "/vcm_out")	
DM_Gain	expr	vfreq('ac "/vdm_out")	
CMRR	expr	dB20((DM_Gain / CM_Gain))	
CMRR_at_DC	expr	value(CMRR 10)	68.93
VDDL_Gain	expr	vfreq('ac "/vps_out_vddl")	
VDDH_Gain	expr	vfreq('ac "/vps_out_vddh")	
PSRR_VDDL	expr	dB20((DM_Gain / VDDL_Gain))	
PSRR_VDDH	expr	dB20((DM_Gain / VDDH_Gain))	
Loop_Gain_Phase	expr	phaseDegUnwrapped(getData("loopGain" ?result "st...	
Loop_Gain_dB20	expr	db(mag(getData("loopGain" ?result "stb")))	
PSRR_H_at_DC	expr	value(PSRR_VDDH 10)	58.84
PSRR_L_at_DC	expr	value(PSRR_VDDL 10)	50.17
PM	expr	getData("phaseMargin" ?result "stb_margin")	45.39

Transient Analysis

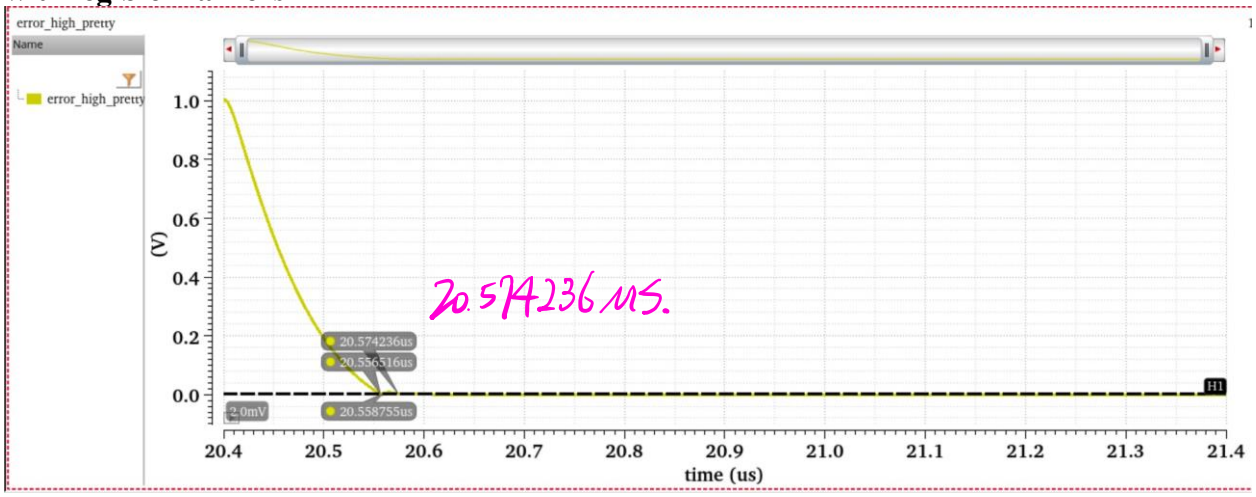
All waveforms in a plot



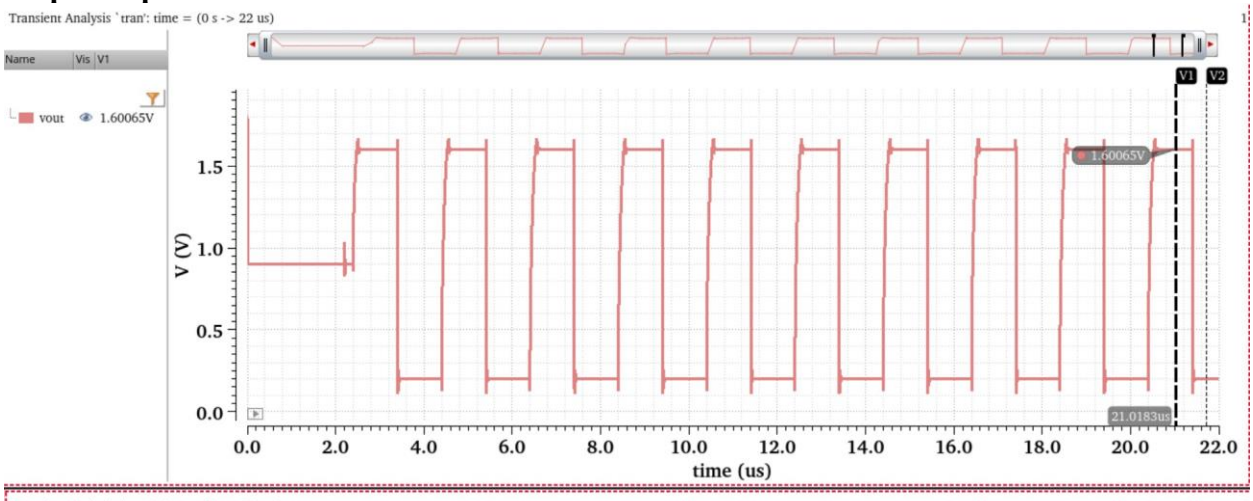
1. Waveform of the voltage at the load capacitor with legible markers for the settling time of the rising and falling 1.4V and 20mV output steps

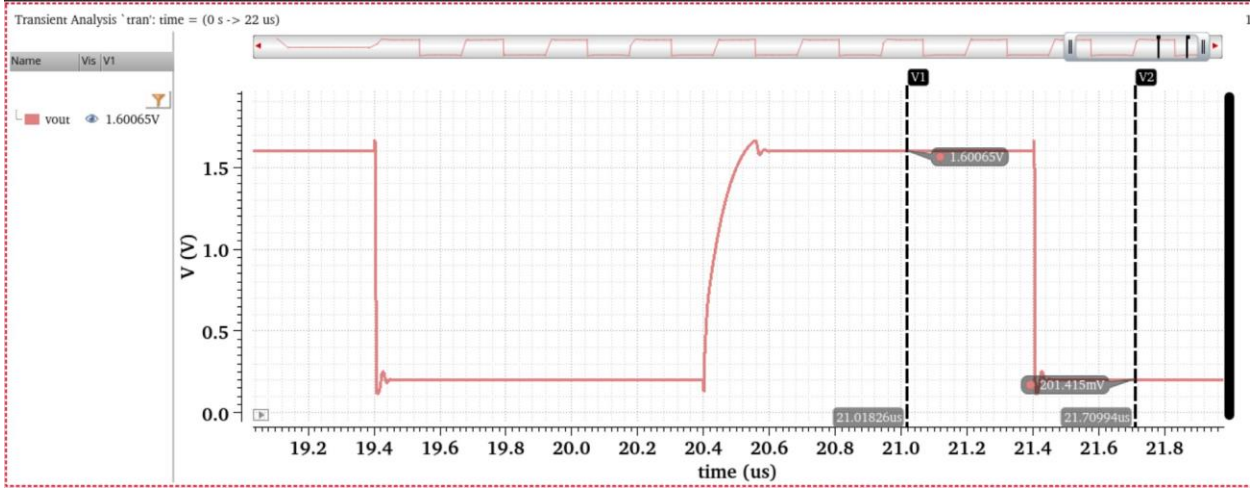


2. Settling error for rising and falling 1.4V and 20mV output steps at the load capacitor with legible markers

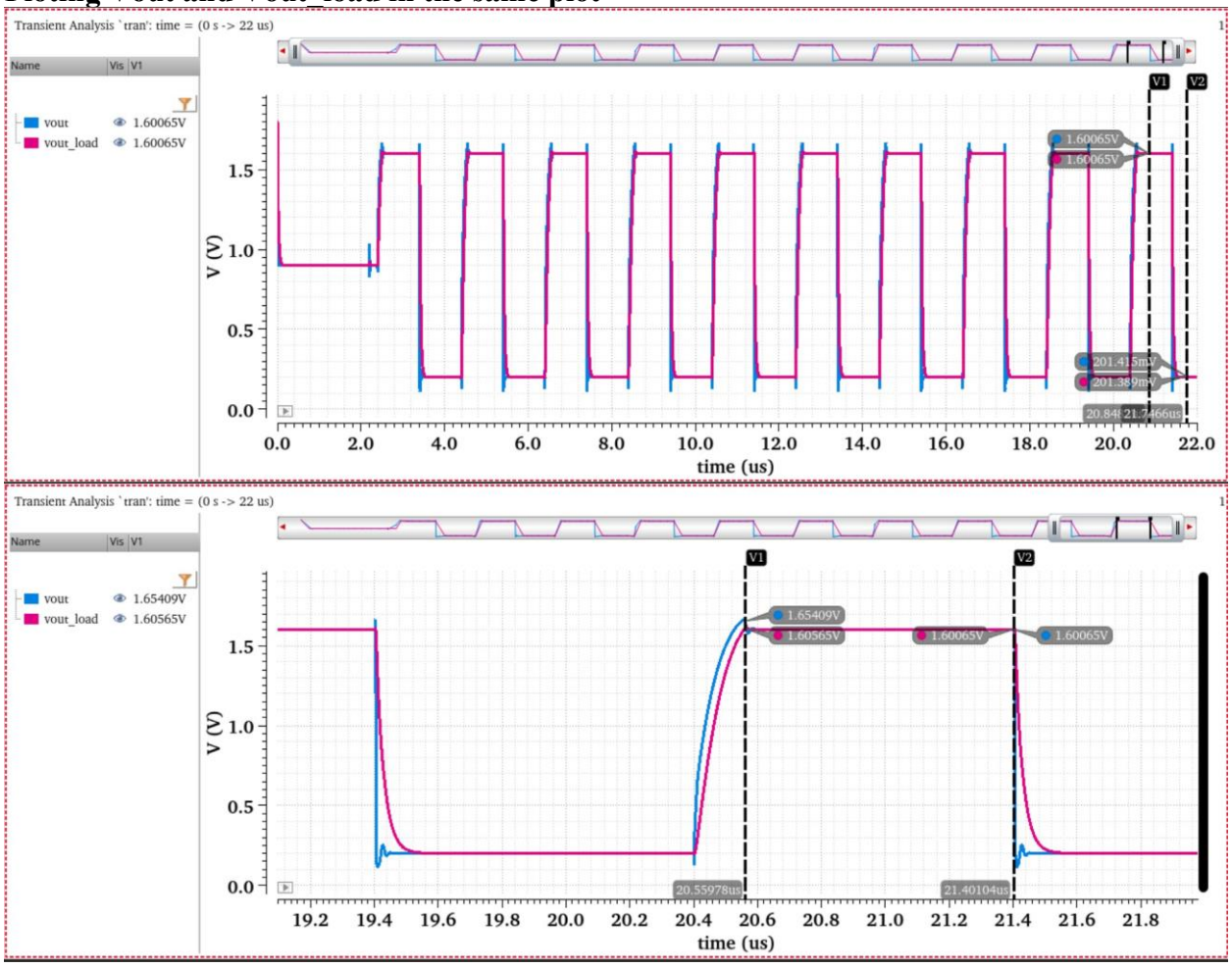


3. Waveform of the voltage at amplifier output for the rising and falling 1.4V and 20mV output steps



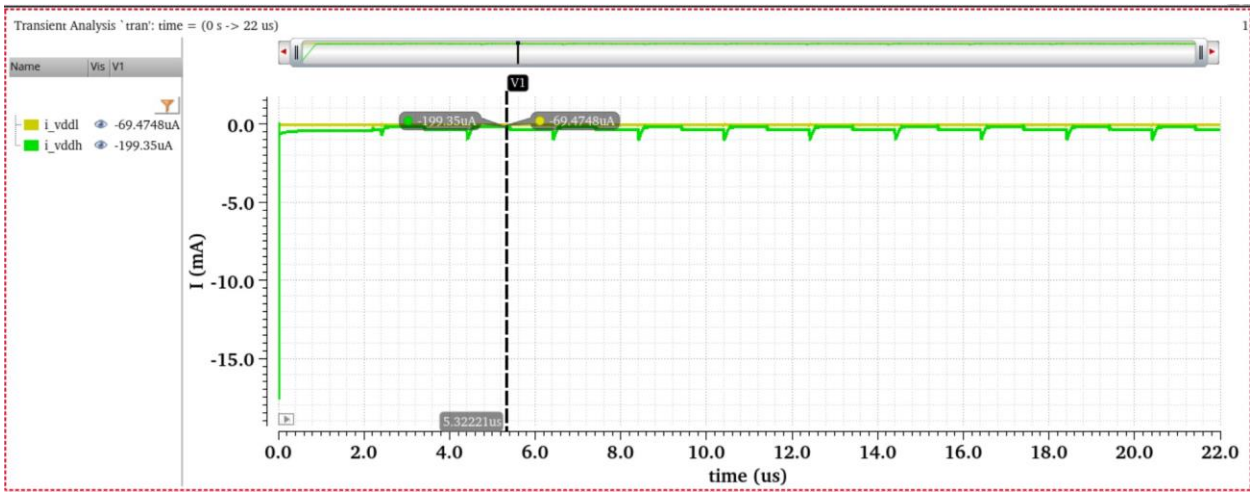


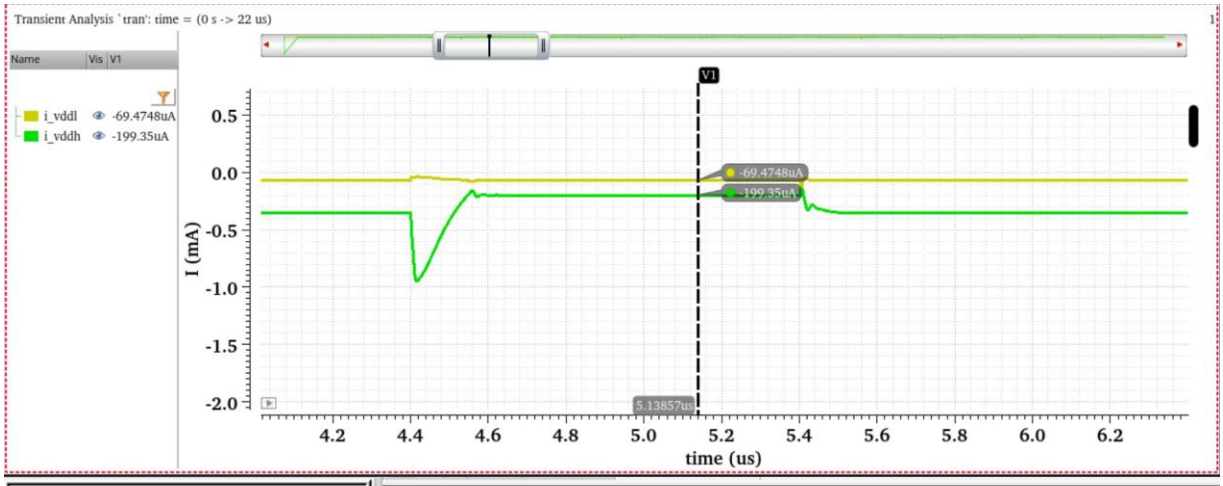
Ploting Vout and Vout_load in the same plot

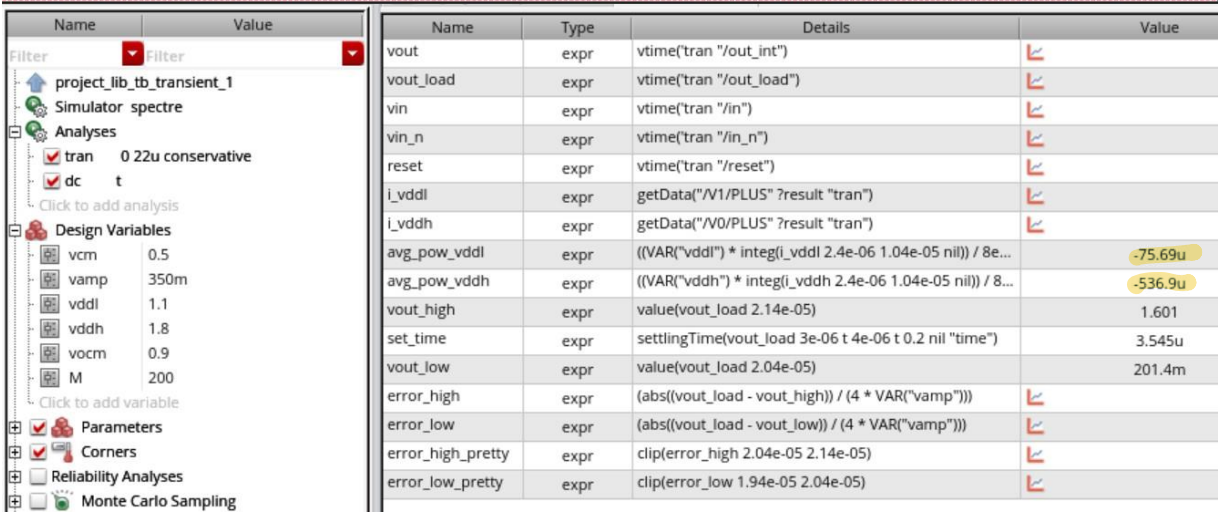


The overshoot from Low to High is the result of too much RC compensation, but this compensation is crusial for the High to Low. The linear decrease in High to Low can be improve with more compensation comparing with other transitions.

4. Waveform of the currents drawn from VDDH and VDDL







Name	Type	Details	Value
vout	expr	vtime('tran "/out_int")	
vout_load	expr	vtime('tran "/out_load")	
vin	expr	vtime('tran "/in")	
vin_n	expr	vtime('tran "/in_n")	
reset	expr	vtime('tran "/reset")	
i_vddl	expr	getData("/V1/PLUS" ?result "tran")	
i_vddh	expr	getData("/V0/PLUS" ?result "tran")	
avg_pow_vddl	expr	((VAR("vddl") * integ(i_vddl 2.4e-06 1.04e-05 nil)) / 8e...	-75.69u
avg_pow_vddh	expr	((VAR("vddh") * integ(i_vddh 2.4e-06 1.04e-05 nil)) / 8...	-536.9u
vout_high	expr	value(vout_load 2.14e-05)	1.601
set_time	expr	settlingTime(vout_load 3e-06 t 4e-06 t 0.2 nil "time")	3.545u
vout_low	expr	value(vout_load 2.04e-05)	201.4m
error_high	expr	(abs((vout_load - vout_high)) / (4 * VAR("vamp")))	
error_low	expr	(abs((vout_load - vout_low)) / (4 * VAR("vamp")))	
error_high_pretty	expr	clip(error_high 2.04e-05 2.14e-05)	
error_low_pretty	expr	clip(error_low 1.94e-05 2.04e-05)	

Design Considerations and Trade-Offs

Primary Focus on Power and Settling Time

The paramount concern in the design process revolves around minimizing power consumption, as it directly impacts the Figure of Merit (FOM). Given that settling time is relatively easier to attain, the main emphasis is on achieving low power while meeting specified requirements.

Telescopic Cascode and Initial Design:

- **Voltage Gain Optimization:** The telescopic cascode is chosen to achieve a high voltage gain of around 300V/V, crucial for minimizing static error.
- **Output DC Voltage for Second Stage:** Initial design includes setting the output DC voltage for the second stage input. The accurate sizing of transistors is not critical, considering the subsequent stages will alter the original biasing point.

Challenges in Power Reduction

- **Power-Settling Time Trade-Off:** Achieving low power consumption while maintaining low settling time becomes a challenging trade-off.
- **Choice of Supply Voltages:** Utilizing VDDL (1.1V) for the first stage and the RC compensation. However, for the class AB amplifier, a higher VDDH (1.8V) is employed to ensure an output voltage swing over 1.4V (0.2V~1.6V).

Trade-Off Strategies I took

- **Increase in Vcm and MOS Transistor Widths:**
  Approach: Elevate the settling error by increasing the input common voltage (Vcm).
  Trade-Off: This approach sacrifices CMRR but is mitigated by increasing the width of Vcm MOS transistors from 20um to 100um in the first stage. The impact on power consumption in the first stage is acceptable due to its relatively lower contribution.

- **Compensation Capacitance Size Reduction:**
  Approach: Decrease the size of the compensation capacitance by a factor of ten (from 300pF to 30pF).
  Trade-Off: While reducing settling time, this decreases the Phase Margin. However, compensating for the Phase Margin reduction is manageable by increasing the compensation resistance.

- **Avoid Decreasing VDDH:**
  Rationale: Instinctively decreasing VDDH is considered but dismissed due to the significant negative impact on settling time.

Optimization and Conclusion:
The iterative approach involves evaluating the trade-offs and optimizing key parameters to achieve the desired balance between low power consumption and rapid settling time. The final design strategically incorporates these trade-off strategies to meet stringent specifications and enhance the overall performance of the operational amplifier.

Here's my other thoughts on optimizing FOM (If I have more time):

1. Decrease Stage 1 Current (Reduction in power consumption)
2. Increase MOS Lengths of Stage 1 (Higher gain with an allowance for increased dynamic error)
3. Tuning Biasing Voltages Using Current Mirror (Precise control over biasing conditions)
4. Decrease Lengths of Stage 2 (Trade-off power for improved settling time)
5. Decrease RC Compensation (Optimize settling time without compromising stability)

Final Result:

Property	Specification	Achieved
Power Supplies	VDDL≤1.1V | VDDH≤1.8V	VDDL=1.1V|VDDH=1.8V
Closed Loop DC Gain	2	2
Load	RL=400Ω | CL=60pF	RL=400Ω | CL=60pF
Max. Settling Time	180ns	174ns
Total Error	≤ 0.2%	0.193%
Power Consumption	≤ 1.1mW	610uW
Output Voltage Swing	≥ 1.4V	≥ 1.4V
Max. Mirror Ratio	20	20
Max. Added Capacitance	4pF	30f
CMRR at DC	≥ 65dB	68.93dB
PSRR at DC	≥ 50dB	50.17dB
Phase Margin	≥ 45°	45.39°
FOM	≥ 5.05	9.43

V. Conclusion

This project has been a challenging analog design experience for me, providing insights into the complexities of putting the theoretical knowledge we learned in class into a practical, optimized circuit. My design successfully meets the specified static and dynamic error requirements, achieving a delicate balance between gain, settling time, and power consumption. The chosen two-stage architecture, featuring a telescopic cascode for the first stage and a class AB amplifier with miller compensation for the second, has proven effective in delivering the desired performance.

I believe the homework assignments served as a critical foundation for the design project. The practical relevance of the coursework facilitated the application of learned concepts to real-world project scenarios. However, the condensed timeframe, while posing challenges, elevated the difficulty level of the project, fostering a more engaging and intellectually stimulating experience. My initial struggle with the Matlab script caused me a little delay for the rest of the design. I appreciate the guidance provided by GSIs Avi and Ashwin played a pivotal role in overcoming design hurdles. Their patience and assistance during lab sessions and office hours were instrumental in resolving my issues and refining the design.

The LCD amplifier, despite its demanding nature, proved unquestionably worth the effort. This project experience deepened my knowledge in designing amplifiers with high gain while focusing on the frequency response. The project's alignment with coursework and the challenges it presented served as a culmination of the learning experience.

While the project has reached a commendable state, I desire more time to explore the optimization of the FOM using my new Matlab scripts. I would like to do this during the winter break and would like to share my design result with the Professor and GSIs.

In conclusion, the LCD amplifier design project played an important for my gaining hands-on learning experiences. The encountered challenges, coupled with the support received, have contributed not only to the successful completion of the project but also to personal and intellectual growth, reinforcing the value of practical, applied knowledge in the field of analog circuit design. Thank you, Professor Muller and GSI for designing this project.