CHIH-CHIEH (MORRIS) FAN

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SUMMARY

Morris experienced 4 years in Analog Integrated Circuit Design along with Virtuoso, Customer Compiler, and 180nm **taped-out at TSRI**, Taiwan. In charge of designing **two PCB taped-out** testing boards using Altium Designer at BWRC Lab. He is admitted in NTU GIEE and is an incoming **M.S. ECE student at UCSD specializing in Analog Circuits.**

- **Analog CAD Tools** Cadence, HSPICE, Laker/Custom Compiler, Composer/Virtuoso, Altium Designer
- **Languages/Frameworks** C/C++, Python, Verilog, Vim Editor, MATLAB, HTML

EDUCATION

University of California, San Diego — La Jolla, CA

M.S. in Electrical and Computer Engineering — *Sep. 2024 – Jun. 2026*

University of California, Berkeley — Berkeley, CA

Exchange in Electrical Engineering and Computer Sciences — *Aug. 2023 - May. 2024*

- **Coursework:** Analog Circuits Design, Digital IC Design, ASIC Lab, Photovoltaic Device, Communication Networks.
- **Undergraduate Research:** "Dual Port SRAM22 PCB Layout Design" and "BAG3 Generator Design" at BWRC Lab.
- **Student Assistant:** Provide peer advising and professional front-line customer service for UC Berkeley Summer Session (SSALLEX) program at Berkeley Extension. ($18.07/hr, 10hrs a week. Supervisor: Nicolai Sinn, nsinn@berkeley.edu)

National Tsing Hua University (NTHU) (GPA 3.97/4.30, 3.83/4.00) — Hsinchu, Taiwan

B.S. in Electrical Engineering — *Sep. 2021 - Jun. 2023*

- **Coursework:** Analog Circuits Design, VLSI, Microelectronics, Signals and Systems, Solid State Electronics, Feedback Control System, Semiconductor Fabrication (Lithography), Linear Algebra, Discrete Math, Probability, PDE, ODE.
- **Capstone Project:** ADC for “IOT Sensor Interface Circuit Chip". In charge of 30% chip layout and 100% PCB layout.

PROJECT/RESEARCH EXPERIENCE

BAG3 Generator for Analog Design Assistance — Berkeley, CA

Undergraduate Research led by Prof. Borivoje Nikolic, BWRC Lab, EECS, UC Berkeley — *Oct. 2023 - Present*

- Developed expertise in BAG flow using Python and design a generator for chip layout design and **circuit optimization**.
- Designing the chip layout and schematic, measurements, simulations, by writing Python and C++ scripts.

Dual Port SRAM22 PCB Layout Design — Berkeley, CA

Undergraduate Research led by Prof. Borivoje Nikolic, BWRC Lab, EECS, UC Berkeley — *Sep. 2023 - Dec. 2023*

- Designed PCB Layout for PhD student Rahul’s SRAM22 chip for measurements and verifications.
- Layout using **Altium Designer**, gaining PCB taped-out experience, writing Testplan, Bom Builder, and PartSync.

IoT Sensor Interface Circuit Chip Design [poster][paper][slides] — Hsinchu, Taiwan

Capstone project led by Prof. Kea-Tiong (Samuel) Tang, EE, NTHU — *Feb. 2023 - Jan. 2024*

- Developed expertise in designing a **low-noise, high-bandwidth** ADC Circuit for E-nose and reduce power costs by **10%**.
- **Taped-out** with 180nm fabrication at TSRI, in charge of PCB layout, gained experience in full Analog IC design routine.

Low-Power, High-Slew OP Amplifier Design for LCD Display [Report] — Berkeley, CA

Linear IC Design course taught by Prof. Rikky Muller, EECS, Berkeley — *Nov. 2023 - Dec. 2023*

- Designed a two-stage (telescopic cascode & Class AB Amplifier) with low power and low settling error.
- Achieved a 600uW of power consumption and 0.17us settling time, 50% better than the SPECs.

128*16 bits ROM Memory Macro Design [paper] — Hsinchu, Taiwan

VLSI course taught by Prof. Meng-Fan (Marvin) Chang, EE, NTHU — *Sep. 2022 - Jan. 2023*

- Designed a NOR-based ROM memory array with 0.18μm CMOS process.
- Achieved a read time of under 5 nanoseconds, which is **10% lower** than the SPEC.

AWARDS

NTHU Pilot Program Scholarship of 2023 and 2024 — Sep. 2023

UCLA Overseas Exchange Scholarship (Full Sponsored) [link] (Sponsored by NTHUEE) — Mar. 2022

2021 Code for Gender Hackathon Finalist, Rank 8th/50 [slides][link] (Issued by Womany X Google) — Aug. 2021

Dean List [link] (Ranked $\mathbf{2^{nd}}$ out of 124 students at NTUST ECE, GPA 4.21/4.30, Top 1%) — Jan. 2021

First Place in Taiwan College Student Start-Up Competition [certificate][link] (out of 30 teams from Taiwan) — Oct. 2020