Advancements and Challenges in Chiplet Testing

YONG LI, University of Massachusetts, Amherst, USA

While Chiplet-based architectures provide incomparable modularity, cost efficiency, and design flexibility, they also introduce new testing challenges. This paper summarizes some recent developments in chiplet test methodologies: boundary scan enhancements, Built-In Self-Test techniques, and dynamic test configurations. These will include the boundary scan architecture improvement for 2.5D interconnects, BIST schemes for the inter-die connection in 3D-stacked systems, and TAP-based dynamic configuration for heterogeneous environments. Solutions that address these main challenges of limited accessibility and power deliverability inside Chiplet ecosystems and an absence of standardization.

ACM Reference Format:
Yong Li. 2024. Advancements and Challenges in Chiplet Testing. 1, 1 (December 2024), 3 pages. https://doi.org/10.1145/nnnnnnn.nnnnnnn

Introduction

Chiplets are small pieces of a big chip. They are somewhat like building blocks that can work together to make a larger system. The use of chiplets is better than using one big chip, as it can improve the efficiency in manufacturing. When one small part has a problem, only that part is wasted, not the whole chip. This makes chiplets more cost-effective.

Chiplets also provide more flexibility to designers. They can combine different types of chiplets, like memory and processors, to make better systems. It is also easier to upgrade: one chiplet can be replaced with its new version while keeping other chiplets the same.

But testing chiplets is extremely challenging. The small size and proximity to each other make the connections hard to reach, and power delivery during testing can be problematic. High-speed connections like UCIe further complicate testing because they require specialized tools.

This paper will explain the problems that exist in chiplet testing and the ways researchers are finding around them. The paper is based on recent studies found on chiplet technologies, focusing on testing methods and challenges.

Key Challenges in Chiplet Testing

Chiplets testing faces many challenges. First, there is an issue of accessibility. Accessibility to the minute interconnects between chiplets is difficult in advanced designs such as 2.5D and 3D, where the interconnects are packed and hidden, hence direct testing cannot be done easily [5]. Another challenge is the delivery of power. Power has to be provided to chiplets even while they are under test, but this sometimes leads to a lot of problems such as improper power distribution or noise. All these may interfere with the test result outcomes [4]. Another complicated activity involves testing the interconnects. High-speed interfaces like UCIe require very specialized test mechanisms for performance testing. Traditional techniques, like boundary scan, may not work that effectively for such interfaces [3].

Author's Contact Information: Yong Li, yonli@umass.edu, University of Massachusetts, Amherst, Amherst, MA, USA.

ACM XXXX-XXXX/2024/12-ART
https://doi.org/10.1145/nnnnnnn.nnnnnnn

There is also a lack of standard testing protocols. The different chiplets could be sourced from different vendors, and there is no universal standard to ensure their compatibility with each other, thereby making the testing more laborious and time-consuming [4].

Advancements in Testing Methodologies

Recent research offers practical solutions to some of the challenges in chiplet testing. Boundary scan, BIST, and dynamic configuration methods have been gaining considerable momentum in addressing problems associated with interconnect test and fault detection.

Boundary Scan Enhancements

Although it was originally designed for testing at the PCB level, boundary scan testing has been extended to meet the demands of chiplet systems. For instance, the paper * "An Improved Test Structure of Boundary Scan Designed for 2.5D Integration" proposes an addition of extra scan cells in the boundary scan architecture. It enhances observability and fault coverage for the connections based on interposers in 2.5D designs. The study highlights the practical implementation where the modified boundary scan detects interconnect faults such as opens and shorts with a 20

Besides, the inclusion of IEEE 1838 in the 3D test infrastructure also solves the challenges of IEEE 1149.1 for the stacked die because features such as die-level isolation and finer granularity with test access points enable more efficient testing for vertically stacked systems by offering multi-layer compatibility [1].

Built-In Self-Test (BIST)

Other serious development suitable for chiplet testing is BIST. The paper * "Efficient Built-In Self-Test Scheme for Inter-Die Interconnects of Chiplet-Based Chips" presents the embedding of test circuits into a chiplet itself. That approach works pretty well in the cases of 3D stacked systems where access to the inter-die connections is barely possible. In general, the proposed BIST scheme applies approximation algorithms, keeping very good accuracy with the benefit of decreasing test time and power consumption. The experimental results of the study reveal that while the test execution time reduced by 30%, the test efficiency notably increased as compared to external testing setups [3].

Dynamic Testing Configurations

Dynamic configuration using TAP controllers is another innovative solution for heterogeneous chiplet systems. Researchers in *A Dynamically Configurable Chiplet Testing Technology Based on TAP Controller Architecture* present a TAP-based architecture for dynamic configuration of test protocols by the chiplets. This architecture will also allow the testing of individual chiplets selectively in multi-vendor environments, drastically reducing test setup times. The paper presents, as an example, testing of a system with three different kinds of chiplets and shows that configuration time reduction by up to 25% is achievable without sacrificing compatibility with existing test standards [2].

These developments show that focused innovations in boundary scan, BIST, and dynamic testing are driving the development of new test methods for chiplets. In addressing specific challenges relating to accessibility, interconnect faults, and heterogeneity at the system level, the various solutions make possible increasingly efficient and reliable testing processes.

Relevance to Modern Chiplet Design

Chiplet testing improvements have a direct impact on the design and functionality of chiplet-based modern systems. In particular, boundary scan improvement allows the manufacturer to find defects in the connections between interposers, and thus helps to keep up the reliability of 2.5D architectures [5]. The early detection of such defects will allow designers to improve yields and system performance. The BIST methodologies simplify the

test process by integrating fault-detection mechanisms into the chiplet itself, which is quite useful in detecting faults in 3D stacked systems. BIST not only reduces testing costs but enhances test coverage, hence making the tool important in high-density chiplet packaging [3].

Dynamic configuration techniques involving TAP controllers provide adaptability for chiplet systems that are heterogeneous. Chiplets from different vendors may implement different technologies, and that would ensure that each can be tested without having specific tools for each vendor [2]. This flexibility is crucial in reducing integration time and improving compatibility across ecosystems.

Standardized protocols, such as the one proposed in IEEE 1149.1 and its extensions, allow for a common framework for testing. This decreases development time for test tools and allows consistent test results across different chiplet designs. Such standardization is a key ingredient to scaling chiplet technologies for broader industrial adoption [1].

In summary, these testing advances address the technical challenges of chiplet systems and pave the way for more efficient, scalable, and reliable designs in the semiconductor industry.

Conclusion and Future Directions

Chiplet-based designs are greatly favored due to the benefits of modularity, flexibility, and cost efficiency. However, such advantages introduce unique challenges, particularly in testing. The discussion focused on main challenges regarding accessibility, power delivery problems, and high-speed interconnect complexities like UCIe. Furthermore, improvements to boundary scan techniques, BIST, dynamic test configurations, and even the motivation for standardization were covered as some of the latest advancements [1–3, 5]. These enhancements address most of the challenges currently present; however, much work remains to be done. Future research work in testing shall be oriented toward integrating AI and ML for developing fault prediction and detection capabilities. In addition, thermal-aware testing methodologies are required in terms of enhancement with the continuing development of chiplet systems for performance and density.

Other key areas of interest in future research involve developing common testing frameworks that can easily be integrated across different vendor ecosystems. Such frameworks will become highly critical with increased chiplet adoption to ensure interoperability, thereby reducing testing costs.

Testing, thus, remains at the tail-end, one of those key success factors in the chiplet-based architecture. It is when test methodologies further innovate and are refined that the full potential of chiplets for enabling the next generation of high-performance systems in the semiconductor industry gets realized.

References

[1] 2013. IEEE Standard for Test Access Port and Boundary-Scan Architecture. *IEEE Std 1149.1-2013 (Revision of IEEE Std 1149.1-2001)* (2013), 1–444. https://doi.org/10.1109/IEEESTD.2013.6515989

[2] Zhikuang Cai and Yunbo Wang. 2022. A Dynamically Configurable Chiplet Testing Technology Based on TAP Controller Architecture. In *2022 IEEE 5th International Conference on Electronics Technology (ICET)*. 590–594. https://doi.org/10.1109/ICET55676.2022.9824550

[3] Yi-Chun Huang, Pei-Yun Lin, Jin-Fu Li, Hong-Siang Fu, and Yung-Ping Lee. 2024. Efficient Built-In Self-Test Scheme for Inter-Die Interconnects of Chiplet-Based Chips. In *2024 IEEE International Test Conference (ITC)*. 149–156. https://doi.org/10.1109/ITC51657.2024.00034

[4] M. Hutner, R. Sethuram, B. Vinnakota, D. Armstrong, and A. Copperhall. 2020. Special Session: Test Challenges in a Chiplet Marketplace. In *2020 IEEE 38th VLSI Test Symposium (VTS)*. 1–12. https://doi.org/10.1109/VTS48691.2020.9107636

[5] Zhen Zhang, Jinghe Wei, Yujia Yin, Jian He, and Ying Gao. 2023. An Improved Test Structure of Boundary Scan Designed for 2.5D Integration. In *2023 8th International Conference on Integrated Circuits and Microsystems (ICICM)*. 643–648. https://doi.org/10.1109/ICICM59499.2023.10365967