An Improved Test Structure of Boundary Scan Designed for 2.5D Integration

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***Abstract*—While chiplet provides more IC design opportunities, 2.5D advanced heterogeneous integration brings more challenges to test due to its complex structure and interconnection. This paper proposes an improved test structure of boundary scan aiming at the interconnection in different directions between 2.5D stacked chiplets. By segmenting the boundary scan chain inside each chiplet and make each segment configurable, we test interconnections in different directions between chiplets at the same time, with shorter test vector and smaller area compared to ieee 1149.1. Additionally, a new configuration method based on the standard TAP state machine is suggested in order to shorten the configuration time for interconnection testing. The total test vector in the scenario of three core interconnect testing is lowered by 76.58% compared to the standard one, additionally cutting the configuration time by 82.76% when compared to employing user-defined instructions reserved in the standard. The area is 10.65% smaller than the typical testing structure.**

Keywords—chiplet, interconnect test, ieee 1149.1, 2.5D IC, DFT

I. INTRODUCTION

With the progress of process nodes, Moore's Law is gradually being invalid. Similarly, various factors such as power need to be considered during design [1-2]. Against the backdrop of the high cost of advanced process nodes, the importance of packaging technology continues to increase. Chiplet has been introduced as one solution. Advanced packaging methods such as 2.5D packaging integrate chiplets into heterogeneous systems, with lower cost, higher performance, lower power consumption, and shorter construction period. It can effectively meet the needs of the market [3–9]. In 2021, Pascal Vivet et al. designed and developed a 96-core processor called IntAct with 6 chiplets to meet the needs of high-performance computing, avoiding the challenges of improving performance in traditional single-chip architectures. At the same time, Chiplet has been successfully mass-produced in the industry, such as Intel's Stratix 10, Foveros, Kaby Lake-G, Tofino2 and other chips [3].

Chiplets also have some drawbacks, such as difficulty in testing, which is more important during the production of multi-core stacked chips. Chiplet-stacked chips have a unique structure known as interposers, and traditional testing schemes cannot meet the testing needs of interconnections in different directions within them. Secondly, the multi-core integrated chip has a higher I/O port and interconnection density than the traditional chip. Using a 1-bit boundary scan chain to move out serially will greatly increase the test time and cost. Finally, in the scenario of multi-core stacking, the number of I/O ports and interconnections increases, while most of them are used for internal interconnections and cannot be used as exposed test ports. Compared to traditional chips, the available test ports are reduced, further increasing the difficulty of testing [5].

In the field of VLSI testing, the common test methods are the boundary scan test and the scan test. We mainly apply the boundary scan since we focus on the scale interconnections in the multi-core 2.5D integration, where there are already two standards. IEEE 1149.1 takes traditional board-level chips as the research object and proposes to use a unified interface for boundary scan testing. IEEE 1687 focuses on embedded systems and proposes a multi-level network architecture based on SIB(Segment Insert Bit) to flexibly access different devices. In addition, IEEE 1687 also defines PDL (Procedural Description Language) and ICL (Instrument Connectivity Language) to achieve redirection of test modes [10–11].

There are already many new methods while testing multi-core stacked chips. In [12–13], an automatic core detection structure was proposed that can automatically detect upper and lower cores without configuration. Based on this, a Chiplet-Footprint structure and a complete testing architecture were designed in conjunction with IEEE 1687, which can access any core for testing and easily retarget testing modes. In [5,14], the author proposed solutions for pre-bond test of the interposer, at-speed test, self-test of high-density I/O and interconnection, external test scheduling and low-power test. In terms of at-speed test, the boundary scan chain is divided into a scan-in chain and a scan-out chain according to its functions to enable data scan-in and scan-out in parallel, reducing interconnect testing time. In [15], aiming at the problem that small leakage current cannot be detected in some interconnections that cannot be accessed directly in Info WLCSP with traditional methods, the BSC (Boundary Scan Cell) was optimized based on the traditional boundary scan test, and the EBSC (Enhanced BSC) that can compare current with the reference current was designed to detect small leakage current. In [16], the author designed the TAP-CA (TAP controller architecture) for 3D

stacked multi-core, where each core shared the TAP-CA, which can separately test each core and shut down non-test cores, reducing power consumption.

However, the optimization and improvement of interconnection test are relatively vacant, and IEEE 1687 can only control the boundary scan chain on the level of die, resulting low efficiency in testing interconnections in different directions between chiplets, where we will mainly focus on later. Since IEEE 1687 is nearly same as IEEE 1149 in the aspect of boundary scan, we will base our work on IEEE 1149.

In this paper, we propose an optimized boundary scan test structure based on IEEE 1149.1 with the following functions:

A. *Flexible Control of the Boundary Scan Chain to Shorten the Boundary Scan Chain Actually Used*

Group the boundary scan chain, insert 2-MUX between adjacent groups to control whether the group is connected to the boundary scan chain.

B. *Minimize the Configuration Time of Internal Configuration Registers as Much as Possible*

This new method based on IEEE 1149.1 minimize the configuration time while barely increasing the area by adding the function of the partial state of the standard state machine. We also add a 'lock' to avoid duplicate configuration.

C. *Simultaneously Test Interconnections in Different Directions*

Testing interconnections of dies in different directions must be tested independently using the traditional test structure. The structure we proposed can generate relevant signals to test interconnection in different directions (which we will use 'bidi-test' to refer to in the following text) simultaneously, compatible with standard tests, with improved efficiency.

Rest of this paper is organized as follows. Section II entails the improved test structure proposed. Section III describes the test steps of the traditional test structure and the improved test structure proposed. And section IV shows the experimental results, including waveform and indicators such as area, etc.

II. Proposed Test Structure

Figure 1 shows the basic structure of the proposed test structure, containing 3 modules except the core: Boundary Scan Groups, TAP-Main, Scan Chain Retarget Controller. The 'Boundary Scan Chain' module included groups of short boundary scan chains, which were split from the boundary scan chain according to their connected chiplets. Every two adjacent groups were connected by a 2-mux. The 'TAP-Main' was almost the same as what the standard asked, except for extracting some signals needed by other modules. The 'Scan Chain Retarget Controller' aimed to reconfigure the boundary scan chain inserted; it was also responsible for transporting the configuration signal needed by the 2-muxes of the 'Boundary Scan Groups' and generating the signals enabling the bidi-test, as well as controlling the source of TDO (Test Data Out). The detailed information will be introduced in the following parts.

A. *Boundary Scan Groups*

Figure 2 depicts the detailed structure of 'Boundary Scan Groups'. The upper part displays the split boundary scan chain, and every two adjacent boundary scan groups are connected by a 2-mux. The select signal of the 2-mux is Config_sel_i. When the value is 0, the forward boundary scan group is linked to the boundary scan chain. The test architecture is compatible with the standard with all Config_sel_i 0. Considering that the condition that all groups were not linked is realized by the instruction 'BYPASS', and the situation with all select signals value 1 realize the same function, we especially regulate that all boundary scan groups were inserted when all config_sel_i are 1 yet with a function different from the standard. For example, all config_sel_i being 0 means that the test circuit works in standard mode with all boundary scan groups inserted, the condition that all config_sel_i are 1 indicates the same boundary scan chain, but it can enable bidi-test, which cannot be realized in standard mode. This logic is realized by the lower part. If a die has N dies connected to it, there are normally N 2-muxes and N select signals to control them.

There is another detail that the internal pins and their BSCs of every boundary scan group are in order, as shown in figure 3. Each die has one TDI (Test Data In) pin and one TDO (Test Data Out) pin, and the test data within one chiplet goes from TDI to TDO. Since the output pins and their corresponding BSCs must be assigned while shifting test data in and the input ones must be observed while shifting test data out, we force the input pins and BSCs near the TDI pin and the output ones near the TDO pin to shorten the test vector as much as possible.

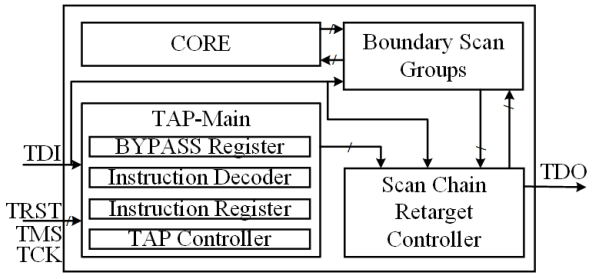

Fig. 1. Structure of the Proposed Structure and Circuit

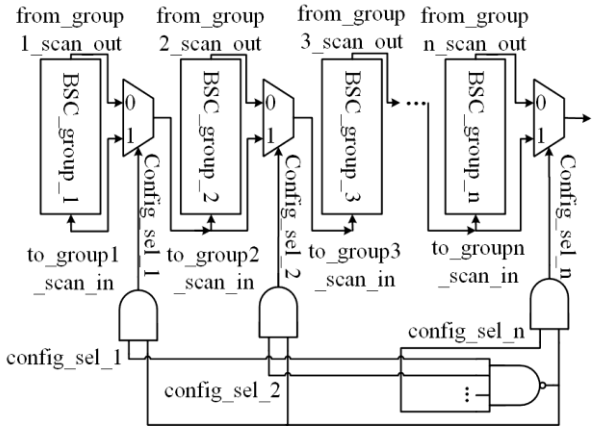

Fig. 2. Boundary Scan Groups

B. TAP-Main

The module 'TAP-Main' has almost the same function of generating the control signal of the test circuit as the standard one, yet we need to extract some signals to other modules. In addition, the proposed structure transfers the output control logic of TDO to the module 'Scan Chain Retarget Controller'. Table 1 lists the additional signals extracted and their functions.

C. Scan Chain Retarget Controller

The whole block diagram of the module 'Scan Chain Retarget Controller' is displayed in figure 4, containing 3 sub-modules. Module 'Config Register Chain' stores the configuration signals required to retarget the boundary scan chain. And the 'Bidi Connect Test' generates the select_jtag_output signals of all boundary scan groups, while the 'TDO Control' is designed to select the source of TDO according to the test mode that the circuit is working on.

As described in subsection II.A, a chiplet requires an N-bit select signal while there are N chiplets connected to it. The module 'Config Register Chain' works on the storage and transmission of these signals. To avoid duplicating these registers while using the new config method proposed (which we will introduce later), we set a 'lock' register at the head of the config register chain. The 'lock' register will enable the assignment of the following config registers when valuing 1, nevertheless, it will keep the values of config registers. Figure 5 shows the circuit of the 'Config Register Chain'. It deserves to be mentioned that in the scenario where multiple chiplets are interconnected, as shown in figure 12, the config registers of different chiplets are sequentially connected. When configuring, it is necessary to first assign the 'lock' registers in each chain and then assign the configuration registers following every 'lock' register since each chain is opened at this time.

Figure 6 shows the schematic of module 'Bidi Connect Test'. According to standard regulations, when testing interconnected chiplets or chips, test data must go from the chiplet or chip working under the instruction 'EXTEST' to the other one under the instruction 'SAMPLE/PRELOAD' to check out the fault of interconnection. Therefore, in the case of multi-die interconnection, the dies can only be tested in pairs, and the interconnections in different directions need to be tested separately, increasing the length of test vectors. To solve this problem, we designed the module 'Bidi Connect Test' to enable the boundary scan groups linked to transmit test data externally by setting the signal select_jtag_output high while the chiplet is working under the instruction 'SAMPLE/PRELOAD'. We can test bidirectional connections using one test vector and test multiple chiplets together rather than test them in pairs by enabling each chiplet to work under specific instructions, decreasing the length of test vectors. We will introduce this test scheme in detail in section III.

Figure 7 displays the basic circuit of module 'TDO control', which especially regulates the output path of the configuration data. We need to transmit configuration signals during the configuration cycle, which is specified by the configuration method we proposed. If the chiplet is working under the instruction 'BYPASS', directly short-circuit the TDI with TDO, otherwise transmit the configuration data. Considering that we add a 'lock' register at the head of the configuration register chain, we transmit the configuration data only if the 'lock' register values 1, meaning that the configuration register chain is configurable. Also, since we group the boundary scan cells and rebuild the boundary scan chain, the test data should be the output data of the boundary scan group linked last.

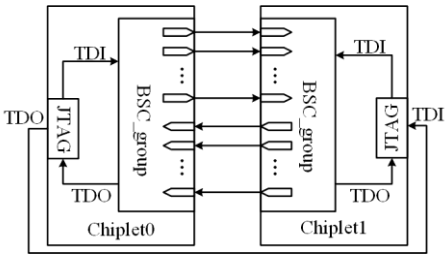

Fig. 3. Internal Order of Boundary Scan Group

TABLE I. ADDED PINS AND THEIR FUNCTION OF TAP-MAIN

SIGNAL	FUNCTION
STATE[3:0]	1.controlling the assignment of config register 2.controlling the output of TDO
sample_preload	1.indicating that the test structure of the die works on the SAMPLE/PRELOAD test mode
select_jtag_output	1.indicating whether the output BSCs can transfer test data out
tdr_mux.etc	1.providing the source of TDO
BYPASS_decoded	1.controlling the output of TDO

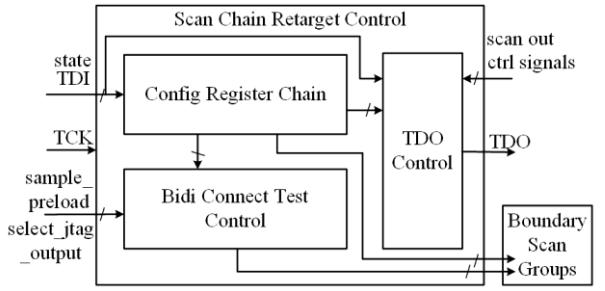

Fig. 4. Scan Chain Retarget Controller

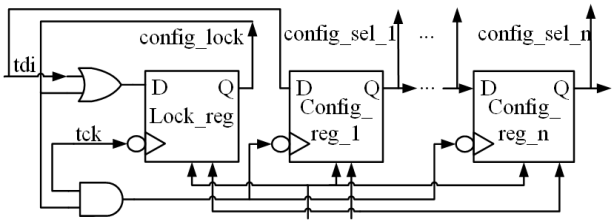

Fig. 5. Config Register Chain

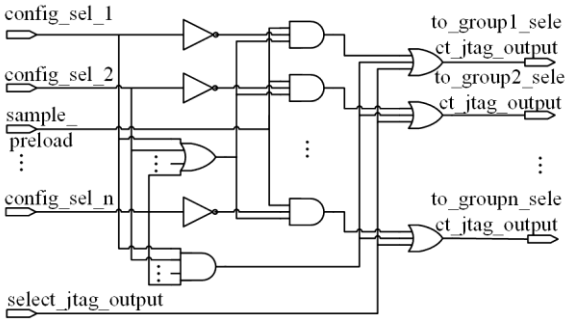

Fig. 6. Bidirectional Connect Test Control

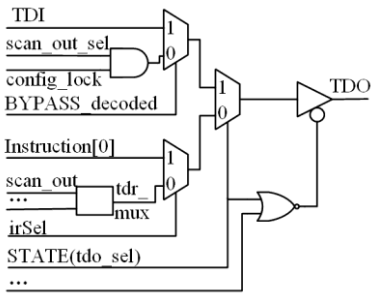

Fig. 7. TDO Control

D. A Fast Configuration Method Based On Standard FSM

The state diagram for the standard TAP controller contains two branches, controlling the data registers and instruction registers respectively as illustrated in figure 8. Using the user-defined instructions of the standard to configure registers is accompanied by significant time expenditure, so we introduce a fast configuration method. We observed that the assignment of the configuration registers during some continuous state will not affect the normal operation of the boundary scan chain, as the shadowed states marked in figure 9. We extend the configuration periods by increasing the loop of states 'run-test/idle'. This method has a time complexity of O(kN-4), while that of using user-defined instructions is O(4N+kN+6+5), where N is the number of chiplets remaining to configure and kN is the number of registers remaining to configure.

III. TEST FLOW

A. Standard Test Flow

When testing interconnections between chiplets using the standard testing structure, we can only test interconnections between the same two chiplets. We should also make the chiplet located at the emission end work under the instruction 'EXTEST' and the chiplet located at the receiving end work under the instruction 'SAMPLE/PRELOAD'. The remaining chiplets on the scan path work under the instruction 'BYPASS'. Based on the above analysis, if there are interconnections in two directions between two chiplets, it is necessary to conduct testing in two stages based on the direction of the interconnections to be tested. Figure 10 is the flow chart for testing interconnection using the standard test structure.

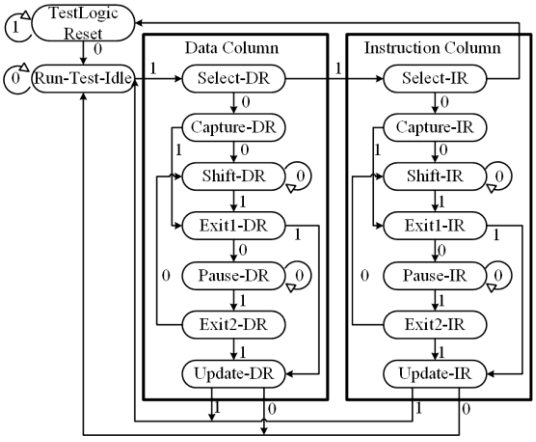

Fig. 8. Standard State Diagram

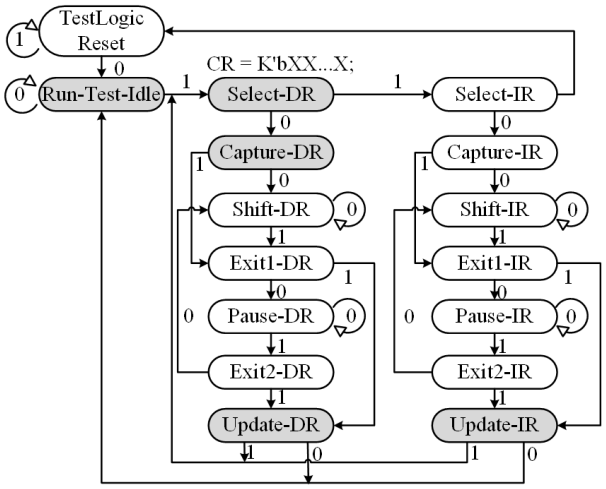

Fig. 9. State Diagram of Configuration Method Proposed

B. Test Flow of Proposed Test Structure

Unlike standard tests, using the optimized test structure we proposed can simultaneously test interconnections in different directions and those between different chiplets. Since the boundary scan chain in a single chiplet is segmented in our optimized structure, relevant configuration registers need to be configured to link boundary scan cells or groups that need to be tested. Use the command 'BYPASS' to bypass the chiplets that have no boundary scan cell or group needed to be tested or accessed. For chiplets in which all internal boundary scan cells or groups should be connected and tested, meaning that the whole chiplet needs to be linked, different from the standard test structure, it is necessary to plug all boundary scan cells or groups into the boundary scan chain by the configuration register, as the method used for partially linked chiplets. In addition, different from the requirements of the standard test structure for the instructions that chiplets work under, when using the optimized test structure, the first chiplet linked into the boundary scan chain needs to work under the instruction 'EXTEST', and the rest of the chiplets plugged need to work under the instruction 'SAMPLE/PRELOAD'. Finally, inject the corresponding test vector according to the boundary scan cells or groups to be accessed for testing. The flow chart for testing interconnections using the optimized test structure is shown in Figure 11.

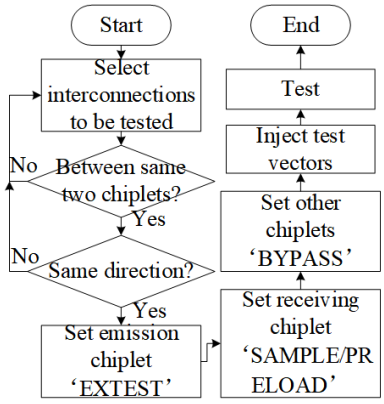

Fig. 10. Flow Chart of Standard Interconnection Testing

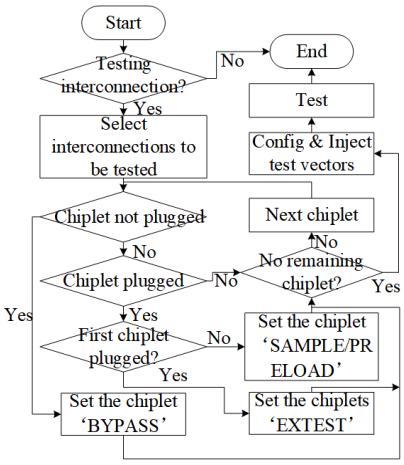

Fig. 11. Flow Chart of Proposed Interconnection Testing

IV. Experiments and Results

A. Test Object

Apply the optimized test structure to 2.5D interconnected chiplets as shown in figure 12, each chiplet containing 768 pins. Since each core has two interconnected objects, considering the top layer as one connected object, each chiplet contains one 3-bit configuration register (including a 1-bit 'lock' register).

B. Simulation Results

According to the analysis in previous sections, when testing the interconnections between the three chiplets shown in figure 12, chiplet0 needs to work under the instruction 'EXTEST', while chiplet1 and chiplet2 work under 'SAMPLE/PRELOAD'. At the same time, the pins of chiplet0 and chiplet2 connected to the top layer need not be linked to the boundary scan chain. Therefore, we input 12'b101010101000 from TDI to set the instruction and reconstruct the boundary scan chain before injecting the test data for the first time by inputting 9'b111101101 from TDI. The configuration assignment is shown in figure 13. The last 6 signals are 'select_jtag_output' of two boundary scan groups in 3 chiplets in sequence. After configuration, every select_jtag_output of the boundary scan group accessed was successfully enabled. The complete waveform of the interconnection test is shown in figure 14, with compare_fail_count valuing 0, which indicating TDO completely consistent with TDO_exp, meaning that the test passed and the interconnection test function of the optimized test structure is normal.

In addition, we set the instruction to make chiplet0 work under 'EXTEST', and that of chiplet1 and chiplet2 'BYPASS', to verify the compatibility between the optimized test structure and the standard test. That is, to set instructions, we inject 12'b111111111000 from TDI at the beginning, followed by test data. The complete waveform of the standard test is presented in figure 15, from which we can discover that the signal compare_fail_count values 0, meaning TDO is consistent with TDO_exp and the pass of the standard test, and proving that the optimized test structure is compatible with the standard test. Use the standard test structure, the optimized test structure using standard reserved user-defined instructions, and the optimized test structure using the fast configuration method proposed in this article to test the interconnections shown in figure 12. We compare these structures from three aspects: test vector length, additional periods for configuration, and area. Relative data is depicted in table 2 using the tool 'Design

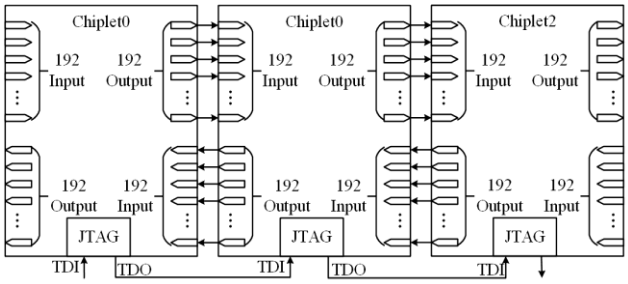

Fig. 12. Test Object

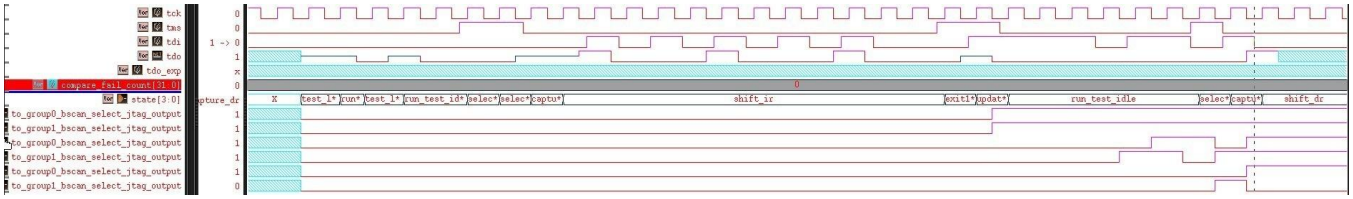

Fig. 13. Configuration Process of Interconnect Test

Fig. 14. Simulation Waveform of Interconnect Test

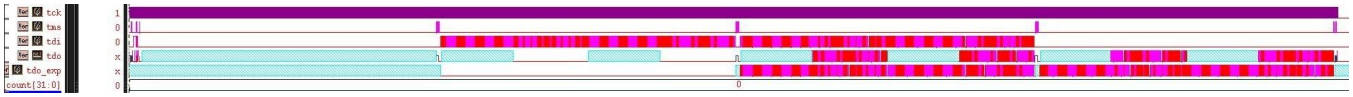

Fig. 15. Simulation Waveform of Standard Test

TABLE II. COMPARISON BETWEEN TEST STRUCTURE AND CONFIGURATION METHOD

	$L_{Test\ Vec}$	Red(%)	CT_{Added}	Red(%)	$Area_{cell}$	Red(%)	$Area_{TOT}$	Red(%)
Std Test	25360	0	0	-	980151	0	975764	0
User-defined IR	5940	76.58%	29	0	857849	-12.48%	870537	-10.78%
Proposed Test	5940	76.58%	5	82.76%	859134	-12.35%	871888	-10.65%

CT_{Added}: Added Configuration Time in clock cycles.

Compiler 16.03', based on the SMIC 180nm process. The core area is 48427639um2, the cell area is 47578501um2 and the interconnect area 849138um2. The areas in table.2 below are all the areas of the test circuits, excluding the core part.

With a reduction of 76.58% in the three core interconnect testing scenario, the table shows that the optimized test structure suggested in this article has a considerable performance benefit in shortening test vectors. In addition, compared to using user-defined instructions as specified in the standard, the fast configuration method suggested in this article reduces the required configuration cycles by 82.76% in the case of the three core interconnect testing scenario. At the same time, huge modules are broken up into smaller modules. Despite the addition of logic, the circuit's area is actually decreased. The test structure utilizing the fast configuration approach is reduced by 10.65% whereas the test circuit configured with user-defined instructions is reduced by 10.78%, a difference of only 0.13%.

V. CONCLUSIONS

For the needs of interconnection test, we suggest in this article an efficient testing structure and a quick configuration approach based on IEEE 1149. We also present the testing procedure. The boundary scan chain is divided into sections and controlled in accordance with the interconnection objects in our suggested test structure. In order to realize simultaneous bidi-test, we reassign the crucial signal select_jtag_output. Furthermore, setting configurable cycles in standard FSM can shorten configuration time by improving state utilization. This test structure may decrease the test vector by 76.58% when compared to the standard structure in the case of three core interconnection, and it can minimize the configuration cycle needed for quick configuration techniques by 82.76% when compared to using user-defined configuration instructions. Finally, the proposed testing structure reduces the standard area by 10.65%, while the fast configuration method only results in an increase of 0.13% in comparison to employing user-defined instructions.

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