A Dynamically Configurable Chiplet Testing Technology Based on TAP Controller Architecture

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***Abstract*—Aiming at the impact of Chiplet-to-Chiplet testing and the problem of insufficient number of chip ports after integration, the paper proposes a dynamically configurable Chiplet testing technology based on TAP controller architecture (TAP CA). The TAP CA includes TAP state machine controller module, instruction register module and data register module. The TAP state machine controller is used to control the instruction register, and then control and configure the corresponding data register through the instruction register. Finally, the data register is used to control the enable and disable operations of each Chiplet. When the Chiplet is enabled, the Chiplet enters the testing phase. Based on the IEEE 1687 standard, the TAP state machine inside TAP CA is used to realize built-in-self-test. Finally the data value of the configured data register is used to complete the output operation of chip. The above circuit is implemented based on TSMC 40nm process, and the area of TAP CA is only 12085.517 um^2. The ports for the memory testing of the Chiplet are only 5 JTAG ports. The built-in-self-test of all Chiplets can be implemented serially one by one based on TAP CS, and the Chiplet under testing is not affected by other Chiplets.**

Keywords—Chiplet, IJTAG, TAP controller architecture, dynamic configuration

I. INTRODUCTION

According to Moore's Law, the number of transistors integrated on a semiconductor chip has doubled every 18 to 24 months. For more than 50 years, related chip technologies have developed rapidly. So Chiplet came into being. In 2016, DARPA launched the CHIPS project, which pushed the idea of Chiplets to the entire industry. Multiple Chiplets are integrated in the IC circuit, different Chiplets may be designed by different designers, and all Chiplets have their own special testing requirements. The most common is to have its own TAP controller and its own associated test circuit[1], so larger integrated circuits contain different Chiplet designs. According to the way of Chiplet integration, how to test Chiplet after integration is a topic of current academic research.

Over the past few years, several different designs for test (DFT) methods have been proposed to test Chiplet integrated circuits. In [2], the authors proposed an IJTAG based test method to illustrate the integration of the Chiplet-detection mechanism in 3D test architecture, it can be used within any other test standard such as IEEE 1500, IEEE 1149.7, or IEEE 1687. In [3], the authors proposed a new 3D-DFT architecture, based on IEEE 1687 IJTAG standard, using Chiplet footprints, for testing a multi-chip active interposer 3D system. In [4], the authors proposed a 3D DFT architectures based on IEEE P1687 (IJTAG), where DFT is inserted using a commercial EDA tool using high level Instrument Connectivity Language (ICL) and Procedural Description Language (PDL).

However, these integration methods still face many test challenges after integration, including some test problems before and after integration. For example, the mutual connection between some Chiplets directly leads to the mutual influence of Chiplet-to-Chiplet during the test. After integration, it's impossible to package all the ports of the Chiplet into the chip, which will lead to insufficient number of ports, so the utilization of ports becomes more and more important.

This paper proposes a dynamically configurable Chiplet testing technology based on TAP controller architecture (TAP CA). TAP CA is shared and dynamically configured during testing. TAP CA includes TAP state machine controller module, instruction register module and data register module. The TAP state machine controller controls the instruction register, which then controls and configures the data register through the instruction register. Finally, data registers are used to control the enable and disable operations of each Chiplet. After the Chiplet is enabled, the Chiplet enters the test phase. Based on IEEE 1687 IJTAG standard, TAP CA can be used as a shared module for each chip test to ensure the independence of each Chiplet. The above architecture eliminates the need for the number of chip test ports, ensures the independence of each Chiplet test, the test configuration is very flexible, and power consumption is reduced.

This paper is outlined as follows: Section II outlines the architecture of Chiplet testing. Section III details the Chiplet testing Technology based on TAP CA. Section IV presents the flow and result analysis of Chiplet testing based on TAP CA. Section V makes the conclusion.

II. THE ARCHITECTURE OF CHIPLET TESTING

As an example, this paper first introduces the architecture of Chiplet testing, the testing meets the following requirements.

1) Provide the DFT testing architecture and testing flow, which can realize the correct testing of Chiplet memory before and after integration.

2) TAP CA meets the shareability to ensure that Chiplets are independent and do not affect each other.

3) Taking full advantage of the configurability and extensibility of the data register.

4) Eliminate the need for the number of chip ports, reducing manufacturing costs.

5) Meet the requirements of test area and reduce the test power consumption.

As shown in Fig. 1, three Chiplets are integrated in the chip. Each Chiplet is embedded with IEEE 1687 architecture, so the built-in-self-test of Chiple can be implemented before integration. After integration, the TAP CA is used as the shared module of all Chiplets testing. The TAP CA module has three functions: 1) TAP CA contains the TAP state machine controller, the TAP state machine control instructions and data registers, the data registers directly control the enable and disable operations after Chiplet integration; 2) TAP CA controls the mode selection signal, so for post-integration testing, all TAP state machines inside Chiplet itself are disabled; 3) The SIB/TDR structure of Chiplet is controlled by The TAP state machine inside TAP CA, and the TAP serial chain based on IEEE 1687 standard is used to realize built-in-self-test.

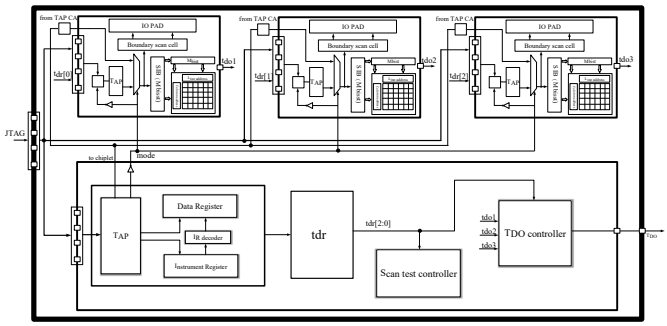


Fig. 1. The architecture of Chiplet testing

The proposed Chiplet testing architecture design is based on the following two main test access mechanisms (TAMs):

1) Based on the dynamically configurable TAP CA, it realizes the enable operations of the Chiplet and test Chiplet with IEEE1687 standard.

2) Based on the dynamically configurable TAP CA, it controls the opening and closing of the scan chain, and finally to test the internal scan chain of Chiplet. Scanning tests are not described in this article.

The IJTAG TAP chain provides dynamic access to any embedded test engine, the memory of Chiplet can be tested based on the IEEE 1687 standard. Before integration, the IEEE 1687 standard is used to form a TAP serial chain to test the memory of Chiplet through SIB/TDR. After integration, the TAP state machine inside the TAP CA is used to control the mode signal and test the memory of Chiplet based on the IEEE 1687 standard. The control signals (TRST, TCK and TMS) of the 3 Chiplets are common, and the pattern is input by the external TDI, and the TDO is controlled by the TDO controller. The proposed Chiplet architecture reduces the number of ports on the chip and test power consumption, ensures independence of Chiplet testing and configuration flexibility of test data register. Chiplet testing technology based on TAP CA will be described in detail in Section III.

III. The Chiplet Testing Technology Based on TAP CA

A. Configuration Principle of TAP CA

TAP CA can be used to enable and disable testing of any Chiplet after it is integrated into the chip. As shown in Fig. 2, TAP CA includes TAP state machine controller module, instruction register module and data register module. A reconfigurable technology that enables and tests Chiplets is designed using the above-mentioned modular design based on JTAG control signals. TMS is the test mode selection signal, TCK is the test clock signal, TDI is the test data input signal, and TRST is the reset signal. The above control signals are used to select the state of the TAP state machine. The irce is open signal of the capture of the instruction register; The irse is open signal of the shift of the instruction register; The irue is open signal of the update of the instruction register; The drce is open signal of the capture of the data register; The drse is open signal of the shift of the data register; The drue is open signal of the update of the data register.

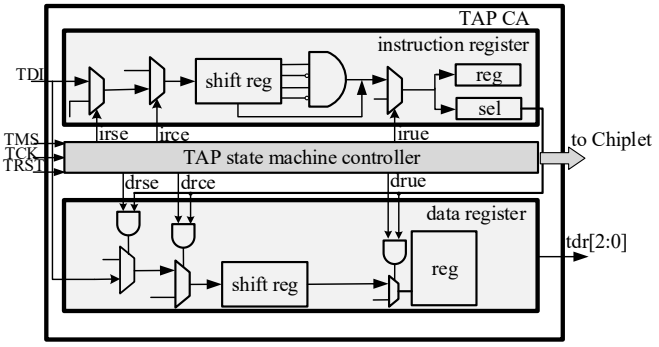


Fig. 2. Dynamically configurable TAP CA

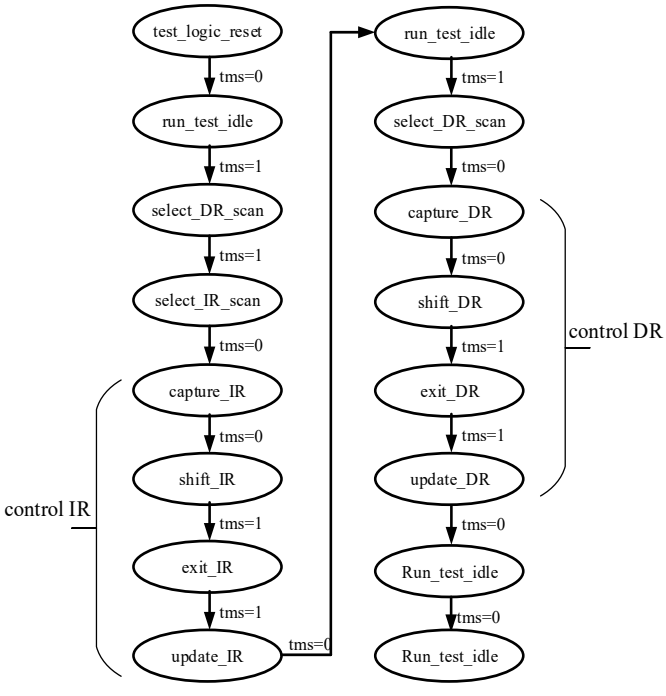


Fig. 3. TAP state control flow

All Chiplets are disabled after integration to wait for the configuration of TAP CA to realize the enabled operation of each Chiplet. The input signals of the TAP state machine controller are composed of TMS/TCK/TRST. The signals control the instruction register and data register by selecting the state of the TAP state machine controller. The TAP state control flow is shown in Fig. 3.

When the TAP state machine is in irce state, the instruction register begins to capture operation. When the TAP controller is in the irse state, data is shifted directly from the TDI port into the shift register. At this time, the value of the shift register (for example, 4'b1010 represents the value of controlling the instruction register) directly reaches the instruction decoder. The output signal of the instruction decoder is defined as sel. When the instruction decoder recognizes the value relative to the decoded instruction, it outputs the high level(sel=1), and the instruction decoder controls the opening of the data register. Otherwise the instruction decoder is low level and the data register cannot be controlled by the TAP state machine. When the TAP controller is in the irue state, the update register can load value into the output of the instruction register.

When sel=1, the data register can be controlled. The data register contains multiple bit widths, and the length of the bit width is equal to the number of Chiplet. When the TAP state machine is in the drce state, the data register begins to capture operation. When the TAP controller is in the drse state, the data is shifted from TDI into the shift register, so the value of the data register is configured as 3'b010. The output signal of the data register is used as the JTAG input control of the Chiplet. Hence, if the control signal is 1, the JTAG input of the Chiplet is enabled; if the control signal is 0, the JTAG input of the Chiplet is disabled.

The above architecture constitutes the enable operation of the Chiplet, then the TAP state machine in the TAP CA and the IEEE 1687 standard are used to control built-in-self-test circuit to complete the memory test of all Chiplets.

B. Chiplet Testing Based on TAP CA

The proposed Chiplet testing based on TAP CA is shown in Fig. 4. Before integration, the test mode signal was used as an external port to directly control the input signal of Chiplet's MBIST. When mode=0, the TAP inside Chiplet is enabled and selected to control MBIST, and the test input signal comes from the JTAG signal of the Chiplet. The TAP serial chain is formed based on the IEEE 1687 standard, and the built-in-self-test is realized by using the SIB/TDR structure to test the memory of the Chiplet.

After integration, the test mode signal is controlled by TAP CA. When the TAP state machine inside TAP CA does not perform the operation of TMS = 1 for 5 consecutive times, the control signal always keeps the low level. Therefore, the control signal becomes a mode signal through reverse operation to control the input of the multiplexer. According to the design, the input signal of the test MBIST comes from the ports of Chiplet(From TAP CA). It means that the TAP state machine of Chiplet is replaced by the TAP state machine of TAP CA. The mode signal passes through the inverter, which prohibits the TAP of Chiplet itself and reduces the test power consumption. According to the above design, the TAP state machine in TAP CA is used to control the SIB/TDR structure and then realize the memory test of all Chiplets after the integration. During the Chiplet testing, TAP CA is used for the test control of each Chiplet respecticely, which ensures the independence of Chiplet and does not affect each other. For the built-in-self-test, only five JTAG ports are used to test the Chiplet's memory, which greatly reduces the package of chip ports.

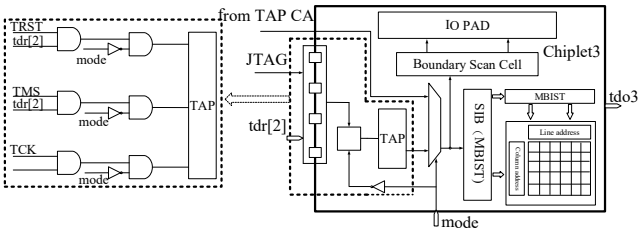


Fig. 4. Chiplet testing based on TAP CA

C. Chiplet Testing Control Module

The proposed Chiplet testing control module is shown in Fig.5. The output of the data register and the external JTAG signals as the input to the AND gate logic, which controls the enable and disable testing of each Chiplet. For the integrated three Chiplets, if the second Chiplet (defined as Chiplet2) is tested, the value of configured data register is 3'b010, so the JTAG input of Chiplet2 is enabled, and JTAG input of other Chiplets are disabled because of the AND gate logic. So when Chiplet2 is in the testing phase, other chiplets are not enabled operation. The value of the data register is not only the JTAG input signal for Chiplets, but also the output signal for selecting the Chiplet. When tdr[2:0] is 3'b010, the chip selects the test output of Chiplet2 as the output of the chip, the test result of the Chiplet2 can be observed on the external TDO port of the chip. Similarly, when tdr[2:0] is 3'b100, Chiplet1 is enabled, and then enters the testing phase, and other Chiplets are disabled. when tdr[2:0] is 3'b001, Chiplet3 is enabled, and then enters the testing phase, and other Chiplets are disabled.

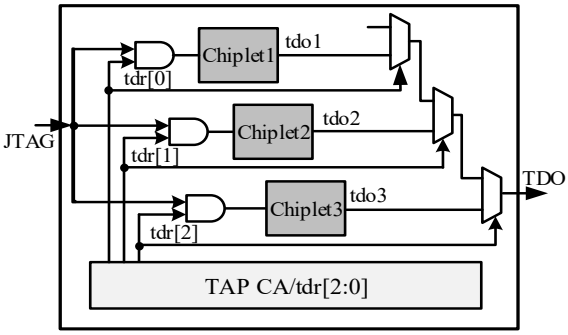


Fig. 5. Chiplet testing control module

IV. The Flow and Result Analysis of Chiplet Testing Based on TAP CA

A. The Chiplet Testing Flow Based on TAP CA

The proposed Chiplet testing flow based on TAP CA is shown in Fig. 6. First of all, for the Chiplet testing before integration, the DFT structure design includes boundary scan test, built-in-self-test and scan test, which should be properly

tested in order to form the test vector. Then the TAP CA module is designed, which includes TAP state machine controller module, instruction register module and data register module. The data register can be properly controlled by the TAP state machine and the instruction register. The above structure is integrated into one chip. The test vector of TAP CA is used to verify whether the external JTAG ports of chip can configure and control the internal data register correctly. If so, the test vector of TAP CA is combined with the test vector of Chiplet to form the test vector based on TAP CA control, and finally realize the testing of Chiplet by TAP CA. If it cannot be configured correctly, and the integrated circuit architecture of the chip should be checked.

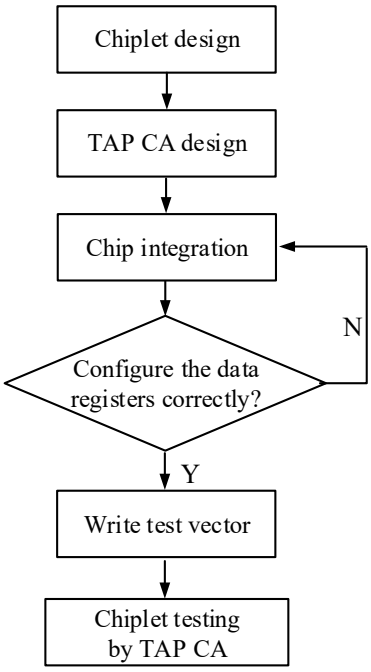
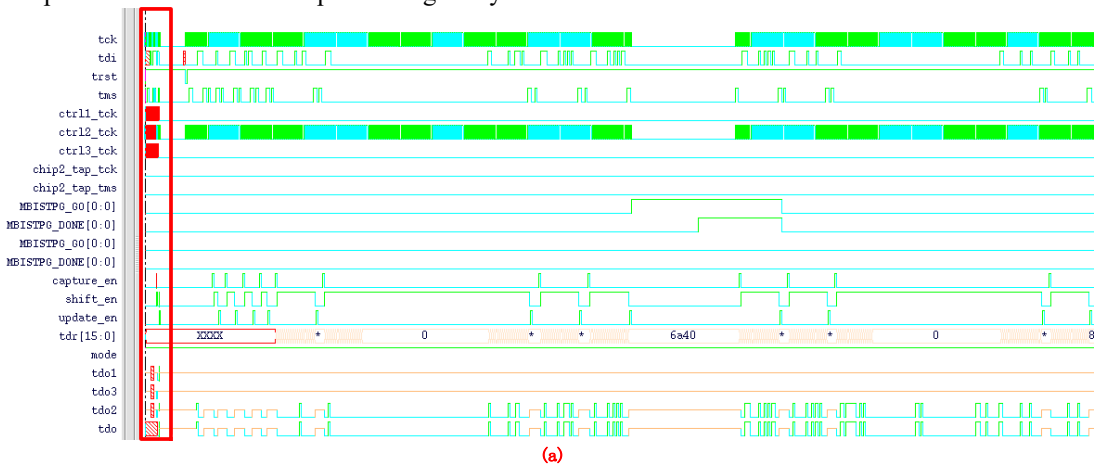


Fig. 6. The Chiplet testing flow based on TAP CA

B. The Chiplet Testing Result Analysis Based on TAP CA

Take testing Chiplet2 as an example, the whole process is divided into two stages: first configuration and then testing. Chiplet2 testing result based on TAP CA is shown in Fig. 7, where Fig. 7.a represents the result of Chiplet testing analysis based on TAP CA, and the red frame represents the configuration of Chiplet, which is enlarged to Fig. 7.b. The area of the designed TAP CA is only 12085.517um^2. The average power consumption of the TAP CA structure in the whole chip is 2.24mW. Compared to some chiplets with interconnected structures, this architecture makes full use of the sharing of TAP CA to realize the serial testing of each chiplet. There is no test control logic connected to each other between the chiplets, which fully guarantees the independence of the testing of each Chiplet. The tms and tck signals are used as state control signals of the TAP state machine controller inside the TAP CA. When the TAP state machine enters the instruction shift state, the irse of the instruction register is 1. When the clock edge arrives, the test data is shifted into the shift register from TDI. The bit width of the shift register is 4, and the instruction shift state of 4 cycles needs to be maintained. When the instruction shift register is shifted to 4'b1010 (instruction[3:0] =4'b1010), the instruction decoder decodes the relative instruction successfully, and the control signal of the data register is 1(sel=1). When the TAP state machine enters the data shift state, the ijtag_se(drse) of the data register is 1. When the clock edge arrives, the data is shifted from TDI to the shift register of the data register module. When test Chiplet2, the shifted data value is 3'b010.If the test data register is configured successfully, the data register is used to control the JTAG input signal of each Chiplet. So the untested Chiplets are prohibited, both ctrl1_tck and ctrl3_tck are 0. When the Chiplet2 is enabled, and then the Chiplet2 enters the testing phase. The TAP state machine inside TAP CA does not perform the operation of TMS = 1 for 5 consecutive times, the control signal always keeps the low level, according to the design, the mode is 1. The built-in-self-test input signals of all Chiplets come from the TAP state machine inside the TAP CA. The TAP state machine of Chiplet itself is also disabled during the test, so chip2_tap_tck=0. After the above circuit control is completed, the TAP state machine controller is used to control the SIB/TDR structure to implement the built-in-self-test. According to the go/done signal, the built-in-self-test of the Chiplet controlled by the TAP CA is completed and error-free. According to the configuration of data register, the chip selects tdo2 as the output of tdo, and tdo1 and tdo3 have no data output. Therefore, the testing of other Chiplets can also be implemented one by one through the JTAG port, and the Chiplet under testing is not affected by other Chiplets.



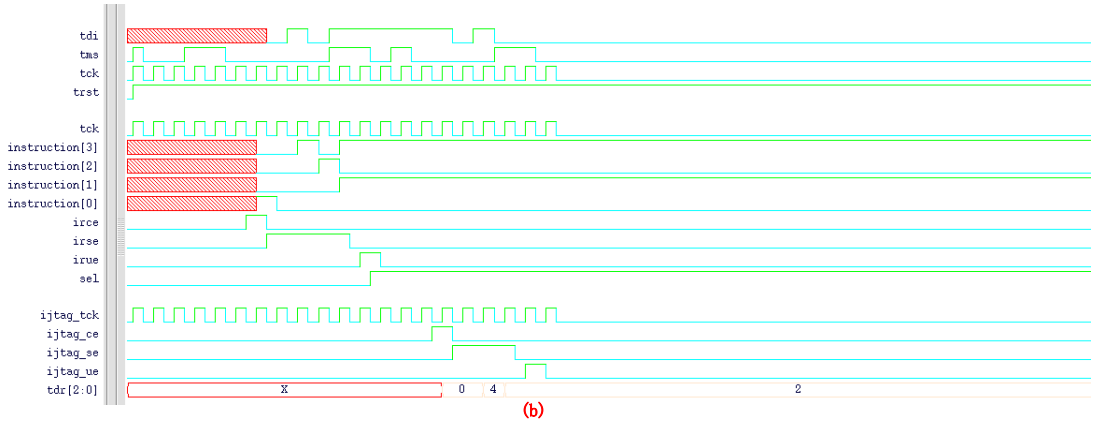


Fig. 7. (a) The result of Chiplet testing based on TAP CA (b) The configuration of enabling Chiplet

V. CONCLUSION

This paper proposes a dynamically configurable Chiplet testing technique based on the TAP CA, which eliminates the needs of the number of test ports of the chip. The TAP CA not only enables each Chiplet after integration, but also tests the memory of Chiplet. It can also be shared to achieve the independence of each Chiplet test. During the testing, both TAP state machine inside Chiplet and untested Chiplet are disabled, which reduce power consumption. This work opens up prospects for the Chiplets integration. The technology of testing can be applied to Chiplet testing.

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