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Integrated Design Ecosystem for Chiplets Heterogeneous Integration and Chip-to-Chip Interconnects in Advanced Packaging Technology

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***Abstract*—As chiplets containing multiple diverse functional dies are integrated into a single package, the demand for advanced packages with higher density interconnects and larger footprint body sizes has surged. However, the inherent complexity and dense connectivity of these advanced packages present significant challenges when employing traditional Electronic Design Automation (EDA) tools for packaging design and assembly manufacturing validation. Moreover, as chiplet-based designs transition from single monolithic die to multi-chiplet configurations, effectively planning, managing, and optimizing the top-level design and connectivity to achieve optimal performance, power, and area (PPA) among the chiplets becomes increasingly challenging and complicated compared to the traditional approach of separately planning and executing IC and package layout designs. Furthermore, the design of interconnect interfaces and protocols among chiplets is also very crucial. These designs must align with performance expectation, manufacturing processes, and system integration requirements while ensuring interoperability and maintaining a balance between performance and flexibility. Additionally, different application domains require distinct interconnect interfaces, often with conflicting performance indices such as transmission bandwidth, latency, and power consumption. Especially, the use of die-to-die interconnects for chiplets integration often takes the proprietary links from different customers, thus creating design boundaries and limiting the widespread adoption of advanced packaging technology and chiplets from various suppliers. Therefore, the development of new system-level design methodologies and design ecosystem are required.**

In this paper, we introduce a novel Integrated Design Ecosystem (IDE) to enhance design flexibility across various advanced packaging technologies including 2.5D Si TSV and High Density Fanout (HD FO) Redistribution Layer (RDL), while accommodating diverse customer design systems. The IDE has demonstrated a significant 50% improvement in design cycle time by seamlessly integrating IC design tool with package design tools. It also addresses design-for manufacturing (DFM) validation and electrical performance considerations. Additionally, we outline the design considerations and specifications for interconnect interfaces by leveraging the Universal Chiplet Interconnect Express (UCIe) standard. A comparative analysis is conducted using advanced x32 and x64 UCIe standards within the context of advanced High-Density Fanout Chip-on-Substrate (FOCoS) packaging technology. The results demonstrate that achieving higher performance with x64 need more complex RDL signal routing with significantly smaller RDL land/space (L/S) down to 1.7/1.7um, compared to x32 with RDL L/S of 2/2um while maintaining the consistent transmission speed of 32Gbps. Finally, an advanced mechanical analysis workflow for chiplet-based design is proposed and the turnkey toolbox is also presented. This comprehensive toolbox encompasses the designs of RDL interposer and package, electrical performance modeling and simulation, mechanical and thermal stress analysis, material selection, and reliability testing in assembly production.

Keywords*— *Chiplets integration, Integrated Design Ecosystem (IDE), Fanout RDL interposer, 2.5D Si TSV interposer, FOCoS (Fanout Chip on Substrate), Universal Chiplet Interconnect Express (UCIe), die to die interconnect, Warpage, Mechanical analysis.

I. INTRODUCTION

Chiplet-based heterogenous integration has gained significant attention across various domains including HPC, networking, AI, 5G, and edge computing. This growing adoption can be attributed to its compelling value propositions for yield improvement, IP reuse, performance enhancement, and cost optimization. To enable chiplets integration, various advanced packaging technologies have been deployed, such as 2.5D Si TSV interposer, Fanout RDL organic interposer and 3D hybrid bonding [1~4]. With these advanced packaging technologies, chiplets achieve high density die to die interconnection enhancing the integration of various chip systems and optimizing the performance and power consumption.

However, compared to the traditional monolithic SoC, integrating chiplets with diverse functional dies into a single package has encountered many challenges. Firstly, the demand for advanced packages with higher density interconnects and larger footprint body sizes has surged. These advanced packages often exhibit package layout density tens or even

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hundreds of times greater than conventional FCBGA packages. Designing chiplet-based solutions for these advanced packages with such dense and complex connectivity presents significant challenges when utilizing traditional EDA tools for packaging design and assembly manufacturing validation. Secondly, monolithic IC chip design and package layout design are traditionally planned and executed separately, but with the die partitioning and chiplets integration, optimizing the layout for optimal PPA among the chiplets becomes more challenging. Thirdly, designing interconnect interfaces and protocols among chiplets is also very crucial. These designs must align with performance expectations, manufacturing processes, and system integration requirements while ensuring interoperability and balancing performance and flexibility. Especially, different application domains require distinct interconnect interfaces, often with conflicting performance indices such as transmission bandwidth, latency, and power consumption. Most importantly, the die-to-die interconnects used for chiplets integration often take the proprietary links from different customers, which creates design boundaries and limits the adoption of advanced packaging technology and chiplets from various suppliers [5~7]. Therefore, an innovative chip-to-package system-level design flows and ecosystem are required to overcome these challenges and accelerate the complex design achievements. This design ecosystem can aggregate data from various suppliers and ensure the chiplets compatibility, scalability, and interoperability for various market applications.

In this paper, a new Integrated Design Ecosystem (IDE) is introduced. This IDE system not only can enhance design flexibility across various advanced packaging technologies including 2.5D Si TSV and HD FO RDL, but also can accommodate diverse customer design systems. The IDE has demonstrated a significant 50% improvement in design cycle time by seamlessly integrating IC design tool with package design tools. It also addresses DFM validation and electrical performance considerations. Furthermore, the design considerations and specifications for interconnect interfaces are also presented by leveraging the Universal Chiplet Interconnect Express (UCIe) standard. A comparative analysis is conducted using advanced x32 and x64 UCIe standards within the context of advanced FOCoS packaging technology. The results reveal that achieving higher performance with x64 need more complex RDL signal routing with significantly smaller RDL land/space (L/S) down to 1.7/1.7um, compared to x32 with RDL L/S of 2/2um, while maintaining the consistent transmission speed of 32Gbps. Finally, an advanced mechanical analysis workflow for chiplet-based designs is proposed along with the introduction of a comprehensive turnkey toolbox. This toolbox encompasses the designs of RDL interposer and package, electrical performance modeling and simulation, mechanical and thermal stress analysis, material selection, and reliability testing in assembly production.

II. Integrated Design Ecosystem

With the adoption of die partitioning and integration of multiple chiplets, the new chiplet-based design ecosystem must ensure signal integrity, minimize interconnect delay and latency between chiplets, optimize power delivery effectiveness, manage thermal issues, and conduct comprehensive design verification across multiple interfaces and chiplet interactions. Meanwhile, when dealing with the advance packages with ultra-high I/O density like FOCoS RDL routings or 2.5D IC interposer routings, this design system can provide a specialized layout design rule check (DRC) and layout versus schematic (LVS) capabilities and reduce the design cycle time, which is not generally supported by conventional package design tools, as the design cycle time for chiplets integration using advanced packages can be very long. Therefore, a new chiplet- to-package integrated design ecosystem is proposed for using advanced FOCoS RDL organic interposer and 2.5D Si interposer packaging technologies.

A. Design Flow for Standard Substrate with Monolithic Chip

In a standard substrate design with monolithic die, a template with various design rules is set up including assembly and electrical rules within the design tool. Some rules may require manually verification. After importing the package netlist into the package design tool like Cadence APD, the layout drawing and DRC checking can be performed smoothly. Since the design tools for standard substrate with monolithic chip have been widely used in the market for decades, numerous design functions have been developed to assist package designer in efficient and accurate substrate design. After completing the substrate design validation, the substrate layout drawing is exported in Gerber file format for substrate manufacturing. Fig. 1 shows the design flow for a standard substrate with monolithic chip.

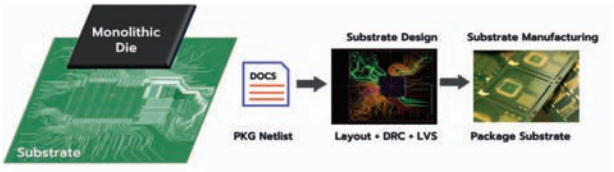

Fig. 1 Design flow for standard substrate with monolithic chip.

B. Integrated Design Ecosystem Solutions for Advanced High Density Fanout RDL Interposer and 2.5D Interpsoer

Compared to a monolithic SoC on a standard substrate, integrating of chiplets with diverse functional dies into a single package demands an advanced package consisting of an interposer with higher density interconnects and a larger footprint body size. Such advanced package will exhibit package layout density with tens or even hundreds of times greater than a standard FCBGA package. Fig. 2 shows the schematic structures of a standard package with monolithic chip (a) versus advanced package with chiplets integration (b). It demonstrates that the layout density for an advanced package with FO RDL interposer for two chiplets integration has increased up to 160k compared to the standard substrate with a monolithic chip of only about 30k at the same package body size of 62.5x62.5mm^2. Additionally, an interposer that provides high density

interconnects between chiplets has been used in the advanced package. Therefore, a new package design system needs to incorporate not only substrate design but also the interposer design. This interposer design flow involves understanding the design requirements, creating the schematic and layout design, verifying the design through simulations, and preparing the design for manufacturing. This process ensures that the RDL interposer meets the signal and power integrity requirements, as well as thermal, mechanical and manufacturing requirements, while also reducing the design cycle time for advance packages with ultra-high I/O density routings. The design flow for interposer with chiplets integration is shown in Fig. 3.

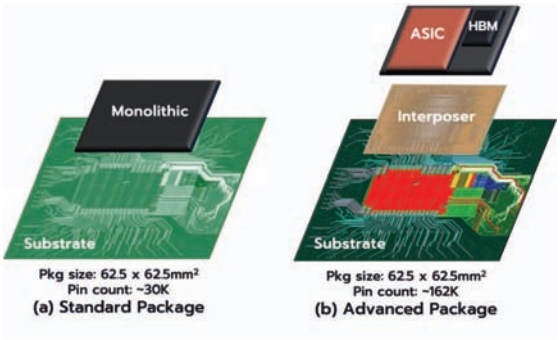

Fig. 2 Schematic structures of standard package with monolithic chip (a) vs advanced package with chiplets integration (b)

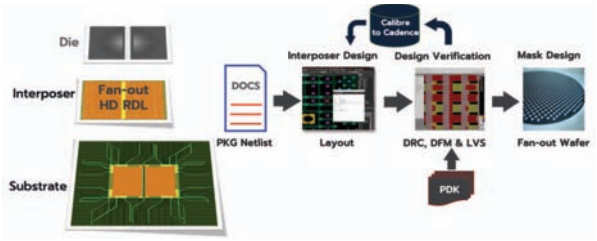

Fig. 3 Design flow for interposer with chiplets integration.

Due to the high-density interconnection in the interposer, the design cycle time for chiplet-based design is significantly longer than standard substrate design. To reduce the design cycle time, an auto-router program typically used for IC design has been developed and integrated with package mask layout tool. Upon receiving new netlists of chiplets, the auto-router program will initiate mask layout to complete the layout drawing. Unlike substrate Gerber file format, the layout drawing is generated in GDS (graphic data system) file format. GDS is a binary file format used primarily for integrated circuits (IC) design, including IC layout, mask data preparation, and lithography simulation. It allows to transfer layout data between different EDA tools in the design flow. Therefore, the layout drawing automatically generated by the auto-router can be imported back to the existing package substrate design tool for modification and optimization, thereby reducing the design cycle time. The auto-router can assist package designer in quickly completing preliminary designs and making modification and optimization. Furthermore, approximately 70% of interposer layout drawings, such as die to die interface, chip to substrate I/O layout and power distribution network (PDN) layout, can be accomplished by the auto-router. Fig. 4 shows the layout drawings generated by the auto-router.

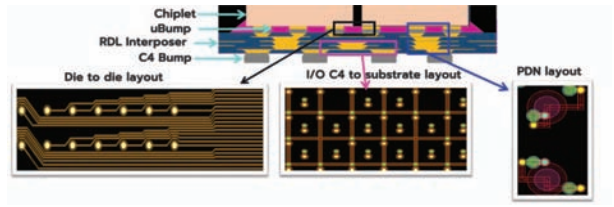

Fig. 4 Layout drawings generated by auto-router

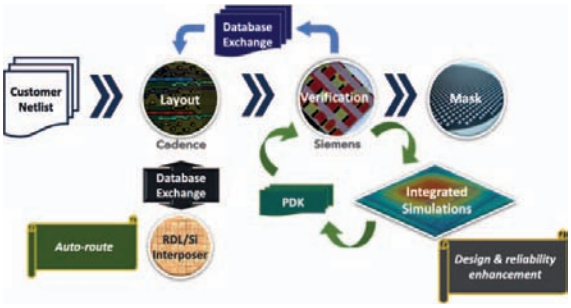

Fig. 5 Chip-to-package IDE design platform for chiplets integration

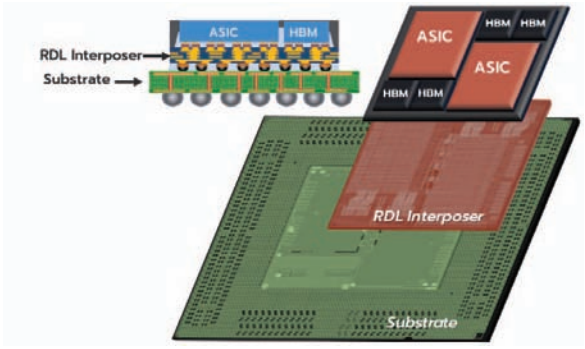

Fig. 6 Chip-to-package IDE design for chiplet integration with 2 ASICs and 4 HBMs on FOCoS RDL package

After the chiplet-based layout design is completed, the next step is validation, which includes DRC, DFM and LVS checks. The validation ensures that the design meets all requirements, such as electrical performance, interoperability, and manufacturability, making it ready for deployment or production. Both layout and verification are essential yet time-consuming iterative processes within the design workflow. Design complexity can result in thousands of verification errors in the first design layout, requiring significant effort to resolve each error throughout the entire cyclical design & verification

phases. Especially, when the design and validation tools are different from different EDA suppliers, how to quickly and easily modify the thousands of design errors becomes serious issues and leads to prolong design cycle times. Therefore, a software program is also developed in chiplet-based design platform to link the design and validation tools from different suppliers to fix the error locations easily and effectively. Fig. 5 shows the chip-to-package IDE platform for chiplets integration. This IDE platform has incorporated an auto-router IC design with package design tools to enhance RDL interposer routings in design workflow, especially IDE streamlines the compatibility among multiple EDA vendors to simplify the layout and verification processes, which has resulted in a 50% reduction in design cycle time. Fig. 6 shows an example of IDE design for a chiplet integration with 2 ASIC dies and 4HBMs on a FOCoS RDL interposer platform. The fanout module size is 50x43 mm^2 with 5 RDLs and L/S 2/2um, and package body size is 87.5x77.5mm^2.

III. Case studies for chiplets die to die interface design through UCIe standard

The D2D interconnect is a key enabler in the transition from monolithic SoC to multi-die chiplets integration within the same package. However, in many cases, the design of die-to-die interconnects is proprietary and protected by the chip design owners, which creates design boundaries and limits the widespread adoption of chiplets from various suppliers. To overcome these challenges, standardization of die-to-die interface is one of the most important efforts for building the universal chiplets ecosystem. Most recently, industry has merged standardization efforts into UCIe, which encompasses the full protocol stack from the transaction layer to packaging. The key attributes of die-to-die interface standards are outlined in UCIe specification 1.0 and 1.1[8]. These attributes are instrumental in defining the interfaces focusing on optimization of PPA and cost consideration. The block diagram of UCIe Physical layer (PHY) for advanced package modules is shown in Fig.7. It consists of a pair of clocks, x64 or x32 single-ended data lanes, a data valid lane in each direction (transmit and receive) and a track lane. Furthermore, the UCIe D2D interface bump out diagram for advanced packaging with the bump pitch between 40um to 50um is shown in Fig. 8. It showcases 10 columns for both x64 and x32 TX and RX data lanes and total 156 lanes for D2D interface routings.

The designs for D2D interconnects for both x64 and x32 on FoCoS RDL interposers are conducted with a ubump pitch of 45um. In FoCoS RDL D2D interface design, the design of experiments (DoE) are performed under different RDL L/S with 2/2um and 1.7/1.7um for different RDL layers ranging from 5 RDLs to 6 RDLs, as well as two isolation ground layers for signal-to-signal type design with ground RDL traces surrounding (SGSGSG). The electrical performance of the UCIe D2D interface is analyzed on FOCoS RDL advanced packages under various DoE conditions. The results are shown in Figure 9.

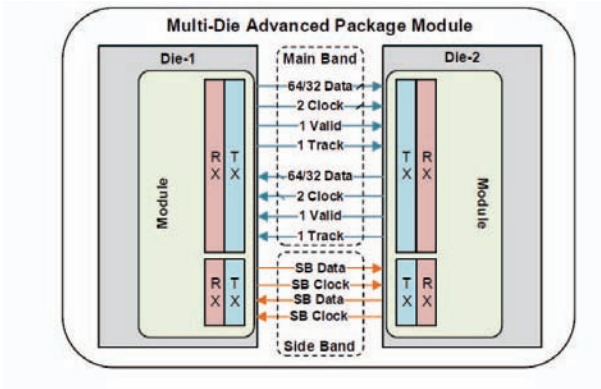

Fig. 7 Block diagram of UCIe PHY for Advanced package modules

(a) x64 *(b) x32*

Fig. 8 UCIe D2D interface bump out diagram for advanced packaging with bump pitch between 40um to 50um

It indicates that good electrical performance is achieved for x32 under 5RDLs with 3RDLs signal fine line (L/S 2/2um) and vis land pad of 14um routings at the data rate of 32Gbps, as shown in Fig. 9 (a). For x64, a minimum of 6 RDLs with 4 signal fine lines (L/S <2/2um) are required for UCIe D2D interface routings. Good electrical performance is achieved only with the routing GSGSG pattern by using smaller RDL L/S 1.7/1.7um and via pad 10um at the data rate 32Gbps, as shown in Fig.8 (d), compared to x32 design with RDL L/S 2/2um and 3RDLs signal fine line routings due to the higher density routing requirement from doubling data transmission lines. If maintaining the same design condition as x32 with RDL L/S 2/2um and via land 14um, the data rate for x64 must be reduced to 16Gbps to meet the electrical performance requirement, as shown in Fig.8 (b). The data rate can be further increased to 24 Gbps when reducing the via land size from 14um to 10um under the same RDL L/S 2/2um, as shown in Fig.8 (c).

As x64 has doubled data transmission lanes and requires higher D2D interconnect density compared to x32, more RDL layers routings and smaller RDL L/S, along with smaller dimension of via land, will increase the data rate and improve the electrical performance for x64 D2D designs.

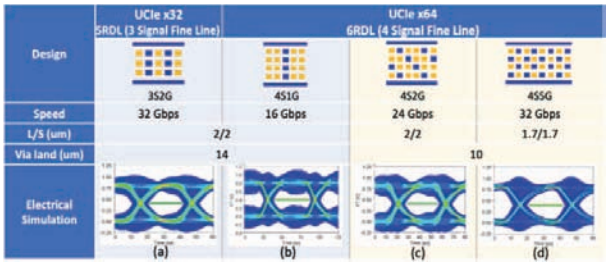

Fig. 9 Electrical performance analysis for UCIe D2D interfaces with x32 and x64 on advanced FoCoS RDL package

IV. Mechnical Analysis Workflow and Design Turnkey Toolbox for Chipelts Integration

Traditional mechanical analysis and simulation workflows are primarily tailored for monolithic SoC-based designs and are not readily adaptable to chiplet-based designs. Chiplet integration often involves combining chips and substrates made from different materials, such as silicon, organic substrates, and interposers. These heterogeneous materials have different mechanical properties, thermal coefficients of expansion (CTE), and stiffness characteristics, making it challenging to accurately predict their behavior under mechanical stress and thermal cycling. Meanwhile, chiplets integration also utilizes various advanced packaging technologies, such as 2.5D Si TSV, FO RDL and 3D integration. Each packaging technology introduces unique mechanical challenges related to thermal management, stress distribution, and interconnect reliability. Moreover, with the higher interconnect densities and more complex interconnections between chips, substrates, and package layers for chiplets integration can lead to signal integrity issues, mechanical coupling effects, and increased susceptibility to electromigration and mechanical failures.

To address these challenges, a comprehensive approach has been developed that integrates mechanical analysis, simulation, and testing throughout the chiplets integration design process. Fig. 10. shows the advanced mechanical analysis workflow for chiplets integration. It includes the data collection and measurement, such as assessing chip-to-package warpage using shadow Moiré, analyzing and simulating the mechanical behavior of chiplet-based systems through the tool like FEM (Finite Element Method) modelling, and finally evaluating long-term reliability of chiplets integration designs by examining factors such as solder joint fatigue, interconnect reliability, and mechanical stability over time. The goal of this mechanical analysis and simulation is to ensure that chiplets integration designs meet mechanical requirements encompassing reliability, thermal management, and structural integrity. Fig. 11 shows the comparison between the warpage obtained from measurements and mechanical simulation on a FOCoS RDL package with two chiplets integration. It demonstrates the alignment between the warpage measured by shadow moiré and the results from mechanical simulation using the mechanical analysis and simulation system. Ultimately, a comprehensive design turnkey toolbox for chiplets integration has been established, as shown in Fig.12.

This toolbox encompasses the designs of RDL interposer and package, electrical performance modeling and simulation, mechanical and thermal stress analysis, material selection, and reliability testing in assembly production.

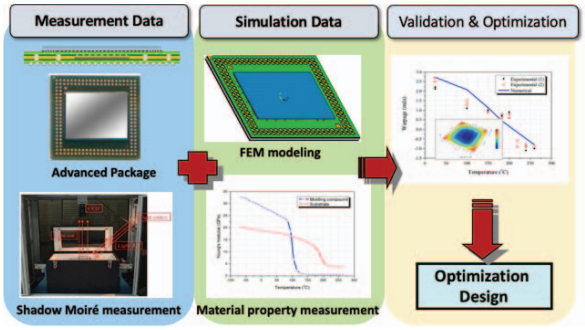

Fig. 10 Mechanical analysis and simulation workflow for chiplets integration

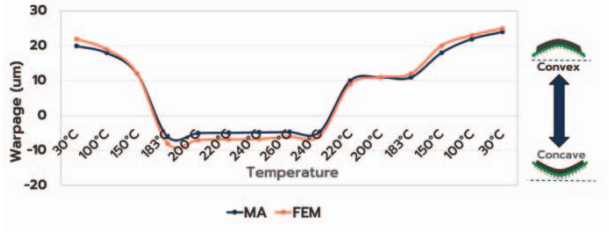

Fig. 11 Comparison between the warpage from measurement and mechanical simulation for FOCoS chiplets integration module

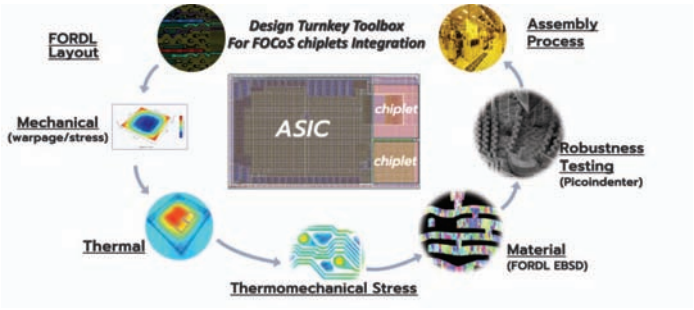

Fig. 12 Design turnkey toolbox for chiplets integration

V. Summary

The rapid evolution of chiplets and heterogeneous integration technologies is driving the need for innovative design approaches and ecosystem to meet complex design requirements while ensuring interoperability and balancing performance and flexibility. The proprietary nature of die-to-die interconnects presents challenges and creates boundaries and limitations for widespread adoption of advanced packaging technologies and chiplets from various suppliers. To address these challenges, a novel IDE has been introduced to enhance

design flexibility across various advanced packaging technologies including 2.5D Si TSV and HD FO RDL, while accommodating diverse customer design systems. The IDE has demonstrated a significant 50% improvement in design cycle time by seamlessly integrating an auto-router of IC design tool with package design tools. Moreover, by leveraging UCIe standard for die-to-die interconnect design using advanced x32 and x64 within the context of FOCoS packaging technology, the results demonstrate that achieving higher performance with x64 need more complex RDL signal routing with significantly smaller RDL L/S down to 1.7/1.7um compared to x32 with RDL L/S of 2/2um at the consistent transmission speed of 32Gbps. Additionally, an advanced mechanical analysis workflow has been proposed to address mechanical challenges in chiplet-based designs. Finally, a comprehensive turnkey toolbox is presented, encompassing various design aspects including RDL interposer and package co-design, electrical performance modeling, and simulation, mechanical and thermal stress analysis, material selection, and reliability testing. This integrated approach aims to streamline the chiplets integration processes and accelerate design achievements in advanced packaging technologies.

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