

Development of a High Power Density Inverter

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Master of Science in Electrical and Renewable Energy Engineering

By

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Abstract

RISING in switching frequency directly reduces passive component requirement in power converters, improves achievable control bandwidth, and in theory, enables miniaturization. Soft switching is used to reduce frequency dependent loss, so that power converters can be scaled, with good efficiency, to very high switching frequency. With new circuit architecture, new optimal control method, and the new high bandgap power mosfets, it becomes possible to reduce the size of inverter and achieve dramatic improvements in transient response.

While soft switching technique diminishes mosfet turn-on loss, it often rises other types of losses such as inductor core loss, and mosfet's body-diode conduction loss. Unfortunately, these losses are also frequency dependent (meaning the losses increase with frequency). To reduce these losses, existing techniques focus on optimizing either inductor ripple current or mosfet turn-on delay. Since the two type of loss mechanisms have a close relationship, existing techniques only achieve sub-optimal result. Simulations and experiments in this thesis suggest that true optimal operating point, where loss is lowest, can be found by tuning in both directions (optimizing inductor ripple current and mosfet turn-on delay).

In this thesis, zero voltage resonant transition of a half-bridge is review with amendments to make the analysis correct in high frequency converters where the resonant transition occupies a large part in a switching cycle. Then this thesis describes a programmatic tuning approach for ZVRT converter to achieve lowest loss under all operating conditions. While this

initial brute-force approach cannot find the true optimal operating point (still sub-optimal), its result is better than single direction approaches found in the literature, and it shows that there is space for efficiency/power density improvement in converters that have a half-bridge as basic building block.

2KVA inverter prototypes are built and tested. The final prototype has power density larger than 50W/In³, with peak efficiency 99% and CEC efficiency 96%, at switching frequency from 250 KHz to 1MHz. It is not new for DC-DC converter to have power density larger than 50W/In³, but for DC-AC inverter, such level of compactness is new. Experimental result confirmed the effectiveness of the proposed control method in improving efficiency and power density of inverter.

The inverter is designed for residential PV systems (i.e. systems up to 10kW). It is designed to work with the new differential power processing (DPP) converters and Tesla's POWERWALL battery. Together, the three parts will create a residential PV system that is not only compact, which can be mounted easily to existing home structure, but also has lowest leveled-cost-of-energy (LCOE).

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Acknowledgments

Chapter 1

Introduction

For the future to be good, we need solar, storage, and (of course) ...

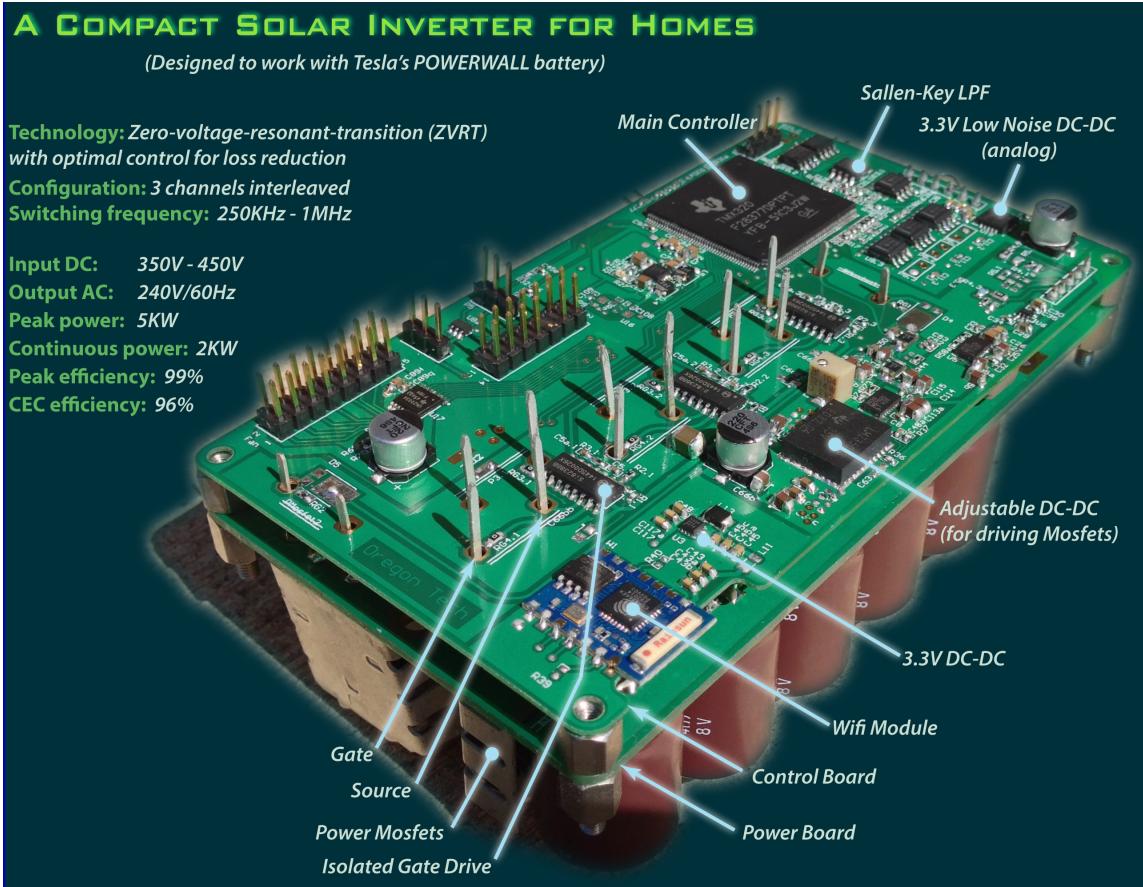


Fig. 1 A high power density inverter (designed to work with Tesla's PowerWall battery).

In a recent report, the 2015 edition of Energy Technology Perspectives (ETP 2015), International Energy Agency (IEA) asserted, “A concerted push for clean-energy innovation is the only way the world can meet its climate goals”. In addition to international agreements to cut carbon emission, we need “enabling technology” that can integrate intermittent renewable energy sources into the electrical grids, “if we are to have a chance of keeping the world below

2 degrees Celsius of warming - a level beyond which truly dangerous climate change might set in.”

1.1 Introduction

Inverter plays a key role in the future of renewable energy. It is the touch point for utilities to understand and control renewable power generation and integration into the electrical grid. Reducing the size, cost and improving efficiency, reliability of inverters could have tremendous benefits for the electrical grid in particular, and for the society in general. Recently, there has been growing interest in increasing solar inverter power density. Reducing the size and weight of inverters will make them cheaper for manufacturing, installation, and maintenance. Ultimately, it will encourage the use of solar PV in homes, which leads to more efficient distributed electrical grid, and help bring affordable micro-grids to remote regions of the globe.

1.2 The Thesis Organization

In this thesis, Chapter 2 gives a short review of traditional solar system configurations and solar inverter. It also reviews a new configuration in solar system, called differential power processing (DPP).

Chapter 3 reviews power converter, soft switching techniques to reduce switching loss, and scaling of power converter

Chapter 4 reviews existing techniques for loss reduction in Zero-voltage-resonant-transition converters. Then the ZVRT in power converter is reviewed with amendments to make it correct in high frequency.

Chapter 5 describes the proposed optimal control method for loss reduction.

Chapter 6 describes the inverter design.

Chapter 7 is conclusion and future directions

Chapter 2

Inverter in Solar Systems

RENEWABLE plus storage plays an important role in the future of our energy. However, both are DC sources, whereas most of our energy demands are AC. The question is should we turn to use DC power, or use an inverter to convert DC power into our familiar AC power? Some researchers suggest using DC power directly, since it is more efficient. However, they ignore the huge cost of the solution. It is far cheaper to use an inverter to convert DC into AC, than it is to redesign everything else to run on DC. In the near future, inverter remains an essential part in solar, storage and other renewable energy systems.

2.1 Solar Inverter and Traditional Solar System Configurations

2.1.1. Solar system

Installed Solar PV systems range from modest residential rooftop units to megawatts scale utility systems, with commercial PV system installations have power capacity in between. [1]:

- Residential: systems up to 10 kilowatts (kW)
- Commercial: systems ranging between 10 kW and 1 megawatt (MW)
- Utility: Systems larger than 1MW

Inevitably, there are overlaps in the three market segments. For example, some residential systems have capacity larger than 10 kW, while some commercial PV systems have capacity larger than 1MW. In 2014, only 0.3% of the PV system installations in the US are utility-scale. Nevertheless, utility-scale PV systems account for more than 55% of the total capacity additions (Fig. 2) [1].

2.1.2. Solar inverter in solar system

The most popular classification of solar inverters is based on the connection type of PV modules into the inverter, which divides inverters into four types: central inverter, string inverter, multi-string inverter, and micro-inverter [2]–[5].

Capacity Additions (MW)

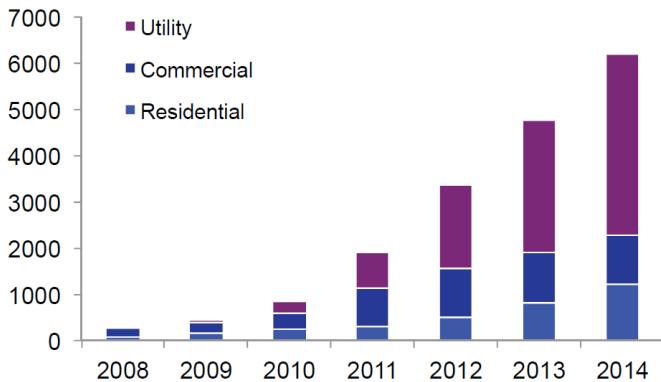


Fig. 2. Annual U.S. PV Installation by Market Segment [1].

Central inverter, as its name

implied, is based on centralized concept (a small number of very large inverters). In this configuration, PV modules are connected in series to create strings that have sufficiently high-voltage output. These strings are then connected in parallel (with diodes to protect the reversed current that may damage PV modules). Then the parallel of strings are connected to a large central inverter (Fig. 4a). In this centralized configuration, MPPT is done in the central inverter.

The string and multi-string inverter are based on a more decentralized concept. Instead of connecting all strings to a single large central inverter and doing MPPT in the central inverter, each string is connected to a smaller inverter (string inverter) or to separated ports of inverter (multi-string). Fig. 4 b and c show the connection of string and multi-string inverter. In these configurations, MPPT is done at each strings (string-level MPPT), avoiding mismatch, partial shading between strings (not between modules). Therefore, MPPT efficiency is better compare to the central inverter configuration.

In the most decentralized concept, each module has its own power electronic converter (i.e. module-level-power-electronics or MLPE), which can be a micro-inverter ((Fig. 4d) or a module DC optimizer. In this configuration, MPPT is done at each module, avoiding mismatch, partial shading between modules. As a result, MPPT efficiency is the best compare to previous configurations.

However, MLPE configuration has a little higher power loss compare to other configurations. In the case of micro-inverter, high voltage conversion ratio limits the efficiency. With current technology, it is relatively not efficient when boosting from a low voltage output of a PV module to the standard line voltage (which is about 8x higher). Although DC optimizer doesn't have a high voltage conversion ratio, it processes all the power through at least two stage: DC optimizer and central (or string) inverter. The intermediate bulk power-processing limit the overall efficiency.

MLPE increases MPPT efficiency but, at the same time, it increases power loss. The question is which configurations yield highest energy: central, string, or MLPE? Elasser et al. [6] conducted a comparative study of the annual energy yield between different configurations: centralized, string, and MLPE. The paper concluded that an energy gain in the range of 4% to 12% could be achieved from “distributed configurations” (MLPE) over centralized configurations. The study may has a little bias toward MLPE, but it shows a general comparison.

In real solar systems, the overall price-per-watt depends highly on other factors. For example, micro-inverter offers a modular design that help reduce cost of installation for small and medium size solar systems. Trade-off needs to be considered carefully when designing solar PV systems. The general rule in the industry is that large solar farms

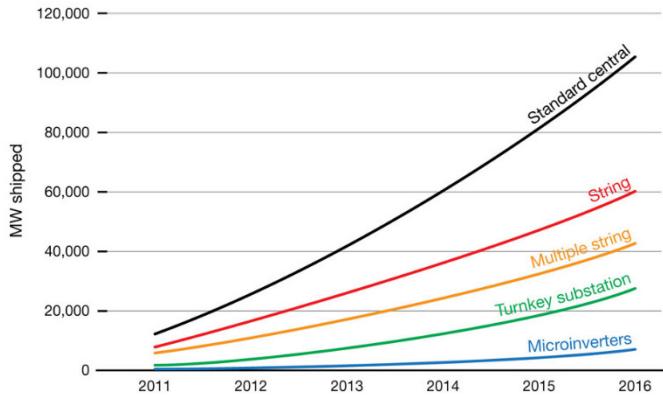


Fig. 3. Solar inverter installation market forecast.
(Courtesy IMS Research)

prefer centralized concept and small ones prefer MLPE. Indeed, a research by IMS forecasts that a strong growth of central inverter (Fig. 3.) is driven mainly by the increasing installation of utility scale PV projects.

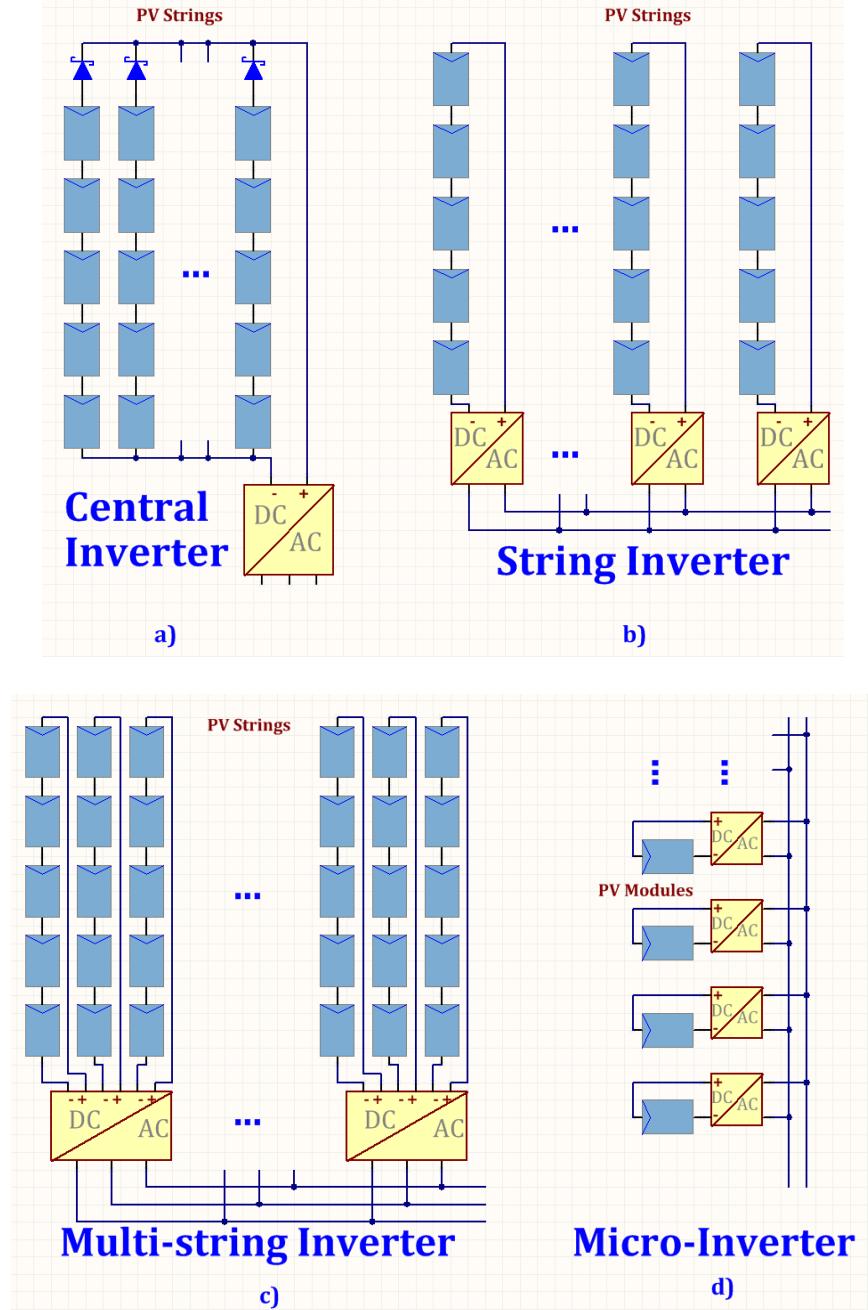


Fig. 4. Grid-tie inverters: a) Central Inverter, b) String Inverter, c) Multi-string Inverter, d) Micro inverter.

2.2 Sub-module differential power processing

Central inverter achieves higher power efficiency but has less MPPT efficiency due to module mismatch, or partial shading. MLPE improves MPPT efficiency at the cost of higher power loss. A new concept, named “sub-module differential power processing,” suggested by Dr. Krein and Dr. Pilawa-Podgurski [7]–[14], improves both power efficiency and MPPT efficiency, compares to previous configurations (Fig. 5, and Fig. 7).

The innovative idea is the “differential power processing,” in which only the difference in peak power generation between sub-modules is processed/balanced (Fig. 6) so that sub-module in a string operates at its peak power. In other words, instead of processing all power from PV module (as MLPE does), small, low cost DC-DC converters are used to transfer in/out the mismatch in peak-power generation between sub-modules, so that each sub-module can operate at its peak power without affecting other sub-module (Fig. 6).

The system MPPT algorithm has two parts working cooperatively: a distributed MPPT algorithm controls the power transfer between sub-modules to ensure sub-modules peak production, a traditional centralized MPPT algorithm, which is already available in a central inverter, make sure peak power production for the system. The beauty in the new solution is that it is an add-on to old solar systems to improve overall power production, in a very smart way [7], [12], [14].

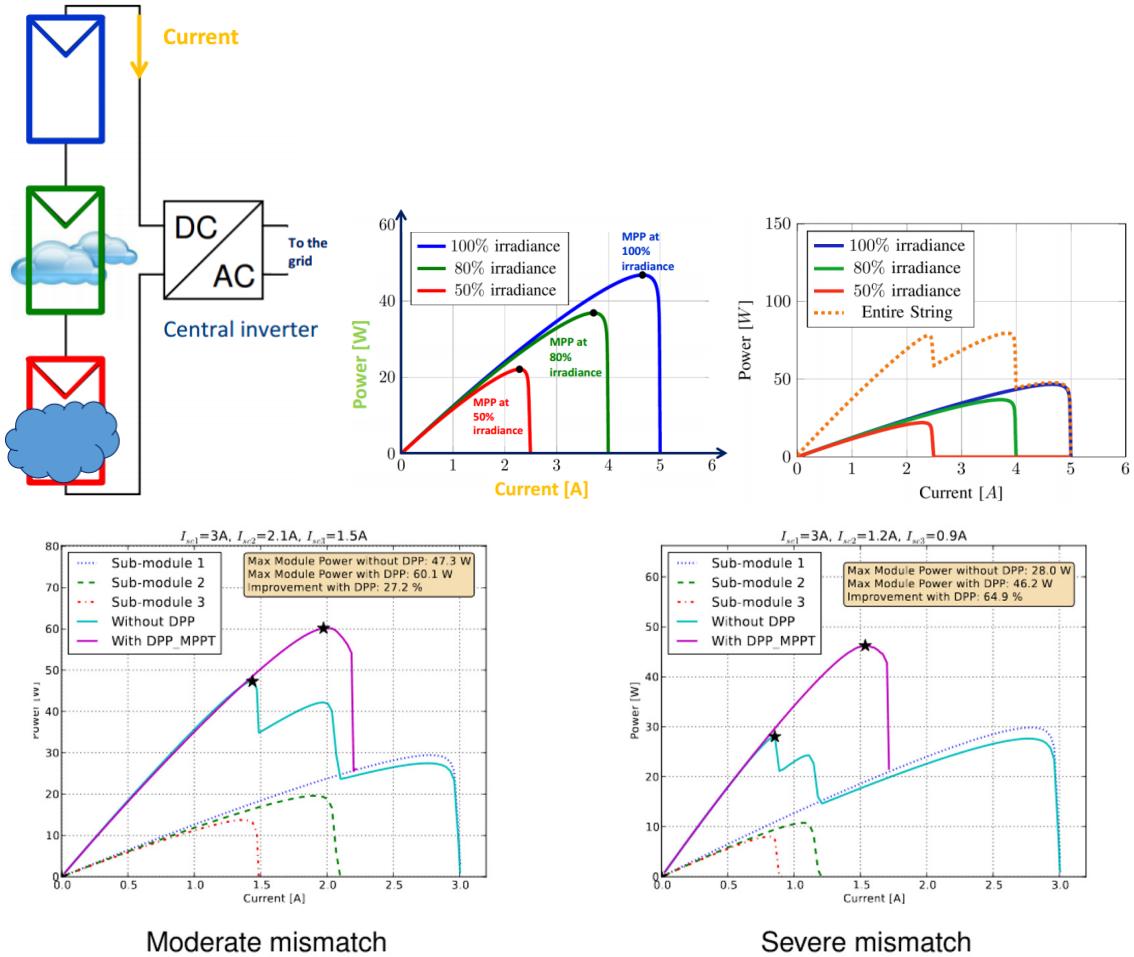


Fig. 5. Mismatch of peak power generation due to: partial shading, manufacturing variations, and aging. DPP can track the true highest power point [11].

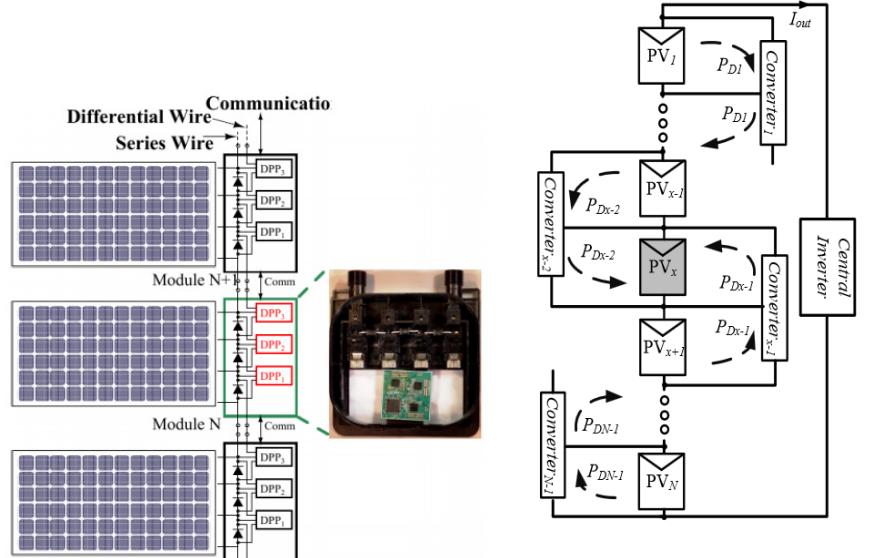


Fig. 2. Example of the power flow for a N PV panel string connected to $N-1$ gyrator DPPs, containing a shaded PV at the x location.

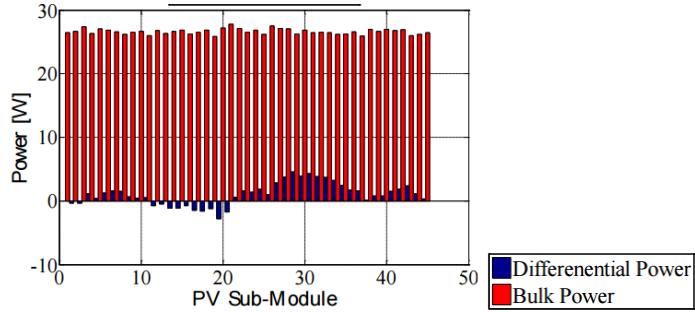


Fig. 6. In differential power processing (DPP) configuration, each DPP converter processes the power difference, so that each sub-module can operate at different maximum power point. This configuration avoids intermediate conversion of the bulk power. The bulk power goes directly into the central inverter. Therefore, power efficiency is higher, DPP power rating is smaller, system size, and cost improves significantly [11].

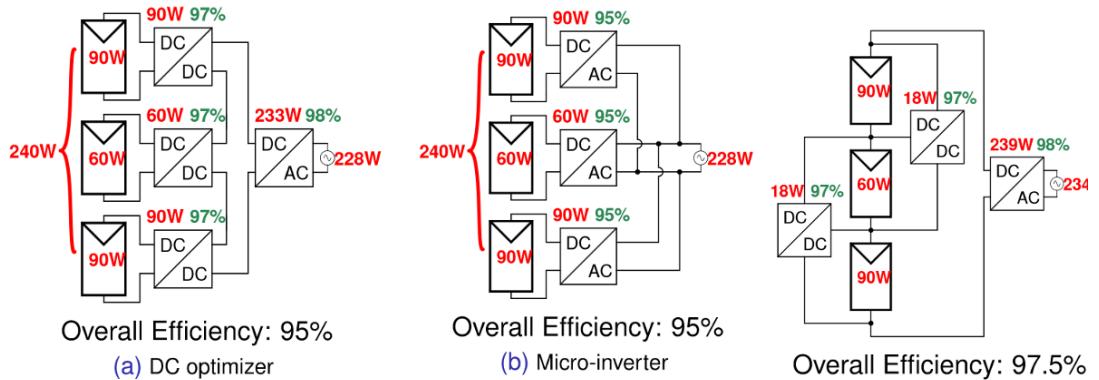


Fig. 7. Compare to MLPE, differential power processing (DPP) significantly improve power yield of a PV system [11].

Chapter 3

Switch Mode Power Converter

The concept of “electronic power converter” was defined in 1944, by Alexanderson and Phillipi, as power converters based on electronic means, and limited to “the conversion of power as distinguished from electric energy for purposes of communication” [15]. Since then, electronic power converter has become a vital part in all electronic devices and systems. It converts, regulates electric power from various sources to a suitable, well-regulated output for consumption, transmission, or storage.

In general, electronic power converters can be divided into four categories: DC-DC converter, AC-DC rectifier, DC-AC inverter, and AC-AC cycloconverter [16]. The newer type of converter, AC-AC cycloconverter, converts an AC power input into an AC output with controllable magnitude and frequency. As an example, a cycloconverter is used in the output stage of Enphase’s micro-inverter to convert high-frequency AC current, generated by a resonant inverter, to a much lower AC line-frequency current. The added cycloconverter gives the system flexibility to perform advanced functions, such as, active/reactive power control, fault-ride-through, internal impedance control.

3.1 Switch Mode Power Converter

Power converters are also categorized based on the operation of its internal active switching devices (transistors or mosfets): linear mode, and switch mode. Linear mode power converter (Fig. 8) has active devices operate in linear mode, while switch mode power converter has active devices operate in saturated mode (i.e. on/off mode). Linear mode power converter (Fig. 8) has limited capability (it can only convert a higher DC voltage to a lower DC voltage) and has low efficiency, but produces less noise output. The main application of

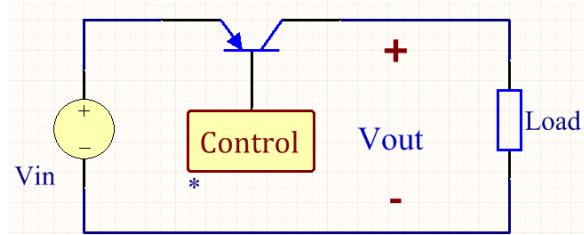


Fig. 8. Linear mode power converter

linear mode power converter is low noise, low power DC-DC. Due to low efficiency, linear power converter is not used in high power applications. The main reason is not to conserve energy, despite the nobility of such pursuits. Rather, it is because low efficiency converter generates too much heat that we cannot adequately cool it with current technology [16].

On the other hand, switch mode converter is very flexible and has high efficiency. In fact, ideal switch mode converter (Fig. 9) has no intrinsic loss mechanism. Losses arise unavoidably from the use of real components that cannot switch instantly and have undesirable parasitic inductance, resistance, and capacitance. These losses constrain not only the efficiency of power converters, but also the reliability, size, cost, and even converter's transient response. Finding a way to reduce these losses is, in a sense, paramount to miniaturization.

The simplest form of Switch Mode Power Converter is the ideal buck converter (Fig. 9). Voltage of the switch node (v_{sw}) is equal to the converter input voltage V_{in} when the switch is in position 2, and is equal to zero when the switch is in position 1 (Fig. 9 and Fig. 10). The switch position is changed periodically with period $T = 1/f$. The duty cycle D is the fraction of time when the switch is in position 2.

With an ideal low pass filter (LPF), all harmonic in the switch node voltage (v_{sw}) is filtered out, leaving only the DC component in the output voltage (v_{out}). From Fourier analysis, the DC component of a periodic waveform is its average value [16]:

$$v_{out} = \frac{1}{T} \int_0^T v_{sw}(t) dt = DV_{in} \quad (1)$$

In theory, output voltage v_{out} of a buck converter only depends only on duty cycle and input voltage. When we change D sinusoidally (i.e. $D = A \sin(\omega t)$), the output voltage v_{out} will change sinusoidally; and when we keep D fixed, v_{out} will be fixed. However, practical buck converter, built from non-ideal components (Fig. 9), generates an output voltage less than (1), and has undesirable harmonics (Fig. 10).

Undesirable harmonics present in the output voltage is because real low pass filter cannot filter out all harmonics. As a result, the output voltage contains some ripple as depicted in Fig. 10. This ripple can be reduced by increasing the switching frequency ($f = 1/T$), or lowering the cut-off frequency of the low pass filter (LPF), which increases the size of inductor and capacitor.

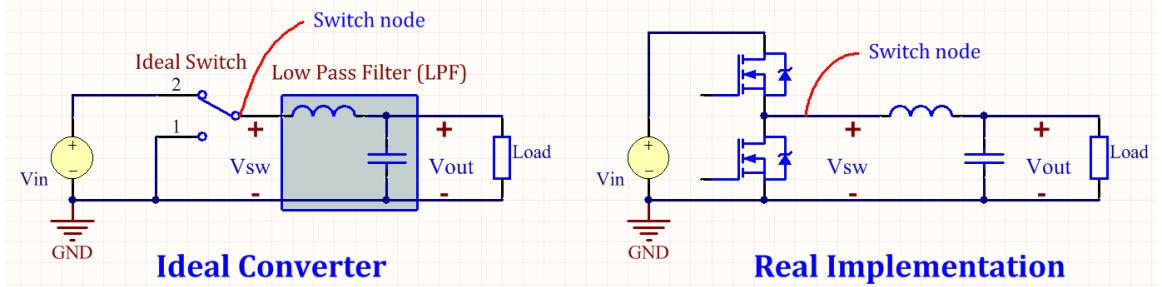


Fig. 9. The buck converter: a simple type of switch mode power converter. The ideal buck converter (left) has 100% efficiency.

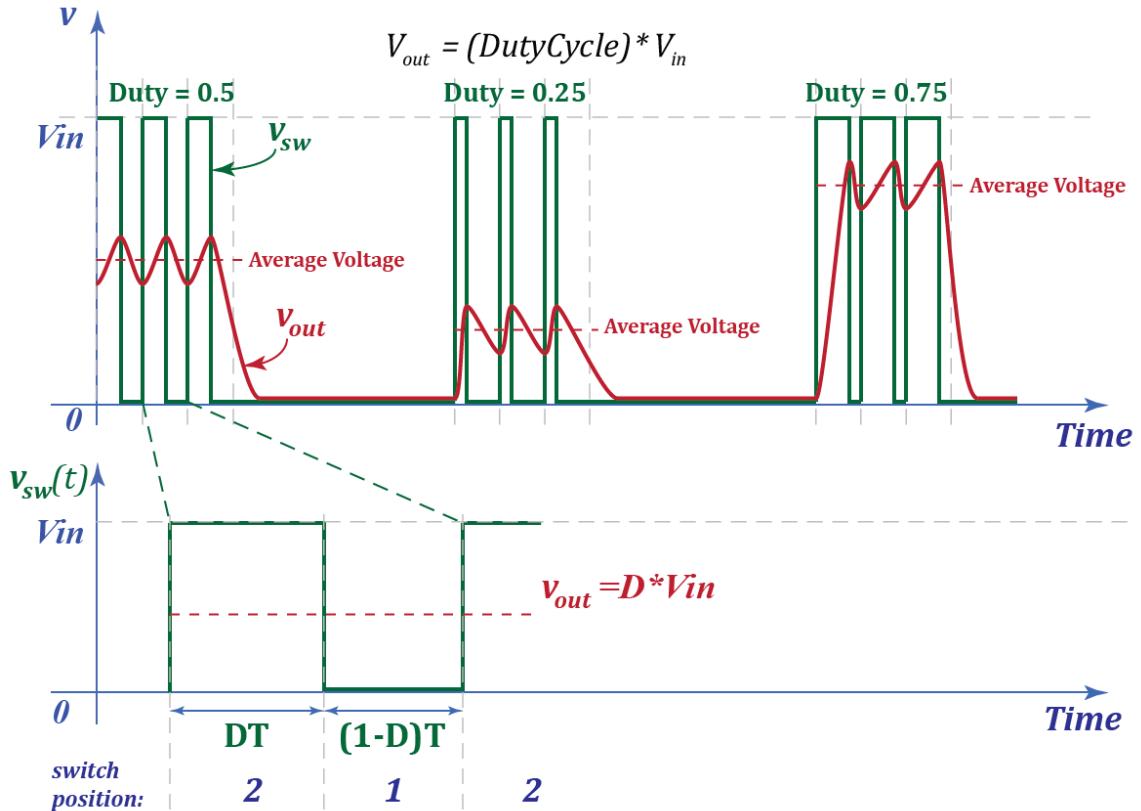


Fig. 10. Buck converter waveforms.

There are two reasons account for the dropping of the output voltage compare to the theoretical value in (1). First, when mosfet or diode is on, there is a voltage drop across them. Therefore, $v_{sw}(t)$ is not a square wave from zero to Vdc, but is a square wave having slightly smaller magnitude. Second, mosfets and diodes do not turn on/off instantly. The transition of $v_{sw}(t)$ from zero to Vdc (or Vdc to zero) takes some time. Therefore, $v_{sw}(t)$ waveform is not a perfect square wave. As a result, the integral (1) approximates DV_{in} :

$$v_{out} = \frac{1}{T} \int_0^T v_{sw}(t) dt \approx DV_{in} \quad (2)$$

Because of the approximation, the output voltage v_{out} is not fixed with a fixed input voltage and duty cycle. In order to keep output voltage constant at a set point, a compensator (i.e. PID) is often used. For example, in DC-DC converters, a compensator monitors output voltage and change duty cycle (D) accordingly to bring output voltage back to set point when load changes; In DC-AC inverters, compensator monitors output RMS voltage and change the magnitude A of the sinusoidal ($D = A\sin(\omega t)$) to keep the RMS constant.

3.2 Soft-switching in Power Converter

Soft-switching is a technique to reduce switching loss in power converters. The main idea behind soft-switching in power converters is that we don't forcefully turn on/off mosfets to drive circuit's voltages to a desired value (or state). Instead, we let the circuit resonate itself to the desired state, then mosfets are switched at zero voltage across their terminals (Drain and Source).

While all soft-switching converters have mosfets turn on at zero voltage, most don't have mosfets turn off at zero current. It is because having Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) at the same time is hard to accomplish without sacrificing other important properties such as controllability. For example, the Sine Amplitude Converter (SAC) [17] achieves both ZVS and ZCS concurrently, but its output voltage is fixed with the transformer turns ratio.

In general, ZVS is preferable over ZCS because turning on mosfets has much higher loss than turning them off. Indeed, when mosfet turns off at high current (with an inductive load), its parasitic capacitor ($C_{out} = C_{oss} + C_{rss}$) serves as a channel for the current to flow, so that the switching-off happens more slowly, generates less ringing. The energy results from simultaneous occurrence of non-zero current and voltage across mosfet's terminals during turn-off transition, is stored in mosfet's output parasitic capacitor ($C_{out} = C_{oss} + C_{rss}$) and can be recover later in during resonant turn-on.

On the other hand, when mosfet turns on at high voltage (non-ZVS), its output parasitic capacitor ($C_{out} = C_{oss} + C_{rss}$), which holding an energy of $\frac{1}{2}CV^2$, is shorted. The energy is dissipated into heat. This capacitive energy is the energy that was stored previously during turn-off. If the energy is not recovered during turn-on (i.e. by ZVS), it is lost.

In addition, the energy results from simultaneous occurrence of non-zero current and voltage across mosfet terminals during turn-on transition, is also dissipated in heat. The question is why don't we turn on mosfet quickly to reduce the time of simultaneously occurrence of non-zero voltage and current in order to reduce the loss? It turns out that when we turn on mosfet quickly, other more severe losses arise, such as diode reversed recovery loss, and loss due to ringing of voltage/current. The worst case happens when the upper mosfet is turned on too fast, body diode of the lower mosfet goes through a process called "reverse recovery", which effectively a short-circuit for the reverse-recovery time (t_{rr}), during which, a large current flows from V_{in} to Ground to creates heat and charges the parasitic inductance of the main power loop. After the reverse-recovery time, energy in the parasitic inductance of the main power loop resonates with the lower mosfet's parasitic capacitance, creates ringing, heat, voltage overshoot, and EMI. This reversed recovery short-circuit is usually the root cause for most EMI problems [18].

3.3 Scaling of Power Converters

On studying commercial power converters, one fact that becomes obvious is that the bulk of the system, that is its volume and weight, comprises cooling and passive energy storage elements. Semiconductor devices, on the other hand, occupy only a small fraction of the total

footprint and cost. Inverter teardown reports from Yole Development, and a latest report from IHS iSuppli reveals mechanical and passive components appropriate 60%-70% of the total inverter cost [19]–[25]. It is obvious that inverter miniaturization approaches should focus on reducing the requirements for cooling and passive energy storage components.

Passive energy storage

requirements scale inversely with switching frequency. According to Dr. Perreault [26], “for operation at the same voltage and current levels but at a factor k_f higher in switching frequency, circuit resistances remain unchanged, while capacitor and inductance values scale inversely with frequency (by a factor $1/k_f$).”

If the (capacitance and inductance) requirements scale inversely with frequency, then how do the volumes scale? The answer is quite subtle as the actual volumes of capacitor and inductor depend on many factors. Reference [26] gives detail answers to this question.

While we had some technologies, especially in packaging, that improved capacitor performance recently, we are still using the same type of inductors that are available decades ago [27]. The bottleneck of the technology (to make smaller, more efficient converter) is the inductor. Fig. 11 shows how inductor volume scales with operating frequency for three different types of core. Core loss is the major loss that limits the rising of operating frequency. We have to hope for progress in material science [27].

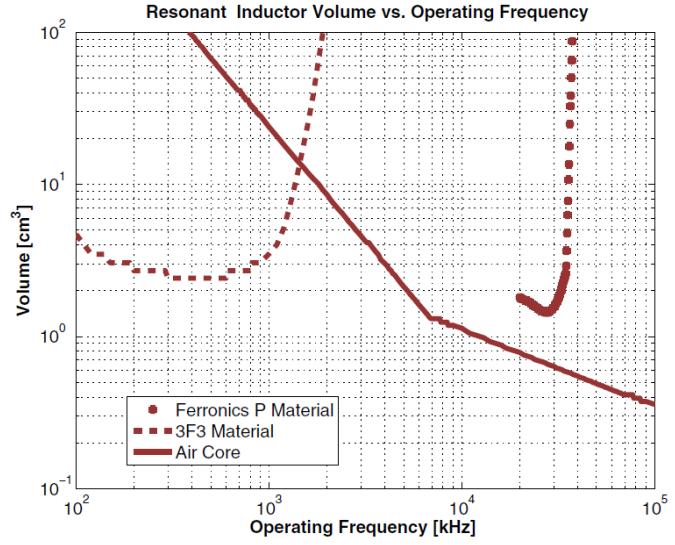


Fig. 11. The reduction of inductor volume with operating frequency dependence of magnetic core materials [26].

Chapter 4

Optimal control of a half-bridge for Loss Reduction

4.1 Introduction

Rising in switching frequency directly reduces passive component requirement in power converters, improves achievable control bandwidth, and in theory, enables miniaturization. Soft-switching [28]–[46] is used to reduce frequency dependent loss, so that power converters can be scaled, with good efficiency, to very high switching frequency [47]. In fact, soft-switching is inevitable in high-frequency, high-power density converters.

Soft-switching techniques in power converters can be classified into three categories [38]: load resonant, resonant link, and resonant transition. Among the three soft-switching techniques, resonant transition is most popular in DC-AC inverter due to great flexibility in control and less dependency on load or operating condition. Resonant transition refers to the change of switch node voltage during dead-time (when mosfets are off) to a zero-voltage state before turning on mosfets. While resonant transition technique (in theory) diminishes mosfet turn-on loss, it often rises other types of losses such as core loss, copper loss, and mosfet's body diode conduction loss.

4.1.1. Optimal control of inductor current to minimize core loss and copper loss

To reduce core loss and copper loss, Baek, Choi, and Cho [48] proposed a “Digital Adaptive Frequency” control method where converter’s switching frequency is controlled to minimize inductor ripple current. The target of [48] is to minimize the peak-to-peak value of the inductor current. However, the analysis in [48] (the traditional analysis) is only correct when the resonant transition time is small, which corresponding to large peak-to-peak inductor current. In other words, the target of the control method belies the theory that the control method is based on.

Indeed, the waveforms showing at the end of [48] is not optimal. The straight resonant transition curves in the waveforms imply that inductor ripple current is large (the transition curves is an S curve when the ripple current is small). In addition, when switching frequency is high, the resonant transition becomes a significant part of the waveform that cannot be neglected. The control method in [48] is ineffective (sub-optimal) for a special case (low frequency case), and incorrect for high frequency case. A more general analysis of Zero-voltage resonant transition (ZVRT) could guide the discovery of a better control method for further loss reduction in low frequency converter, and for a successful applying of the idea in high frequency converter.

Under a DoE award EE0003176, a team led by Dr. Batarseh proposed a “hybrid boundary conduction mode current control method” [49]–[53] for optimizing inductor ripple current. The control method sets upper and lower limits for inductor current and try to turn on/off mosfets so that inductor ripple current changes between these limits. The reported result is better than [48] since this method [49]–[53] directly control the inductor current (compare with indirectly controls of the inductor current in [48]).

However, the method in [49]–[53] relies heavily on sensing the high frequency inductor current. Therefore, it is impractical to increase the switching frequency to very high, not to mention the cost of high bandwidth current sensors. In addition, [49]–[53] does not mention an effective way to estimate the transition time, in order to minimizing mosfet’s body diode conduction loss, which contributes a large part in the overall loss of ZVRT converter.

4.1.2. Minimizing mosfet’s body diode conduction loss

Optimal control of inductor ripple current is essential to reduce conduction loss and core loss. Another frequency dependent loss that also needs to be addressed in high frequency converters is mosfet’s body diode conduction loss, which occurs after the resonant transition is completed, and before mosfets turn on (state 3 and state 7 of the zero voltage resonant transition (ZVRT) in Fig. 14). Since this loss takes place twice in a switching cycle, it is frequency dependent loss (meaning this loss increases when frequency increases). Mosfet conduction loss is generally much lower than its body diode conduction loss (Fig. 12).



Fig. 12. Typical mosfet and its body diode conduction loss

Therefore, it is desirable to minimize, ideally eliminate, the two states (state 3 and state 7 in Fig. 14).

In order to prevent mosfet's body diode conduction states (state 3 and state 7 in Fig. 14), we need to turn on mosfet early, before its body diode begins to conduct. However, turning on mosfet too early results in loss of zero-voltage-switching (i.e. hard-switching), poor efficiency, and in the worst-case, failure of the device due to shoot-through. Ideally, mosfets should be turned on immediately when the voltage across its Drain and Source (V_{ds}) drop to zero.

Existing techniques, [54]–[67], rely on high-bandwidth voltage sensor to detect the moment when V_{ds} drop to zero and turn mosfets on exactly at that moment. Method in [67], a straight implementation of this idea, is not practical in high frequency converter as it requires insanely fast comparators and gate drive circuits. “Adaptive” gate drive technique [63] turns mosfet on at a threshold-crossing point, instead of zero-crossing point, and adjusts the threshold in each switching cycle to match mosfet actual turn-on point with the zero-crossing point. This method, in practice, results in poor performance because of high-sensitivity to circuit

parameters and temperature. Predictive gate drive [62], or delay-locked loops techniques, reduce the dependence on fast comparators but still rely on sensing the switch node voltage, which can be extremely noisy in some cases.

Better results has been reported with “Sensorless” technique [64] which searches for an optimal delay (or deadband) base on an observation that optimal dead-band delay is achieved when efficiency is maximized and duty cycle is minimized. However, the searching process, as described in the paper, is slow and only suitable for DC-DC converter where output voltage is usually fixed. With a fast moving output voltage in DC-AC inverter (i.e. 60Hz sinusoidal), method in [64] will not have enough time to settle down to an optimal delay.

4.1.3. Combined optimization results in lowest loss

Existing techniques focus on minimizing either inductor ripple current [48]–[53], or mosfet’s body diode conduction [54]–[67]. However, experiments suggested that lowest loss obtains by a combined optimization in both directions. The optimal operating point, where loss is lowest, can be found by manually adjusting the switching frequency and dead-band of the ZVRT converter. It is desirable to have a programmatic tuning method so that converter can tune it-self, in both directions, to the true optimal operating point.

In the next section (4.2), zero voltage resonant transition of a half-bridge is review with amendments to make the analysis correct in high frequency converters where the resonant transition occupies a large part in a switching cycle. Then Chapter 5 describes a programmatic tuning approach for ZVRT converter to achieve lowest loss under all operating conditions.

4.2 Zero Voltage Resonant Transition (ZVRT) of a Half-bridge

Half-bridge is the popular building block in power converters. It has a switch node, whose voltage (v_{SW}) can be switched between two different levels. An inductor is usually connected to the switch node, functioning as a low pass filter allowing only DC current to go through. Fig. 13 shows a synchronous buck converter having one half-bridge and one inductor. This

section discusses the resonant transition ZVS of a half-bridge in the buck converter with current/voltage sign convention as shown in Fig. 13.

Zero Voltage Resonant Transition (ZVRT) of a half-bridge was described in [68] (since 1988). However, the description assumes a special case where the inductor current is large and dominantly drives the transition. The result in the paper [68] has been repeated in the literature without concerning about the error that may be large in situations such as high switching frequency, low inductor ripple current, high output voltage. Perhaps, extreme high frequency / high efficiency converter has not been a concern until recently.

As described in [68], the resonant transition happens during the dead-time. When both mosfets are off, the inductor current resonates with parasitic capacitors of the two mosfets to complete the desired transition, which can be rising or falling of the switch node voltage (Fig. 14). With large inductor current (as the paper assumed), the rising and falling transition of the switch node voltage happen so quick that they can be approximated as straight lines.

According to [68], in order for the resonant transition to happen successfully, at the beginning of the transition the inductor current must have

- (a) correct direction, and
- (b) enough energy to fully charge/discharge the two mosfets' parasitic capacitors. In other words, the energy store in the inductor must be larger than the energy required to charge/discharge the two parasitic capacitor:

$$\frac{1}{2}LI_{L0}^2 > C_pV_{in}^2 \quad (3)$$

Where I_{L0} is the inductor current at the beginning of the transition; C_p is the output parasitic capacitance of mosfet (mosfets appear in parallel to inductor so the total capacitance is $2C_p$); V_{in} is the input voltage, and L is the main inductance.

(Note that this ZVS condition is not correct in general. Amendment is provided in 4.2.5)

Fig. 14 shows waveforms of the buck converter with focusing on the rising and falling zero voltage resonant transition (ZVRT). When operating under ZVS, the half-bridge has eight possible states:

State 1: (Before the rising transition) In this state, the lower mosfet is fully on; switch node voltage equals zero ($v_{SW} = 0$); parasitic capacitor of the lower mosfet is fully discharged, while parasitic capacitor of the high mosfet is fully charged to the input voltage ($E = \frac{1}{2}C_pV_{in}^2$). The ZVS condition [68] says that before the rising resonant transition, the inductor current must have negative direction with large magnitude (i.e. equation (3)). (It's up to the designer to set the operating condition such that the inductor current has negative direction with large magnitude, or ZVS won't happen (Fig. 17))

This state ends when the lower mosfet is turned off.

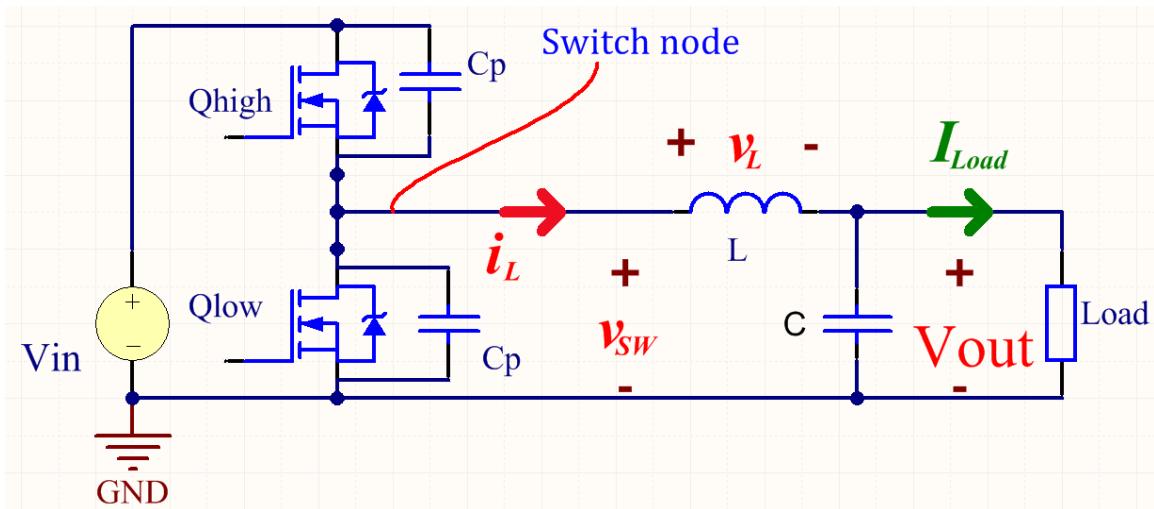


Fig. 13. A buck converter showing sign convention of current and voltage for the discussion

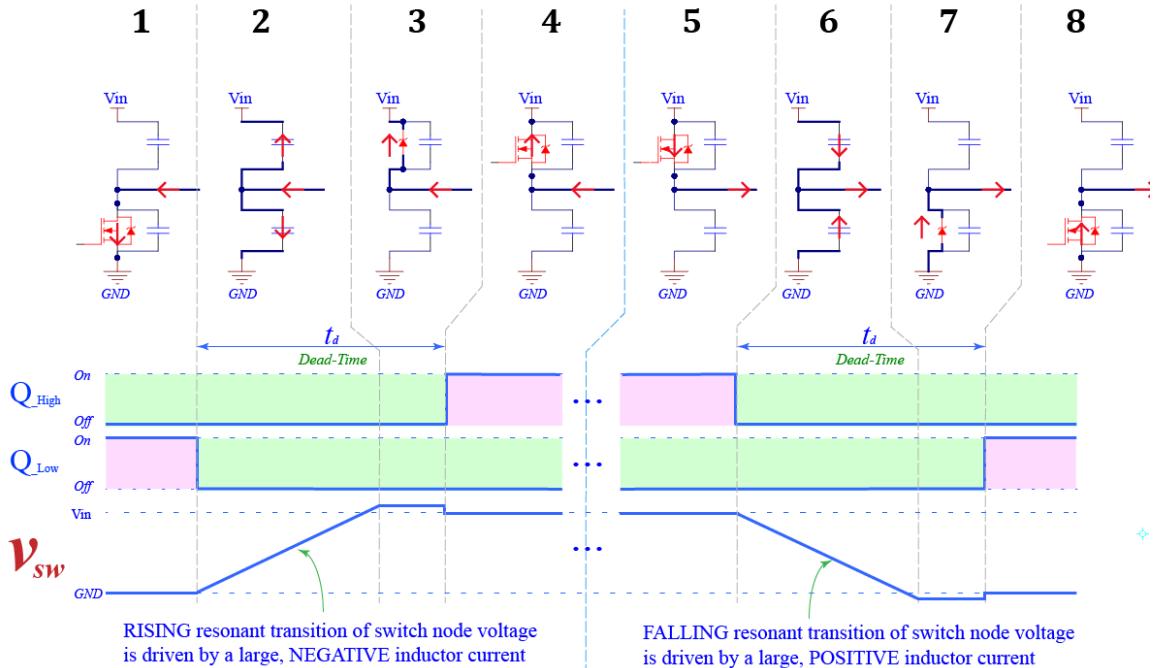


Fig. 14. Resonant transition zero voltage switching of a half-bridge. The **rising resonant transition** of v_{sw} is driven by a large, **negative** inductor current i_L ; and the **falling resonant transition** of v_{sw} is driven by a large, **positive** inductor current. In both situations, Mosfet is turned on with (almost) zero voltage across its Drain and Source terminals.

State 2: (During the rising transition) When the lower mosfet turns off, the current (which has negative direction at the moment) is forced to flow through its parasitic capacitor, charging this capacitor and discharge the parasitic capacitor of the other mosfet. As a result, the switch node voltage is rising as depicts in Fig. 14 (state 2).

This state ends when the switch node voltage reaches V_{in} . At this point in time, parasitic capacitor of the low mosfet is completely charged and that of the high mosfet is completely discharged. (Note that the voltage transition happens quickly, so it can be approximated as a straight line (Fig. 14). Later sections will discuss the general case when the voltage transition happens slower and the transition looks like an S curve because the non-linearity of mosfets output parasitic capacitance)

State 3: (Diode conduction) When the switch node voltage reaches V_{in} , body diode of the high mosfet begins to conduct (forward bias). During this state, voltage across the

high mosfet is its body diode's forward voltage drop, which is usually from 1.2 volts up to more than 3 volts! (Body diode conduction loss is high compare to mosfet conduction loss, Fig. 12; so a high efficiency/high frequency converter avoids this state).

This state ends when the high mosfet is turned on.

State 4: (Mosfet conduction) In this state, the high mosfet is fully on. If it stays on for long enough, the input voltage will force the inductor current to change direction.

This state ends when the inductor current changes from negative to positive direction.

State 5: (Before the falling transition) In this state, the inductor current has positive direction and keeps increasing until its magnitude is large enough for the falling resonant transition condition (i.e. equation (3)).

This state ends when the high mosfet is turned off to start the falling resonant transition.

The falling resonant transition happens similarly to the rising resonant transition. Comparable analysis can be applied to State 6, 7, 8 to explain the falling resonant transition.

4.2.1. Inductor's voltage and current waveforms (v_L, i_L)

In power converter, the switch node voltage (v_{SW}) changes periodically between ground (GND) and V_{in} . Inductor's voltage and current waveforms can be derived from the switch node voltage by applying Kirchhoff's voltage law to the buck converter in Fig. 13:

$$v_L = v_{SW} - V_{out} \quad (4)$$

Inductor current changes according to its voltage:

$$v_L = L \frac{di_L}{dt} \quad (5)$$

With (4) and (5) we can draw the inductor's voltage and current waveform from the switch node voltage v_{SW} , which change periodically between ground (GND) and V_{in} (Fig. 15).

Intuitively, (4) states that when v_{SW} changes from zero to V_{in} , v_L changes from $(-V_{out})$ to $(V_{in}-V_{out})$. And (5) states that the inductor voltage v_L controls how fast its current changes. For example, with a constant positive voltage applied to the inductor ($v_L > 0$), the inductor current increases linearly (a straight line); and with negative constant voltage($v_L < 0$) current decreases linearly. During the transition time, where v_L is not constant, the inductor current is hard to reckon; therefore it is approximated (Fig. 17).

4.2.2. Peak-to-peak value of the inductor current in a special case

Consider the buck converter in Fig. 13, assuming a special case when the transition time is small enough to be neglected (Fig. 16) (this is the case that [69] and many other papers assume). The peak-to-peak value of the inductor current is calculated based on (4) and (5):

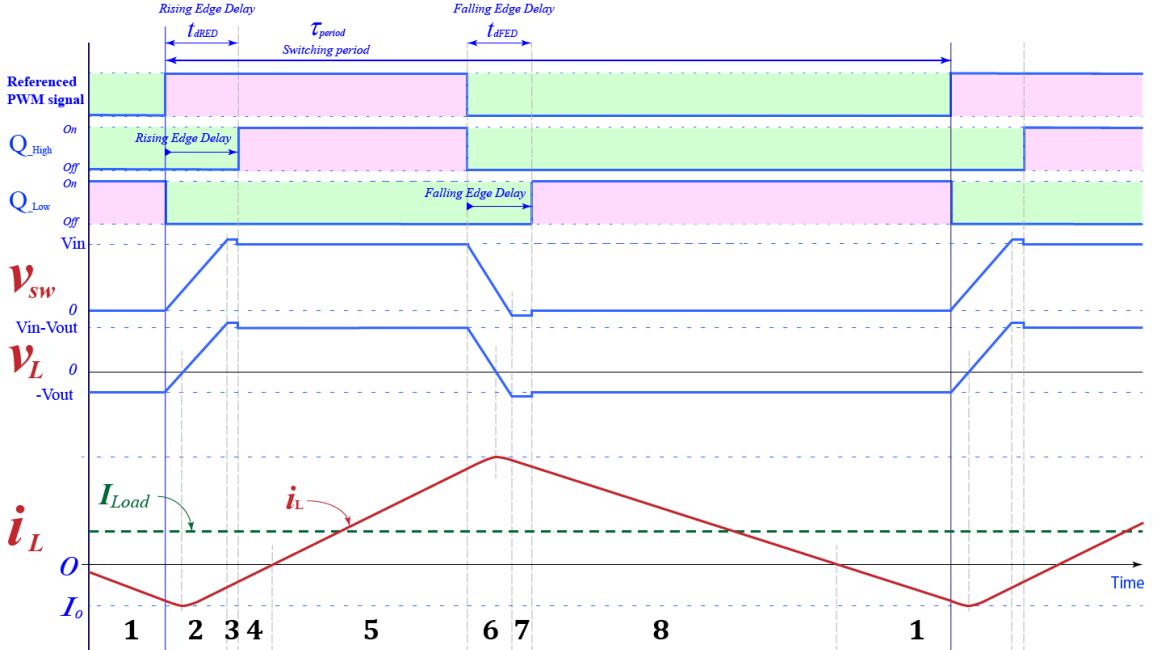


Fig. 15. Voltage and current waveforms of a buck converter operating under ZVS. Inductor current (i_L) is peak when its voltage (v_L) crosses zero during resonant transition states (2 and 6)

$$\begin{cases} v_L = v_{SW} - V_{out} \\ v_L = L \frac{di_L}{dt} \end{cases}$$

In Fig. 16, during the on-time, we have $v_{SW} = V_{in}$, therefore:

$$\begin{aligned} & \begin{cases} v_L = v_{in} - V_{out} \\ v_L = L \frac{di_L}{dt} \end{cases} \\ \Leftrightarrow & L \frac{di_L}{dt} = V_{in} - V_{out} \\ \Leftrightarrow & di_L = \frac{V_{in} - V_{out}}{L} dt \\ \Leftrightarrow & i_L = \frac{V_{in} - V_{out}}{L} \int_0^t dt \\ \Leftrightarrow & i_L = \frac{V_{in} - V_{out}}{L} t + I_{L0} \quad (6) \end{aligned}$$

with I_{L0} is the initial value of i_L (at $t=0$, i.e. the beginning of a switching cycle); and $t \leq D\tau_{period}$ (We're focusing on the on-time only. Similar analysis for the off-time will give same result)

The peak-to-peak value of the inductor current (Fig. 16) can be calculated as:

$$\begin{aligned} I_{Lpk2pk} &= i_L(D\tau_{period}) - i_L(0) = \left(\frac{V_{in} - V_{out}}{L} D\tau_{period} + I_{L0} \right) - \left(\frac{V_{in} - V_{out}}{L} (0) + I_{L0} \right) \\ I_{Lpk2pk} &= \frac{V_{in} - V_{out}}{L} D\tau_{period} = \frac{V_{in} - V_{out}}{Lf} D \end{aligned} \quad (7)$$

Note that peak-to-peak value of the inductor current (7) does not depend on load. Although the conclusion is based on a special case, where the transition time is negligible, it holds true for case that is more general. In a more general case, the ripple current (I_{Lpk2pk})

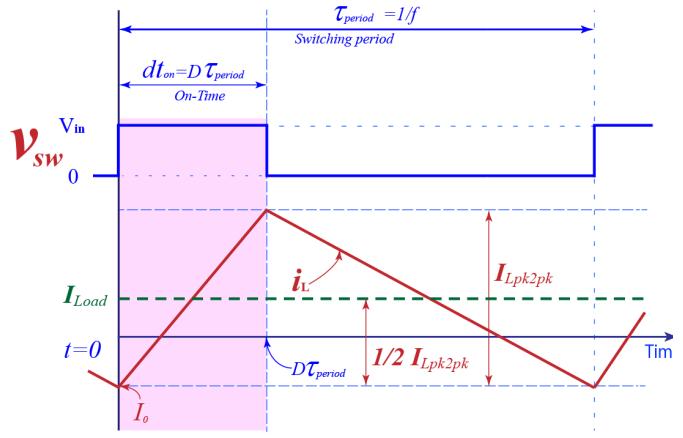


Fig. 16. Inductor peak-to-peak current in buck converter operating under ZVS. In a special case, the peak-to-peak value doesn't depend on load current.

depends slightly on load. Therefore, we can consider it is controlled by inductance, input/output voltage, switching frequency and duty cycle.

4.2.3. Output current or load current (I_{Load})

In steady state operation, output voltage (V_{out}) and current (I_{Load}) of a buck converter (Fig. 13) is constant during a switching period. With ideal LPF, the output current (I_{Load}) is the DC component of the inductor current waveform Fig. 15. From Fourier analysis, DC component of a periodic waveform is its average value:

$$I_{Load} = \frac{1}{T} \int_0^T i_L(t) dt \quad (8)$$

In Fig. 15, I_{Load} is the average line in the center of the i_L waveform.

When I_{Load} changes, the waveform of i_L shifts up or down (Fig. 17) to satisfy (8).

With the special case in Fig. 16 (where the transition time is small enough to be neglected), the averaging can be expressed as:

$$I_{Lpk2pk} = 2(I_{Load} - I_{L0}) \quad (9)$$

$$\Leftrightarrow I_{L0} = I_{Load} - \frac{1}{2} I_{Lpk2pk} \quad (10)$$

Where I_{L0} is the initial value of i_L (at $t=0$, the beginning of a switching cycle);

4.2.4. Operating a half-bridge under ZVS

According to the traditional ZVS condition [68], [69], I_{L0} must have negative direction at the beginning of the rising ZVRT, and positive direction at the falling ZVRT. Consider a situation when load is too heavy Fig. 17, I_{L0} may loss negative direction for rising ZVRT. In

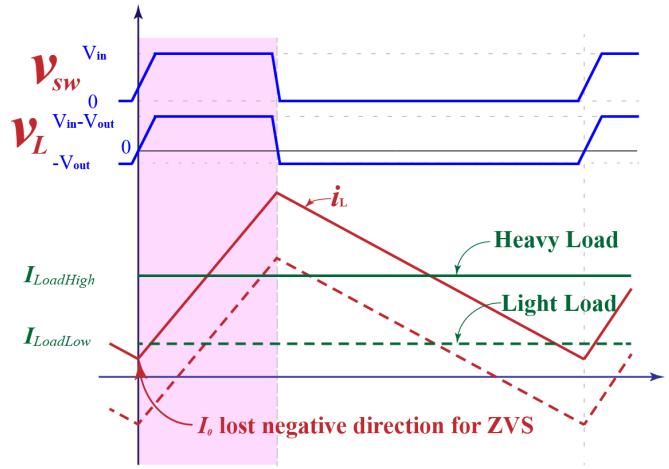


Fig. 17 An increases in I_{Load} shifts the i_L waveform up.

When load current is too high, ZVS is lost because i_L doesn't have negative value for rising resonant transition.

this case, the rising edge of switch node voltage is hard-switching. (Same conclusion can be drawn from (10): I_{L0} is positive when $I_{Load} > \frac{1}{2}I_{Lpk2pk}$)

To ensure ZVRT happens under heavy load, inductor current, i_L , must have large peak-to-peak value. Since the inductor peak-to-peak current stays the same for all loads (from 4.2.2), core loss and conduction loss also stay the same. As a result, a ZVRT converter designed for large load will have poor efficiency under light load because of unnecessarily large inductor ripple current always present.

4.2.5. General case analysis of Zero voltage resonant transition (ZVRT) in a buck converter

The traditional analysis of ZVRT [68] assumes that the inductor current is the only factor contributes to the rising/falling ZVRT (Fig. 14 state 2 and 6). But in fact, the output voltage (V_{out}) plays a significant role in ZVRT. A large output voltage is enough to make the rising resonant transition happen successfully; even when the inductor current is zero, where (3) (the condition in [68]) is not met. A correct ZVRT condition for buck converter must include the contribution of the output voltage (V_{out}).

Consider a buck converter in Fig. 13 and its rising resonant transition in Fig. 14 state 2. The output voltage across the output capacitor is constant during the transition, so it can be modelled as a voltage source. During the rising resonant transition, both mosfets are off. The equivalent circuit is shown in Fig. 18(a). (with disregarding circuit's resistance for now.)

Applying superposition principle, current/voltage values of the circuit in Fig. 18(a) equal to the sum of those of the three circuit in Fig. 18 (b), (c), (d) [with (b), (c) has initial condition zero, and (d) has the initial condition of the original circuit (a).]

The circuit in Fig. 18(b) is an open circuit. With zero initial condition, nothing happens:

$$\begin{cases} v_{swb}(t) = 0 \\ i_{Lb}(t) = 0 \end{cases} \quad (11)$$

The circuit in Fig. 18(c) and (d) is under damped second order system, whose response has the form: $x = e^{\alpha t} [ACos(\omega_0 t) + BSin(\omega_0 t)]$; ($\alpha = 0$ in this case because $R = 0$)

With zero initial condition, the circuit in Fig. 18(c) has a solution:

$$\begin{cases} v_{SWc}(t) = V_{out}(1 - \cos(\omega_0 t)) \\ i_{Lc}(t) = -V_{out} \sqrt{\frac{L}{2C_p}} \sin(\omega_0 t) \end{cases} \quad (12)$$

With $\omega_0 = \sqrt{\frac{1}{2LC_p}}$

Now, consider the rising resonant transition (Fig. 14 State 2), which has an initial condition:

$$\begin{cases} v_{SW}(0) = 0 \\ i_L(0) = I_{L0} \end{cases} \quad (13)$$

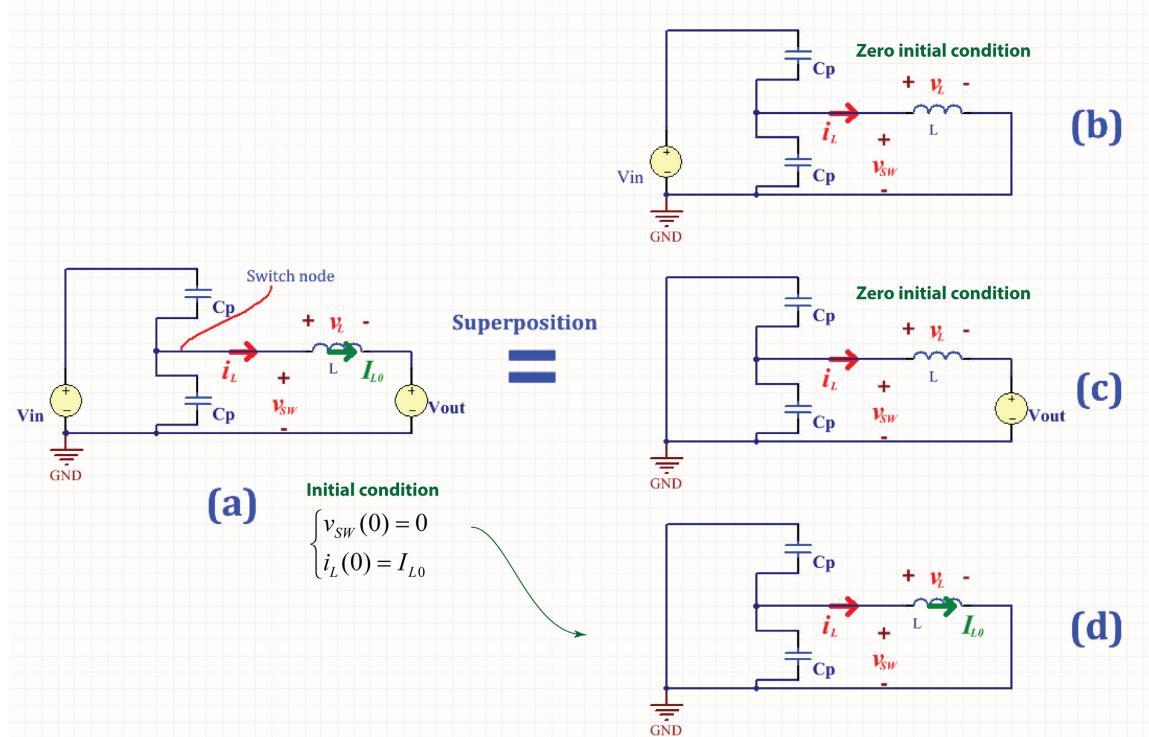


Fig. 18 (a) The equivalent circuit of the rising resonant transition in buck converter (b), (c), (d) applying superposition principle to solve for voltage/current.

The circuit in Fig. 18(d) with the initial condition (9) has a solution:

$$\begin{cases} v_{SWd}(t) = I_{L0} \sqrt{\frac{L}{2C_p}} \sin(\omega_0 t) \\ i_{Ld}(t) = -I_{L0} \cos(\omega_0 t) \end{cases} \quad (14)$$

From (11), (12), (14), the total solution is:

$$\begin{cases} v_{SW}(t) = V_{out} - V_{out} \cos(\omega_0 t) + I_{L0} \sqrt{\frac{L}{2C_p}} \sin(\omega_0 t) \\ i_L(t) = -V_{out} \sqrt{\frac{L}{2C_p}} \sin(\omega_0 t) - I_{L0} \cos(\omega_0 t) \end{cases} \quad (15)$$

$$\text{With } \omega_0 = \sqrt{\frac{1}{2LC_p}}$$

The resonant transition is successful when $v_{SW}(t)$ can rise up to V_{in} . In other words:

$$\text{Max}(v_{SW}(t)) \geq V_{in} \quad (16)$$

From (15):

$$v_{SW}(t) = V_{out} - V_{out} \cos(\omega_0 t) + I_{L0} \sqrt{\frac{L}{2C_p}} \sin(\omega_0 t) \quad (17)$$

$$v_{SW}(t) = V_{out} + \sqrt{V_{out}^2 + I_{L0}^2 \frac{L}{2C_p}} \sin(\omega_0 t + \varphi) \quad (18)$$

$$\text{With } \tan \varphi = -\frac{I_{L0}}{V_{out}} \sqrt{\frac{L}{2C_p}}$$

With (16) and (18), the condition for ZVRT is:

$$\text{Max}(v_{SW}(t)) = V_{out} + \sqrt{V_{out}^2 + \frac{L}{2C_p} I_{L0}^2} \geq V_{in} \quad (19)$$

When $V_{out} = 0$, the general condition (19) becomes the traditional condition (3).

Note that when $V_{out} \geq \frac{1}{2}V_{in}$ and $I_{L0} = 0$, the condition (19) is satisfied but the condition (3) is not. The question is which condition is correct. Simulation result in Fig. 19 confirms that the rising resonant transition happens successfully in this case. This means that (3) is not correct when the output voltage has large effect on the ZVRT; and that the condition (19) is a more general case of (3).

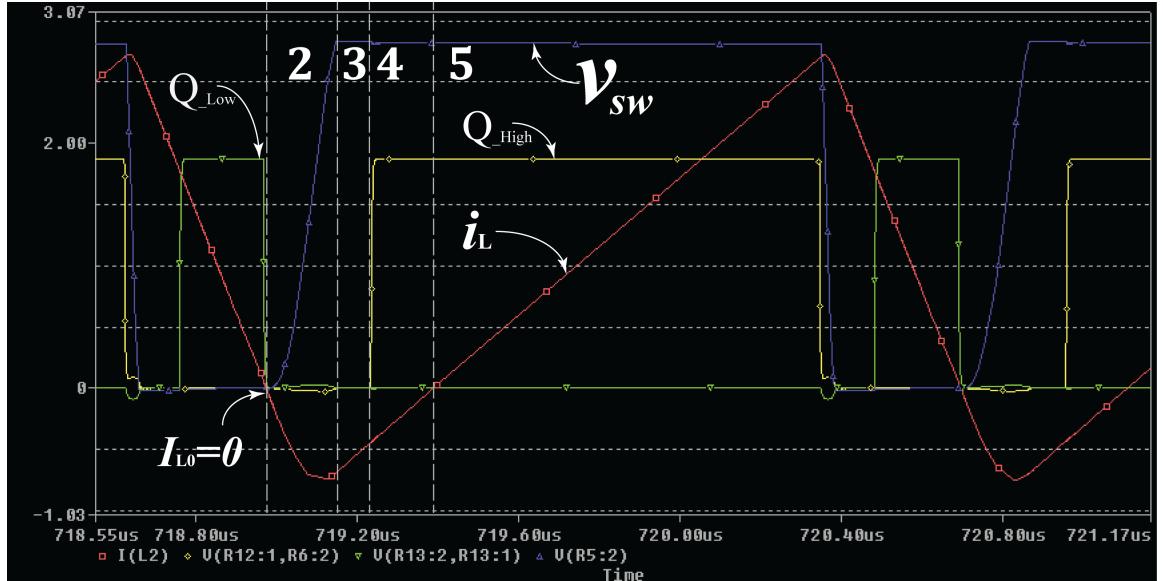


Fig. 19 Simulation confirms that when $V_{out} \geq \frac{1}{2}V_{in}$ the rising ZVRT happens successfully at $I_{L0} = 0$, where the traditional ZVRT condition [48] is not satisfied.

Since it is impractical to sense I_{L0} in a high frequency converter, we substitute (10) into (18)

$$v_{sw}(t) = V_{out} + \sqrt{V_{out}^2 + (I_{Load} - \frac{1}{2}I_{Lpk2pk})^2 \frac{L}{2C_p}} \sin(\omega_0 t + \varphi) \quad (20)$$

I_{Load} is (in theory) constant during a switching cycle. Therefore, it is much easier to sense.

Chapter 5

Proposed optimal control method for loss reduction in high-frequency ZVRT converters

5.1 Introduction

As discussed in 4.1, root causes for losses in ZVRT buck converter are high inductor ripple current, and the conduction of mosfets' body-diode. Existing loss optimization techniques [48]–[53], [54]–[67], focus on a single direction, therefore achieve sub-optimal results.

Experimentally, by manual tuning using an oscilloscope, we can bring a ZVRT buck converter to the true optimal point, where loss is lowest. Fig. 20 shows a waveform of a ZVRT buck converter after manual tuning to achieve lowest lost. Tuning was done to minimize both inductor ripple current and mosfets' body diode conduction. In Fig. 20, mosfet is turned on right when its drain-source voltage reach zero (state 1 and 3 is eliminated); and because of low inductor ripple current, the rising ZVRT follows an S curve (instead of a straight line) and take a large portion of a switching period. The falling ZVRT is faster than the rising ZVRT because load current increases the positive peak inductor current, which drives the falling ZVRT. The efficiency, in this case, is $\sim 99\%$ at switching frequency 781 KHz.

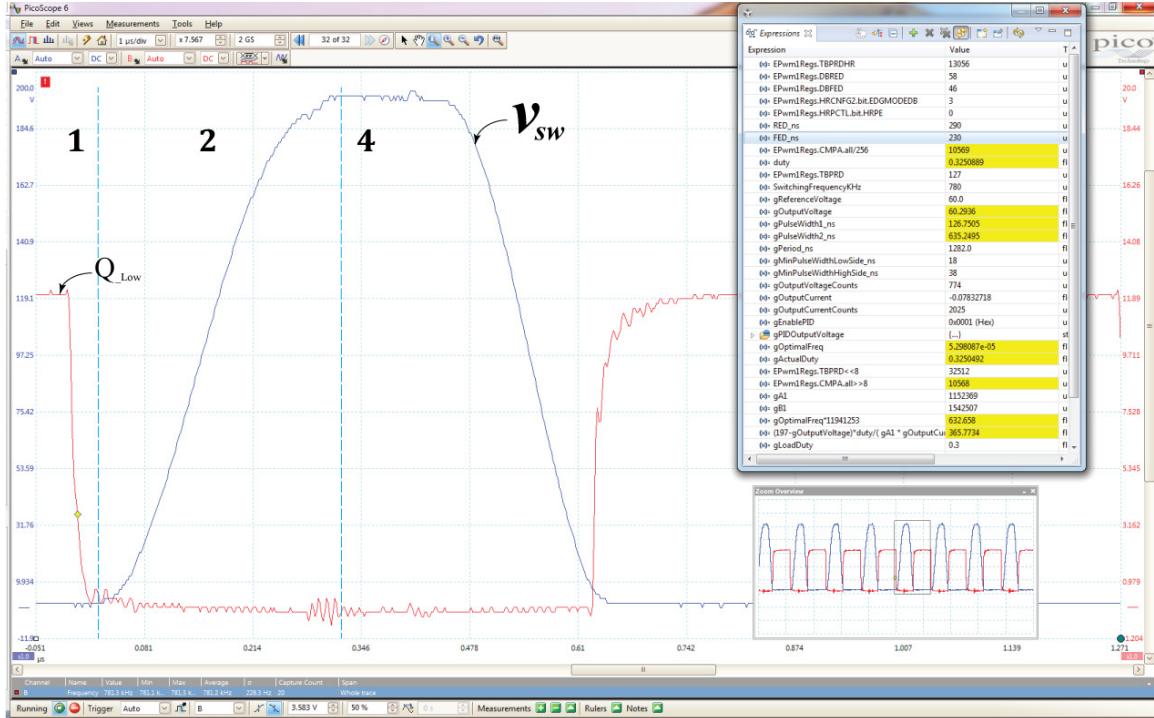


Fig. 20 An experimental ZVRT buck converter operating at optimal operating point, where loss is lowest. A change in load or input voltage moves the optimal operating point. It is desirable that the converter tracks the optimal operating point automatically.

With some approximations, (18) tells us about the rising resonant curve. However, the equation is too complicated to be practically calculated inside a microcontroller, which often cannot afford double-precision floating-point calculation. Single-precision floating-point calculation, which is usually available in a microcontroller, would result in unacceptable large error with complicated equations, such as (18).

5.1.1. Overview of the proposed optimal control method

A simplified method based on curve fitting is developed to calculate the exact optimal operating point. In essence, the method assumes optimal operating point, and tries to calibrate (by curve fittings) the converter to this optimal operating point, with guidance of (18). Experimental results showed the effectiveness of the method.

Fig. 21 shows naming conventions. The “referenced PWM signal” is generated by PWM module inside a microcontroller. To generate the referenced PWM signal, this module takes

two input: switching period (T_{period}), and on-time (t_{on}). Based on this referenced PWM signal, the control signals for the high and low mosfets ($Q_{\text{High}}/Q_{\text{Low}}$) are generated as depicts in Fig. 21. Rising edge delay (REDns) and falling edge delay (FEDns) are the dead-band (or dead-time) during which both mosfets are off. Ideally, REDns should be the time required for the rising ZVRT to complete and FEDns should be the time required for the falling ZVRT to complete. Inside a microcontroller, REDns, FEDns can be set to arbitrary values. In summary, to generate PWM driving signal for the high and low mosfets, the PWM Module needs: period (T_{Period}), on-time (t_{on}), falling edge delay (FEDns), and rising edge delay (REDns).

When the switching frequency is high, it becomes impractical to sense the switch node voltage (v_{sw}) and inductor current (i_L). Therefore, the proposed optimal control method based on other parameters that are constant during a switching period: (a) load current (I_{Load}), (b) input voltage (V_{in}), (c) and output voltage (V_{out}). I_{Load} and V_{out} directly control the rising/falling ZVRT curve, according to (20). V_{out} is the peak that the switch node voltage must rise to in order to complete the ZVRT. Therefore, it indirectly affect the rising/falling time.

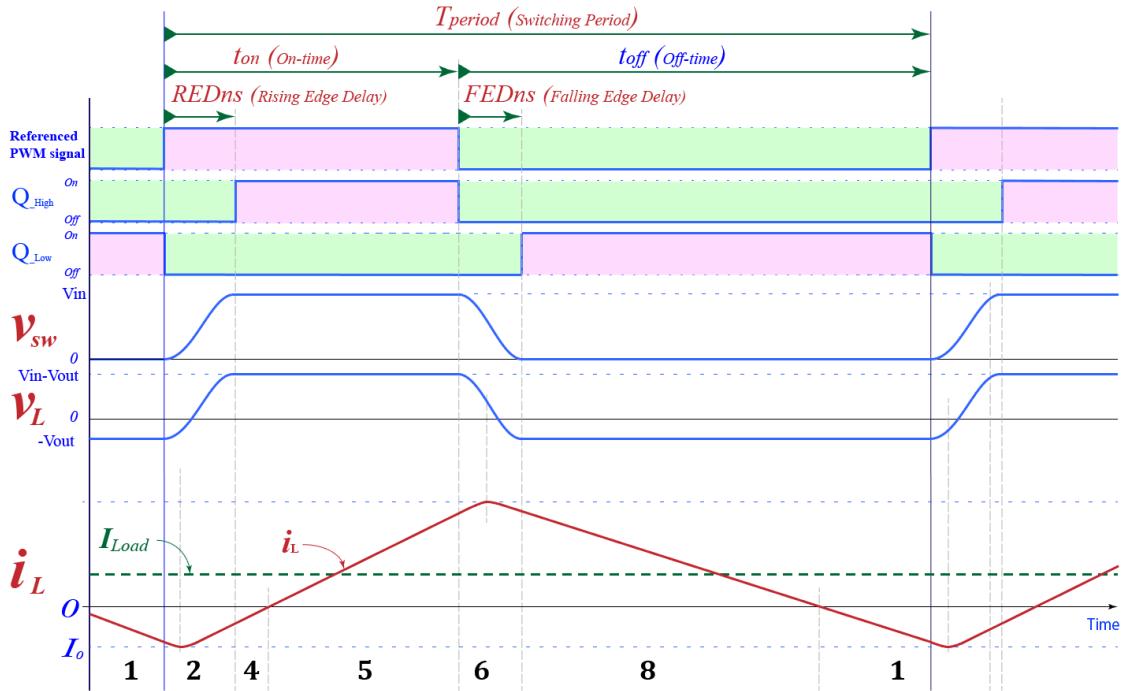


Fig. 21 Waveform of ZVRT in a buck converter with naming convention for the discussion in this section.

Block diagram of the proposed control method is shown in Fig. 22. An optimal operating point (i.e. parameters required to generate PWM waveform in Fig. 21) comprises switching period (T_{Period}), on-time (t_{on}), FEDns, and REDns. These values are written to the PWM module inside a microcontroller for PWM generation.

Calibrations are done at fixed V_{out} and V_{in} . Some example are: $(V_{\text{in}}, V_{\text{out}}) = (200\text{V}, 10\text{V})$, $(V_{\text{in}}, V_{\text{out}}) = (200\text{V}, 20\text{V})$; $(V_{\text{in}}, V_{\text{out}}) = (200\text{V}, 30\text{V})$, $(V_{\text{in}}, V_{\text{out}}) = (200\text{V}, 40\text{V})$, etc. Calibration should be done at all possible operating points that the converter may operate at.

From (18), with a fixed V_{out} , I_{L0} will control the ZVRT curve. At (or near) optimal operating point, inductor ripple current has a lowest value (lowest inductor ripple current is a target that the control method trying to achieve). Therefore, I_{L0} has lowest value (according to (10)). We want to keep I_{L0} at this lowest value. In other words, I_{L0} is considered a constant at the optimal operating point that we selected (or try to calibrate the converter to). Note that, when calibrating the converter, we don't want to push I_{L0} to the lowest possible value. Instead, we keep a safety gap to account for any error that may arise and move the converter to hard-switching region. So I_{L0} is fixed at near the optimal value.

According to (18), when I_{L0} and V_{out} are fixed, the rising resonant curve is fixed. Therefore, the rising edge delay (REDns) is fixed. This conclusion is important for curve fittings. We want to keep as many variable fixed as we can to simplify the relationship. However, the number of calibration cases (that we have to do) increase exponentially with the number of the variable that we fixed. Therefore, a trade-off was made.

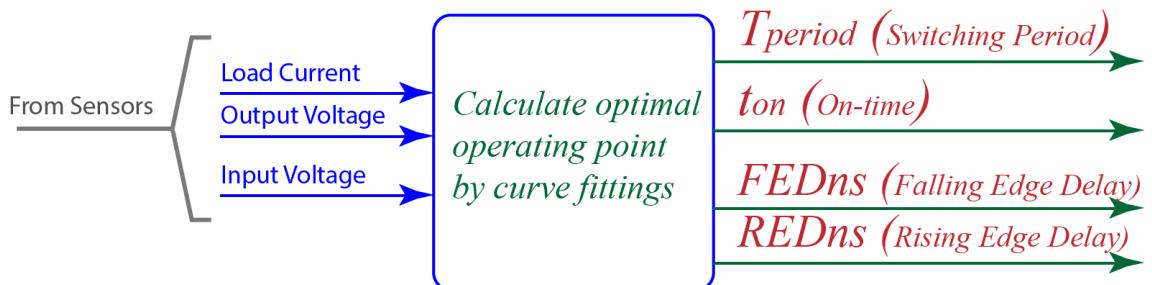


Fig. 22 Block diagram of the proposed control method.

For example, with the circuit in Chapter 6, all calibrations are done with a fixed REDns = 289ns, fixed V_{out} , V_{in} (only I_{load} changes). Larger rising edge delay is possible but has little effect on loss reduction. Much smaller rising edge delay results in high loss due to large inductor ripple current required to enable a quick ZVRT. REDns = 289ns seems to be a good (though not optimal) rising edge delay in all cases, experimentally.

Note that the primary reason to keep REDns at a constant value for all (V_{in} , V_{out}) is simplicity. So that calibration can be completed in a short amount of time with acceptable accuracy. The real optimal value of REDns changes with output voltage because output voltage contributes significantly to the ZVRT (according to (18)). Experiments showed that the current solution is good with a constant REDns for all output voltage. For sure, calibrating the converter to the real optimal REDns will improve efficiency and power density further.

5.1.2. Calibrating and Calculating the on-time (t_{on})

In Fig. 21, notice that the inductor current rises linearly during the on-time (t_{on}). In other words, the on-time directly control the inductor ripple current. The inductor ripple current is approximate according to (7):

$$I_{Lpk2pk} \approx \frac{V_{in} - V_{out}}{L} t_{on} \quad (21)$$

Now, substitute (9) in to (21), we have:

$$2(I_{Load} - I_{L0}) \approx \frac{V_{in} - V_{out}}{L} t_{on} \quad (22)$$

$$\Leftrightarrow t_{on} \approx \frac{2L(I_{Load} - I_{L0})}{V_{in} - V_{out}} \quad (23)$$

With fixed I_{L0} , (23) can be simplified as:

$$t_{on} * (V_{in} - V_{out}) \approx aI_{Load} + b \quad (24)$$

$$t_{on} \approx \frac{aI_{Load} + b}{(V_{in} - V_{out})} \quad (25)$$

(24) is used for calibration which estimate the constant a and b using curve fitting. (25) is used to calculate the on-time (t_{on}) inside a microcontroller.

Fig. 23 shows optimal operating points calibrated at: $V_{in} = 200V$; $V_{out} = 155V$; $REDns = 289ns$. Fig. 24 shows optimal operating points calibrated at: $V_{in} = 200V$; $V_{out} = 120V$; $REDns = 289ns$. Calibration is done manually using an oscilloscope with the circuit in Chapter 6.

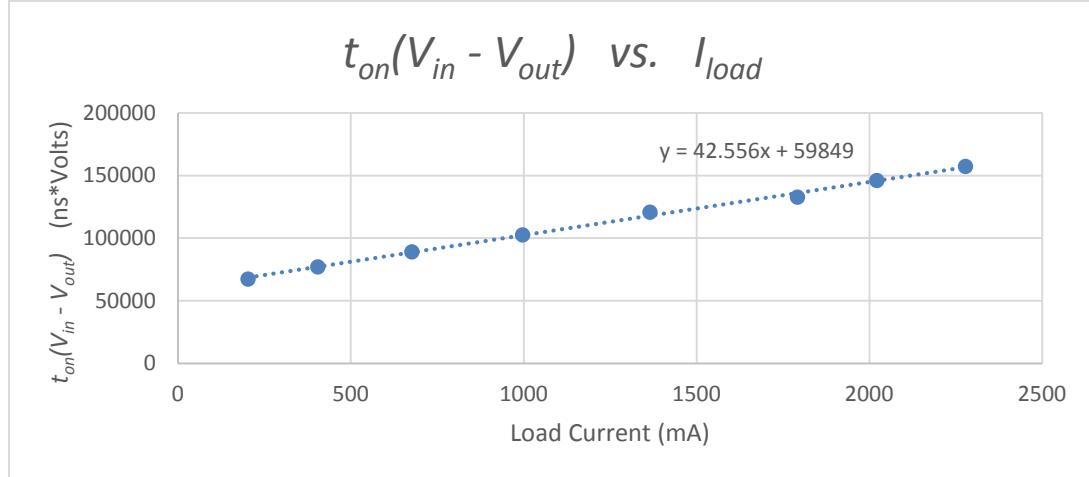


Fig. 23 optimal operating points at: $V_{in} = 200V$; $V_{out} = 155V$; $REDns = 289ns$.

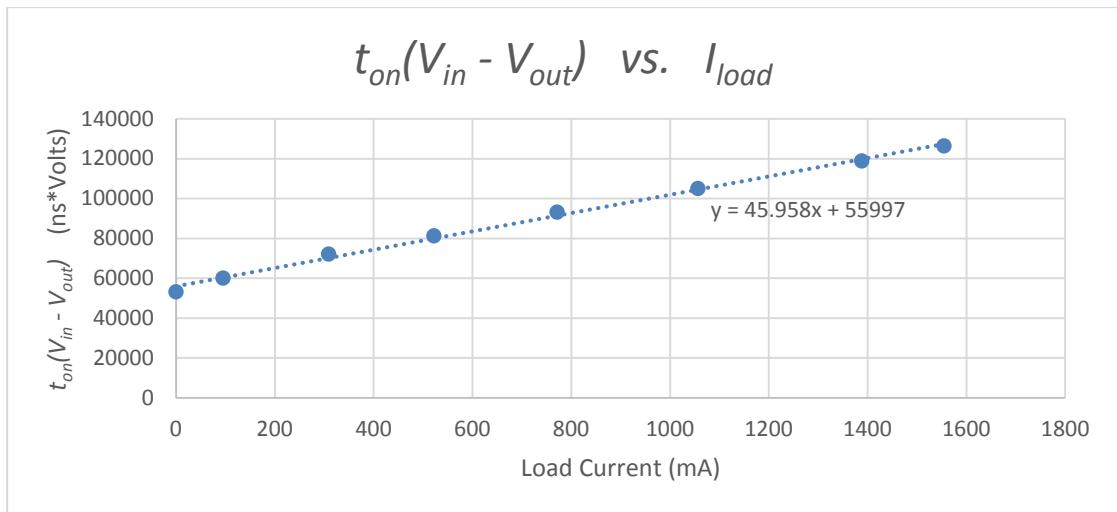


Fig. 24 optimal operating points at: $V_{in} = 200V$; $V_{out} = 120V$; $REDns = 289ns$.

5.1.3. Calibrating and Calculating the falling edge delay (FEDns) and rising edge delay (REDns)

Falling/rising edge delays are to make sure mosfets' body diodes do not conduct. As discussed previously, the rising edge delay is kept constant ($REDns = 289ns$) in all calibrations

for simplification. The falling edge delay depends on the positive peak value of the inductor current, which in turns, depends on load current. A 3rd order polynomial curve is used to approximate the falling edge delay based on load current (I_{load}).

$$\begin{cases} FEDns \approx cI_{Load}^3 + dI_{Load}^2 + eI_{Load} + g \\ REDns \approx h \end{cases} \quad (26)$$

Fig. 25 shows optimal operating points calibrated at: $V_{in} = 200V$; $V_{out} = 155V$; $REDns = 289ns$. Fig. 26 shows optimal operating points calibrated at: $V_{in} = 200V$; $V_{out} = 120V$; $REDns = 289ns$. Calibration is done by manually using an oscilloscope with the circuit in Chapter 6.

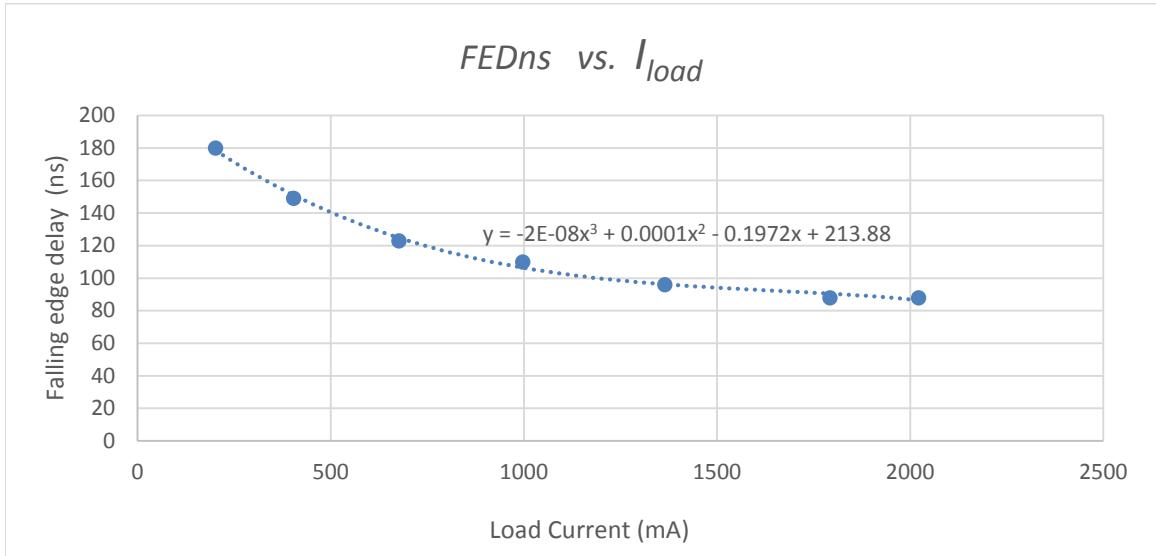


Fig. 25 Falling edge delay of optimal operating points. Calibration done at at: $V_{in} = 200V$; $V_{out} = 155V$; $REDns = 289ns$.

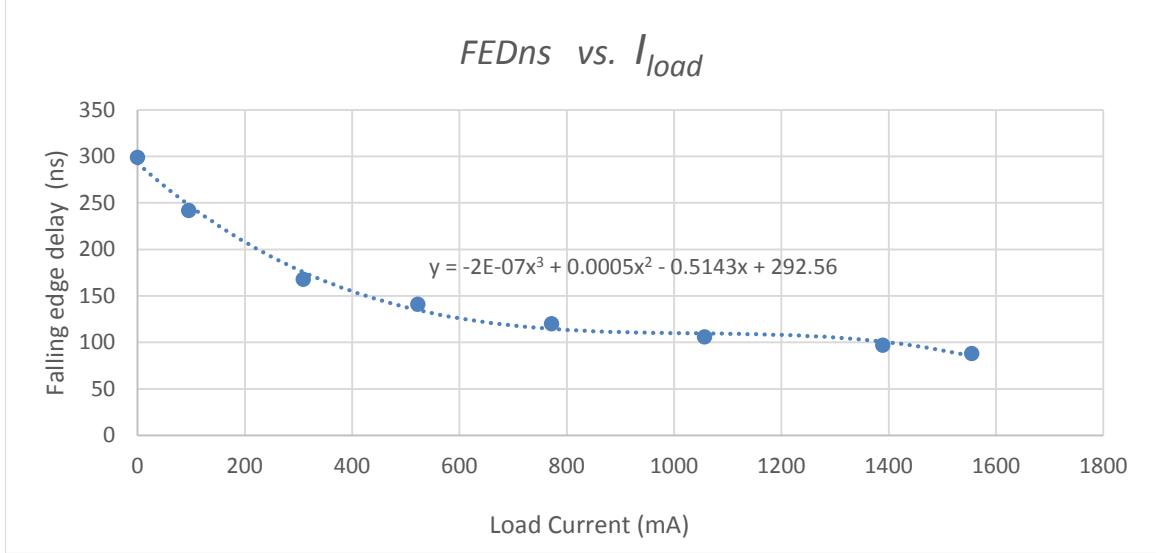


Fig. 26 Falling edge delay of optimal operating points. Calibration done at $V_{in} = 200V$; $V_{out} = 120V$; $REDns = 289ns$.

5.1.4. Calculate the switching period (T_{period})

The on-time is selected to make sure that the inductor ripple current is lowest. Rising/Falling edge delays are to prevent mosfets' body diodes conduction. Switching period is calculate to make sure that output voltage is at the desired set point. According to[16], output voltage of a buck converter is the average of the switch node voltage:

$$V_{out} = \frac{1}{T_{period}} \int_0^{T_{period}} v_{SW}(t) dt \quad (27)$$

In a period, the switch node voltage resonates from zero, to V_{in} , and back to zero. Fig. 27 shows a scope shot of the switch node voltage taken from an experimental circuit. The area below V_{sw} (red curve) is approximated as the area below the dashed green curve:

$$V_{out} = \frac{1}{T_{period}} \int_0^{T_{period}} v_{SW}(t) \approx \frac{1}{T_{period}} \left(t_{ON} - \frac{REDns}{2} + \frac{FEDns}{2} \right) V_{in} \quad (28)$$

$$T_{period} \approx \frac{V_{in}}{V_{out}} \left(t_{ON} - \frac{REDns}{2} + \frac{FEDns}{2} \right) \quad (29)$$

$$T_{period} \approx k \left(\frac{V_{in}}{V_{out}} (t_{ON} - \frac{REDns}{2} + \frac{FEDns}{2}) \right) + l \quad (30)$$

The constants k and l account for unit mismatch in the calculation.

Fig. 28 shows optimal operating points calibrated at: $V_{in} = 200V$; $V_{out} = 155V$; $REDns = 289ns$. Fig. 29 shows optimal operating points calibrated at: $V_{in} = 200V$; $V_{out} = 120V$; $REDns = 289ns$. Calibration is done by manually using an oscilloscope with the circuit in Chapter 6.

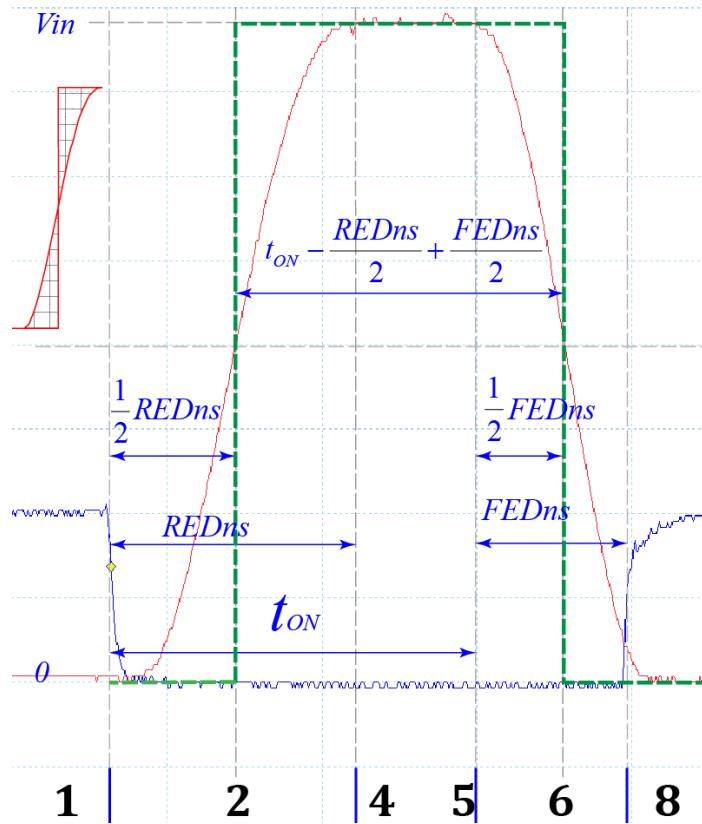


Fig. 27. A scope shot for output voltage calculation. V_{sw} (red curve) resonates from Zero to V_{in} . The area below V_{sw} (red curve) is approximated as the area below the dashed green curve.

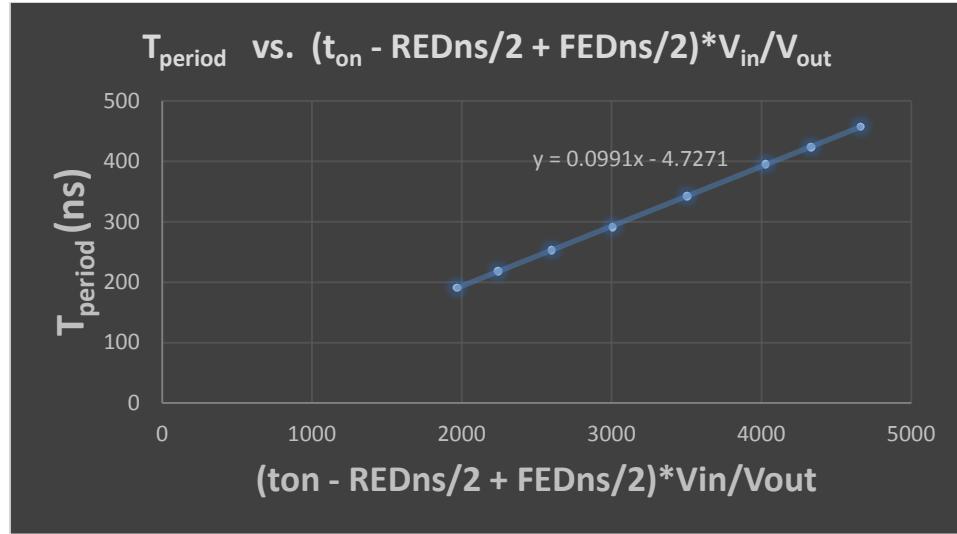


Fig. 28 Periods at optimal operating points.

Calibration done at: $V_{in} = 200V$; $V_{out} = 155V$; $REDns = 289ns$.

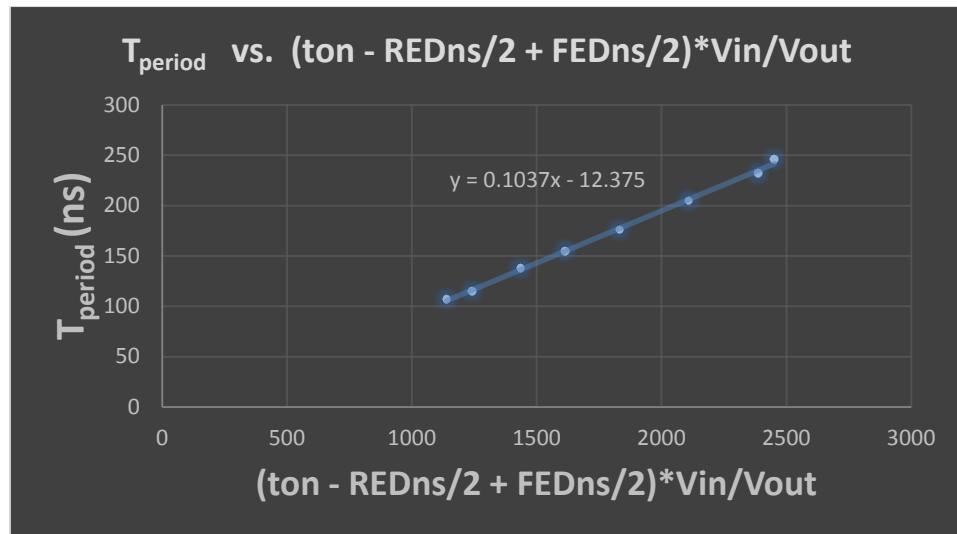


Fig. 29 Periods at optimal operating points.

Calibration done at: $V_{in} = 200V$; $V_{out} = 120V$; $REDns = 289ns$.

5.1.5. Proposed optimal control method for loss reduction

Fig. 30 shows the proposed optimal control method for loss reduction. The constants (a, b, c, d, e, g, k, l) are found by calibrations (at each input/output voltages).

The constant h, rising edge delay (REDns), represents the point that we want to calibrate the converter to. In other words, h is selected based on how near to the optimal operating

point that we want the converter to operate. For example, the inverter in Chapter 6 has REDns = h = 289ns. Experimental observations show a larger REDns has little improvement to efficiency but with trade-off for instability, because inductor current is too near the lowest value the converter may go into hard-switching region and totally disrupt all the calculations. On the other hand, a smaller REDns results in low efficiency because of large inductor ripple current.

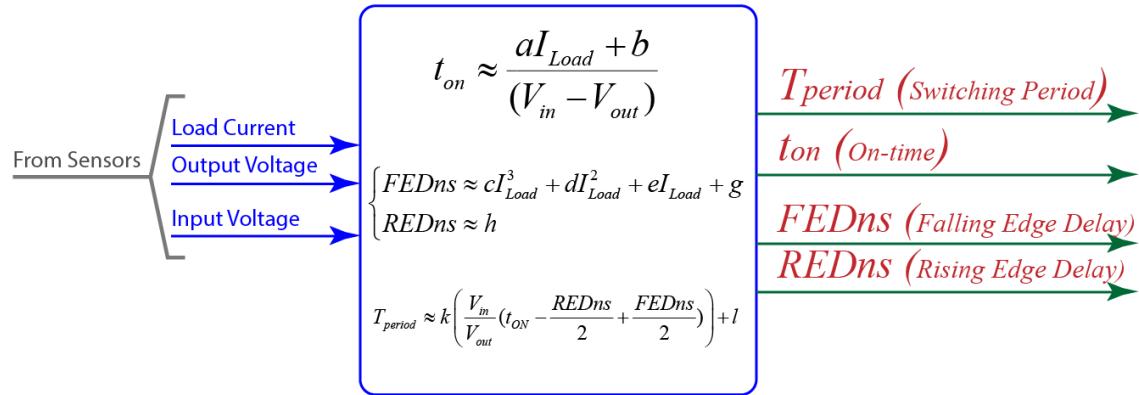


Fig. 30 Optimal control method for loss reduction based on calibration and curve fittings.

For DC-AC inverter where output voltage can be any point from zero to peak voltage. The constants are calibrated at each step-size from zero to peak. For example, with output 110VAC, the peak is 155V (110*1.4142~155V), then the constants are calibrated at, for example: 25V, 35V, 45V, 55V, ..., 155V. The smaller the step size is, the better the approximation and better efficiency but longer calibration time.

5.1.6. Experimental results with the proposed control method

This section shows some waveforms of an experimental converter after calibrations. Waveforms show that the converter tracks the optimal operating point surprisingly well when load changes. Load used in the experiment is a self-made controllable resistive load, which can be controlled to sink any desirable current.

In these figures, the red curve is the switch node voltage; the blue curve is gate voltage of the low mosfet. gLoadDuty (from 0.0 to 1.0) is the variable controlling load current; increase this variable will increase load current. gOutputCurrent (mA) is the output current measured from the onboard current sensor. gOutputVoltage, gInputVoltage are the output, input voltage

respectively, measured by the onboard voltage sensors. gReferenceVoltage is the desired set point for output voltage. gReferenceVoltage is set at a fix voltage for testing the control method. The final inverter will have gReferenceVoltage being changed sinusoidally.

The calculated efficiency is the efficiency of the power stage only. The real efficiency will be lower when we include the power loss that is consumed by other circuits such as: sensor, microcontroller, mosfet drivers, fan, etc.

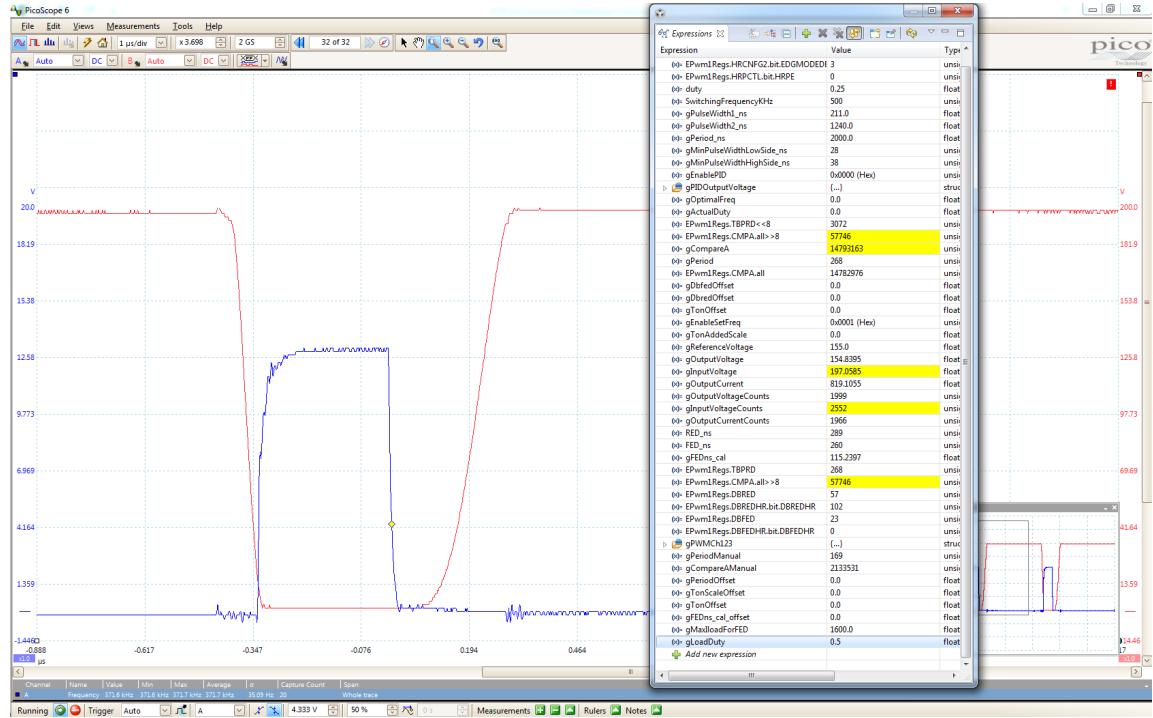


Fig. 31. Load test at $V_{in} = 200$, $V_{out} = 155$, $I_{load} = 0.81$, Efficiency $\sim 99.6\%$ at $f = 371$ KHz

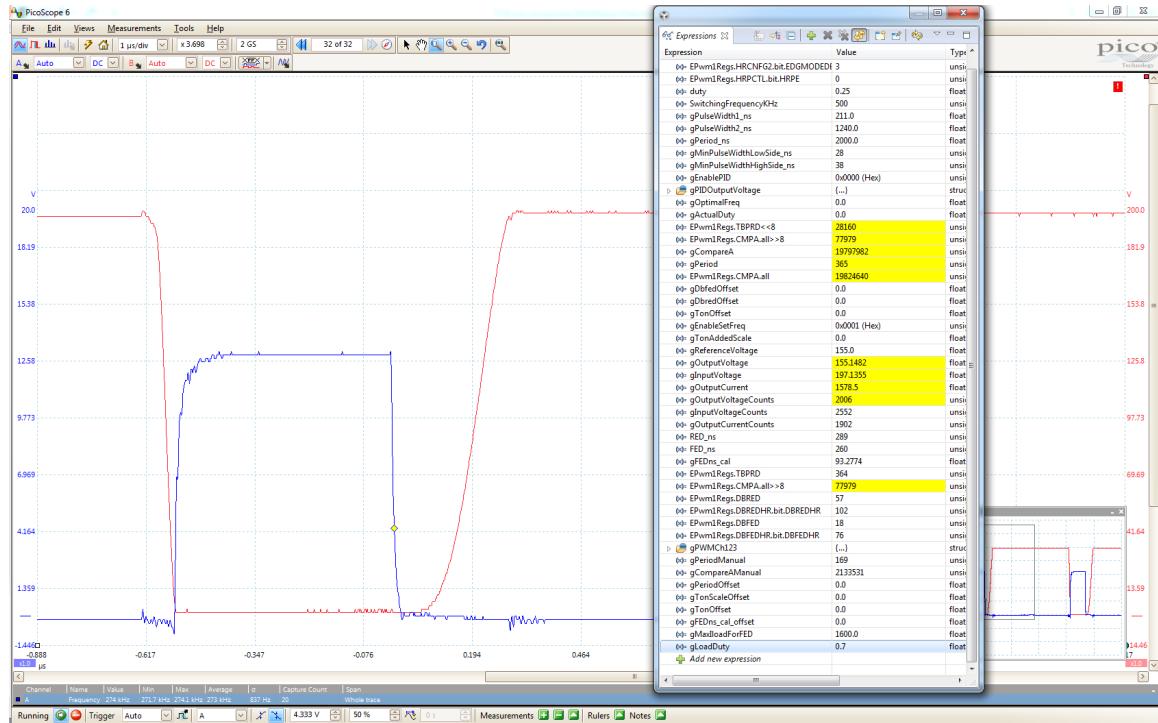


Fig. 32. Load test at $V_{in} = 200$, $V_{out} = 155$, $I_{load} = 1.56$. Efficiency $\sim 99.1\%$ $f=273\text{Khz}$

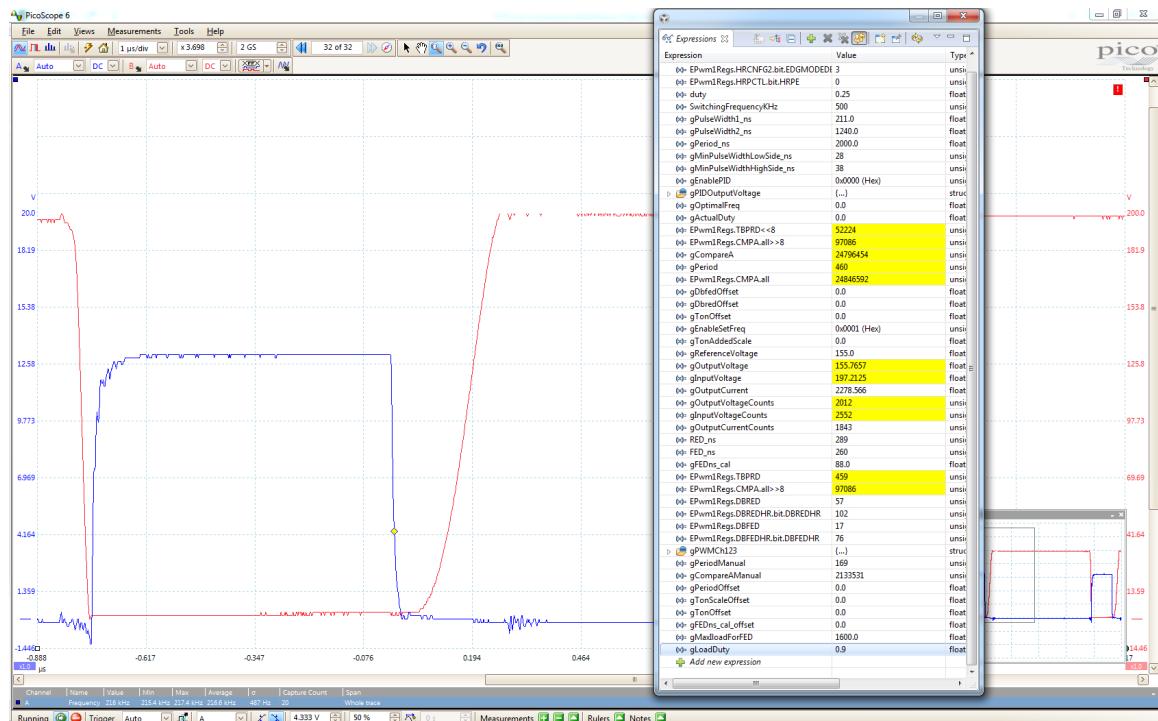


Fig. 33. Load test at $V_{in} = 200$, $V_{out} = 155$, $I_{load} = 2.26$; Efficiency $\sim 98.6\%$; $f=217\text{Khz}$

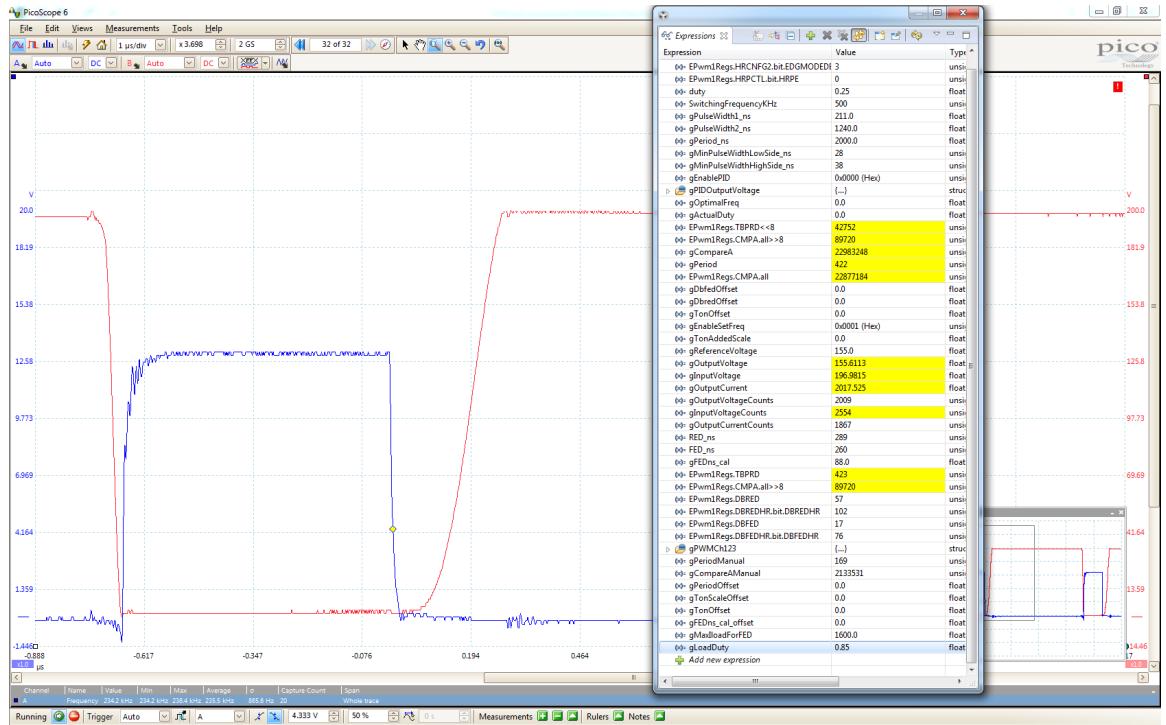


Fig. 34. Load test at Vin = 200, Vout = 155, Iload = 1.99 ; Efficiency ~98.5%; f=235Khz

Vin(V)	Iin (A)	Vout (V)	Iload (A)	Pin (W)	Pout (W)	Efficiency (%)
197.2	0.64	155.2	0.81	126.208	125.712	99.61
197.1	1.242	155.5	1.56	244.798	242.580	99.09
197.1	1.531	155.7	1.91	301.760	297.387	98.55
197.1	1.597	155.8	1.99	314.769	310.042	98.50
197.1	1.808	156	2.25	356.357	351.000	98.50
197.1	1.815	156.1	2.26	357.737	352.786	98.62
197.3	0.66	100.7	1.29	130.218	129.903	99.76

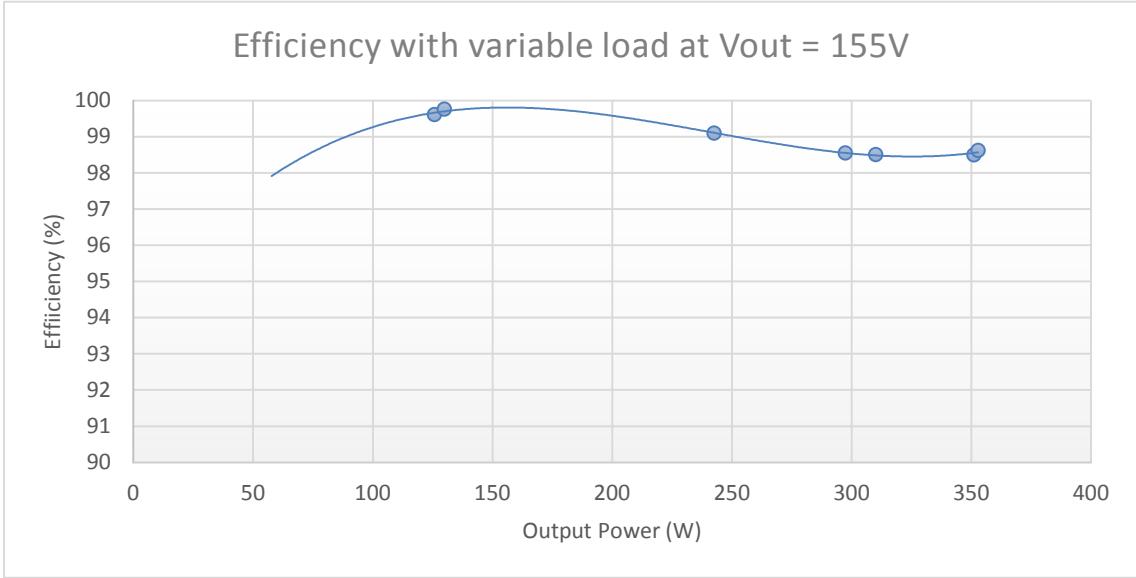


Fig. 35. Efficiency of the converter at Vin = 200V, Vout = 155V

5.1.7. Conclusion

Experimental results show the effectiveness of the proposed optimal control method. The power stage has high efficiency even at high switching frequency. For example, the case in Fig. 31, the efficiency measured 99.6% while the converter operating at 371 KHz.

As discussed earlier, to save time, the calibration was done with a fixed rising edge delay (REDns = 289ns) for all input/output voltages. In fact, the rising resonant curve depends on output voltage(18). Therefore, the optimal REDns may not be the same for all output voltage. Calibrating the converter to the true optimal REDns may give even better result.

One drawback of the proposed control method is that it requires long calibration time. However, calibration can be automated with artificial intelligence, machine learning, or other techniques. This is one of the recommended future directions.

Chapter 6

Inverter Design

6.1 Circuit Topology and Overview of the Inverter

Circuit topology of the inverter is shown in Fig. 36. It comprises three half-bridge (on the left of Fig. 36) soft-switching at high frequency with 120° phase-shifted to each other, and one half-bridge (on the right of Fig. 36) switching at line-frequency (i.e. 60Hz in US). Interleaved operation of the three high frequency half-bridge gives many benefits, such as: high efficiency, high power density, better control dynamics, lower EMI, and higher reliability [70]–[74].

The modulation is similar to [75]. In the positive part of the sinusoidal cycle of the output voltage, QA is off and QB is on. Therefore, voltage at node N is zero ($v_N=0$). The voltage at node L (v_L) is controlled, by the three high frequency half-bridge (on the left of Fig. 36) according to the optimal ZVS control method in Chapter 5, such that its value swings from zero to peak and back to zero, generating the positive half of the sinusoidal cycle (Fig. 37). Similarly, to generate the negative half of the sinusoidal cycle, QA is on and QB is off ($v_N=V_{in}$); the output voltage at node L (v_L) is controlled to swing from V_{in} to negative peak and back to V_{in} (Fig. 37) generating the negative half of the sinusoidal cycle.

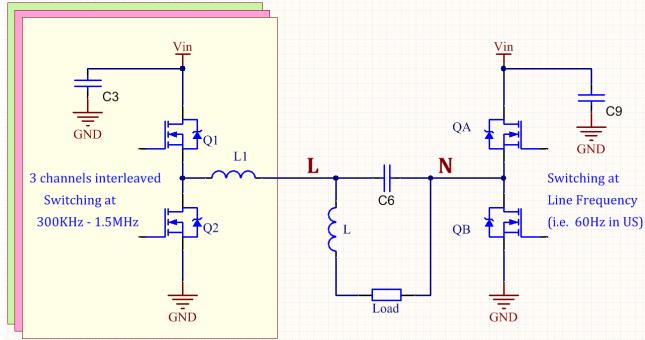


Fig. 36 Circuit topology.

Fig. 37 shows voltage waveforms. The PWM is shown according to the traditional PWM modulation method (not according to the new control method in Chapter 5) for illustration purpose only. In the actual circuit, since the left half-bridges of the inverter operate according to the optimal control method, as described in Chapter 5, the waveform of the switch node voltages are different from the traditional PWM modulation. One obvious difference is that

the switch-node voltage waveform of the inverter (in this thesis) does not have a constant period as in the traditional PWM modulation in Fig. 37.

6.2 Block Diagram and Design Configuration

Fig. 38 shows system diagram of the inverter. The inverter has two isolated current sensors and two isolated voltage sensors for sensing input/output voltage/current. The optimal control method (described in Chapter 5) is based on feedback signals of these sensors. The inverter also has eight isolated gate drive for driving the eight mosfets. In the initial development, isolation is preferable. However, in final release, to reduce cost and save space, isolation may not needed.

A low cost Wifi module (ESP8266) is used to communicate with cloud service. Thingspeak.com is chosen for simplicity and demonstration purpose. Thingspeak is free and has a RESTful open API allowing easily monitoring and control.

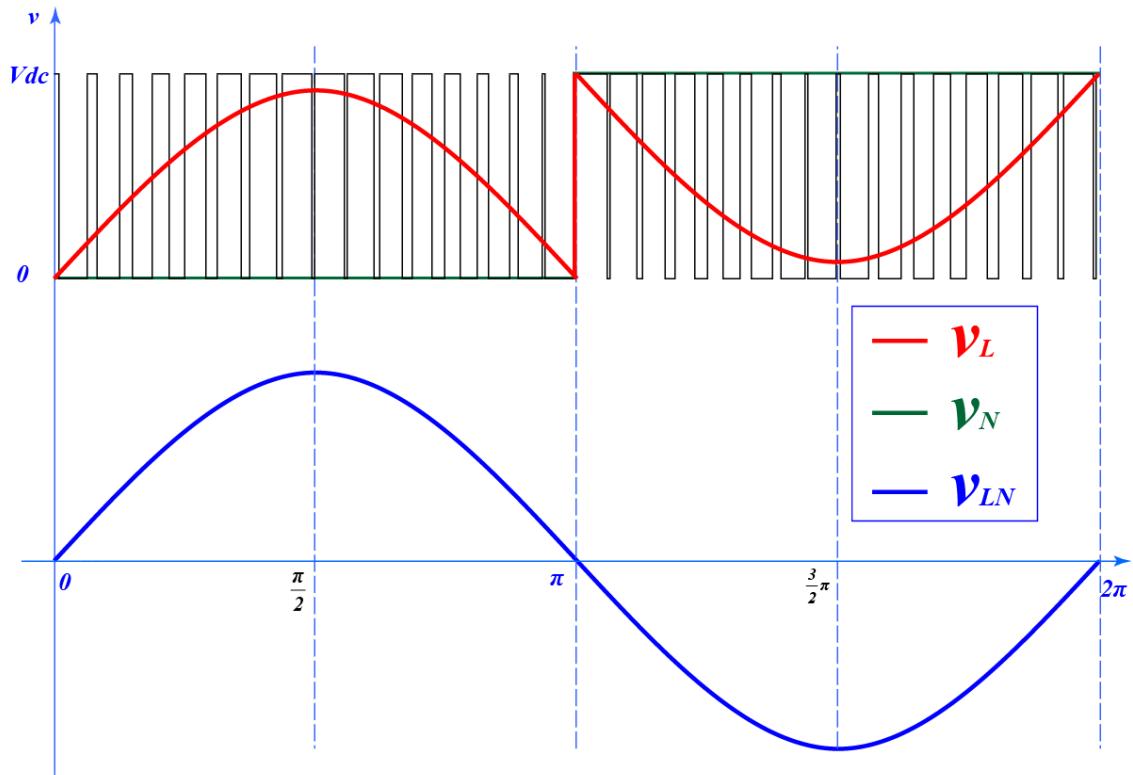


Fig. 37 Waveform during positive half and negative half of a sinusoidal cycle.
With line frequency equal 60Hz, 2π equal 16.667 mili-seconds.

At the beginning of the development, a powerful DSP was selected (TMS320F28377D – 200MHz dual-core) in order to support any complicated control algorithm that may be required. However, with the simplicity of the final proposed control method in Chapter 5, a much smaller and lower cost microcontroller (such as Cortex-M4) is more than enough to do the task. Changing to smaller microcontroller also saves board space, eliminates complicated power supplies and external voltage reference, improving overall power density. (TMS320F28377D requires dual power supplies: 1.2V and 3.3V, and external voltage reference for ADC. Most Cortex-M4 requires a single 3.3V supply, and has internal voltage reference.)

The inverter design is divided into three boards for modularity and efficient space usage: power board, control board, and fly-back PSU board. Hardware design is discussed in the following sections. Firmware is continuously updated to add more features. Current version is located at: <https://github.com/ptLong/OitSolarInverter>

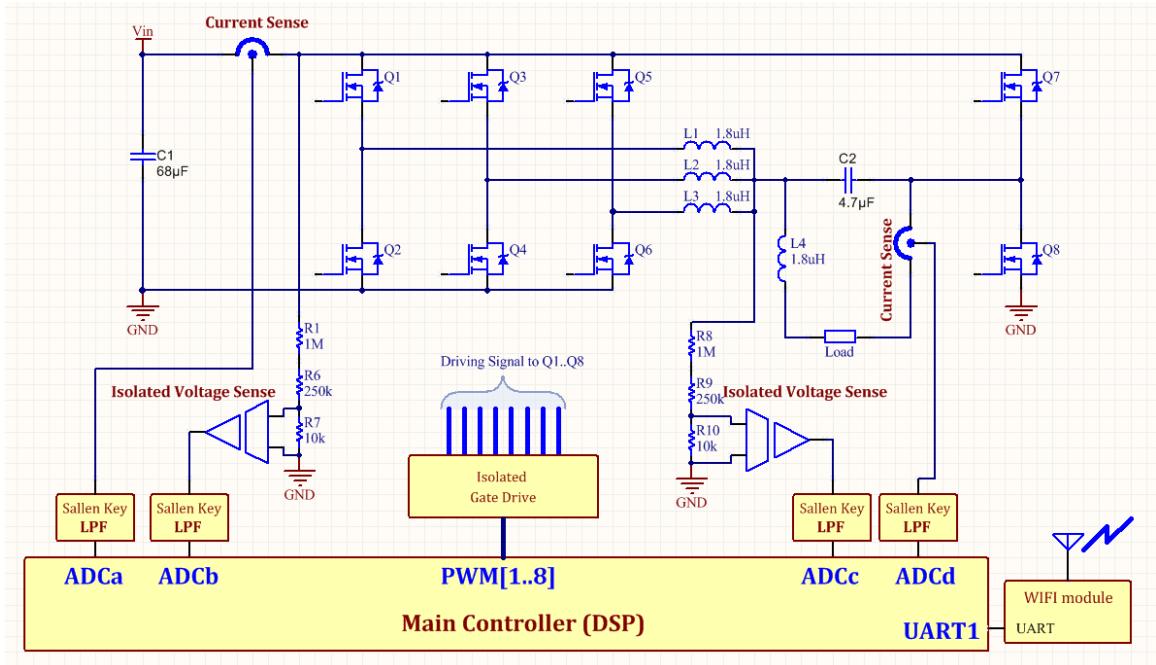
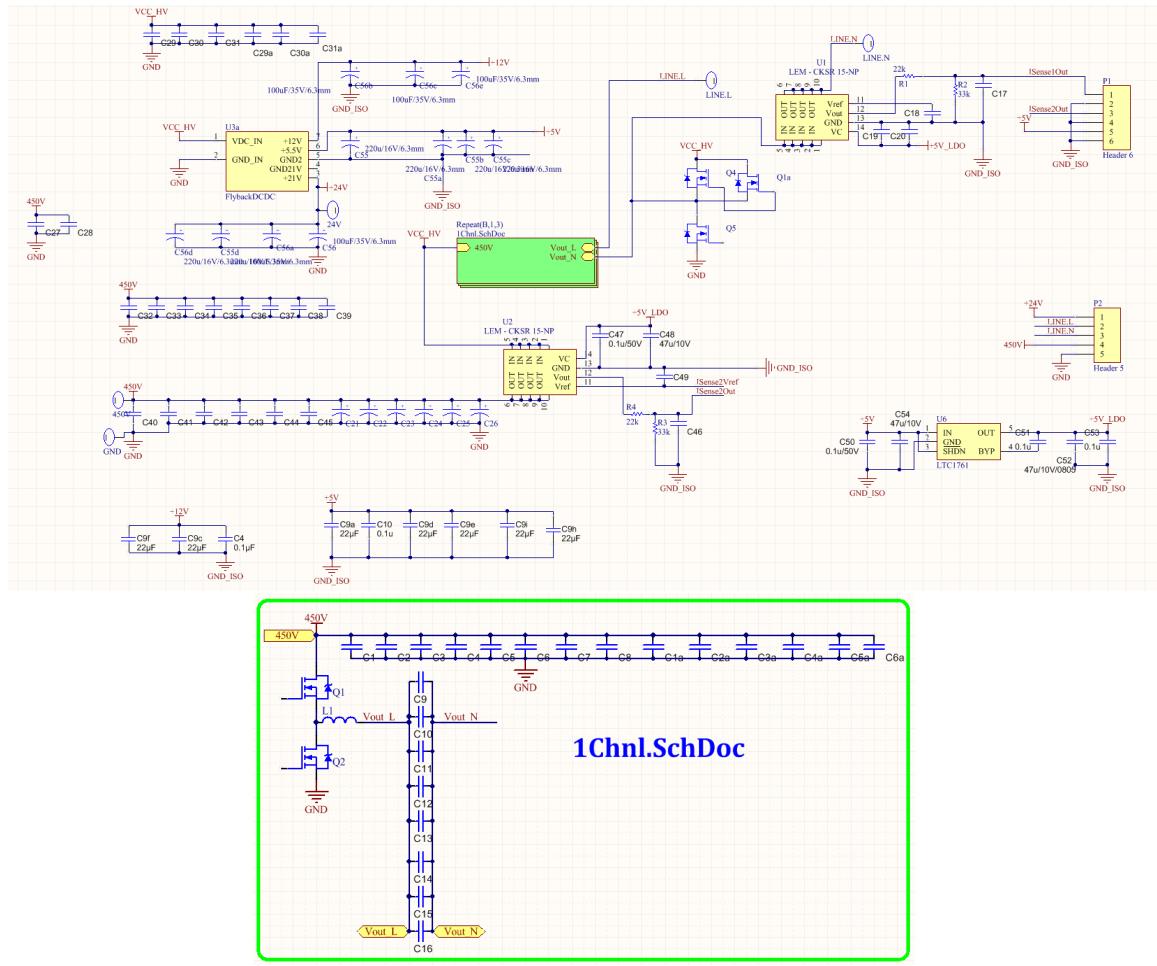


Fig. 38 System Diagram of the Inverter

6.3 Power Board

The power board contains all power components: mosfets (Q1 to Q8), inductors, capacitors, current sensors, and a low noise DC-DC converter supplying 5V for the current sensors. Operating at high frequency, the inverter is extremely sensitive to PCB layout. PCB layout of the power board was done carefully following recommendations in [76], [77]. As discuss in the paper, depending on the placement of the ceramic capacitors (with respect to the power mosfets that they support), there are three types of high frequency power loop: lateral, vertical, and optimal. Among the three types of power loops, the optimal power loop has lowest parasitic inductance. Therefore, it results in lowest loss and voltage overshoot.

Fig. 39 shows schematics of the power board. Fig. 40 shows PCB design and the actual circuit.



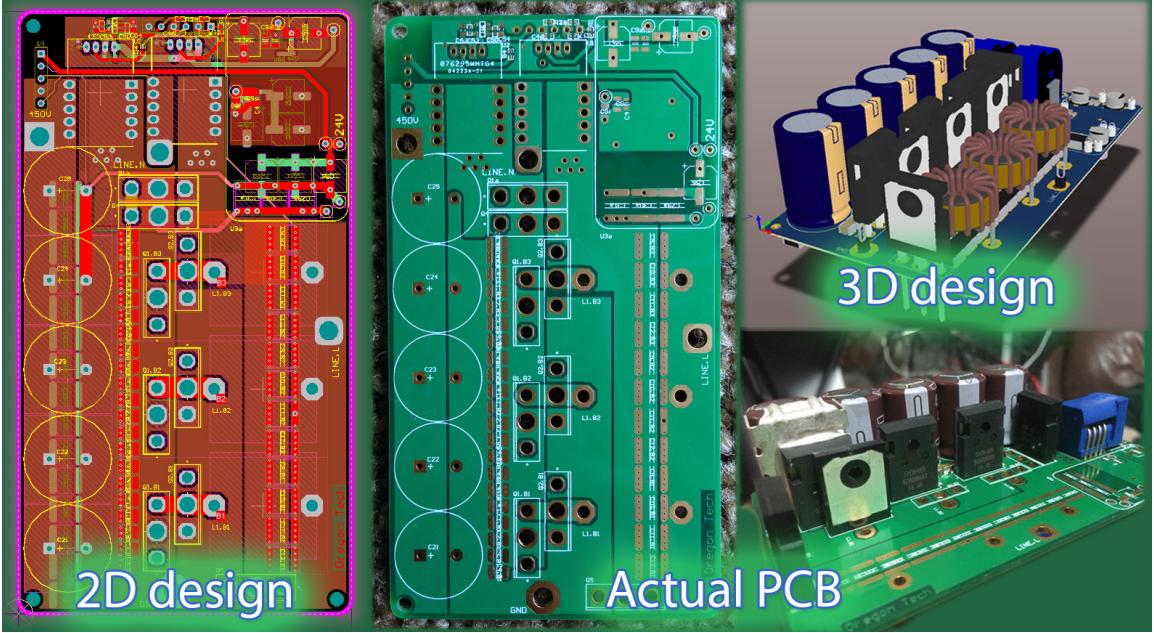


Fig. 40 Pictures of PCB design and real PCB

6.4 Fly-back PSU board

In low power DC-DC applications, fly-back topology is preferable due to simplicity, low cost, and availability of commercial solutions. A fly-back DC-DC converter is designed based on Texas Instruments' UCC28710, PWM controller with primary-side regulation. The Fly-back power supply unit (PSU) converts the high voltage input to low voltages for the controller board (isolated +5.5V), mosfet driving circuits (non-isolated +21V), and fans (isolated +12V). Fig. 41 shows the schematics of the design. Fig. 42 shows PCB design and the actual circuit. The design follows a reference design from Texas Instrument. (For some reasons, the fly-back PSU board does not work very stable. Currently, I'm using an external power supply. More time for debugging is needed to find out why it is not stable.)

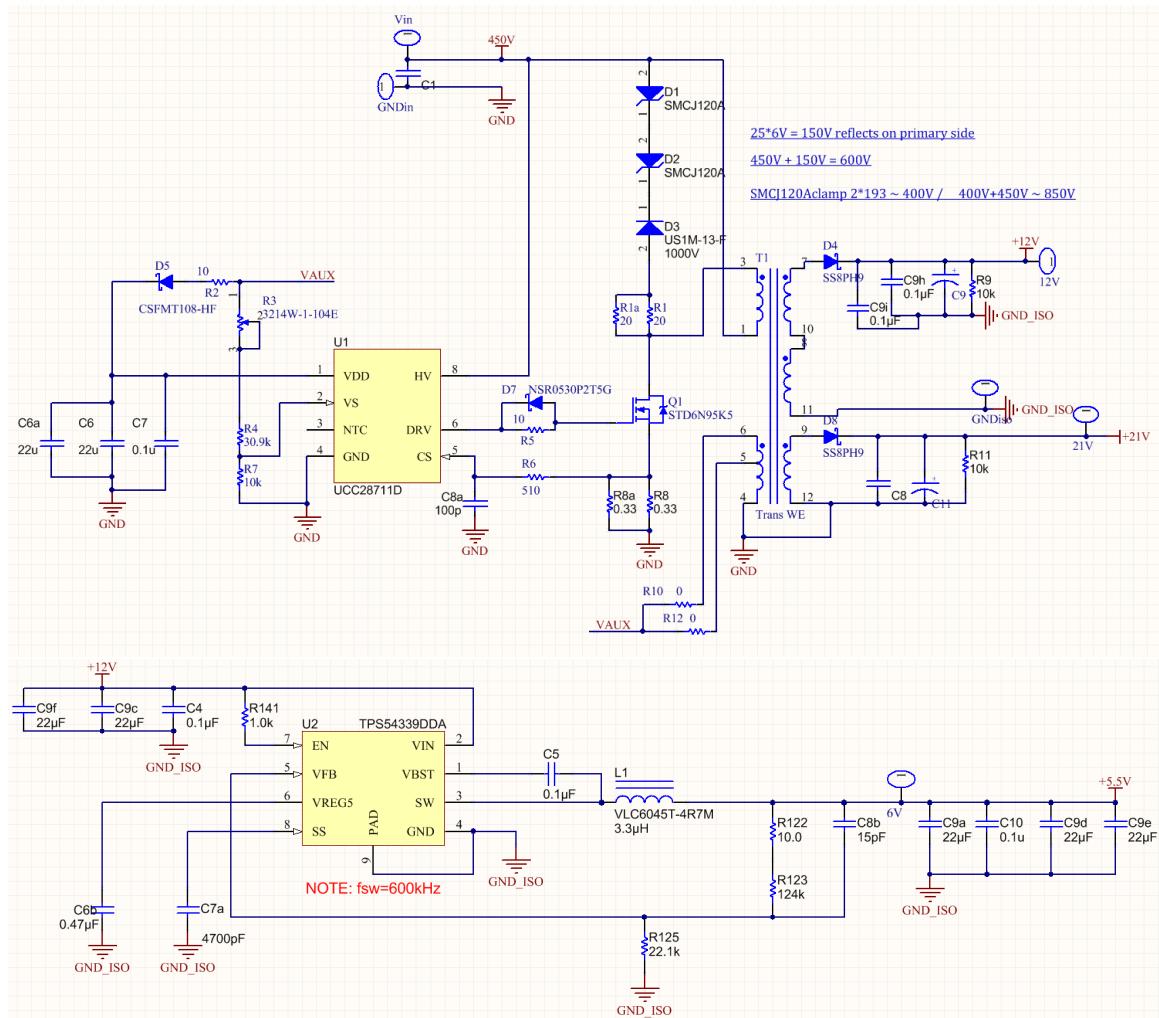


Fig. 41 Schematics of the fly-back PSU

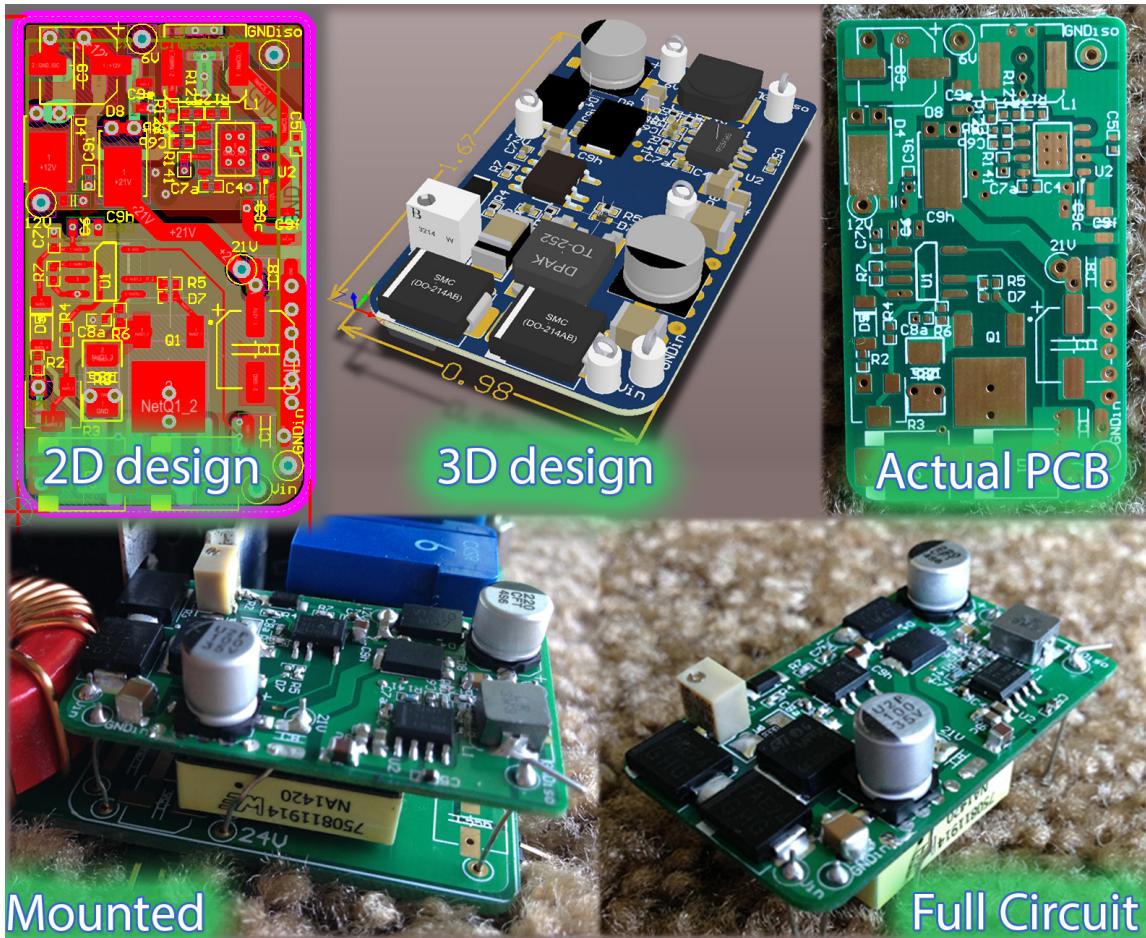


Fig. 42 The fly-back PSU - PCB design and real circuit

6.5 Control board

The control board is the most complicated board. It has the main controller (TMS320F28377D) and other support circuits: signal conditioning, sensing, mosfet driver, communication interface, etc. Careful PCB design is also required. The control board has separated ground planes for analog, digital, and power subsystems to minimize noise coupling that may affect the measurements and control. Fig. 43 shows PCB design and the actual PCB. Fig. 44, and Fig. 45 show the full inverter that has the three board mounted together.

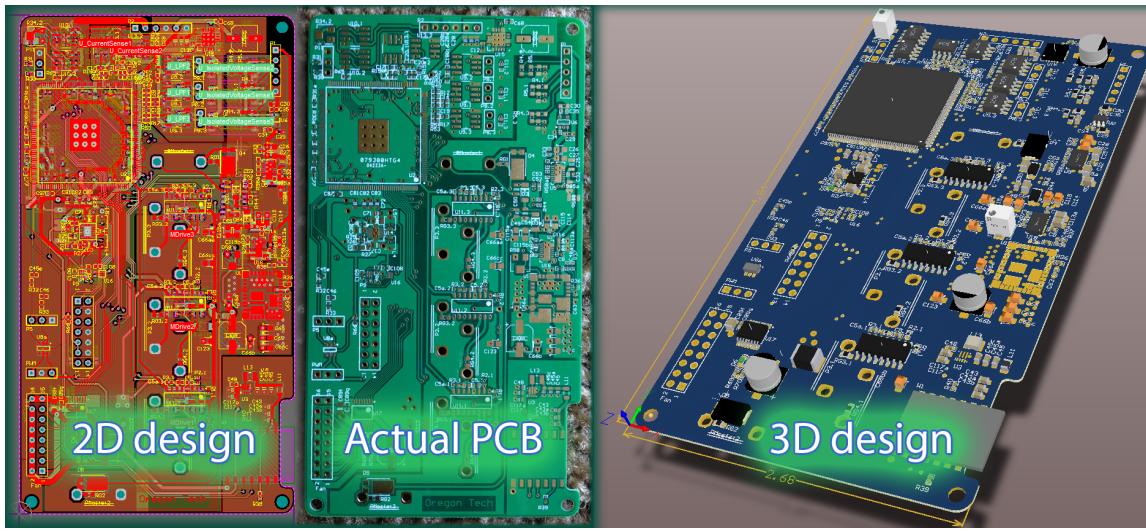


Fig. 43 The Control Board - PCB design and actual PCB

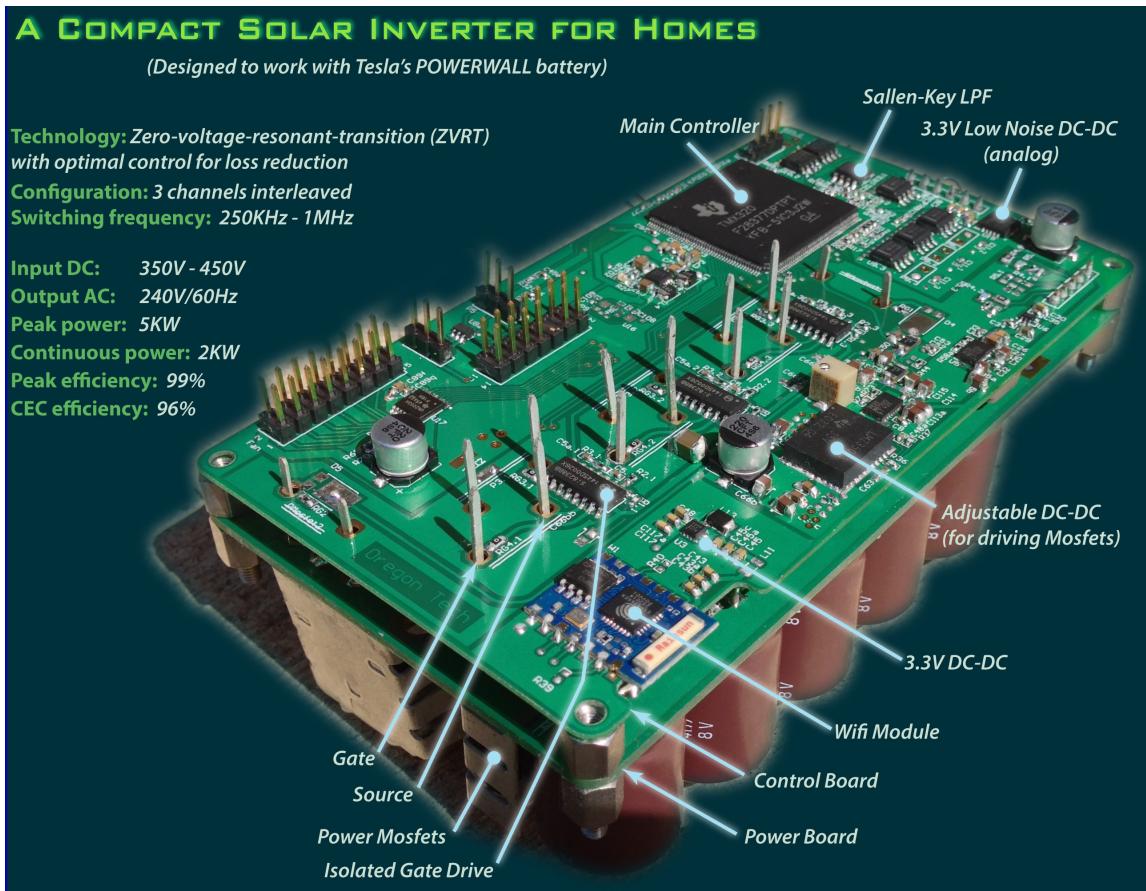


Fig. 44 The inverter - Bottom View

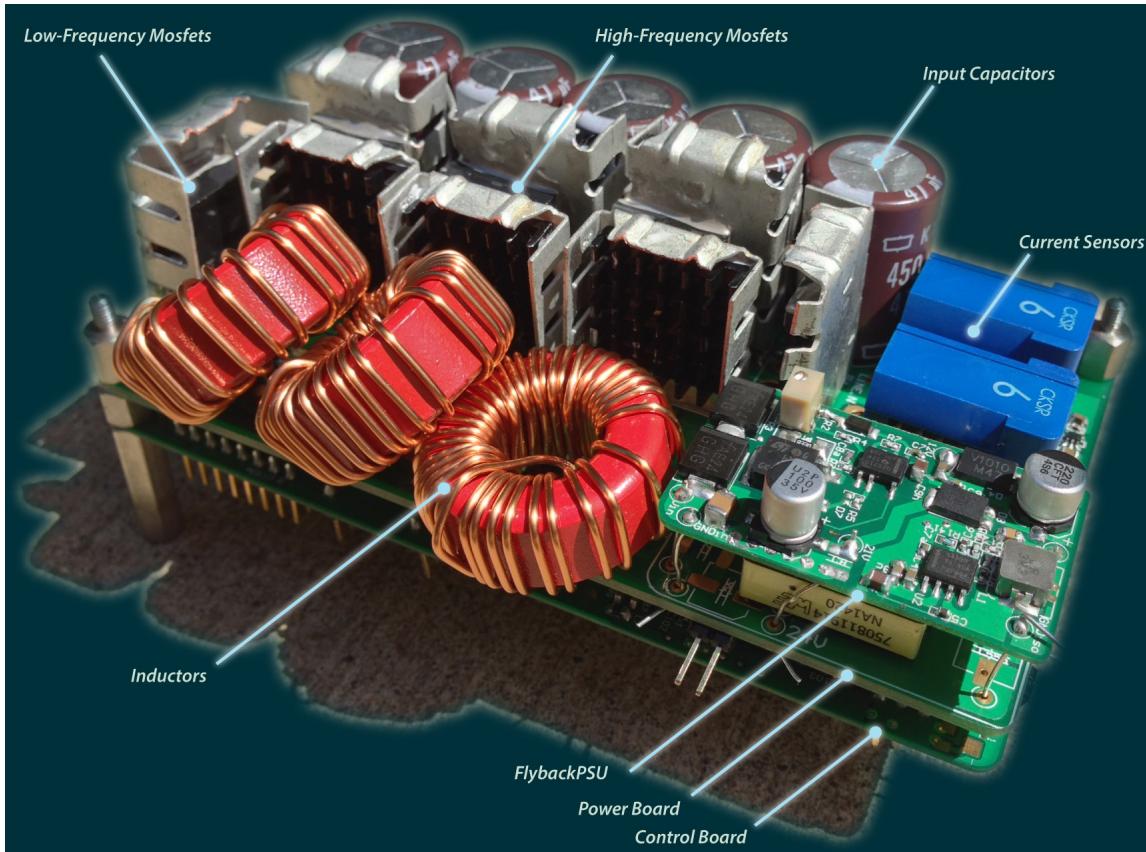


Fig. 45 The inverter – Top View. Power density: $\frac{2000}{2.68 * 4.84 * 1.8} = 85.66$ (Watts/inch³)

6.6 Power Inductor

Initial attempts in rising switching frequency faced serious loss due to many reasons. One of the reasons is that inductor core loss increases exponentially with switching frequency.

Among almost all types of cores that can be found on Digikey, Mouser, and Ebay, Micrometals cores have lowest loss (tests done at 1 MHz). Micrometals offers many materials mixes that have different permeability and loss. For example, mix-17 has extremely low loss but low permeability; mix-26 has much higher permeability but much higher loss. Micrometals offers a software to compare loss and select the best core.

Base on the inductance requirement and switching frequency of the inverter in this thesis, the toroidal core T106-2 (mix-2) is chosen as it balances between loss, permeability, and size. T106-2 has $A_L = 13.5$ Nano-Henry per square of number of turn (nH/N^2). Litz wire is a straightforward choice for high frequency application, since it has lowest AC resistance. For prototype purposes, both Micrometals core and Litz wire can be purchased on Ebay or other sites, such as, www.amidoncorp.com. (Micrometals only accepts purchase order at large quantity.)

6.7 Mosfet Selection

Theoretically, a Figure of Merit (FOM) is used to decide which mosfet is the best. In 1989, Baliga [78] suggested a FOM based on mosfet's on resistance and input capacitance:

$$B_FOM = \frac{1}{R_{on}C_{in}} \quad (31)$$

Then in 1995, Kim [79] showed that mosfet output capacitance is more important, and came up with a new FOM:

$$K_FOM = \frac{1}{R_{on}C_{out}} \quad (32)$$

Recently, in 2004, Dr. Huang [80] suggested a new FOM:

$$H_FOM = \sqrt{R_{on}Q_{GD}} \quad (33)$$

These FOMs were recommended based on certain assumptions about losses in power converters and mechanism of the losses. While the FOMs are good metrics for the majority of situations, they are not useful with the unusual topology and operation of the inverter in this thesis.

6.7.1. *Mosfet breakdown voltage*

In traditional hard-switching inverter, the breakdown voltage of mosfets must be at least 1.5x to 2x the input DC voltage because of high voltage overshoot in hard-switching transitions. The faster the switching transition, the higher the voltage overshoots. For example, with 400VDC input, mosfet breakdown voltage should be higher than 600V for slow switching transition. With the optimal control method in Chapter 5, the inverter operates under ZVS. Therefore, voltage overshoot is almost zero, and lower voltage mosfet can be used. Generally, lower voltage mosfets have better parameters and lower cost.

In this inverter, with designated DC input voltage from 350V to 450V, all power mosfets should have breakdown voltage higher than 500V.

The inverter circuit topology makes it easier for mosfet selection, since it separates mosfets into two categories: high frequency mosfets (the three half-bridge on the left of Fig. 36) and low frequency mosfets (the half-bridge on the right of Fig. 36).

6.7.2. *Low-frequency Mosfet*

Since the low frequency mosfets are switching at line frequency (i.e. 60Hz in US), conduction loss is the primary concern. The low-frequency mosfet selection is straightforward: just select a mosfet that has voltage higher than 500V and has lowest on resistance. STY145N65M5 is selected based on Digikey database. STY145N65M5 has breakdown voltage 650V, typical on-resistance 12 mili-Ohm (lowest among >500V mosfets), and maximum current is 138A. With MDMesh 5 technology, ST created the industry-lowest on-resistance mosfets by increasing the effective die size of the traditional silicon mosfet, and. SiC and GaN, although have better theoretical limit, still haven't catch up.

6.7.3. High-frequency Mosfet

While on-resistance is the decisive factor when choosing low-frequency mosfets, it is less significant when choosing high-frequency mosfets. Choosing the high-frequency mosfets in ZVS converters is much more complicated than choosing low-frequency mosfet. Table 1 summarizes parameters that directly or indirectly affect the performance of the ZVS converter in this thesis. The discussions on these parameters are provided below.

Three noteworthy, commercially available mosfets are considered. GS66508P is a GaN mosfet; C2M0025120D and SCH2080KE are SiC mosfets. Silicon mosfets (such as STY145N65M5) are not considered because it has too high parasitic capacitance, which makes them impractical to be driven at high frequency (~ 1 MHz). In an experiment, the four-Ampere-capable driving chip (Si8238) was burned immediately when driving STY145N65M5 at 1 MHz.

Table 1. High-frequency mosfets comparison

Parameter	GS66508P	C2M0025120D	SCH2080KE	How important?
Vds - Drain-Source Breakdown Voltage (Volts)	650	1200	1200	0
Id - Continuous Drain Current (at 100°C) (Ampere)	20	60	28	0.5
Rds On - Drain-Source Resistance (milli-Ohm)	52	25	80	1
Gate Plateau Voltage (Volts)	3	Not available	9.7	5
Input capacitance (Ciss) or gate charge (Qg)	Low	High	Medium	4
Output capacitance (Coss) or output charge (Qoss)	Low	High	Medium	5
Package	SMD	To-247	To-247	2
Body diode forward voltage drop	3	3.1	1.3	1

❖ Vds – Drain-Source Breakdown Voltage

Drain-Source breakdown voltage is the maximum voltage that mosfet can block. This is a pass/fail criterion, which has no weight in the mosfet selection. For ZVS converter in this thesis, because voltage overshoot is almost zero, mosfet breakdown voltage should be a little higher than the maximum input voltage, which is 450V. All of the three mosfets have voltage higher than 500V.

❖ *I_d – Continuous Drain Current at 100°C*

Continuous drain current is the maximum current that a mosfet can sustain. This parameter is usually given at 25°C and 100°C on device's datasheet. Maximum continuous drain current indirectly depends on the drain-source on-resistance and package (how quickly package dissipates heat). Although higher continuous drain current is preferable, it contributes a very small part in the overall loss, therefore, has very little weight in the mosfet selection.

❖ *R_{Dson} – Drain-Source On resistance*

R_{Dson} is the resistance between Drain and Source terminals of mosfet when it is on. Generally, the on-resistance is a non-linear parameter function of the mosfet's die temperature. It is usually given a typical value (which depends on how manufacturers call "typical"). A chart, showing on-resistance vs. temperature, is also given on the device datasheet.

Since conduction loss contributes a small part in the overall loss, the on-resistance also has little weight in the mosfet selection.

❖ *Gate plateau voltage and input capacitance (C_{iss})*

Input capacitance is the measured capacitance between Gate and Source terminals when V_{ds} = 0. Gate plateau voltage is the highest gate voltage at which mosfet still operates in linear region. It is different from the gate threshold voltage at which mosfet begins to conduct. In switching converter, where switching devices operate in saturated region, we need to drive mosfet's gate with voltage higher than the gate plateau voltage. Gate driving voltage and input capacitance contribute significantly to the gating loss, which is the loss occurs when we charge/discharge mosfets' gate capacitor to turn them on/off:

$$GatingLoss \propto \frac{1}{2} C_{iss} V_{Drive}^2 \quad (34)$$

With V_{Drive} must be larger than gate plateau voltage.

When we turn on mosfet, the energy $\frac{1}{2} C_{iss} V_{Drive}^2$ is stored in the gate capacitance. And when we turning it off, this energy is dissipated into heat inside the mosfet driver (it shorts the

capacitor to ground). Gating loss depends on the number of time we turn mosfet on/off, or the switching frequency.

Loss resulted from switching a millions times per second (1 MHz) is much different from switching twenty thousand times per second (20 KHz). An experiment was done to compare the gating loss between C2M0025120D and SCH2080KE at 1 MHz. In the case C2M0025120D, the driver chip (Si8238) was smoked and almost burned. In the case SCH2080KE, the driver chip was just a little warm. When driving at 20 KHz, in both cases, the driver chip is cool, almost zero heat generated.

Since gating loss contributes a fair part in the overall loss of the ZVS converter, gate plateau voltage and input capacitance has high weight in the mosfet selection.

Although the datasheet of C2M0025120D does not give its gate plateau voltage, the gate plateau voltage of C2M0025120D is comparable to SCH2080KE, since the technology is similar (SiC). GS66508P (GaN) has input capacitance and gate plateau voltage significantly lower than the other two SiC mosfets. Therefore, it is a clear winner in this criterion.

❖ *Output capacitance (C_{oss}) or output charge*

Output capacitance is the capacitance measured at Drain and Source terminals when Gate voltage is at zero. Output capacitance is a non-linear function of the drain-source voltage (V_{ds}). Therefore, some manufacturers give output charge, which is the total charge required to bring V_{ds} to a specific voltage, instead of output capacitance. Generally, output charge doesn't change substantially and is better represent the stored energy when mosfet turns off. The trend is comparing mosfets using output charge instead of output capacitance. However, new device datasheet still gives a curve of output capacitance for backward comparison.

In ZVS converter, mosfet output charge does not contribute directly to the switching loss. However, since high output charge requires a larger inductor ripple current for ZVS, it contributes indirectly to other losses: conduction loss and core loss. Output charge contributes a high weight in the mosfet selection, since a small change in output charge leads to a large change in the required ripple current.

❖ *Package*

Parasitic inductance of mosfet is added to the total inductance of the main power loop. In a switching cycle, the main power loop is charged/ discharged an energy equal:

$$E_{PowerLoop} = \frac{1}{2} L_{PowerLoop} I_{PowerLoop}^2 \quad (35)$$

A part of this energy is dissipated into heat when there is ringing in the circuit. Therefore, mosfet's package inductance contributes a medium weight to the mosfet selection.

❖ *Body diode forward voltage drop*

Although the optimal control method in Chapter 5 reduces mosfet's body-diode conduction significantly, it does not eliminate the body diode conduction. Body diode forward voltage drop still contributes little part to the overall loss of this inverter. Therefore, it has little weight in the mosfet selection.

Among the three mosfets, SCH2080KE has lowest body diode forward voltage drop because it has an integrated Schottky diode. An external Schottky diode can be used, but it is less effective in high frequency since it take sometimes for the current to commutate between the two devices (Mosfet and external Schottky diode). It is better if the two devices are on a same die. In addition, external Schottky diode occupies board space. SCH2080KE has great advantage in this criterion over the other two mosfets.

Due to different device construction, GaN mosfets don't have a body diode like silicon mosfets. The reversed conduction mode of GaN mosfets follows a different mechanism that results in higher voltage drop compares to silicon mosfets. Therefore, it is more critical to minimize the reverse conduction if the converter uses GaN mosfets.

❖ *Conclusion on high frequency Mosfet selection*

The above analysis is just an intuitive discussion for choosing the high-frequency mosfet for the converter in this thesis. Quantitatively comparing mosfets by number is not possible for three reasons. First loss mechanisms in power converters have not been totally understand. Second, new devices behave differently in different circuit topologies. Developments are underway to improve GaN mosfet device model. Quantum based effect, field dependent

mobility, and gate injection current are being studied to incorporate into device model in order to improve calculation accuracy in the near future [81]. Third, there is no standard test procedure/organization for comparing mosfet. Different manufacturers may test their device differently, under different condition, therefore, may come up with different numbers. For example, how manufacturer calls “typical on-resistance” is highly subjective. Building real circuit, with the topology in considering, and comparing the loss is the only precise quantitative method to compare mosfets.

Based on the intuitive analysis, GS66508P is the winner because it has much lower gate plateau voltage, lower input/output capacitance and best package. The body diode forward voltage drop and drain-source on-resistance, which GS66508P is not good, contribute a little to the overall loss of the inverter in this thesis. However, the final inverter uses SCH2080KE because of the availability and lower cost. It was too hard to buy GS6650P since the supplier stock is limited and run out quickly. The C2M0025120D is too expensive for the performance that it gives.

6.8 Current sensor

Fluxgate current sensor CKSR 6-NP is chosen for current sensing. Fig. 46 shows schematics design of current sensor. There are two current sensors onboard for sensing input and output current.

A 4th order low pass filter (LPF) is used to filter out high frequency noises. LPF is designed using Texas Instrument’s FilterPro with Sallen-Key topology and Butterworth response. Fig. 47 shows the design report.

There is also a circuit for overcurrent protection.

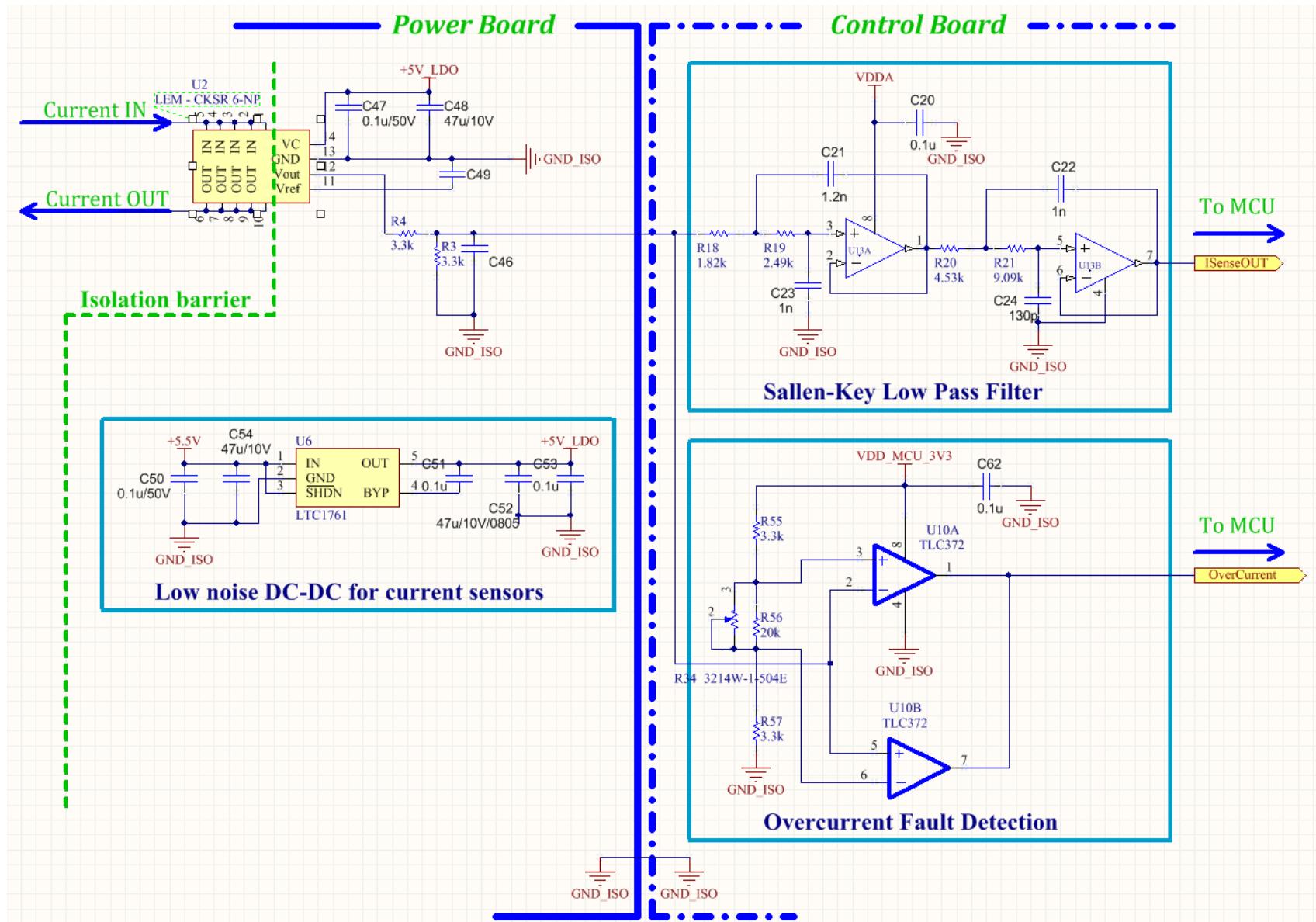


Fig. 46 Schematics of current sensor.

FilterPro Design Report Frequency and Phase Responses

Design Name: Lowpass, Sallen Key, Butterworth **Part:** Ideal Opamp **Order:** 4 Stages: 2
Gain: 1 V/V (0 dB) **Allowable PassBand Ripple:** 1 dB **Passband Frequency:** 68 kHz
Corner Frequency Attenuation: -3 dB **Stopband Attenuation:** -45 dB **Stopband Frequency:** 250 kHz

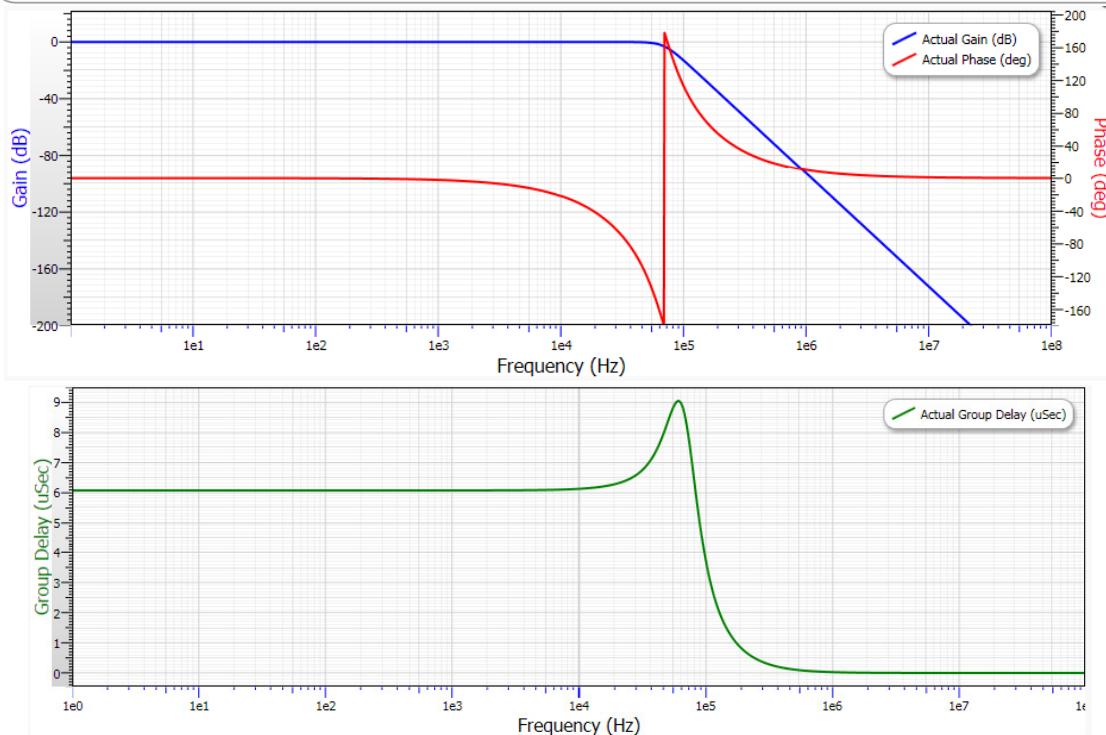


Fig. 47 Response of LPF for current sensors.

6.9 Voltage Sensor

Fig. 48 shows schematics design of voltage sensor.

A 3rd order low pass filter (LPF) is used to filter out high frequency noises. LPF is designed using Texas Instrument's FilterPro with Sallen-Key topology and Butterworth response. Fig. 49 shows design report.

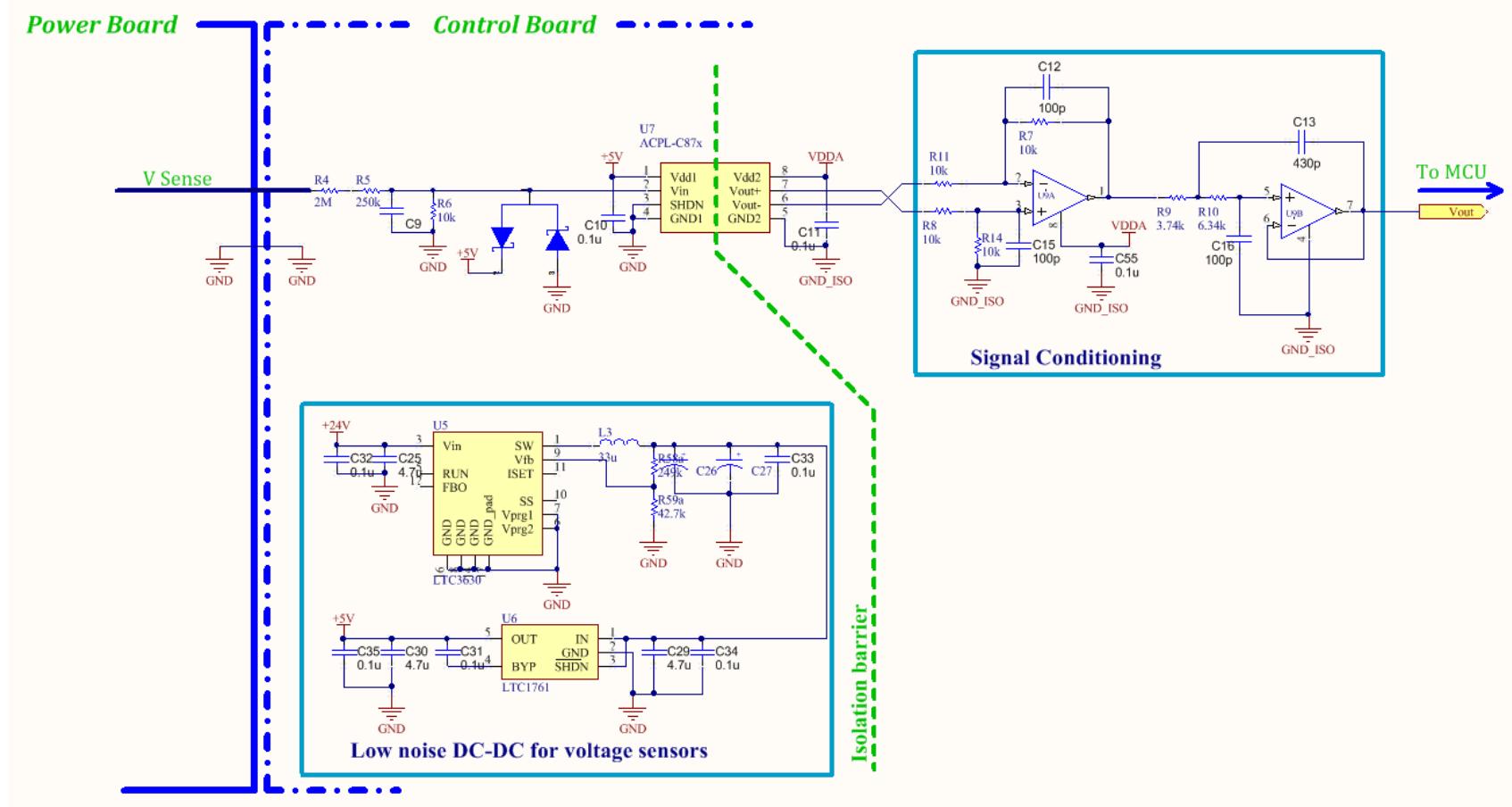


Fig. 48 Schematics of voltage sensor.

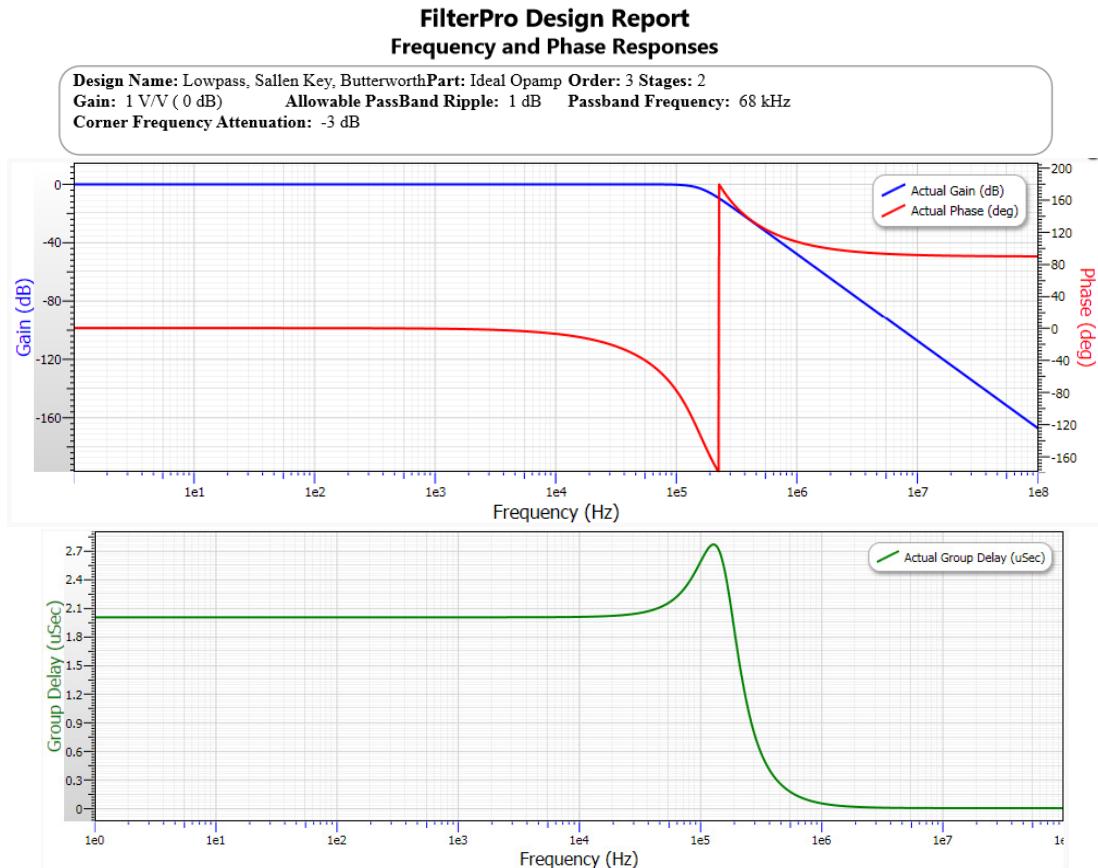


Fig. 49 Response of LPF for voltage sensor.

6.10 Mosfet Drivers

Silab's Si8238 isolated gate drive is used to drive mosfets. Fig. 50 shows the schematics design of the mosfet gate drive circuit.

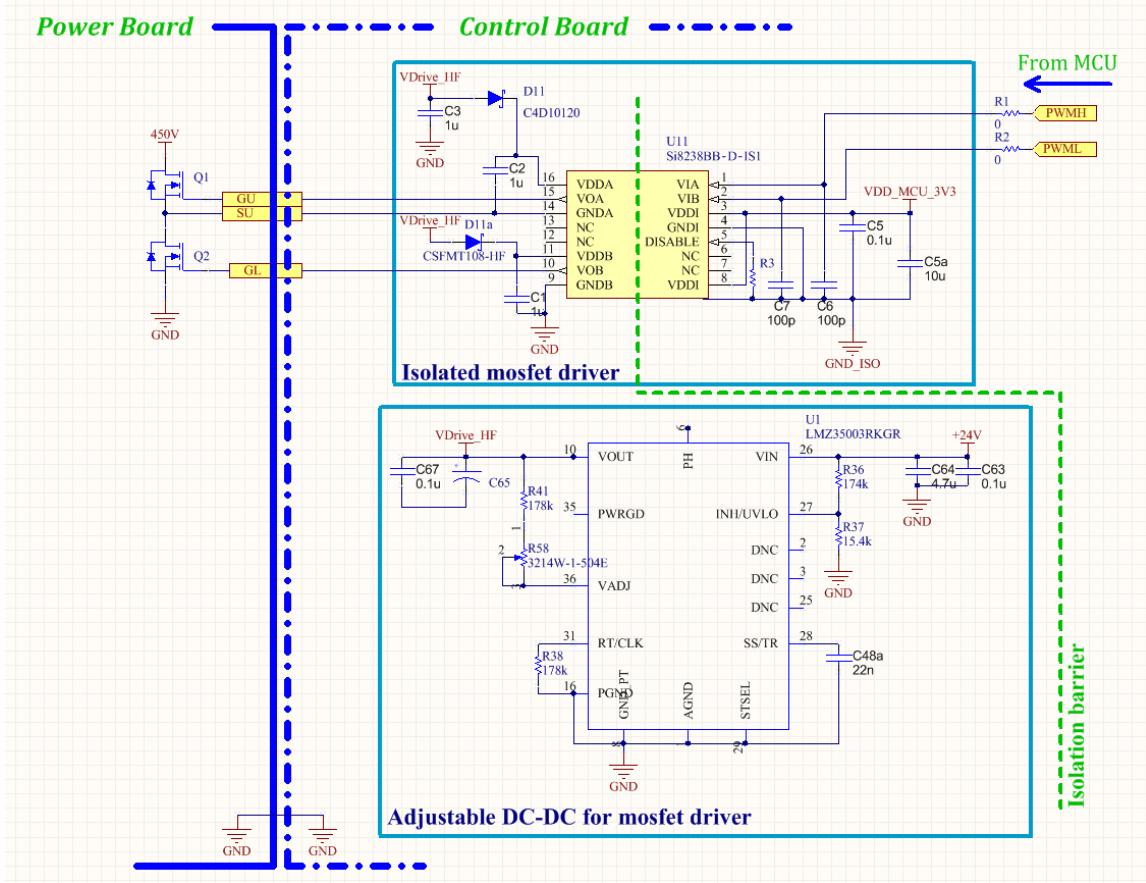


Fig. 50 Isolated mosfet driver.

6.11 Wifi Interface

Internet interface has become inevitable in modern solar PV systems as it improves energy yield and reduces O&M cost, especially for remote PV systems. While power line communication (PLC), or other wireless interface is preferable in remote or large-scale PV systems, Wi-Fi is preferable for residential rooftop PV systems because of the pervasiveness of Wi-Fi signal and the availability of low cost Wi-Fi module.

A low cost Wifi module, ESP8266, is chosen to communicate with the cloud, providing remote monitoring and control function. (ESP8266 costs less than \$5 on Ebay). Fig. 51 shows schematic of the design.

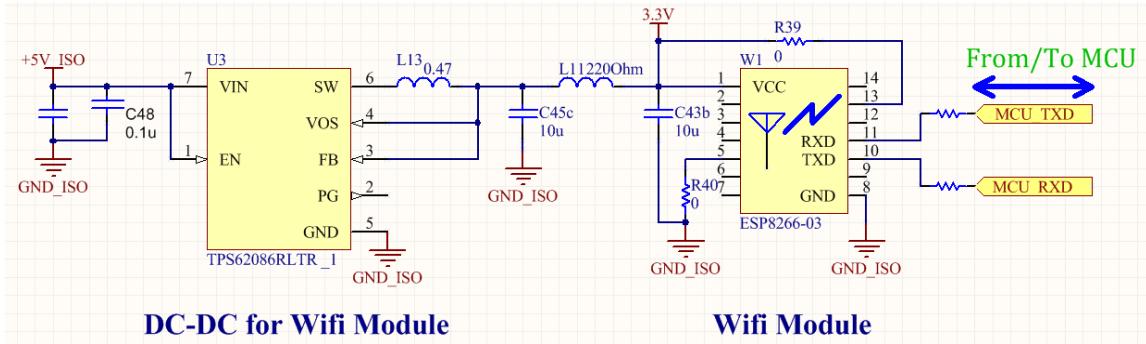


Fig. 51 WiFi module provide an internet interface for remote monitoring and control.

6.12 Other Support Circuits

6.12.1. 1.2V and 3.3V DC-DC for Digital Subsystem

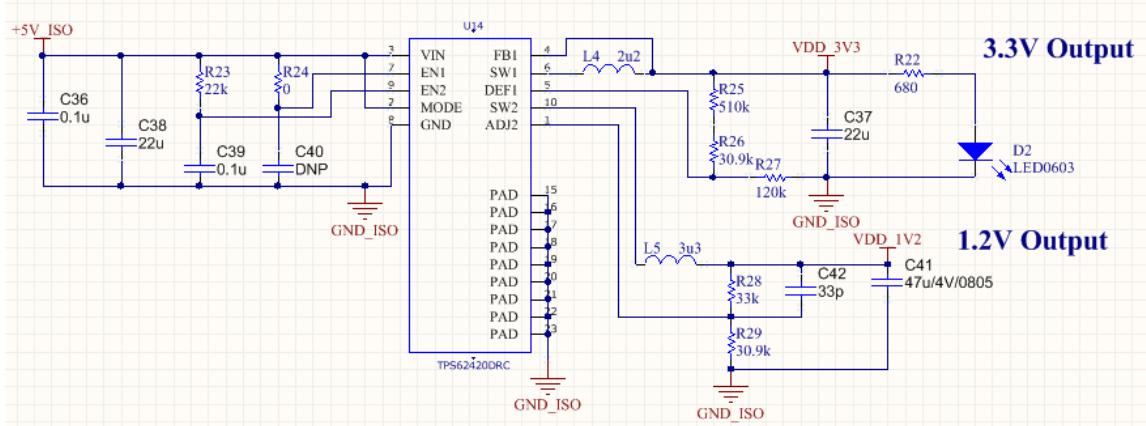
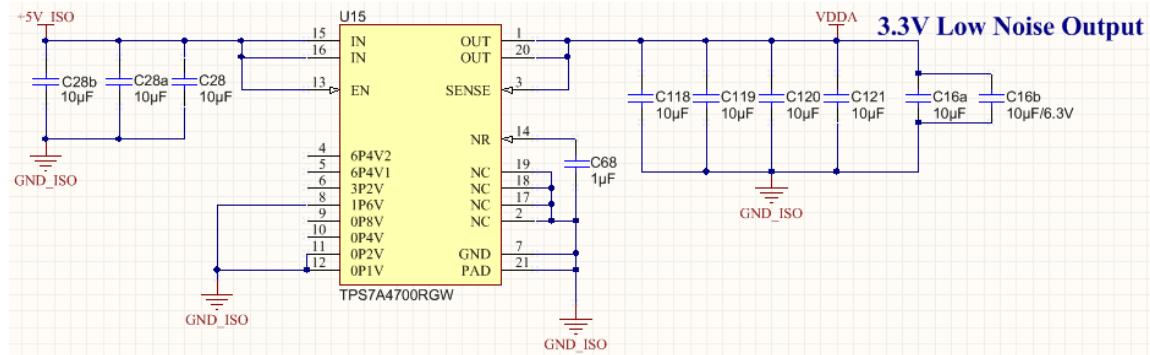
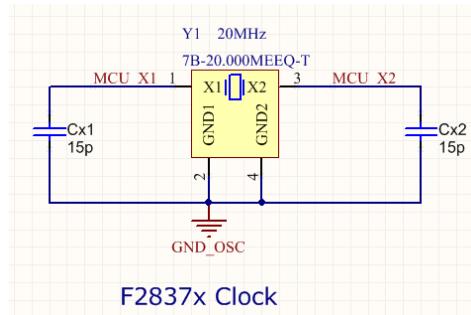


Fig. 52 1.2V and 3.3V DC-DC for digital subsystem

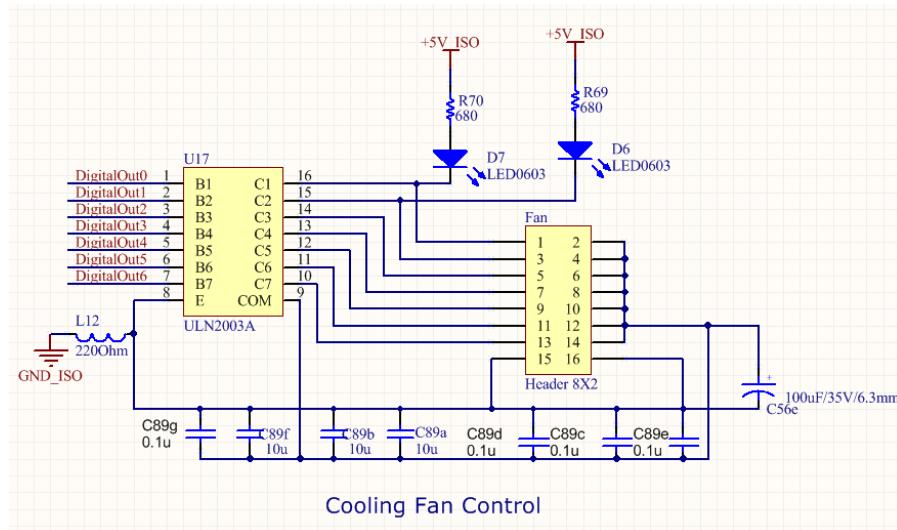
6.12.2. Low Noise 3.3V DC-DC for Analog Subsystem



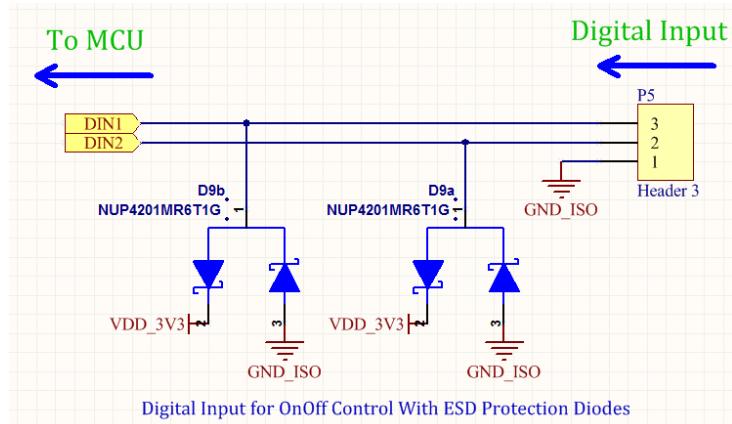
6.12.5. F2837x Clock



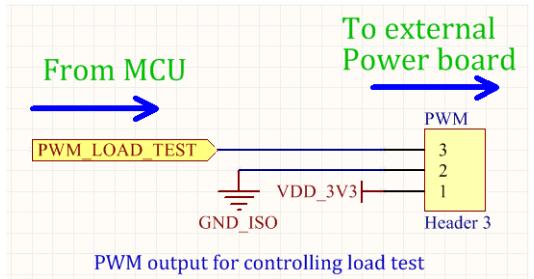
6.12.6. Output On/Off Control for Cooling Fan



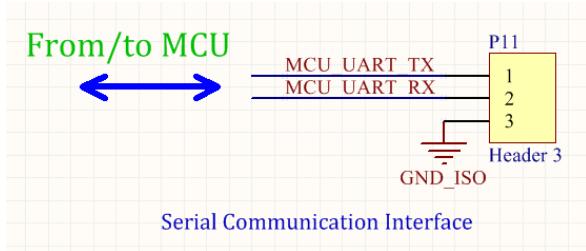
6.12.7. Digital Input for On/Off Control



6.12.8. PWM Output for Controlling Load Test



6.12.9. Serial Interface



Chapter 7

Conclusion and Future Directions

In this thesis, zero voltage resonant transition of a half-bridge is reviewed with amendments to make the analysis correct in high frequency converters where the resonant transition occupies a large part in a switching cycle. Then this thesis describes a programmatic tuning approach for ZVRT converter to achieve lowest loss under all operating conditions. While this initial brute-force approach cannot find the true optimal operating point (still sub-optimal), its result is better than single direction approaches found in the literature [48]–[53], [54]–[67], and it shows that there is space for efficiency/power density improvement in converters that have a half-bridge as basic building block.

One drawback of the proposed control method is long calibration time. Future developments may apply artificial intelligence and machine learning to reduce or eliminate manual calibration.

This thesis does not solve the twice-line frequency energy buffer problem, which is the major application-specific-requirement that limits the scaling of single-phase inverter. Traditionally, large electrolytic capacitors have been used as the energy buffer. However, electrolytic capacitor is well-known root cause of failure in power converter. [82] reports a good method to solve this problem. Future developments may combine [82] with the proposed method in this thesis to design a high power density, high efficiency inverter that has twice-line frequency energy buffer.

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Appendices