组合电路的门电路实现

例：习题2.12 举重比赛有3个裁判，一个是主裁判A，另外两个是副裁判B和C。运动员一次举重是否成功，由裁判员各自按动他面前的按钮决定，只有两个以上（其中必须有主裁判）判定为成功，表示“成功”的灯泡L才亮。试列出真值表和逻辑表达式。

真值表

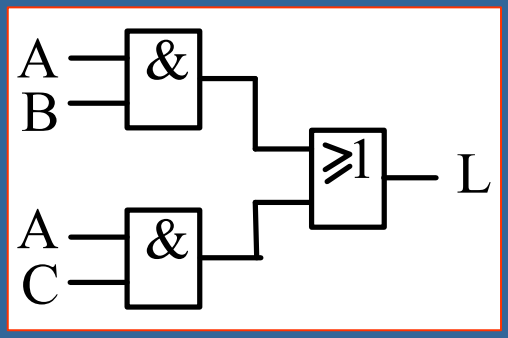
A	B	C	L
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

逻辑表达式：

$L=A\bar{B}C+AB\bar{C}+ABC$

$=AC+AB$

逻辑电路：



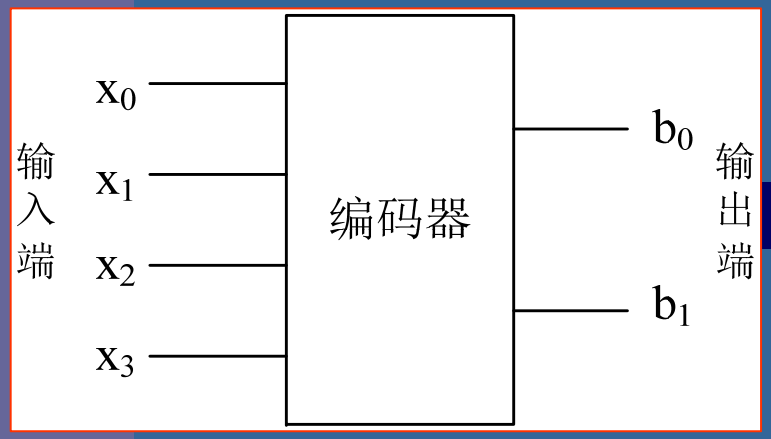
用逻辑门设计组合电路的过程

逻辑功能的（文字/图/表）描述 → 真值表/逻辑表达式 → 优化（简化）逻辑表达式 → 用门电路实现

例1 设计一个4线—2线编码器

编码器（encoder）是将信号或数据进行编制、转换为可用以通讯、传输和存储的信号形式的器件或设备。

框 图

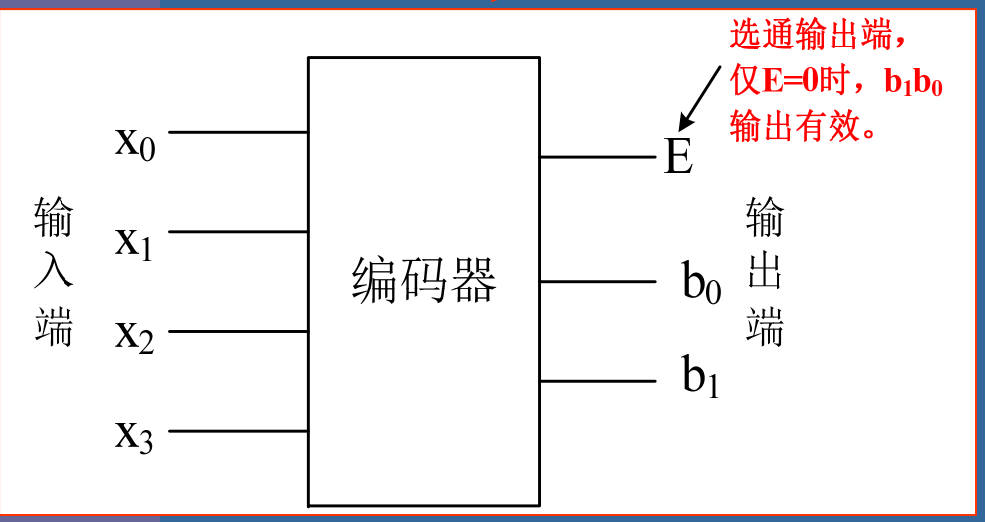


功能表

x_3	x_2	x_1	x_0	b_1	b_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
其 它				?	?

怎么办？能为任意X？

改进框 图

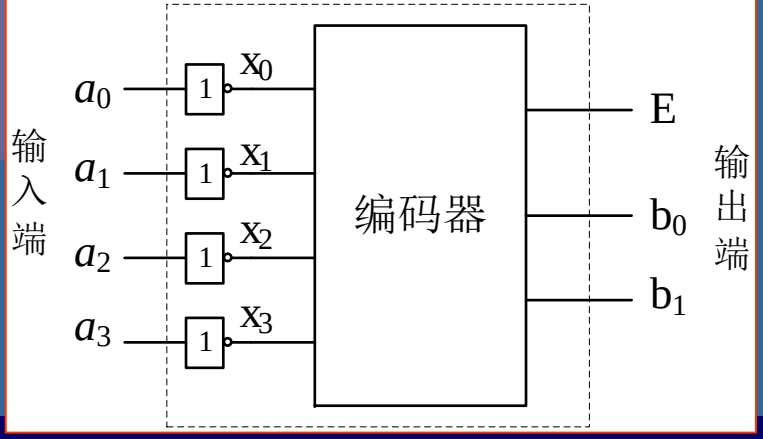


新的功能表

x_3	x_2	x_1	x_0	E	b_1	b_0
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
1	0	0	0	0	1	1
其 它				1	X	X

E=1，b_1b_0输出无意义（即无效）

如果



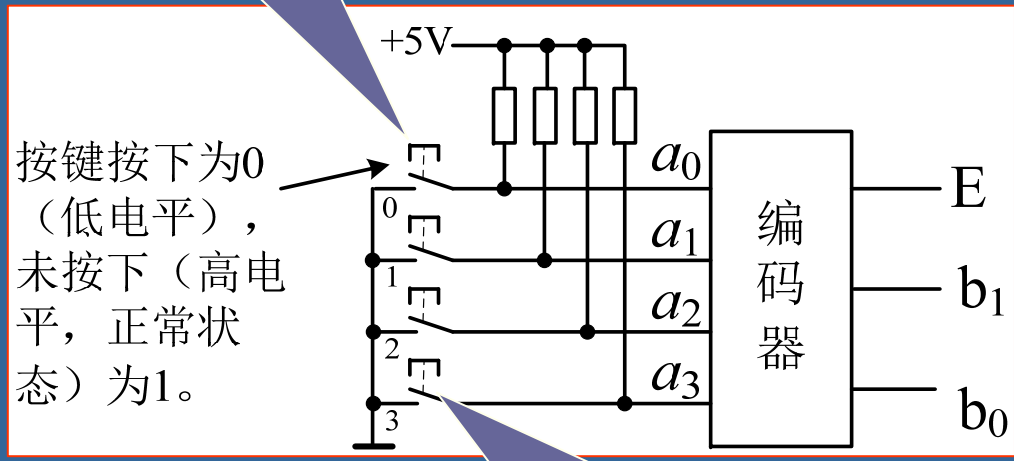
功能表

a_3	a_2	a_1	a_0	E	b_1	b_0
1	1	1	0	0	0	0
1	1	0	1	0	0	1
1	0	1	1	0	1	0
0	1	1	1	0	1	1
	其	它		1	X	X

输入低电平有效

注意：书上按键方向画反了

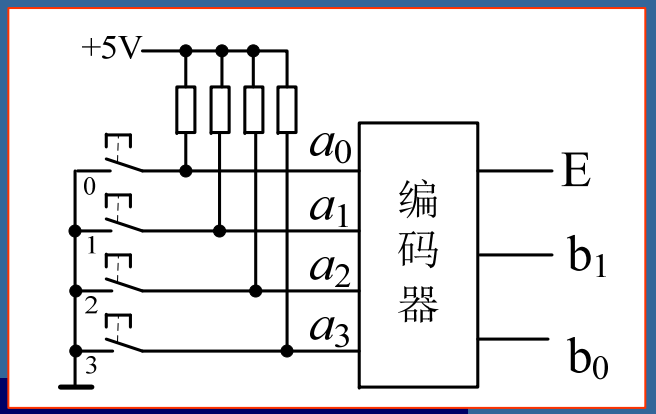
电路图



现在问题是：如何同时按下多个按键怎么办？

答案是采用优先级，即所谓的优先编码。

a_3	a_2	a_1	a_0	E	b_1	b_0
1	1	1	0	0	0	0
1	1	0	X	0	0	1
1	0	X	X	0	1	0
0	X	X	X	0	1	1
1	1	1	1	**1**	X	X



优先编码，a_3的权限最高，a_0的权限最低

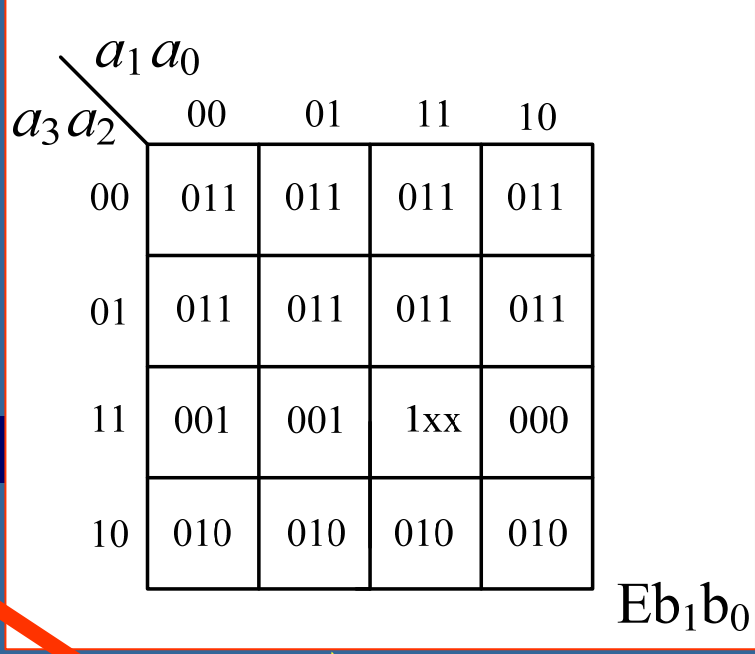
X表示任意，即无论是0还是1

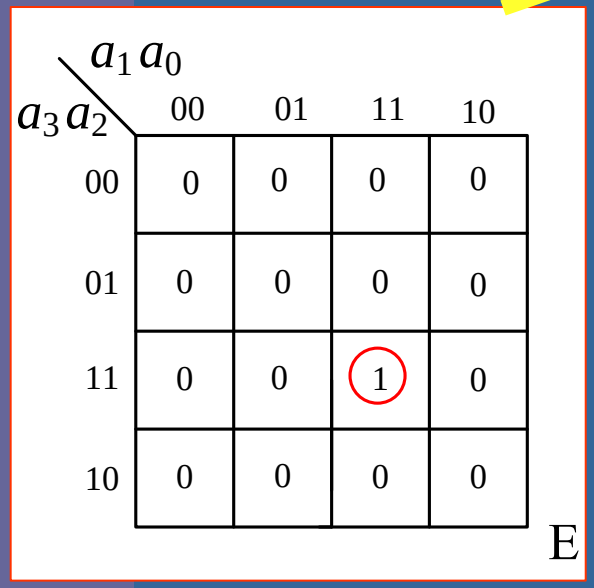
若交换一下行的上下顺序

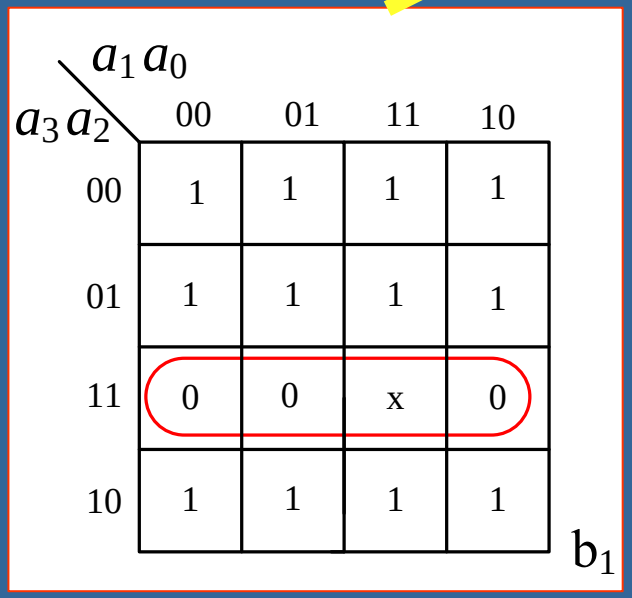
a_3	a_2	a_1	a_0	E	b_1	b_0
1	1	1	1	1	X	X
0	X	X	X	0	1	1
1	0	X	X	0	1	0
1	1	0	X	0	0	1
1	1	1	0	0	0	0

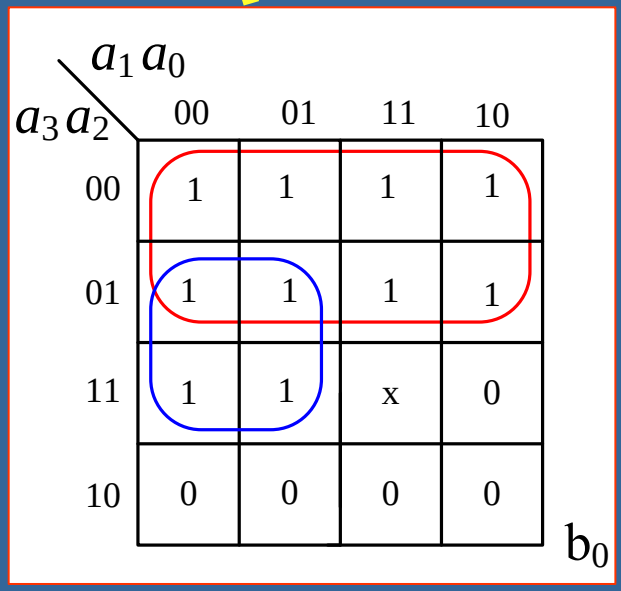
这个就是教材P89 表3-2-1 4线—2线优先编码器功能表

a_3	a_2	a_1	a_0	E	b_1	b_0
1	1	1	1	1	X	X
0	X	X	X	0	1	1
1	0	X	X	0	1	0
1	1	0	X	0	0	1
1	1	1	0	0	0	0









$$E = a_3 a_2 a_1 a_0 \qquad b_1 = \bar{a}_3 + \bar{a}_2 \qquad b_0 = \bar{a}_3 + a_2 \bar{a}_1$$

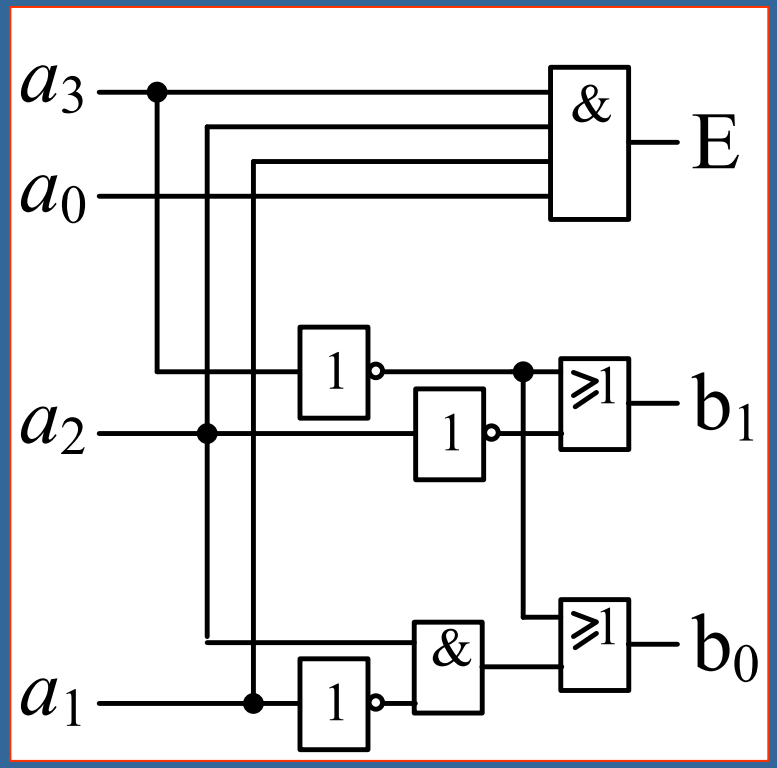
逻辑表达式：

$$E = a_3 a_2 a_1 a_0$$

$$b_1 = \overline{a}_3 + \overline{a}_2$$

$$b_0 = \overline{a}_3 + a_2 \overline{a}_1$$

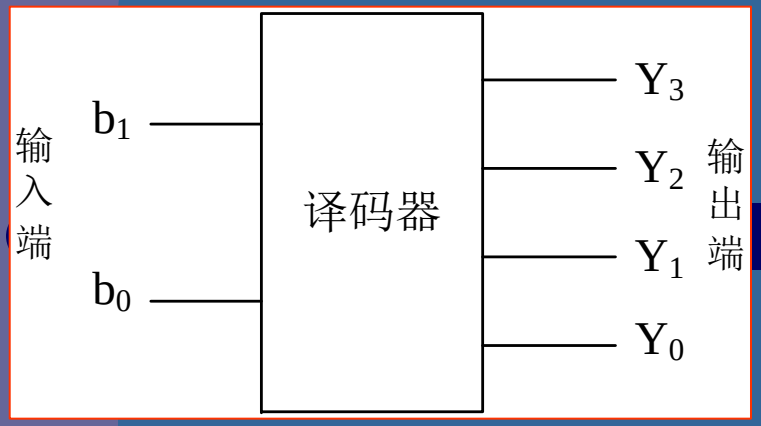
逻辑电路图：



4线—2线优先编码器

例2 设计一个2线—4线译码器

框 图

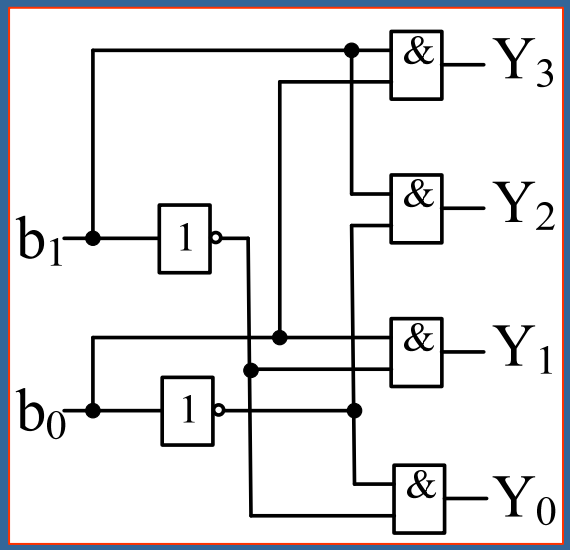


译码是编码的逆过程，在编码时，每一种二进制代码，都赋予了特定的含义，即都表示了一个确定的信号或者对象。把代码状态的特定含义“翻译”出来的过程叫做译码，实现译码操作的电路称为译码器。也就是说，译码器是可以将输入二进制代码的状态翻译成输出信号，以表示其原来含义的电路。

真值表

行号	b_1	b_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	1
1	0	1	0	0	1	0
2	1	0	0	1	0	0
3	1	1	1	0	0	0

逻辑图



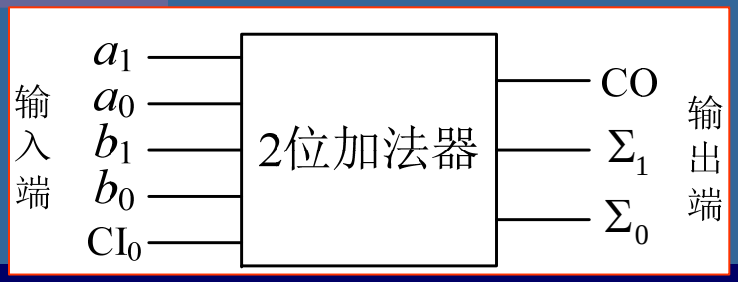
逻辑表达式

$$Y_3 = b_1 b_0 = m_3 \qquad Y_2 = b_1 \bar{b}_0 = m_2$$

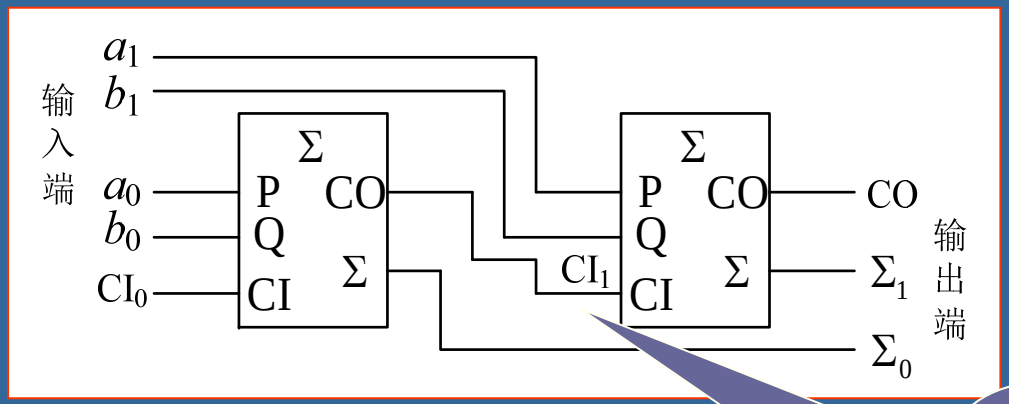
$$Y_1 = \bar{b}_1 b_0 = m_1 \qquad Y_0 = \bar{b}_1 \bar{b}_0 = m_0$$

例3 设计一个2位并行加法器

框 图



根据加法的运算性质，可以分解成两个1位加法器级联而成。



逻辑表达式

$$\Sigma_0 = a_0 \oplus b_0 \oplus CI_0$$

$$\Sigma_1 = a_1 \oplus b_1 \oplus CI_1$$

$$CI_1 = a_0 b_0 + a_0 CI_0 + b_0 CI_0$$

$$CO = a_1 b_1 + a_1 CI_1 + b_1 CI_1$$

但该电路有一个明显的缺点，即只有等CI_1产生后，才能有CO。对于多级电路来说，这样会大大地影响电路运行速度。

逻辑表达式 $\Sigma_0 = a_0 \oplus b_0 \oplus \mathrm{CI}_0$

$\Sigma_1 = a_1 \oplus b_1 \oplus \mathrm{CI}_1$

$\mathrm{CI}_1 = a_0 b_0 + a_0 \mathrm{CI}_0 + b_0 \mathrm{CI}_0$

$\mathrm{CO} = a_1 b_1 + a_1 \mathrm{CI}_1 + b_1 \mathrm{CI}_1$

令

$$\mathrm{G}_0 = a_0 b_0, \quad \mathrm{P}_0 = a_0 + b_0$$

$$\mathrm{G}_1 = a_1 b_1, \quad \mathrm{P}_1 = a_1 + b_1$$

则

$$\because \ \mathrm{P}_0 \cdot \bar{\mathrm{G}}_0 = (a_0 + b_0) \cdot \overline{a_0 b_0} = (a_0 + b_0)(\bar{a}_0 + \bar{b}_0)$$

$$= a_0 \bar{b}_0 + \bar{a}_0 b_0 = a_0 \oplus b_0$$

$$\therefore \ \Sigma_0 = a_0 \oplus b_0 \oplus \mathrm{CI}_0 = (\mathrm{P}_0 \cdot \bar{\mathrm{G}}_0) \oplus \mathrm{CI}_0$$

同理 $\Sigma_1 = a_1 \oplus b_1 \oplus \mathrm{CI}_1 = (\mathrm{P}_1 \cdot \bar{\mathrm{G}}_1) \oplus \mathrm{CI}_1$

$$CI_1 = a_0 b_0 + a_0 CI_0 + b_0 CI_0 = a_0 b_0 + CI_0 (a_0 + b_0)$$

$$= G_0 + CI_0 P_0 = \overline{\overline{G_0 + CI_0 P_0}}$$

$$= \overline{\overline{G}_0 (\overline{CI}_0 + \overline{P}_0)} = \overline{\overline{G}_0 \overline{P}_0 + \overline{G}_0 \overline{CI}_0}$$

$$\because \quad \overline{G}_0 \overline{P}_0 = \overline{a_0 b_0} \cdot \overline{(a_0 + b_0)} = (\overline{a}_0 + \overline{b}_0)\overline{a}_0 \overline{b}_0$$

$$= \overline{a}_0 + \overline{b} = \overline{P}_0$$

$$\therefore \quad CI_1 = \overline{\overline{P}_0 + \overline{G}_0 \overline{CI}_0}$$

$$CO = a_1 b_1 + a_1 CI_1 + b_1 CI_1 = a_1 b_1 + CI_1 (a_1 + b_1)$$

$$= G_1 + CI_1 P_1 = \overline{\overline{G_1 + CI_1 P_1}}$$

$$= \overline{\overline{G}_1 \overline{P}_1 + \overline{G}_1 \overline{CI}_1} = \overline{\overline{P}_1 + \overline{G}_1 CI_1}$$

$$= \overline{\overline{P}_1 + \overline{G}_1 \overline{G}_0 (\overline{CI}_0 + \overline{P}_0)}$$

$$= \overline{\overline{P}_1 + \overline{P}_0 \overline{G}_1 + \overline{G}_0 \overline{G}_1 \overline{CI}_0}$$

变换后的逻辑表达式

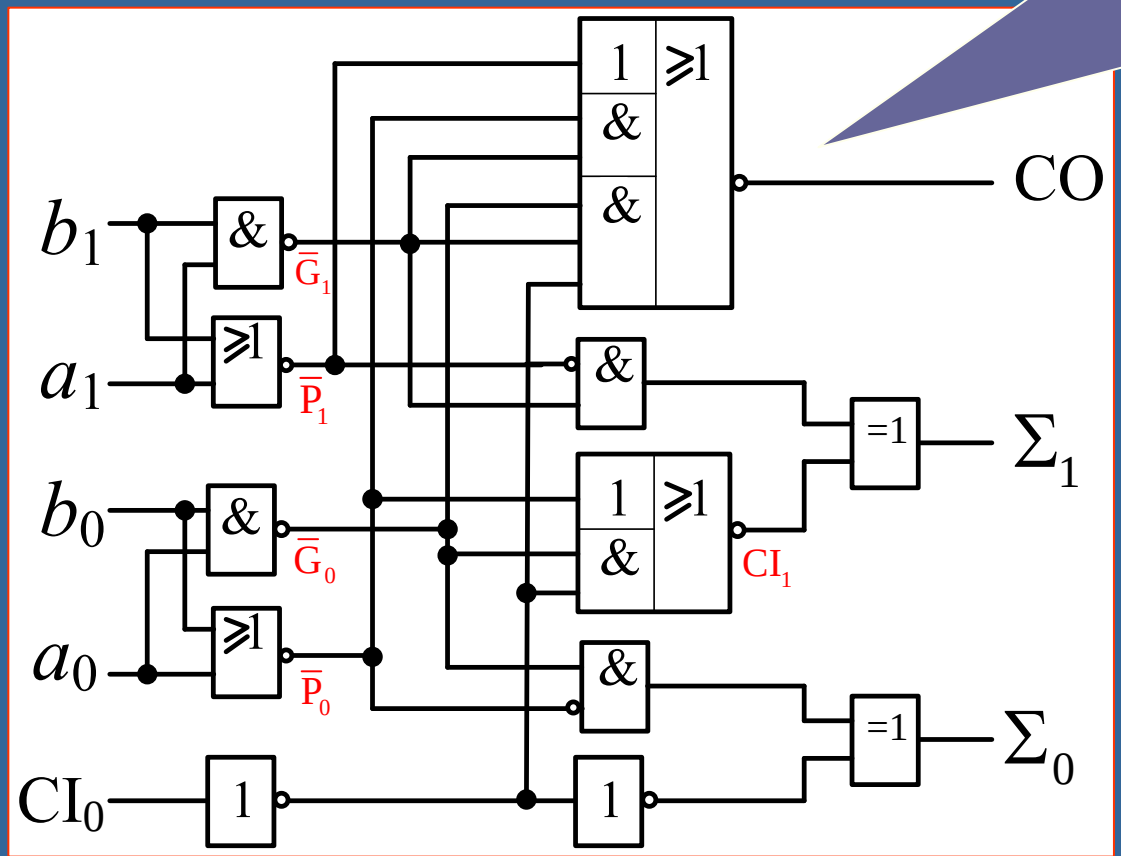
$$\Sigma_0 = (P_0 \cdot \overline{G}_0) \oplus CI_0 \qquad \Sigma_1 = (P_1 \cdot \overline{G}_1) \oplus CI_1$$

$$CI_1 = \overline{\overline{P}_0 + \overline{G}_0 \overline{CI}_0}$$

$$CO = \overline{\overline{P}_1 + \overline{P}_0 \overline{G}_1 + \overline{G}_0 \overline{G}_1 \overline{CI}_0}$$

特点：CO由a_0、b_0、a_1、b_1和CI_0直接产生，不需要CI_1，可提高多级加法器的运算速度。

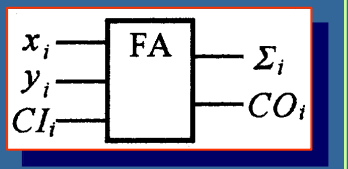
逻辑图



常用组合逻辑模块

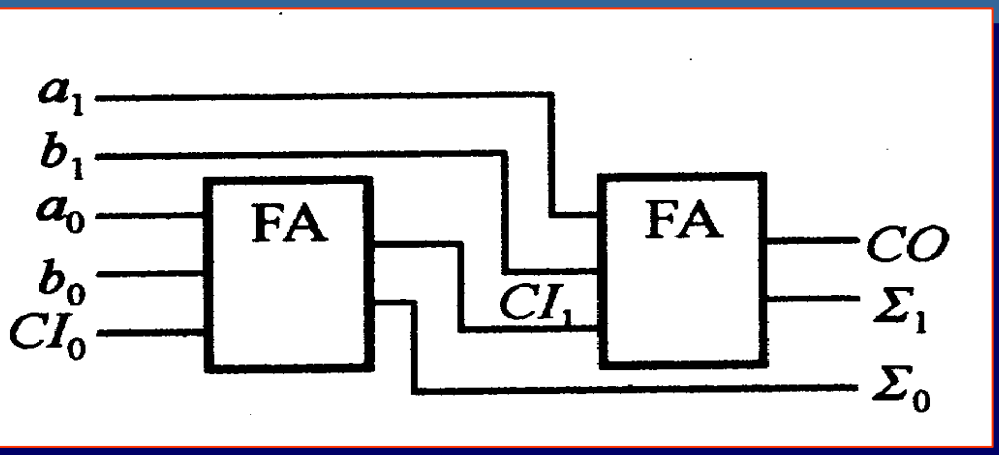
CI_i	x_i	y_i	CO_i	Σ_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

1位全加器



什么叫逻辑模块？

例：由1位全加器组成的2位加法器



逻辑模块化的设计思想

1、逻辑设计一般不宜从零开始，而是将现有模块组合修改从而产生新的电路。

2、逻辑设计要有清晰的思路，即要非常了解各个模块的性能（本课程之重点就是如何组合各模块）。

3、对于具体的模块，可不需过多考虑其内部电路，重点要了解端子上的特性。

常用组合逻辑模块

(教材P108 表3-3-8)

中规模集成电路（MSI）

类　型	类　型		型　号
全加器	2位二进制		74LS82
	4位二进制超前进位		74LS83,74HC283,CD4008B
	BCD码		CD4560B
数值比较器	4位		74LS85,74HC85,CD4063B
	8位		74LS521
	8位(OC输出)		74LS522
优先编码器	10线－4线	输出低电平有效	74LS147,74HC147,74HCT147
		输出高电平有效	CD40147B
	8线－3线	输出低电平有效	74LS148,74HC148
		三态输出低电平有效	74LS348
数据选择器	8选1	同相输出	74LS151,74HC151,CD4051B
		三态输出	74LS251,74HC251,74HCT251
	双4选1	同相输出	74LS153,74HC153,CD4052B
		三态输出	74LS253,74HC253,74HCT253
	四2选1	同相输出	74LS157,74HC157,74HCT157
		反相输出	74LS158,74HC158,74HCT158
		三态输出	74LS257,74HC257,74HCT257
译码器/驱动器	4线－16线	输出低电平有效	74LS154,74HC154,CD4515B
		输出高电平有效	CD4514B
	3线－8线	输出低电平有效	74LS138,74HC138,74HCT138
		三态输出	74LS538
	双2线－4线	输出低电平有效	74LS139,74HC139,74HCT139
		三态输出	74LS539
	BCD－七段码	OC输出低电平有效	74LS46,74LS47
		输出高电平有效	CD4055B
		OC输出高电平有效	74LS49
		输出高电平有效,内部上拉输出	74LS48
	BCD－十进制(4线－10线)	输出低电平有效	74LS42,74HC42,74HCT42
		输出高电平有效,无驱动	CD4028B
		三态输出,无驱动	74LS537

逻辑模块的详细应用资料

（数值比较器7485)

SN5485, SN54LS85, SN54S85
SN7485, SN74LS85, SN74S85
4-BIT MAGNITUDE COMPARATORS

description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

TEXAS INSTRUMENTS

SN5485, SN54LS85, SN54S85
SN7485, SN74LS85, SN74S85
4-BIT MAGNITUDE COMPARATORS

logic diagrams (positive logic)

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS INSTRUMENTS

SN5485, SN54LS85, SN54S85
SN7485, SN74LS85, SN74S85
4-BIT MAGNITUDE COMPARATORS

schematics of inputs and outputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

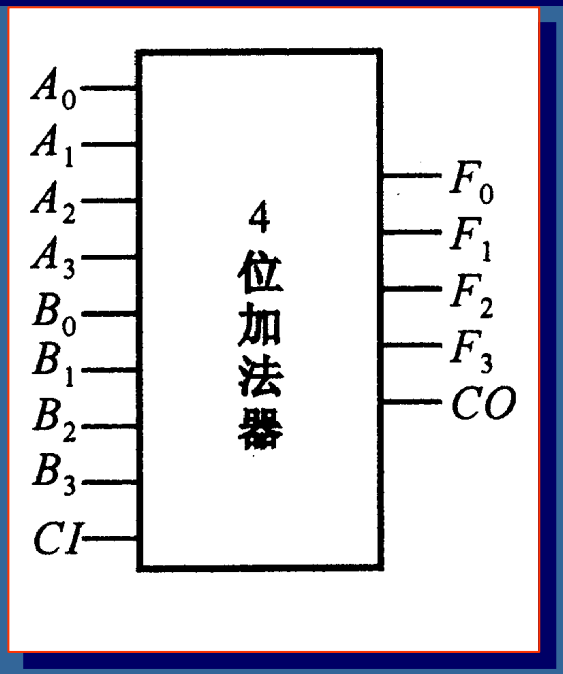
	SN54'/SN54S'	SN54LS'	SN74'/SN74S'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Interemitter voltage (see Note 2)	5.5		5.5		V
Operating free-air temperature range	−55 to 125		0 to 70		°C
Storage temperature range	−65 to 150		−65 to 150		°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A input in conjunction with its respective B input of the '85 and 'S85.

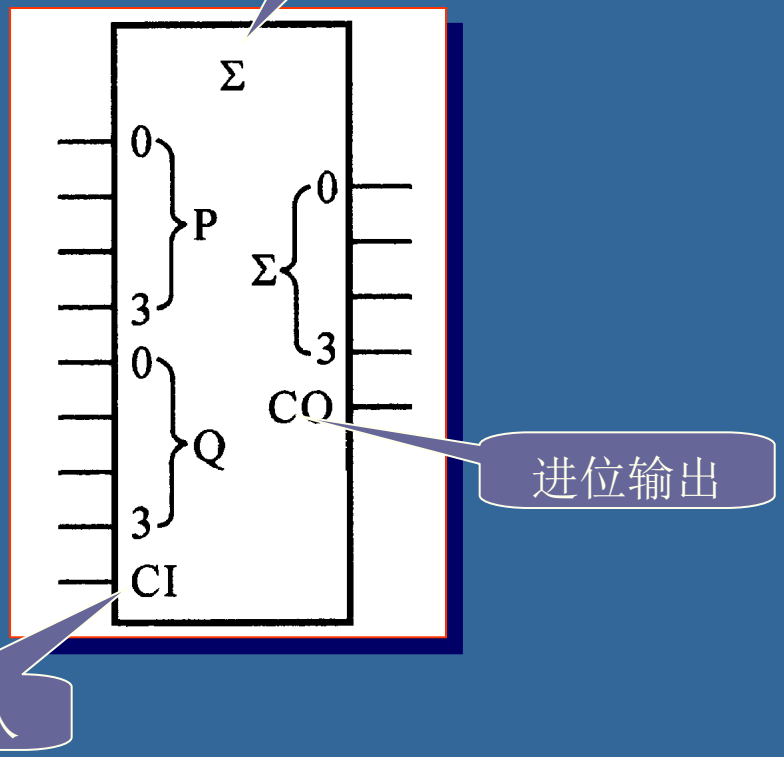
TEXAS INSTRUMENTS

并行加法器

框 图

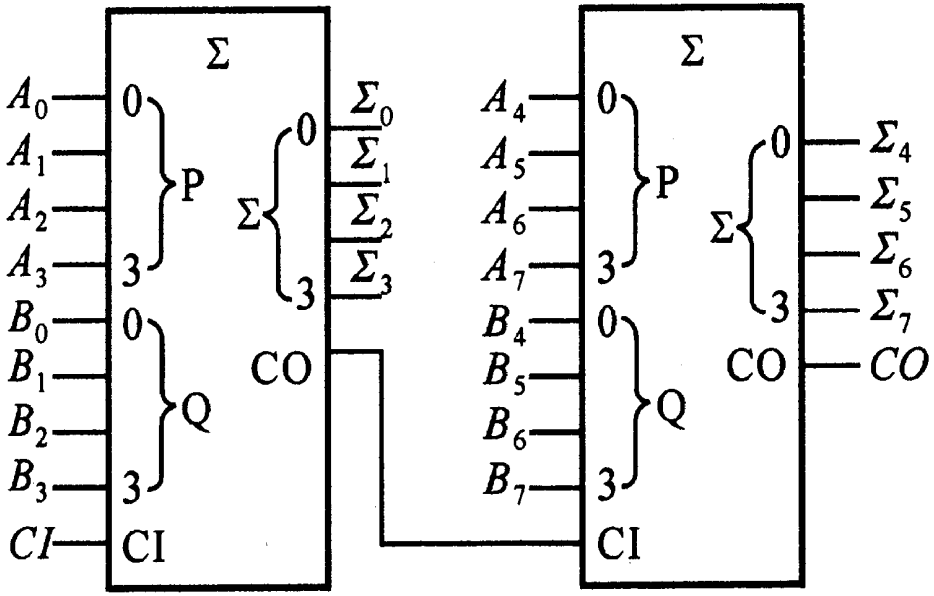


逻辑符号



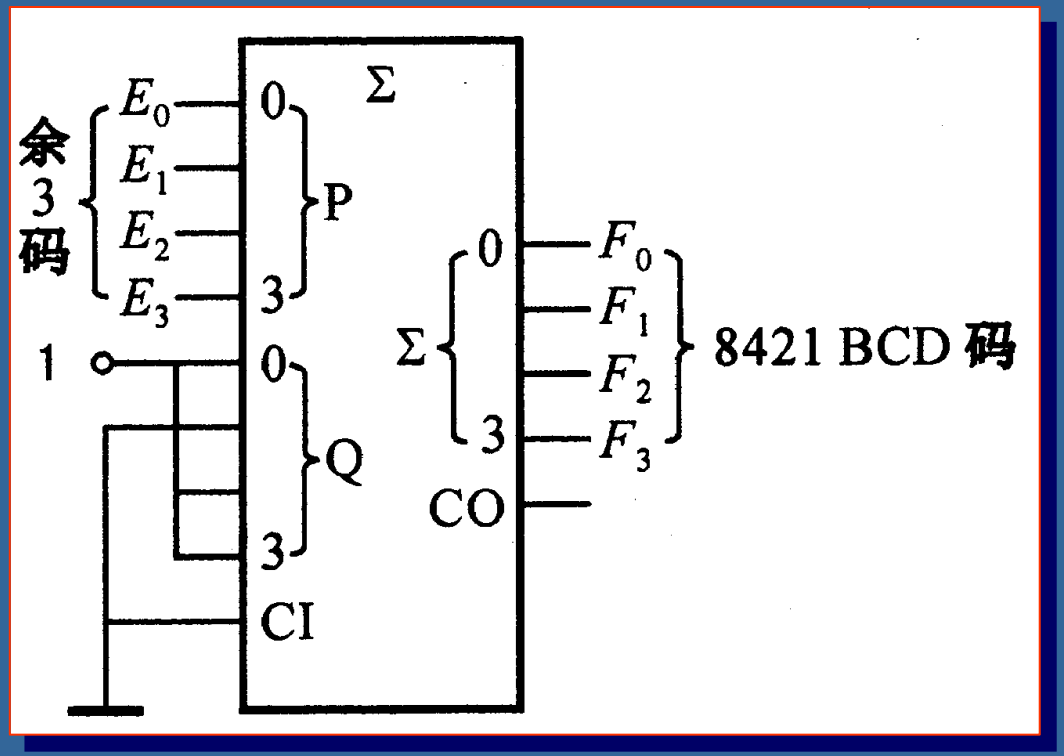
加法器的级联

四位加法器级连成八位加法器



加法器的应用（1）

例　1位余3码到1位8421BCD码转换

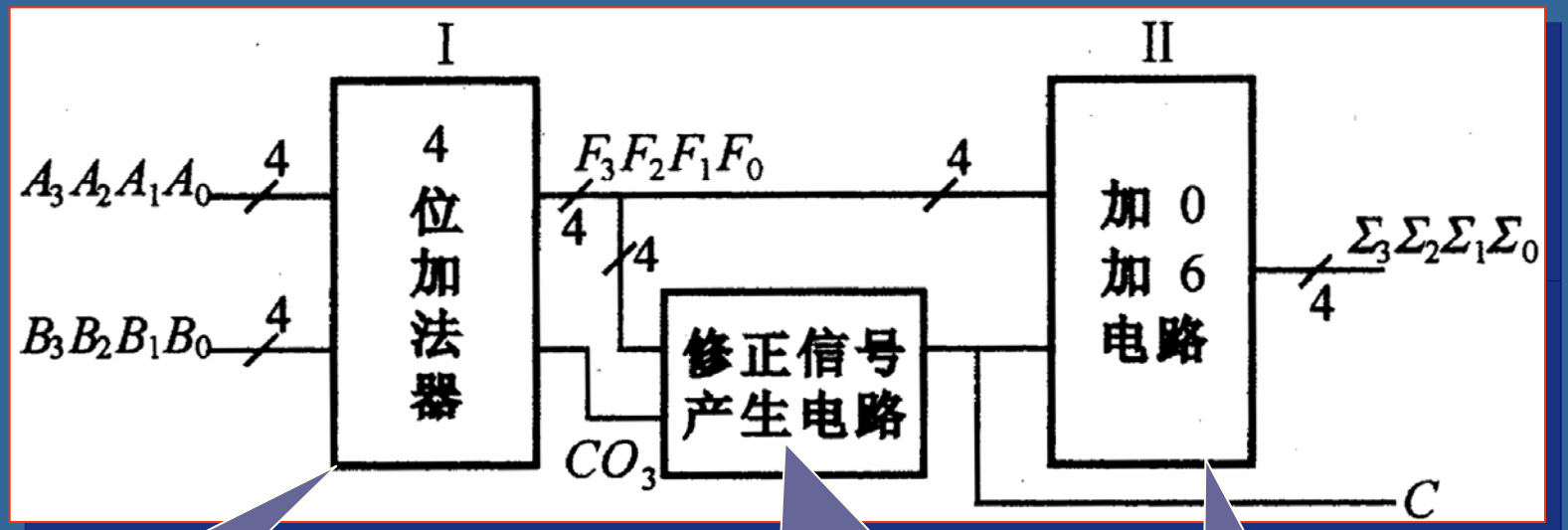


思考：1位8421BCD码转换到1位余3码如何接？

加法器的应用（2）

补充例题 用4位加法器构成1位8421BCD码加法器

1位8421BCD码加法运算规则



加法器I：进行二进制加法：
F=A+B

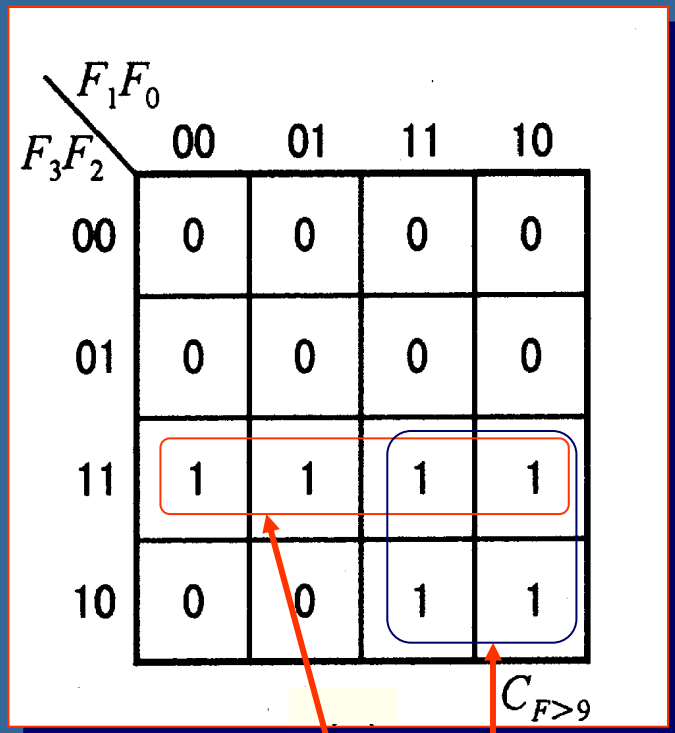
修正信号产生电路：判断是否要修正，修正C=1
$C=CO_3+C_F>9$

加法器II：修正加6,不修正加0。

加法器的应用（2）

修正信号产生修正信号C的求解

和数大于9的卡诺图



逻辑表达式

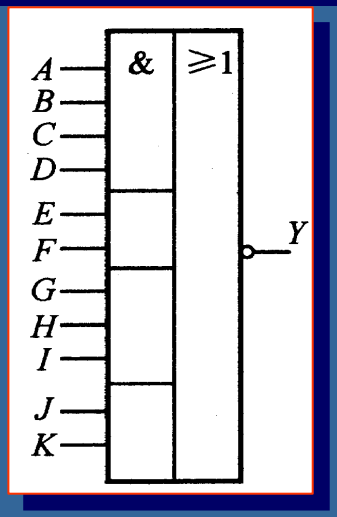
$$C = CO_3 + C_{F>9}$$
$$= CO_3 + F_3F_2 + F_3F_1$$

$$C_{F>9} = F_3F_2 + F_3F_1$$

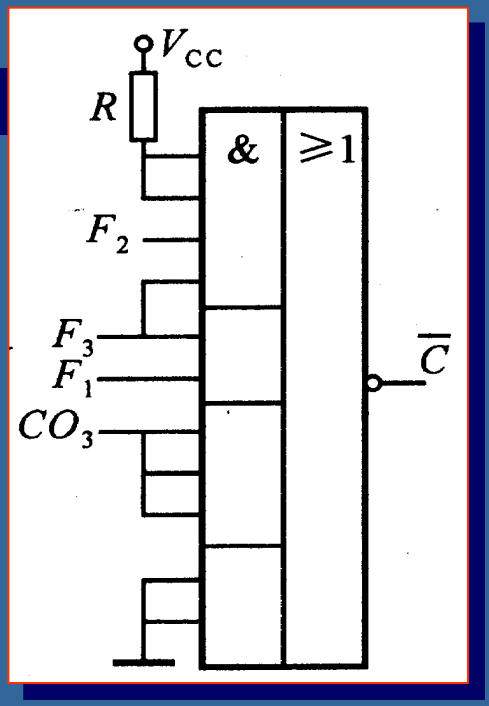
加法器的应用（2）

修正信号产生电路的实现（用与或非门74S64）

74S64



$$C = CO_3 + F_3F_2 + F_3F_1$$



与、或门多余输入端的处理方法

- 与门：悬空（CMOS与门除外）、接高电平、与有信号输入端并联。
- 或门：接低电平、与有信号输入端并联。

加法器的应用（2）

1位8421BCD码加法器