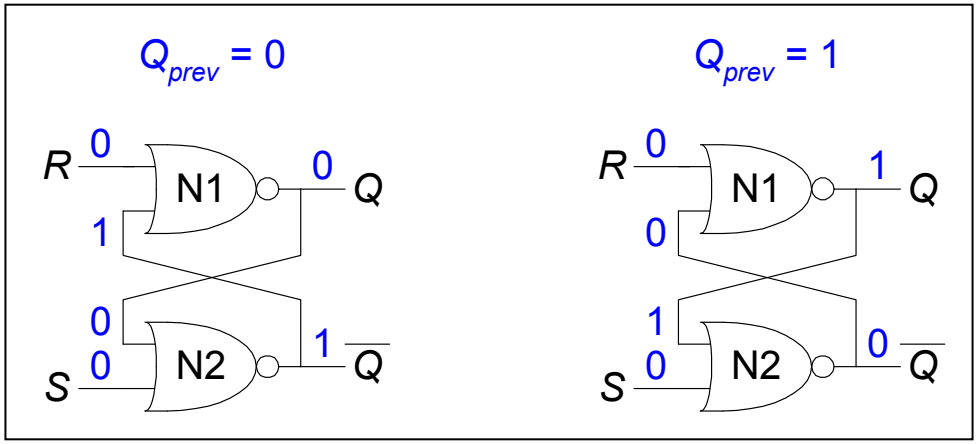
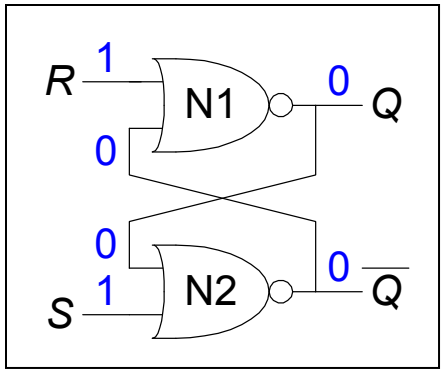
SR Latch Latch(SR锁存器)

– $S = 0, R = 0$: then $Q = Q_{prev}$ and $\overline{Q} = \overline{Q_{prev}}$ (memory!)

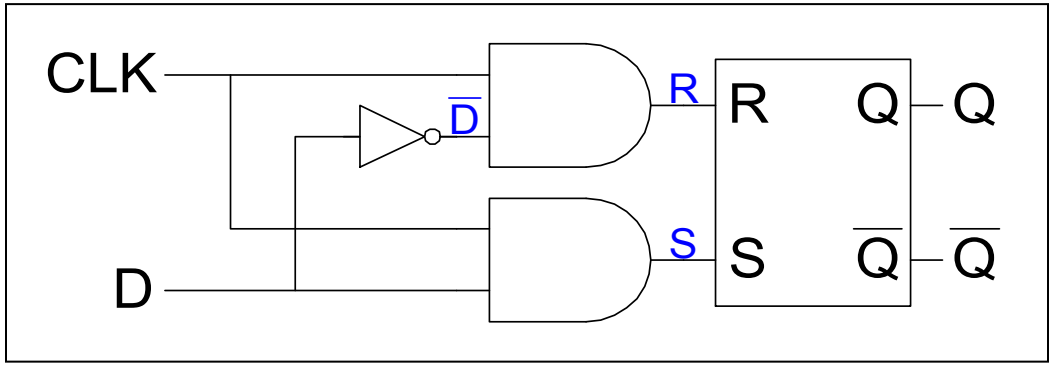


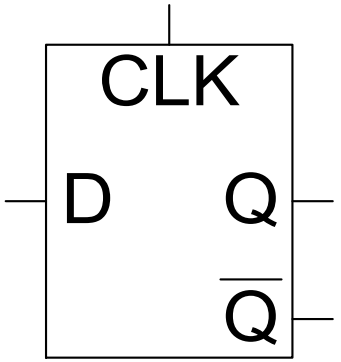
– $S = 1, R = 1$: then $Q = 0$ and $\overline{Q} = 0$ (invalid state: $\overline{Q} \neq$ NOT Q)



D Latch(D锁存器)

锁存器(Latch)是一种对脉冲电平敏感的存储单元电路，它们可以在特定输入脉冲电平作用下改变状态。锁存器的最主要作用是缓存，把信号暂存以维持某种电平状态,其次完成高速的控制器与慢速的外设的不同步问题，再其次是解决驱动的问题，最后是解决一个 I/O 口既能输出也能输入的问题。锁存器是利用电平控制数据的输入，包括不带使能控制的锁存器和带使能控制的锁存器。



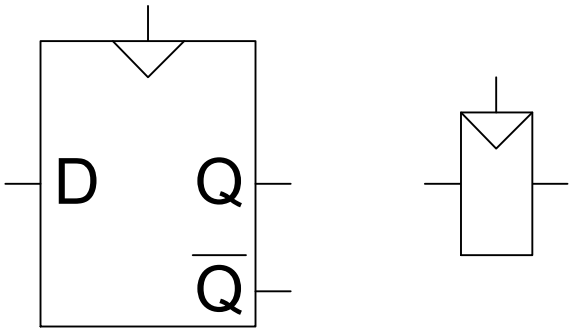


CLK	*D*	$\overline{D}$	*S*	*R*	*Q*	$\overline{Q}$
0	X	$\overline{X}$	0	0	Q_{prev}	$\overline{Q}_{prev}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0

D Flip-Flop (D触发器)。

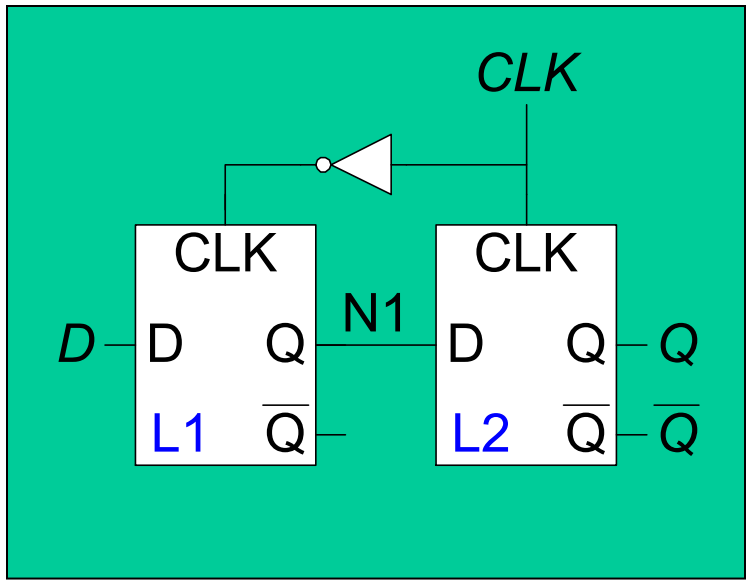
- 具有记忆功能, 时钟边沿触发来更新输出数据的
- Two inputs: *CLK*, *D*
- *Function*
  - The flip-flop "samples" *D* on the rising edge of *CLK*
    - When *CLK* rises from 0 to 1, *D* passes through to *Q*
    - Otherwise, *Q* holds its previous value
  - *Q* changes only on the rising edge of *CLK*
- A flip-flop is called an *edge-triggered* (时钟边沿触发)device because it is activated on the clock edge

D Flip-Flop Symbols



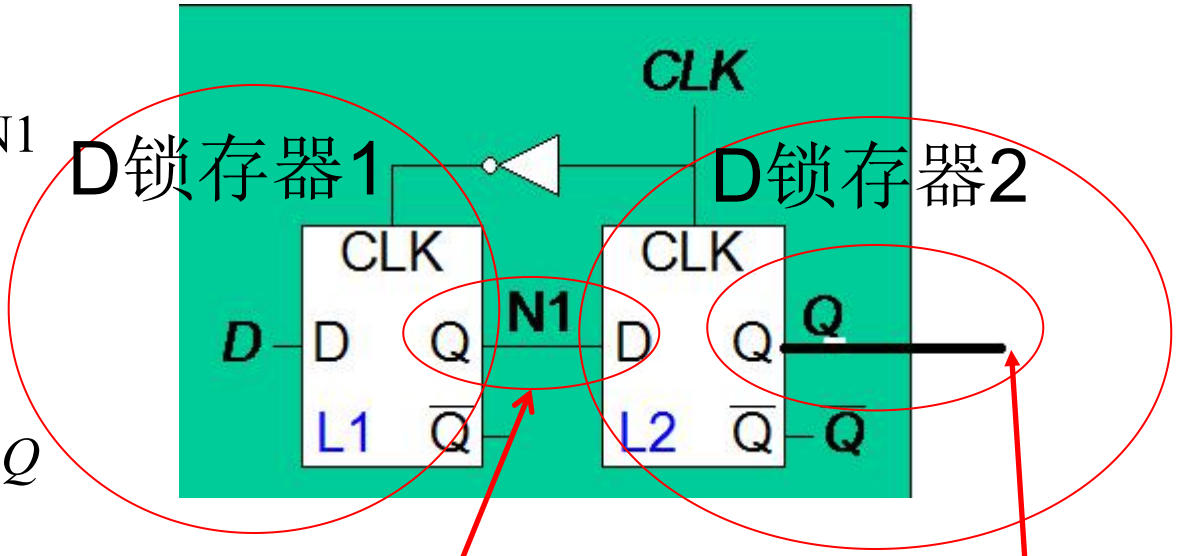
D Flip-Flop Internal Circuit

- Two back-to-back latches (L1 and L2) controlled by complementary clocks
- When *CLK* = 0
  - L1 is transparent
  - L2 is opaque
  - *D* passes through to N1
- When *CLK* = 1
  - L2 is transparent
  - L1 is opaque
  - N1 passes through to *Q*
- Thus, on the edge of the clock (when *CLK* rises from 0→1)
  - *D* passes through to *Q*



D Flip-Flop (D触发器)

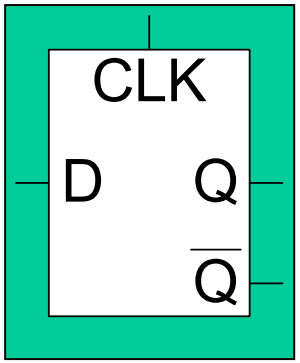
- Two back-to-back latches (L1 and L2) controlled by complementary clocks
- When *CLK* = 0
  - L1 is transparent
  - L2 is opaque
  - *D* passes through to N1
- When *CLK* = 1
  - L2 is transparent
  - L1 is opaque
  - N1 passes through to *Q*

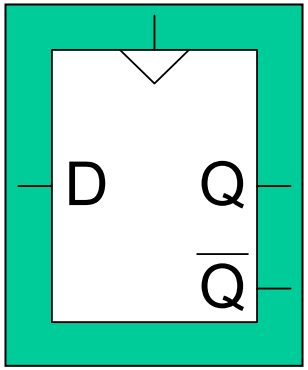


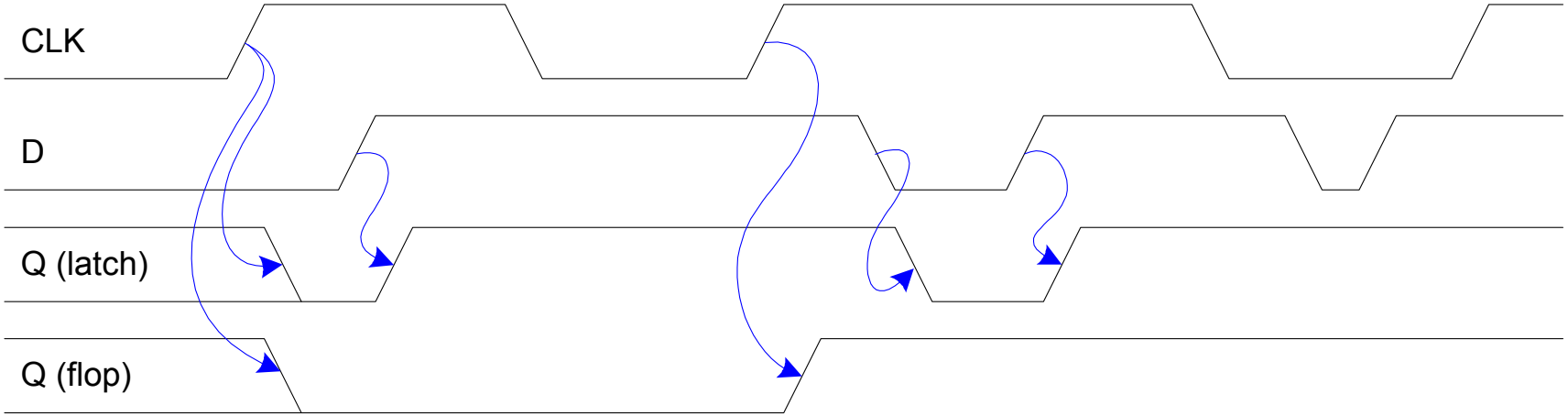
在上个时钟结束时，数据保存在这里

在下个时钟沿到来后，数据从这里输出

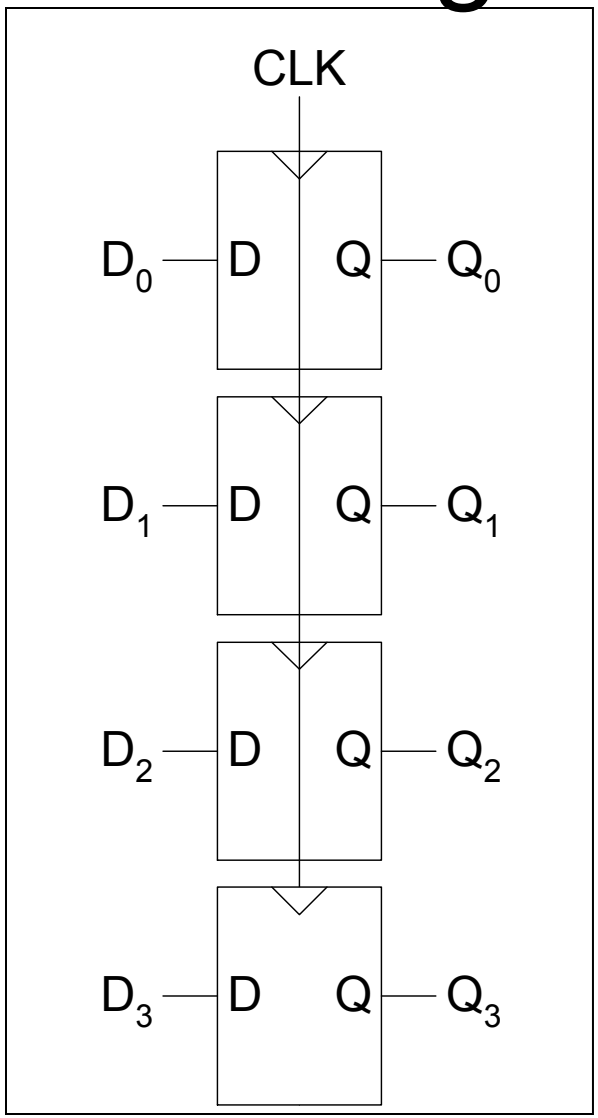
D Latch vs. D Flip-Flop

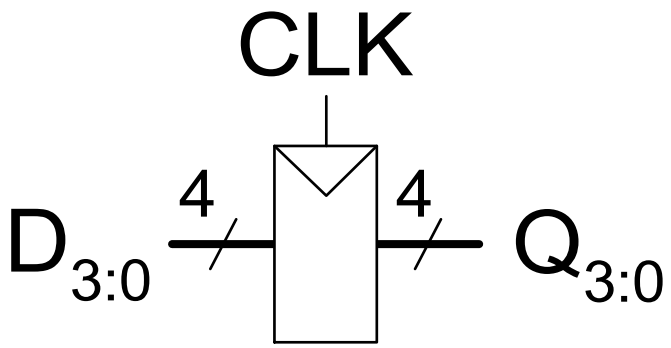






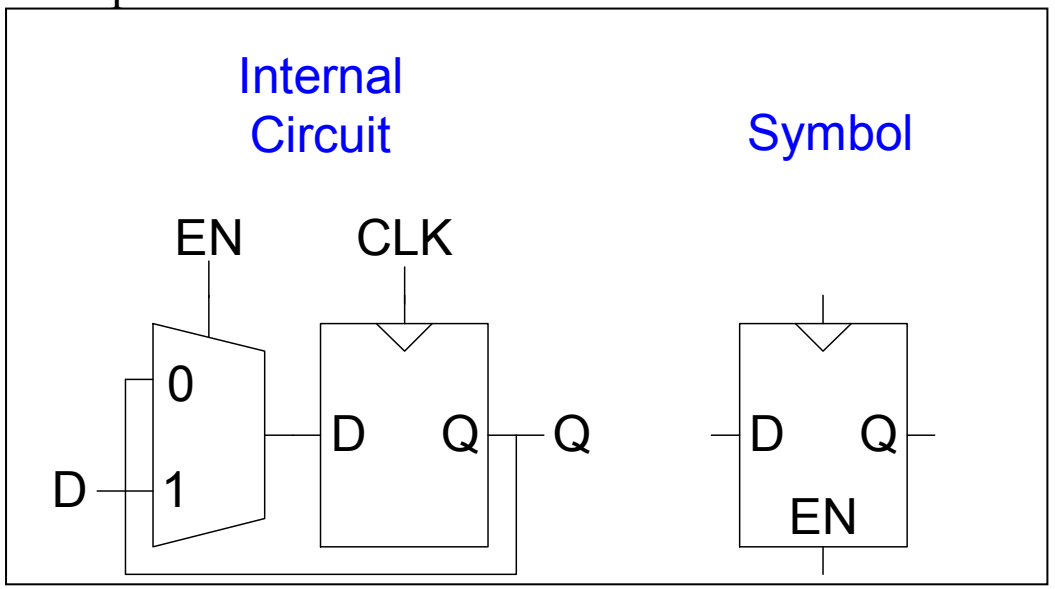
4-bit Registers (4-位寄存器)





Enabled Flip-Flops

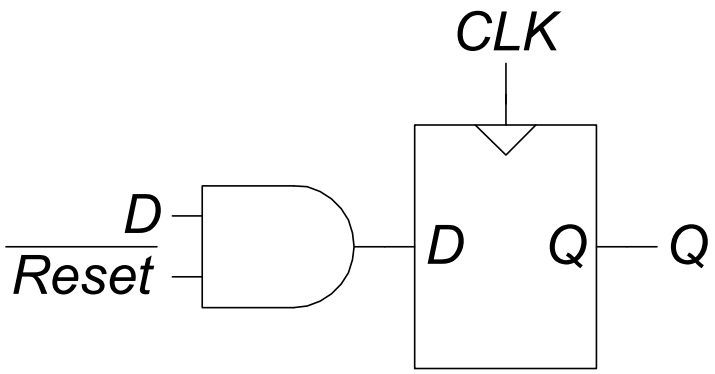
- Inputs: *CLK*, *D*, *EN*
  - The enable input (*EN*) controls when new data (*D*) is stored
- Function
  - *EN* = 1
    - *D* passes through to *Q* on the clock edge
  - *EN* = 0
    - the flip-flop retains its previous state



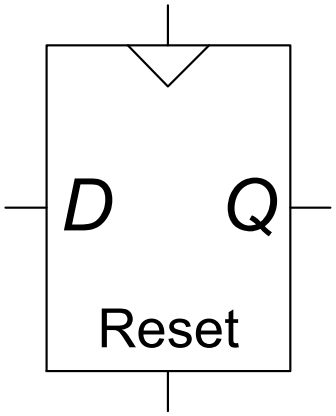
Resettable Flip-Flops

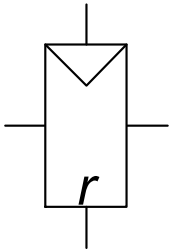
- Inputs: *CLK*, *D*, *Reset*
- Function:
  - *Reset* = 1 (➔ $\overline{Reset} = 0$)
    - *Q* is forced to 0
  - *Reset* = 0
    - the flip-flop behaves like an ordinary D flip-flop

Internal Circuit



Symbols





Settable Flip-Flops

- Inputs: *CLK*, *D*, *Set*
- Funtion:
  - *Set* = 1
    - *Q* is set to 1
  - *Set* = 0
    - the flip-flop behaves like an ordinary D flip-flop

Symbols