```
BEGIN leon2

## Peripheral Options
OPTION IPTYPE = PROCESSOR
OPTION IMP_NETLIST = TRUE
OPTION HDL = MIXED
OPTION IP_GROUP = USER
OPTION ARCH_SUPPORT_MAP = (virtex6 = DEVELOPMENT)

## Bus Interfaces
BUS_INTERFACE BUS = D_AXI, BUS_STD = AXI, BUS_TYPE = MASTER

## Generics for VHDL or Parameters for Verilog
PARAMETER C_D_AXI_PROTOCOL = AXI4, TYPE = NON_HDL, ASSIGNMENT = CONSTANT, DT = STRING,
US = D_AXI
PARAMETER C_D_AXI_ID_WIDTH = 1, ASSIGNMENT = CONSTANT, DT = INTEGER, BUS = D_AXI
PARAMETER C_D_AXI_USER_WIDTH = 1, ASSIGNMENT = CONSTANT, DT = INTEGER, BUS = D_AXI
PARAMETER C_D_AXI_ADDR_WIDTH = 32, ASSIGNMENT = CONSTANT, DT = INTEGER, BUS = D_AXI
PARAMETER C_D_AXI_DATA_WIDTH = 32, ASSIGNMENT = CONSTANT, DT = INTEGER, BUS = D_AXI

## Ports
PORT clk = "", DIR = I, SIGIS = CLK
PORT reset = "", DIR = I, SIGIS = RST
PORT resetn = "", DIR = I, SIGIS = RST
```