

go = Rd / Wv

① hit & wr & valid

COMP - WR

Done = hit & valid  
stall\_out =  $\sim(\text{hit} \& \text{valid})$   
Cache Hit = hit & valid  
enable = 1  
comp = 1  
write = wr

mem\_offset = mem\_offset + add  
cache\_offset = cache\_offset + add  
stall\_out = 1  
mem\_wv = 1  
enable = 1  
select\_vd = 1

FINISH

enable = 1  
Done = 1

go to state

COMP

①, ②, ③  
all false

Done = hit & Rd & valid  
stall\_out =  $\sim(\text{hit} \& \text{Rd} \& \text{valid})$  & go  
Cache Hit = hit & go & valid  
enable = 1, comp = 1  
write = wr

②  $\sim(\text{hit})$  & dirty & valid  
& go

MEM - WB

(&offset - cache)

&offset - cache

cache - offset -  
offset -  
mem - offset -  
offset -  
mem -

cache - res = offset - cache + 1  
mem - res = offset - mem + 1

Cache - offset - add = cache - res [1:07]  
mem - offset - add = mem - res [1:07]

stall\_out = 1  
mem\_rd =  $\sim(\text{offset - cache} [1])$   
enable = 1  
select\_wb = Rd / (wr & (offset - cache != reg\_addr))  
comp =  $\sim(\text{offset - cache} = 0)$   
write = (offset - mem [1])  
cache\_offset = (offset - mem [1]) ? (Cache - offset - add : mem\_offset - mem) ?  
offset - mem : mem\_offset - add

Date