Cycle	Instruction retired	Reason
1	NOP	No instruction retired yet
2	NOP	No instruction retired yet
3	NOP	No instruction retired yet
4	NOP	No instruction retired yet
5	lbi r0, 0	Instruction enter write back stage
6	lbi r5, 43	instruction enter write back stage
7	lbi r6, 43	instruction enter write back stage
8	lbi r7, 43	instruction enter write back stage
9	ld r1, r0, 0	instruction enter write back stage
10	no instruction retired	st r5, r1, 0 was stalled in cycle 7, 8 and 9 because it have data dependency with ld r1, r0, 0 (RAW on r1)
11	no instruction retired	st r5, r1, 0 was stalled in cycle 7, 8 and 9 because it have data dependency with ld r1, r0, 0 (RAW on r1)
12	no instruction retired	st r5, r1, 0 was stalled in cycle 7, 8 and 9 because it have data dependency with ld r1, r0, 0 (RAW on r1)
13	st r5, r1, 0	instruction enter write back stage
14	ld r1, r0, 2	instruction enter write back stage
15	no instruction retired	st r6, r1, 1 was stalled in cycle 12, 13 and 14 because it have data dependency with ld r1, r0, 2 (RAW on r1)
16	no instruction retired	st r6, r1, 1 was stalled in cycle 12, 13 and 14 because it have data dependency with ld r1, r0, 2 (RAW on r1)
17	no instruction retired	st r6, r1, 1 was stalled in cycle 12, 13 and 14 because it have data dependency with ld r1, r0, 2 (RAW on r1)
18	st r6, r1, 1	instruction enter write back stage
19	ld r1, r0, 4	instruction enter write back stage
20	no instruction retired	st r7, r1, 1 was stalled in cycle 17, 18 and 19 because it have data dependency with ld r1, r0, 4 (RAW on r1)

21	no instruction retired	st r7, r1, 1 was stalled in cycle 17, 18 and 19 because it have data dependency with ld r1, r0, 4 (RAW on r1)
22	no instruction retired	st r7, r1, 1 was stalled in cycle 17, 18 and 19 because it have data dependency with ld r1, r0, 4 (RAW on r1)
23	st r7, r1, 1	instruction enter write back stage
24	halt	program halt
	(we don't have reg bypass so we are stalling an additional cycle for each data hazard here)	