

(1)

```
entity myGenent is
    port( clk: in std_logic;
          tst: in std_logic;
          q : out std_logic(2 downto 0);
    end myGenent;
```

Architecture behavioral of myGenent is

```
type state_type is (S0, S1, S2, S3);
signal fc: std_logic;
signal s_teg, s_next: state_type;
signal c_teg, c_nxt: Unsigned(3 downto '0');
begin
```

togi: process (clk)

```
begin
    if (rising_edge(clk)) then
        c_teg <= c_nxt;
        s_teg <= s_next;
    end if;
end process;
```

state: process (s\_teg, tst) begin

```
case s_teg is
    when S0 => if tst = '1' then
        s_next <= S0;
        else
            s_next <= S1;
        end if;
    when S1 => if tst = '1' then
        s_nxt <= S0;
        elsif (fc = '1') then
            s_nxt <= S2;
        else
            s_nxt <= S3;
        end if;
```

```
when s3 => if fst = '1' then  
    s_next <= s0;  
else if (fc = '1') then  
    s_next <= s0;  
else  
    s_next <= s3;  
end if;  
end case;  
end process state;
```

fc <= '1' when c-reg = "1010" else  
 '0';

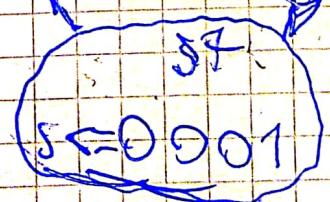
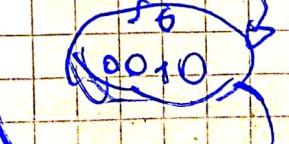
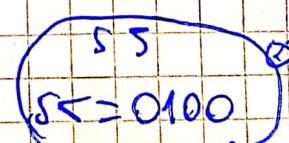
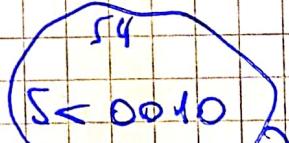
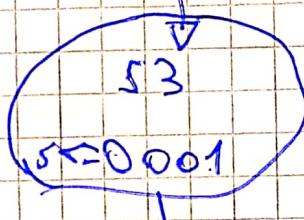
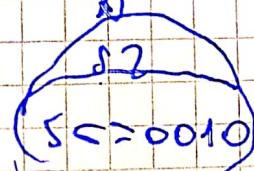
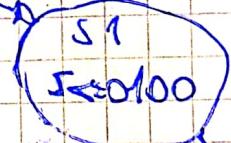
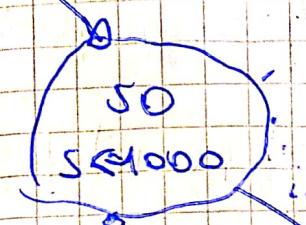
c-reg = "0000" when (fc = '1' || fst = '1'), else  
 c-reg + 1;

q <= "000" when s-reg = s0 else  
 "100" when s-reg = s1 else  
 "010" when s-reg = s2 else  
 "111";

end architecture behavioral;

② ③

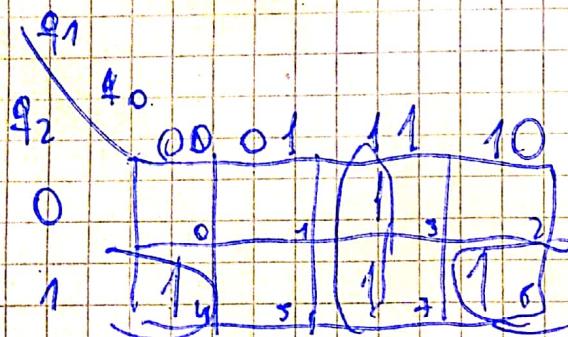
HTST



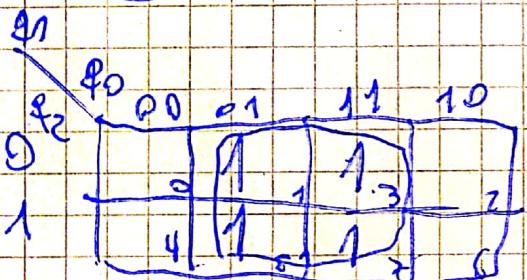
b)

E.A.	$q_2 q_1 q_0$	F	$q_2 q_1 q_0$	S	$q_3 q_2 q_1 q_0$
50	0 0 0	0 0 1	1 0 0 0		
51	0 0 1	0 1 1	0 1 0 0		
52	0 1 1	1 1 1	0 0 1 0		
53	1 1 1	1 1 0	0 0 0 1		
54	1 1 0	1 0 0	0 1 1 0		
55	1 0 0	1 0 1	0 1 0 0		
56	1 0 1	0 1 0	0 0 1 0		
57	0 1 0	0 0 0	0 0 0 1		

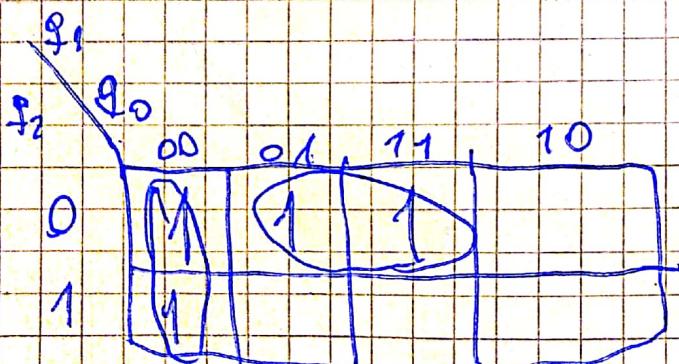
Milizanda flip-flops tipo D  
donde  $q^* = d$



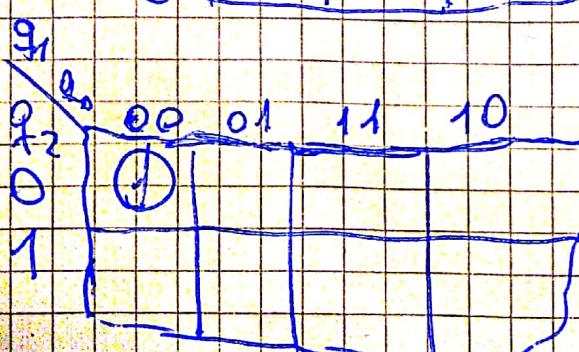
$$d_2 = \bar{q}_0 \cdot q_1 + q_2 \cdot \bar{q}_0$$



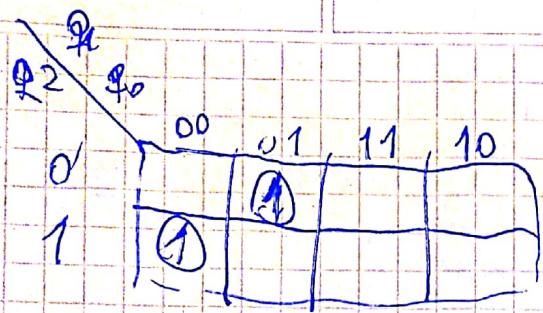
$$d_1 = q_0$$



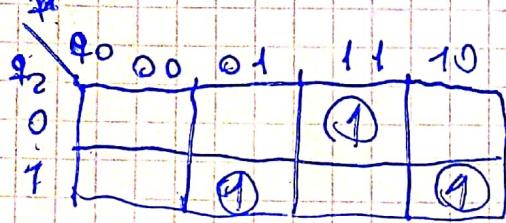
$$d_0 = \bar{q}_0 \cdot \bar{q}_1 + \bar{q}_2 \cdot q_0$$



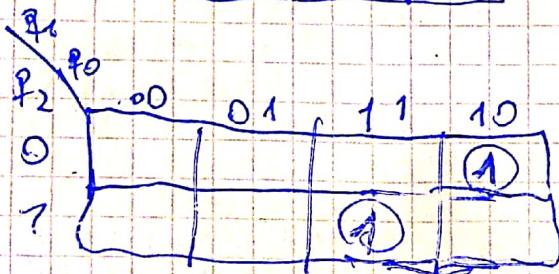
$$S_3 = \bar{q}_2 \cdot \bar{q}_1 \cdot \bar{q}_0$$



$$S_2 = \overline{q}_2 \cdot \overline{q}_1 \cdot q_0 + q_2 \cdot \overline{q}_1 \cdot \overline{q}_0$$



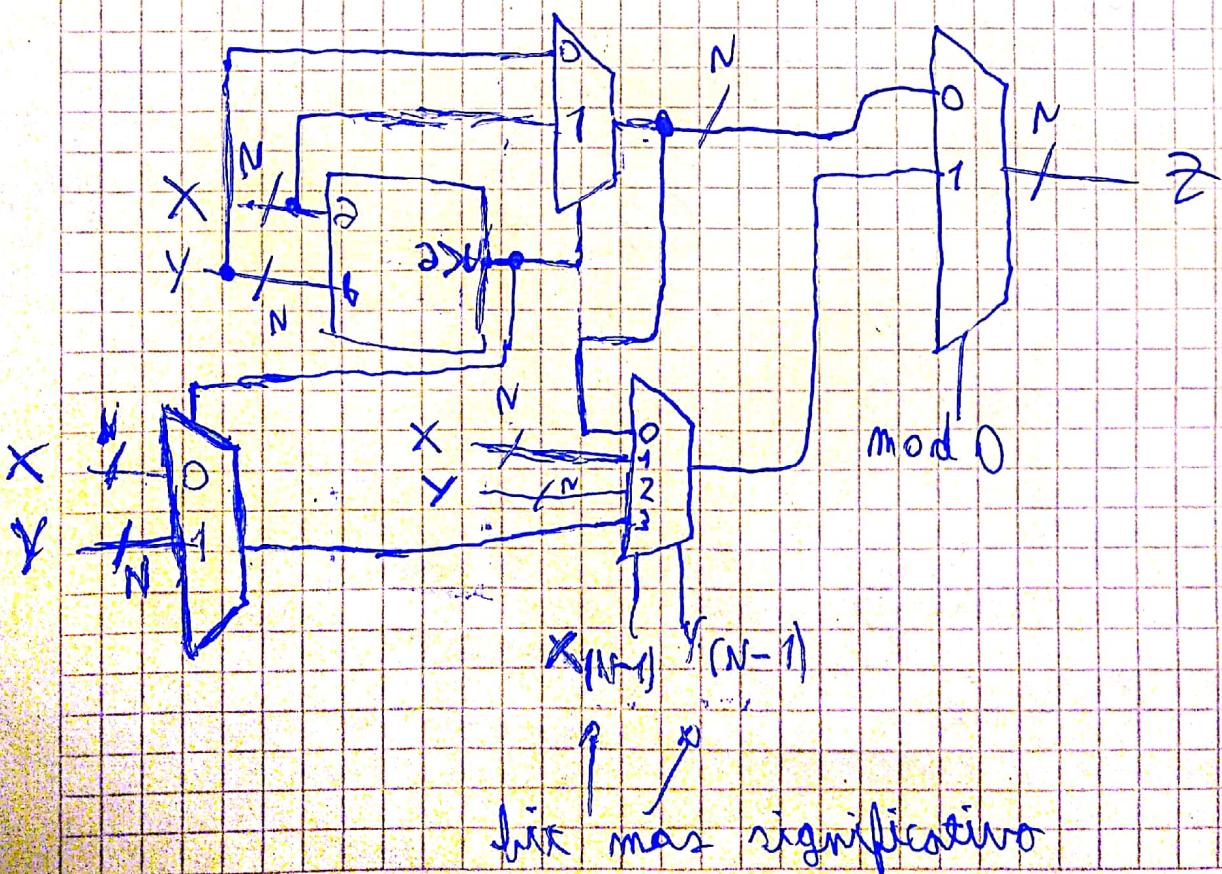
$$S_1 = q_2 \cdot \overline{q}_1 \cdot q_0 + \overline{q}_2 \cdot q_1 \cdot q_0 + q_2 \cdot q_1 \cdot \overline{q}_0$$



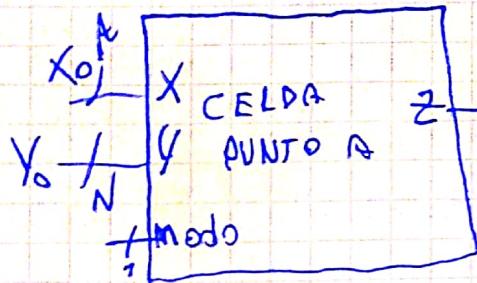
$$S_0 = q_2 \cdot q_1 \cdot q_0 + \overline{q}_2 \cdot \overline{q}_1 \cdot \overline{q}_0$$

$\oplus S_1 = S_0$

(3) @



b



$Z_0$  N

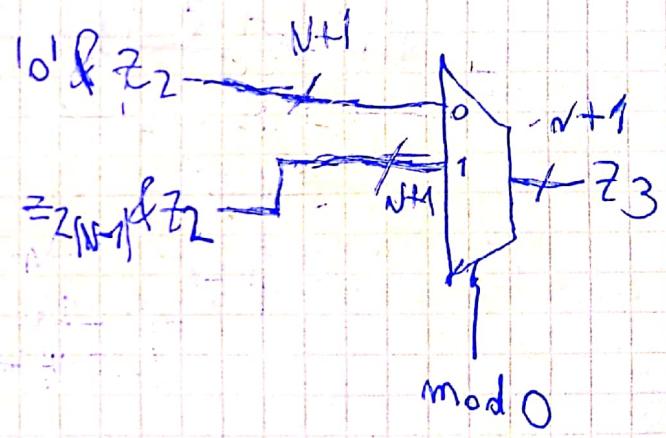


$Z_2$



$Z_1$

c



mod 0