Plantilla Módulo VHDL

```
        ------------------------------------------------LIBRERÍAS-----------------------------------------------------
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;                                       --Si es que se utiliza

        ------------------------------------------------ENTITY-------------------------------------------------------
ENTITY myComponente IS

        GENERIC(
                        parametro1 : NATURAL := valorDefaultP1;
                        parametro2 : INTEGER := valorDefaultP2
                        );

        PORT            (
                        entrada1                : IN    STD_LOGIC;
                        entrada2                : IN    STD_LOGIC_VECTOR( n_msb DOWNTO n_lsb );
                        salida1, salida2        : OUT STD_LOGIC;
                        salida3                 : OUT STD_LOGIC_VECTOR( n_msb DOWNTO n_lsb )
                                );

END ENTITY myComponente;                        --end;  --end myComponente;         --end entity;


        ------------------------------------------- ARCHITECTURE-------------------------------------------------
ARCHITECTURE A_myComponente OF myComponente IS

        SIGNAL      signal_1 : STD_LOGIC;
        SIGNAL      signal_1 : STD_LOGIC_VECTOR( n_msb DOWNTO n_lsb );
        SIGNAL      signal_1 : UNSIGNED ;
        SIGNAL      signal_1 : SIGNED ;

        BEGIN

                ------------------------------------  WITH/SELECT ------------------------------------
                WITH signal_entrada SELECT
                        signal_salida <=        valor_signal_entrada1 WHEN valorConstante1,
                                                valor_signal_entrada2 WHEN valorConstante2,
                                                (...)
                                                valor_signal_entradaN  WHEN  OTHERS;

                ------------------------------------ WHEN/ELSE ------------------------------------
                signal_salida <=        valor_signal_entrada1 WHEN condcion1 ELSE
                                        valor_signal_entrada2 WHEN condcion2 ELSE
                                        (...)
                                        valor_signal_entradaN;

                ------------------------------- UNSIGNED/SIGNED -------------------------------
                TO_UNSIGNED     ( valorInt, tamaño )
                TO_SIGNED       ( valorInt, tamaño )
                TO_INTEGER  ( valorSignedUnSigned )
```

```
---------------------------------- INSTANCIACION ----------------------------------
etiqueta: ENTITY WORK.nombreEntity( nombreArchitecture )
GENERIC MAP
(
        parametroInstancia1 => valorConstante1,
        parametroInstancia2 => valorConstante2
)
PORT MAP
(
        entradasInstancia => signals_entradas,
        salidasInstancia  => signals_salidas
);

------------------------------------- PROCESS -------------------------------------
PROCESS( listaEntradas_Signals_Leídas )
        BEGIN

        ---------------------------------------IF/ELSE---------------------------------------
        IF condicion1 THEN
                bloque1;
        ELSE
                bloque2;
        END IF;

        ---------------------------------------IF/ELSIF---------------------------------------
        IF      condicion1 THEN
                bloque1;
        ELSIF condicion2 THEN
                bloque2;
        ELSIF condicion3 THEN
                bloque3;
        (...)
        ELSE
                bloqueN;
        END IF;

        ---------------------------------------CASE/WHEN---------------------------------------
        CASE signal_entrada IS
                WHEN valorConstante1 =>
                        bloque1;
                WHEN valorConstante2 =>
                        bloque2;
                (...)
                WHEN OTHERS         =>
                        bloqueN;
        END CASE;


END PROCESS;


END ARCHITECTURE A_myComponente;      --end;  end A_myComponente;  end ARCHITECTURE;
```

Plantilla TestBench VHDL

```
        ----------------------------------------------LIBRERÍAS----------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

        ----------------------------------------------ENTITY----------------------------------------------
ENTITY myComponente_TB IS
END myComponente_TB;

        ---------------------------------------- ARCHITECTURE----------------------------------------
ARCHITECTURE A_myComponente OF myComponente IS

        signal s_entrada1, s_salida1, s_salida2         : STD_LOGIC;
        signal s_entrada2                               : STD_LOGIC_VECTOR( n_msb DOWNTO n_lsb );
        signal s_salida3                                : STD_LOGIC_VECTOR( n_msb DOWNTO n_lsb );

BEGIN
                ---------------------------------- INSTANCIACION ----------------------------------
                etiqueta: ENTITY WORK.myComponente( A_myComponente )
                GENERIC MAP
                (
                        parametro1 => valorConstante1,
                        parametro2 => valorConstante2
                )
                PORT MAP
                (
                        entrada1                => s_entradas1,
                        entrada2                => s_entradas2,
                        salida1         => s_salida1,
                        salida2         => s_salida2,
                        salida3         => s_salida3
                );

                ------------------------------------ PROCESS ------------------------------------
                PROCESS
                BEGIN

                        s_entradas1 <= ' ';
                        s_entradas2 <= " ";
                        WAIT FOR 10ns;

                        (...)

                        s_entradas1 <= ' ';
                        s_entradas2 <= " ";
                        WAIT;

                END PROCESS;

END;
```