

Hoja de datos para la realización de parciales/finales de Informática II con el LPC845

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1. Bloque de registros SYSCON

- Habilitación del CLK y reset de los periféricos (detalle más adelante en esta sección):

Table 124. Register overview: System configuration (base address 0x4004 8000)

Name	Access	Offset	Description
SYSAHBCLKCTRL0	R/W	0x080	System clock control 0
SYSAHBCLKCTRL1	R/W	0x084	System clock control 1
PRESETCTRL0	R/W	0x088	Peripheral reset control 0

- Selección del CLK de la UART (detalle en la sección **USARTs**)

UART0CLKSEL	R/W	0x090	Function clock source select for UART0
UART1CLKSEL	R/W	0x094	Function clock source select for UART1
UART2CLKSEL	R/W	0x098	Function clock source select for UART2
UART3CLKSEL	R/W	0x09C	Function clock source select for UART3
UART4CLKSEL	R/W	0x0A0	Function clock source select for UART4

- Selección del CLK del ADC (detalle en la sección **ADC**)

ADCCLKSEL	R/W	0x064	ADC clock source select
ADCCLKDIV	R/W	0x068	ADC clock divider

- Selección de pin como fuente de interrupción externa (detalle en la sección **Interrupciones**)

PINTSEL0	R/W	0x178	GPIO Pin Interrupt Select register 0
PINTSEL1	R/W	0x17C	GPIO Pin Interrupt Select register 1
PINTSEL2	R/W	0x180	GPIO Pin Interrupt Select register 2
PINTSEL3	R/W	0x184	GPIO Pin Interrupt Select register 3
PINTSEL4	R/W	0x188	GPIO Pin Interrupt Select register 4
PINTSEL5	R/W	0x18C	GPIO Pin Interrupt Select register 5
PINTSEL6	R/W	0x190	GPIO Pin Interrupt Select register 6
PINTSEL7	R/W	0x194	GPIO Pin Interrupt Select register 7

1.1. Detalle registro SYSAHBCLKCTRL0

Table 146. System clock control 0 register (SYSAHBCLKCTRL0, address 0x4004 8080) bit description

Bit	Symbol	Value	Description	Reset value
7	SWM	0	Enables clock for switch matrix.	1
		1	Disable	
		1	Enable	
...				
14	UART0	0	Enables clock for USART0.	0
		1	Disable	
		1	Enable	
15	UART1	0	Enables clock for USART1.	0
		1	Disable	
		1	Enable	
16	UART2	0	Enables clock for USART2.	0
		1	Disable	
		1	Enable	
...				
18	IOCON	0	Enables clock for IOCON block.	0
		1	Disable	
		1	Enable	
...				
20	GPIO1	0	Enables clock for GPIO1 port registers.	0
		1	Disable	
		1	Enable	
...				
24	ADC	0	Enables clock to ADC.	0
		1	Disable	
		1	Enable	
...				
27	DAC0	-	Enable clock for DAC0	0
		0	Disable	
		1	Enable	
28	GPIO_INT	0	Enable clock for GPIO pin interrupt registers.	0
		1	Disable	
		1	Enable	

1 habilita el CLK del periférico

0 deshabilita el CLK del periférico

1. Bloque de registros **IOCON**

- Selección del modo de funcionamiento de cada uno de los pines (se ponen algunos a modo de ejemplo)



2.1. Detalle del registro **PIO0_1** a modo de ejemplo (asumir que todos los registros de configuración de pines tienen los mismos bits de configuración):

Table 211. **PIO0_1** register (PIO0_1, address 0x4004 402C) bit description

Bit	Symbol	Value	Description	Reset value
2:0	-		Reserved.	0
4:3	MODE	0x0	Selects function mode (on-chip pull-up/pull-down resistor control).	FAIM value dependent
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	1
6	INV	0	Disable.	1
		1	Enable.	
9:7	-	0	Invert input	0
		0	Input not inverted (HIGH on pin reads as 1; LOW on pin reads as 0).	0
		1	Input inverted (HIGH on pin reads as 0, LOW on pin reads as 1).	
10	OD	-	Reserved.	0b001
10	OD	0	Open-drain mode.	0
		1	Open-drain mode enabled.	

Modo (salida)

0: Sin Open Drain
1: Open Drain activado

Modo (entrada)

- 0: Sin pull-up ni pull-down
- 1: Pull-Down
- 2: Pull-up
- 3: Modo repetidor

Table 198. Register overview: I/O configuration (base address 0x4004 4000)

Name	Access	Address offset	Description
PIO0_17	R/W	0x000	I/O configuration for pin PIO0_17/ADC_9/DACOUT0
PIO0_13	R/W	0x004	I/O configuration for pin PIO0_13/ADC_10
PIO0_12	R/W	0x008	I/O configuration for pin PIO0_12
PIO0_5	R/W	0x00C	I/O configuration for pin PIO0_5/RESET
PIO0_4	R/W	0x010	I/O configuration for pin PIO0_4/ADC_11/TRSTN/WAKEUP
PIO0_3	R/W	0x014	I/O configuration for pin PIO0_3/SWCLK
PIO0_2	R/W	0x018	I/O configuration for pin PIO0_2/SWDIO

Para facilitar el acceso a los registros de configuración de los pines se desarrollan las funciones:

```
void SetPINMODE_IN (uint32_t Pin_index, uint32_t Modo); //Pull-Down o Pull-Up
void SetPINMODE_OUT (uint32_t Pin_index, uint32_t Modo); //Drain Mode
```

Que se utilizan en conjunto con las siguientes constantes de preprocesador (se muestran las primeras a modo de ejemplo):

```
/* IOCON - Peripheral instance base addresses */
/** Peripheral IOCON base address */
#define IOCON_BASE (0x40044000u)
/** Peripheral IOCON base pointer */
#define IOCON ((IOCON_Type *)IOCON_BASE)
/** Array initializer of IOCON peripheral base addresses */
#define IOCON_BASE_ADDRS { IOCON_BASE }
/** Array initializer of IOCON peripheral base pointers */
#define IOCON_BASE_PTRS { IOCON }
```



```
#define IOCON_INDEX_PIO0_17 ( 0 )
#define IOCON_INDEX_PIO0_13 ( 1 )
#define IOCON_INDEX_PIO0_12 ( 2 )
#define IOCON_INDEX_PIO0_5 ( 3 )
#define IOCON_INDEX_PIO0_4 ( 4 )
#define IOCON_INDEX_PIO0_3 ( 5 )
#define IOCON_INDEX_PIO0_2 ( 6 )
```

3. Bloque de registros **SWITCH MATRIX**

- Registros de asociación de pines según su función y habilitación/deshabilitación de funciones especiales:

Table 179. Register overview: Switch matrix (base address 0x4000 C000)

Name	Access	Offset	Description
PINASSIGN0	R/W	0x000	Pin assign register 0. Assign movable functions U0_TXD, U0_RXD, U0_RTS, U0_CTS.
PINASSIGN1	R/W	0x004	Pin assign register 1. Assign movable functions U0_SCLK, U1_TXD, U1_RXD, U1_RTS.
PINASSIGN2	R/W	0x008	Pin assign register 2. Assign movable functions U1_CTS, U1_SCLK, U2_TXD, U2_RXD.
PINASSIGN3	R/W	0x00C	Pin assign register 3. Assign movable function U2_RTS, U2_CTS, U2_SCLK, SPI0_SCK.
PINASSIGN4	R/W	0x010	Pin assign register 4. Assign movable functions SPI0_MOSI, SPI0_MISO, SPI0_SSEL0, SPI0_SSEL1.
...			
PINENABLE0	R/W	0x1C0	Pin enable register 0. Enables fixed-pin functions ACMP_In, SWCLK, SWDIO, XTALIN, XTALOUT, RESET, CCLKIN, VDDCMP, I2C0_SDA, I2C0_SCL, ADC_n, DACOUTn, CAPT_X0, CAPT_X1, CAPT_X2, and CAPT_X3.
PINENABLE1	R/W	0x1C4	Pin enable register 1. Enables fixed-pin functions CAPT_X4, CAPT_X5, CAPT_X6, CAPT_X7, CAPT_X8, CAPT_X4, CAPT_YL and CAPT_YH.

3.1. Detalle de los registros PINASSIGN0 y 1

Table 180. Pin assign register 0 (PINASSIGN0, address 0x4000 C000) bit description

Bit	Symbol	Description
7:0	U0_TXD_O	U0_TXD function assignment. The value is the pin number to be assigned to this function. The following pins are available: PIO0_0 (= 0) to PIO0_31 (= 0x1F) and from PIO1_0 (= 0x20) to PIO1_21(= 0x35).
15:8	U0_RXD_I	U0_RXD function assignment. The value is the pin number to be assigned to this function. The following pins are available: PIO0_0 (= 0) to PIO0_31 (= 0x1F) and from PIO1_0 (= 0x20) to PIO1_21(= 0x35).
23:16	U0_RTS_O	U0_RTS function assignment. The value is the pin number to be assigned to this function. The following pins are available: PIO0_0 (= 0) to PIO0_31 (= 0x1F) and from PIO1_0 (= 0x20) to PIO1_21(= 0x35).
31:24	U0_CTS_I	U0_CTS function assignment. The value is the pin number to be assigned to this function. The following pins are available: PIO0_0 (= 0) to PIO0_31 (= 0x1F) and from PIO1_0 (= 0x20) to PIO1_21(= 0x35).

Table 181. Pin assign register 1 (PINASSIGN1, address 0x4000 C004) bit description

Bit	Symbol	Description
7:0	U0_SCLK_IO	U0_SCLK function assignment. The value is the pin number to be assigned to this function. The following pins are available: PIO0_0 (= 0) to PIO0_31 (= 0x1F) and from PIO1_0 (= 0x20) to PIO1_21(= 0x35).
15:8	U1_TXD_O	U1_TXD function assignment. The value is the pin number to be assigned to this function. The following pins are available: PIO0_0 (= 0) to PIO0_31 (= 0x1F) and from PIO1_0 (= 0x20) to PIO1_21(= 0x35).
23:16	U1_RXD_I	U1_RXD function assignment. The value is the pin number to be assigned to this function. The following pins are available: PIO0_0 (= 0) to PIO0_31 (= 0x1F) and from PIO1_0 (= 0x20) to PIO1_21(= 0x35).
31:24	U1_RTS_O	U1_RTS function assignment. The value is the pin number to be assigned to this function. The following pins are available: PIO0_0 (= 0) to PIO0_31 (= 0x1F) and from PIO1_0 (= 0x20) to PIO1_21(= 0x35).

**UART0
(TX y RX)**

**UART1
(TX y RX)**

3.2. Detalle del registro PINENABLE0

Table 195. Pin enable register 0 (PINENABLE0, address 0x4000 C1C0) bit description

Bit	Symbol	Value	Description	Reset value
14	ADC_0	ADC_0 function select.		1
		0	ADC_0 enabled on pin PIO0_7.	
		1	ADC_0 disabled.	
15	ADC_1	ADC_1 function select.		1
		0	ADC_1 enabled on pin PIO0_6.	
		1	ADC_1 disabled.	
16	ADC_2	ADC_2 function select.		1
		0	ADC_2 enabled on pin PIO0_14.	
		1	ADC_2 disabled.	
17	ADC_3	ADC_3 function select.		1
		0	ADC_3 enabled on pin PIO0_23.	
		1	ADC_3 disabled.	
18	ADC_4	ADC_4 function select.		1
		0	ADC_4 enabled on pin PIO0_22.	
		1	ADC_4 disabled.	
19	ADC_5	ADC_5 function select.		1
		0	ADC_5 enabled on pin PIO0_21.	
		1	ADC_5 disabled.	
...				
26	DACOUT0	DACOUT0 function select.		1
		0	DACOUT0 enabled on pin PIO0_17.	
		1	DACOUT0 disabled.	

0 habilita la función especial en el pin
1 deshabilita la función especial en el pin

4. Bloque de registros GPIO

Table 255. Register overview: GPIO port (base address 0xA000 0000)

Name	Access	Address offset	Description
DIR0	R/W	0x2000	Direction registers port 0
DIR1	R/W	0x2004	Direction registers port 1
MASK0	R/W	0x2080	Mask register port 0
MASK1	R/W	0x2084	Mask register port 1
PIN0	R/W	0x2100	Port pin register port 0
PIN1	R/W	0x2104	Port pin register port 1
MPIN0	R/W	0x2180	Masked port register port 0
SET0	R/W	0x2200	Write: Set register for port 0 Read: output bits for port 0
SET1	R/W	0x2204	Write: Set register for port 1 Read: output bits for port 1
CLR0	WO	0x2280	Clear port 0
CLR1	WO	0x2284	Clear port 1
NOT0	WO	0x2300	Toggle port 0
NOT1	WO	0x2304	Toggle port 1

DIRECCIÓN:
0 entrada
1 salida

PIN:
Escribir/Leer el valor del pin

SET/CLR/NOT:
Escribir un 1 (SET), escribir un 0 (CLR) o cambiar el valor (NOT) de un pin

4.1. Prototipos de funciones de configuración de dirección y lectura/escritura de pines

```
void SetDIR (uint32_t Puerto, uint32_t Pin, uint32_t Direccion);
void SetPIN (uint32_t Puerto, uint32_t Pin, uint32_t Estado);
uint32_t GetPIN (uint32_t Puerto, uint32_t Pin);
```

5. Bloque de registros Systick

- Registros de control, conteo, recarga y calibración del Systick:

Table 434. Register overview: SysTick timer (base address 0xE000 E000)

Name	Access	Address offset	Description
SYST_CSR	R/W	0x010	System Timer Control and status register
SYST_RVR	R/W	0x014	System Timer Reload value register
SYST_CVR	R/W	0x018	System Timer Current value register
SYST_CALIB	R/W	0x01C	System Timer Calibration value register

5.1. Detalle del registro CSR

Table 435. SysTick Timer Control and status register (CSR) bit description

Bit	Symbol	Description
0	ENABLE	System Tick counter enable. When 0, the counter is disabled.
1	TICKINT	System Tick interrupt enable. When 1, the System Tick interrupt is enabled. When 0, the System Tick interrupt is disabled. The interrupt is generated when the counter counts down to 0.
2	CLKSOURCE	System Tick clock source selection. 1 indicates that the CPU clock is selected as the reference clock. 0 indicates that the HSE oscillator is selected as the reference clock.
15:3	-	Reserved, user space. The value read is 0.
16	COUNTFLAG	Returns 1 if the counter has overflowed this register. Reserved, user space. The value read is 0.
31:17	-	Reserved, user space. The value read is 0.

ENABLE:
1 habilita el systick

TICKINT:
1 habilita interrupciones

CLKSOURCE:
1 indica que la fuente de CLK es el frountend (CPU clock) como referencia
0 indica que la fuente de CLK es frountend/2

COUNTFLAG:
1 indica que se venció el tiempo. Se limpia al ser leído.

6. Registros para interrupciones (NVIC e interrupciones de pin)

6.1. Detalle del registro ISER0

- Habilitación de interrupciones en el NVIC

Write — Writing 0 has no effect, writing 1 enables the interrupt.

Read — 0 indicates that the interrupt is disabled, 1 indicates that the interrupt is enabled.

Table 110. Interrupt Set Enable Register 0 register (ISER0, address 0xE000 E100) bit description

Bit	Symbol	Description	Reset value
0	ISE_SPI0	Interrupt enable.	0
1	ISE_SPI1	Interrupt enable.	0
2	ISE_DAC0	Interrupt enable.	0
3	ISE_UART0	Interrupt enable.	0
4	ISE_UART1	Interrupt enable.	0
5	ISE_UART2	Interrupt enable.	0
6	-	Reserved	0
7	ISE_I2C1	Interrupt enable.	0
8	ISE_I2C0	Interrupt enable.	0
9	ISE_SCT	Interrupt enable.	0
10	ISE_MRT	Interrupt enable.	0
11	ISE_CMP or ISE_CAPT	Interrupt enable for both comparator and Capacitive Touch.	0
12	ISE_WDT	Interrupt enable.	0
13	ISE_BOD	Interrupt enable.	0
14	ISE_FLASH	Interrupt enable.	0
15	ISE_WKT	Interrupt enable.	0
16	ISE_ADC_SEQA	Interrupt enable.	0
17	ISE_ADC_SEQB	Interrupt enable.	0
18	ISE_ADC_THCMP	Interrupt enable.	0
19	ISE_ADC_OVR	Interrupt enable.	0
20	ISE_SDMA	Interrupt enable.	0
21	ISE_I2C2	Interrupt enable.	0
22	ISE_I2C3	Interrupt enable.	0
23	ISE_CT32b0	Interrupt enable.	0
24	ISE_PININT0	Interrupt enable.	0
25	ISE_PININT1	Interrupt enable.	0
26	ISE_PININT2	Interrupt enable.	0

6.2. Detalle del registro PINTSEL_n

- Selección de pin como fuente de interrupción externa

Table 167. Pin interrupt select registers (PINTSEL[0:7], address 0x4004 8178 (PINTSEL0) to 0x4004 8194 (PINTSEL7)) bit description

Bit	Symbol	Description	Reset value
5:0	INTPIN	Pin number select for pin interrupt or pattern match engine input. (PIO0_0 to PIO0_31 correspond to numbers 0 to 31) (PIO1_31 correspond to numbers 32 to 63)	0
31:6	-	Reserved	1 indica P0.0, 1 indica P0.1, etc

6.3. Bloque de registros PININTERRUPT

- Registros para la configuración de interrupciones de pin

Table 269. Register overview: Pin interrupts and pattern match engine (at 0xA000 4000)

Name	Access	Address offset	Description
ISEL	R/W	0x000	Pin Interrupt Mode register
IENR	R/W	0x004	Pin interrupt level or rising edge interrupt enable register
...			
IENF	R/W	0x010	Pin interrupt active level or falling edge interrupt enable register
...			
IST	R/W	0x024	Pin interrupt status register

6.3.1 Detalle del registro ISEL

- Modo de la interrupción (flanco/nivel):

Table 270. Pin interrupt mode register (ISEL, address 0xA000 4000) bit description

Bit	Symbol	Description	Reset value	Access
7:0	PMODE	Selects the interrupt mode for each pin interrupt. Bit n configures the pin interrupt selected in PINTSEL _n . 0 = Edge sensitive 1 = Level sensitive	0	R/W
31:8	-			

0 selecciona interrupción por flanco
1 selecciona interrupción por nivel (1 bit por cada fuente de interrupción)

6.3.2 Detalle del registro IENR

- Habilitación interrupción por flanco ascendente o habilitación del nivel:

Table 271. Pin interrupt level or rising edge interrupt enable register (IENR, address 0xA000 4004) bit description

Bit	Symbol	Description	Reset value	Access
7:0	ENRL	Enables the rising edge or level interrupt for each pin interrupt. Bit n configures the pin interrupt selected in PINTSEL _n . 0 = Disable rising edge or level interrupt. 1 = Enable rising edge or level interrupt.	0	R/W
31:8	-			

0 deshabilita flanco ascendente (o nivel)
1 **habilita** flanco ascendente (o nivel) (1 bit por cada fuente de interrupción)

6.3.3 Detalle del registro IENF

Table 274. Pin interrupt active level or falling edge interrupt enable register (IENF, address 0xA000 4010) bit description

Bit	Symbol	Description	Reset value	Access
7:0	ENAF	Enables the falling edge or configures the active level interrupt for each pin interrupt. Bit n configures the pin interrupt selected in PINTSELn. 0 = Disable falling edge interrupt or set active interrupt level LOW. 1 = Enable falling edge interrupt enabled or set active interrupt level HIGH.	0	R/W

0 deshabilita flanco descendente (o selecciona nivel BAJO)
 1 habilita flanco descendente (o selecciona nivel ALTO) (1 bit por cada fuente de interrupción)

6.3.4 Detalle del registro IST

Table 279. Pin interrupt status register (IST, address 0xA000 4024) bit description

Bit	Symbol	Description	Reset value	Access
7:0	PSTAT	Pin interrupt status. Bit n returns the status, clears the edge interrupt, or inverts the active level of the pin selected in PINTSELn. Read 0: interrupt is not being requested for this interrupt pin. Write 0: no operation. Read 1: interrupt is being requested for this interrupt pin. Write 1 (edge-sensitive): clear rising- and falling-edge	0	R/W

1 en algún bit indica que la interrupción está activa. Se debe escribir un 1 para limpiar el flag

7. Bloque de registros USARTs

7.1 Detalle del registro PRESETCTRL0 (SYSCON)

- Reset de los periféricos (0 resetea, 1 para volver a funcionamiento normal):

Table 148. Peripheral reset control 0 register (PRESETCTRL0, address 0x4004 8088) bit description

Bit	Symbol	Value	Description	Reset value
14	UART0_RST_N	-	UART0 reset control	1
		0	Assert the UART0 reset.	
15	UART1_RST_N	-	UART1 reset control	1
		0	Assert the UART1 reset.	
16	UART2_RST_N	-	UART2 reset control	1
		0	Assert the UART2 reset.	
		1	Clear the UART2 reset.	

7.2 Detalle del registro UARTrCLKSEL (SYSCON)

Bit	Symbol	Value	Description
2:0	SEL	-	Peripheral clock source
		0x0	FRO
		0x1	Main clock
		0x2	FRG0 clock
		0x3	FRG1 clock
		0x4	FRO_DIV = FRO / 2
		0x5	Reserved
		0x6	Reserved
		0x7	None

Selecciona la fuente del CLK que alimenta a la USARTn

7.3 Bloque de registros USART

- Configuración de las características de la comunicación serie:

Table 323. Register overview: USART (base address 0x4006 4000 (USART0), 0x4006 8000 (USART1), 0x4006 C000 (USART2), 0x4007 0000 (USART3), 0x4007 4000 (USART4))

Name	Access	Offset	Description
CFG	R/W	0x000	USART Configuration register. Basic USART configuration settings that typically are not changed during operation.
...			
STAT	R/W	0x008	USART Status register. The complete status value can be read here. Writing ones clears some bits in the register. Some bits can be cleared by writing a 1 to them.
...			
INTENSET	R/W	0x00C	Interrupt Enable read and Set register. Contains an individual interrupt enable bit for each potential USART interrupt. A complete value may be read from this register. Writing a 1 to any implemented bit position causes that bit to be set.
INTENCLR	W	0x010	Interrupt Enable Clear register. Allows clearing any combination of bits in the INTENSET register. Writing a 1 to any implemented bit position causes the corresponding bit to be cleared.
RXDAT	R	0x014	Receiver Data register. Contains the last character received.
...			
TXDAT	R/W	0x01C	Transmit Data register. Data to be transmitted is written here.
BRG	R/W	0x020	Baud Rate Generator register. 16-bit integer baud rate divisor value.

7.3.1 Detalle del registro CFG

Table 324. USART Configuration register (CFG, address 0x4006 4000 (USART0), 0x4006 8000 (USART1), 0x4006 C000 (USART2), 0x4007 0000 (USART3), 0x4007 4000 (USART4)) bit description

Bit	Symbol	Value	Description	Reset Value
0	ENABLE	0	USART Enable. 0: Disabled. The USART is disabled and the internal state machine and counters are reset. While Enable = 0, all USART interrupts and DMA transfers are disabled. When Enable is set again, CFG and most other control bits remain unchanged. For instance, when re-enabled, the USART will immediately generate a TXRDY interrupt (if enabled in the INTENSET register) or a DMA transfer request because the transmitter has been reset and is therefore available.	0
1	-	1	Enabled. The USART is enabled for operation.	NA
32	DATALEN	0x0	Reserved. Read value is undefined; only zero should be written.	NA
		0x0	Selects the data size for the USART. 0: 7 bit Data length.	00
		0x1	8 bit Data length.	
		0x2	9 bit data length. The 9th bit is commonly used for addressing in multidrop mode. See the ADDDET bit in the CTL register.	
		0x3	Reserved.	
54	PARITYSEL	0x0	Selects what type of parity is used by the USART. 0: No parity.	00
		0x1	Reserved.	
		0x2	Even parity. Adds a bit to each character such that the number of 1s in a transmitted character is even, and the number of 1s in a received character is expected to be even.	
		0x3	Odd parity. Adds a bit to each character such that the number of 1s in a transmitted character is odd, and the number of 1s in a received character is expected to be odd.	
6	STOPLEN	0	Number of stop bits appended to transmitted data. Only a single stop bit is required for received data.	0
		0	1 stop bit.	
		1	2 stop bits. This setting should only be used for asynchronous communication.	
87	-	0	Reserved. Read value is undefined; only zero should be written.	NA
9	CTSEN	0	CTS Enable. Determines whether CTS is used for flow control. CTS can be from the input pin, or from the USART's own RTS if loopback mode is enabled.	0
		1	No flow control. The transmitter does not receive any automatic flow control signal.	
10	-	0	Reserved. Read value is undefined; only zero should be written.	NA
11	SYNCEN	0	Selects synchronous or asynchronous operation. 0: Asynchronous mode is selected.	0
		1	Synchronous mode is selected.	

ENABLE:

1 habilita la UART
0 deshabilita UART

DATALEN:

Cantidad de bits de datos

PARITY:

0: Sin paridad
2: Paridad PAR
3: Paridad IMPAR

STOPLEN:

0: 1 bit de stop
1: 2 bits de stop

CTSLEN:

0: sin control de flujo
1: con control de flujo

SYNCEN:

0: com asincrónica
1: com sincrónica

7.3.2 Detalle del registro BRG

Table 332. USART Baud Rate Generator register (BRG, address 0x4006 4020 (USART0), 0x4006 8020 (USART1), 0x4006 8020 (USART2), 0x4007 0020 (USART3), 0x4007 4020 (USART4)) bit description

Bit	Symbol	Description	Reset Value
15:0	BRGVAL	<p>This value is used to divide the USART input clock to determine the baud rate, based on the input clock from the FRG.</p> <p>0 = The FRG clock is used directly by the USART function.</p> <p>1 = The FRG clock is divided by 2 before use by the USART function.</p> <p>2 = The FRG clock is divided by 3 before use by the USART function.</p> <p>...</p> <p>0xFFFF = The FRG clock is divided by 65,536 before use by the USART function.</p>	0
31:16	-	Reserved. Read value is undefined, only zero should be written.	NA

$$\text{Velocidad (baudios)} = \text{CLK_UART} / (\text{BRGVAL} * \text{Oversampling})$$

(Oversampling suele ser 16)

Bit0: Se recibió un dato completo
(listo para ser leído en RXDAT)

Bit2: La UART se encuentra lista
para enviar un nuevo dato

7.3.3 Detalle de los registros INTENSET, INTENCLR y STAT

- Registros de habilitación/deshabilitación de interrupciones y estado de la comunicación (los 3 registros tienen los bits en las mismas posiciones)

Bit	Symbol	Description
0	RXRDY	Receiver Ready flag.
1	-	Reserved. Read value is undefined, only zero should be written.
2	TXRDY	Transmitter Ready flag.
3	TXIDLE	Transmitter idle status.
4	-	Reserved. Read value is undefined, only zero should be written.
5	DELTACTS	This bit is set when a change in the state of the CTS input is detected.
6	TXDISINT	Transmitter Disabled Interrupt flag.
7	-	Reserved. Read value is undefined, only zero should be written.
8	OVERRUNINT	Overrun Error interrupt flag.
10:9	-	Reserved. Read value is undefined, only zero should be written.
11	DELTARXBRK	This bit is set when a change in the state of receiver break detection occurs.
12	START	This bit is set when a start is detected on the receiver input.
13	FRAMERRINT	Framing Error interrupt flag.
14	PARITYERRINT	Parity Error interrupt flag.
15	RXNOISEINT	Received Noise interrupt flag.
16	ABERR	Autobaud Error flag.

8. Registros para la configuración del ADC

8.1 Detalle de los registros ADCnCLKSEL/ADCnCLKDIV (SYSCON)

- Selección del CLK del ADC:

Table 141. ADC clock source select register (ADCCLKSEL, address 0x4004 8064) bit description

Bit	Symbol	Value	Description	Reset value
1:0	SEL	Clock source for ADC clock.	0x0	
		0x0	FRO	
		0x1	SYS PLL	
		0x2	None	
		0x3	None	
31:3	-		Reserved	-

Table 142. ADC clock divider register (ADCCLKDIV, address 0x4004 8068) bit description

Bit	Symbol	Value	Description	Reset value
7:0	DIV		ADC clock divider values. 0: ADC clock disabled. 1: Divide by 1. ... 255: Divide by 255.	0x0
31:8	-		Reserved	-

Selección del CLK que alimenta el ADC (**CLKSEL** selecciona la frecuencia, que es dividida por el valor de **CLKDIV**)

8.2 Bloque de registros ADC

Table 452. Register overview : ADC (base address 0x4001 C000)

Name	Access	Address offset	Description
CTRL	R/W	0x000	A/D Control Register. Contains the clock divide value, enable bits for each sequence and the A/D power-down bit.
-	-	0x004	Reserved.
SEQA_CTRL	R/W	0x008	A/D Conversion Sequence-A control Register: Controls triggering and channel selection for conversion sequence-A. Also specifies interrupt mode for sequence-A.
SEQB_CTRL	R/W	0x00C	A/D Conversion Sequence-B Control Register: Controls triggering and channel selection for conversion sequence-B. Also specifies interrupt mode for sequence-B.
SEQA_GDAT	R/W	0x010	A/D Sequence-A Global Data Register. This register contains the result of the most recent A/D conversion performed under sequence-A
SEQB_GDAT	R/W	0x014	A/D Sequence-B Global Data Register. This register contains the result of the most recent A/D conversion performed under sequence-B
...			
INTEN	R/W	0x064	A/D Interrupt Enable Register. This register contains enable bits that enable the sequence-A, sequence-B, threshold compare and data overrun interrupts to be generated.

...

8.2.1 Detalle del registro CTRL

Table 453. A/D Control Register (CTRL, addresses 0x4001 C000) bit description

Bit	Symbol	Value	Description
7:0	CLKDIV		The system clock is divided by this value plus one to produce the sampling clock. The sampling clock should be less than or equal to 30 MHz for 1. Typically, software should program the smallest value in this field maximum clock rate or slightly less, but in certain cases (such as high-impedance analog source) a slower clock may be desirable.

CLKDIV
El ADC divide el CLK
por CLKDIV x 25
para llegar a la freq.
de muestreo

ASYNCMODE		Asynchronous operation mode
	0	<p>Synchronous mode.</p> <p>The ADC clock is derived from the main system clock based on the selected in the CLKDIV field. The ADC clock starts in response to eliminate any uncertainty in the launching of an ADC conversion or any synchronous (on-chip) trigger. In synchronous mode with the bit set, sampling of the A/D input and start of a conversion initiate clocks after the leading edge of a (synchronous) trigger pulse.</p>
	1	<p>Asynchronous mode.</p> <p>The ADC clock is based on an alternative independent clock source this clock source and the mechanism for programming it is chip-select frequency of this clock is limited to 15 MHz max. In addition, the A never be faster than 10 times the APB bus clock rate.</p>

ASYNCMODE

0: muestreo sincrónico
1: muestreo asincrónico

9	-	Reserved. Do not write a one to these bits.
10	LPWRMODE	<p>Select low-power ADC mode.</p> <p>The analog circuitry is automatically powered-down when no conversion is taking place. When any (hardware or software) triggering event is detected, the analog circuitry is enabled. After the required start-up time, the regular conversion will be launched. Once the conversion completes, the analog circuitry will again be powered-down provided no further conversions are triggered.</p> <p>Using this mode can save an appreciable amount of current when the ADC is required relatively infrequently.</p> <p>The penalty for using this mode is an approximately 15 ADC clock cycles delay from the time the trigger occurs until sampling of the A/D input commences.</p> <p>Remark: This mode will NOT power-up the ADC when the ADC is powered down in the system control block.</p>

LPWRMODE:
0: modo bajo
consumo (se apaga
el ADC)
1: funcionamiento
normal

	0	Disabled. The low-power ADC mode is disabled. The analog circuitry remains activated even when no conversions are made.
	1	Enabled. The low-power ADC mode is enabled.
29:11		Reserved, do not write ones to reserved bits.

CALMODE:
1: modo calibración
(se baja solo luego
de 29useq)

8.2.2 Detalle del registro **SEQn_CTRL**

Table 454. A/D Conversion Sequence A Control Register (SEQA_CTRL, address 0x0000_0000)

Bit	Symbol	Value	Description
11:0	CHANNELS		<p>Selects which one or more of the twelve channels will be converted when this sequence is launched. A value of 0 means no conversion. A value of 1 causes the corresponding channel to be included in the conversion sequence. A value of 2 causes both channels to be included, etc.</p> <p>When this conversion sequence is triggered, either via software command or via a hardware trigger, A/D conversions will begin on the selected channel(s) in sequence, beginning with the lowest numbered channel.</p> <p>Remark: This field can ONLY be changed while the sequencer is inactive. If it is set to a value other than 0, it must be written again when the sequencer is active. It is allowed to change this field and start a conversion sequence at the same time.</p>
14:12	TRIGGER		<p>Selects which of the available hardware trigger sources will initiate the conversion sequence to be initiated. Program bit 14 is the enable bit.</p> <p>Remark: In order to avoid generating a spurious write to this field only when the SEQA_ENA bit is set, it is recommended to write this field and set bit 33 in the same write operation.</p>

CHANNELS:
Selecciono que
canales muestrean la
secuencia

		Change the head and set bit 3 in the same way.
27	BURST	<p>***</p> <p>Concurrent sequences will consequently always be triggered sequentially.</p> <p>Writing a 1 to this bit will cause this conversion to be triggered sequentially. The sequence will be cycled through. Other sequence A triggers will be ignored.</p> <p>Repeated conversions can be halted by clearing this bit. It will be automatically set again currently in progress will be completed before the next conversion starts.</p>

BURST:
1 activa el muestreo
a la frecuencia de
CLK seleccionada

		re-sampled and the conversion sequence will
30	MODE	Indicates whether the primary method for retrieving this sequence will be accomplished via reading (SEQA_GDAT) at the end of each conversion, result registers at the end of the entire sequence. Impacts when conversion-complete interrupt/D will be generated and which overrun condition interrupt as described below.
0		End of conversion. The sequence A interrupt/D of each individual A/D conversion performed or mirror the DATAVALID bit in the SEQ_A_GDAT register. The OVERRUN bit in the SEQ_A_GDAT register of an overrun interrupt if enabled.

MODE:
: Lectura del
resultado por el
registro GDAT
0: Lectura del
resultado por el
registro DAT

		1	End of sequence. The sequence A interrupt/DMA trigger is generated when the sequence A conversion is completed. This interrupt/DMA trigger is generated when the entire set of sequence-A conversions complete. It is generated when the sequence A conversion is explicitly cleared by software or by the DMA-clear function. The OVERRUN bit in the SEQQA_GDAT register is set when the sequence A conversion is completed. The generation of an overrun interrupt/DMA trigger is inhibited when the sequence A conversion is not completed. The sequence A conversion is not completed when the sequence A conversion is explicitly cleared by software or by the DMA-clear function.
31	SEQQA_ENA		Sequence Enable. In order to avoid spurious interrupt/DMA triggers, the following sequence of operations should be taken to only set the SEQQA_ENA bit when the input is in its INACTIVE state (as defined by the INACTIVE bit in the SEQQA_GDAT register). If this condition is not met, the sequence will be triggered even if the SEQQA_ENA bit is enabled.

SEQn_ENA:
1: habilita seqN
0: deshabilita seqN

8.2.3 Detalle del registro INTEN

- Habilitación de las interrupciones:

Table 464. A/D Interrupt Enable register (INTEN, address 0x4001 C064) bit description

Bit	Symbol	Value	Description	Reset value
0	SEQA_INTEN		Sequence A interrupt enable.	0
		0	Disabled. The sequence A interrupt/DMA trigger is disabled.	
		1	Enabled. The sequence A interrupt/DMA trigger is enabled and will be asserted either upon completion of each individual conversion performed as part of sequence A, or upon completion of the entire A sequence of conversions, depending on the MODE bit in the SEQA_CTRL register.	
1	SEQB_INTEN		Sequence B interrupt enable.	0
		0	Disabled. The sequence B interrupt/DMA trigger is disabled.	
		1	Enabled. The sequence B interrupt/DMA trigger is enabled and will be asserted either upon completion of each individual conversion performed as part of sequence B, or upon completion of the entire B sequence of conversions, depending on the MODE bit in the SEQB_CTRL register.	
2	OVR_INTEN		Overrun interrupt enable.	0
		0	Disabled. The overrun interrupt is disabled.	
		1	Enabled. The overrun interrupt is enabled. Detection of an overrun condition on any of the 12 channel data registers will cause an overrun interrupt request. In addition, if the MODE bit for a particular sequence is 0, then an overrun in the global data register for that sequence will also cause this interrupt request to be asserted.	

**1 habilita la interrupción correspondiente,
0 la deshabilita**

8.2.4 Detalle del registro SEQn_GDAT

- Lectura del resultado del ADC (para la secuencia A o B):

Table 465. A/D Sequence A Global Data Register (SEQA_GDAT, address 0x4001 C010) bit description

Bit	Symbol	Description
3:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.
15:4	RESULT	This field contains the 12-bit A/D conversion result from the most recent conversion performed under conversion sequence associated with this register. The result is the a binary fraction representing the voltage on the currently-selected input channel as it falls within the range of V _{REFP} to V _{REFN} . Zero in the field indicates that the voltage on the input pin was less than, equal to, or close to that on V _{REFN} , while 0xFFFF indicates that the voltage on the input was close to, equal to, or greater than that on V _{REFP} . DATAVALID = 1 indicates that this result has not yet been read.
29:26	CHN	These bits contain the channel from which the RESULT bits were converted (e.g. 0000 identifies channel 0, 0001 channel 1...).
30	OVERRUN	This bit is set if a new conversion result is loaded into the RESULT field before a previous result has been read - i.e. while the DATAVALID bit is set. This bit is cleared, along with the DATAVALID bit, whenever this register is read. This bit will contribute to an overrun interrupt request if the MODE bit (in SEQA_CTRL) for the corresponding sequence is set to '0' (and if the overrun interrupt is enabled).
31	DATAVALID	This bit is set to '1' at the end of each conversion when a new result is loaded into the RESULT field. It is cleared whenever this register is read. This bit will cause a conversion-complete interrupt for the corresponding sequence if the MODE bit (in SEQA_CTRL) for that sequence is set to 0 (and if the interrupt is enabled).

Resultado de la conversión. Los bits **CHN** indican el canal al que se corresponde el resultado, el bit **OVERRUN** indica si me perdí de leer una conversión, y el bit **DATAVALID** se pone en 1 cuando termina una conversión y vuelve a 0 cuando se lee el registro