DEPARTMENT OF ELECTRONIC & ELECTRICAL ENGINEERING

University of Strathclyde Engineering

Semester 2 Assignment

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EE466: Power Electronics, Machines, and Applications

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I hereby declare that this work has not been submitted for any other degree/course at this University or any other institution and that, except where reference is made to the work of other authors, the material presented is original and entirely the result of my own work at the University of Strathclyde.

q1 Question 1

q1a)

q1a)i) Thermal circuit diagram

A diagram for a power converter comprised of an IGBT and a diode is constructed in Figure 1. Note, the convention for a shared heatsink is adopted where both the power dissipation contributions from the IGBT and diode are present at T_S.

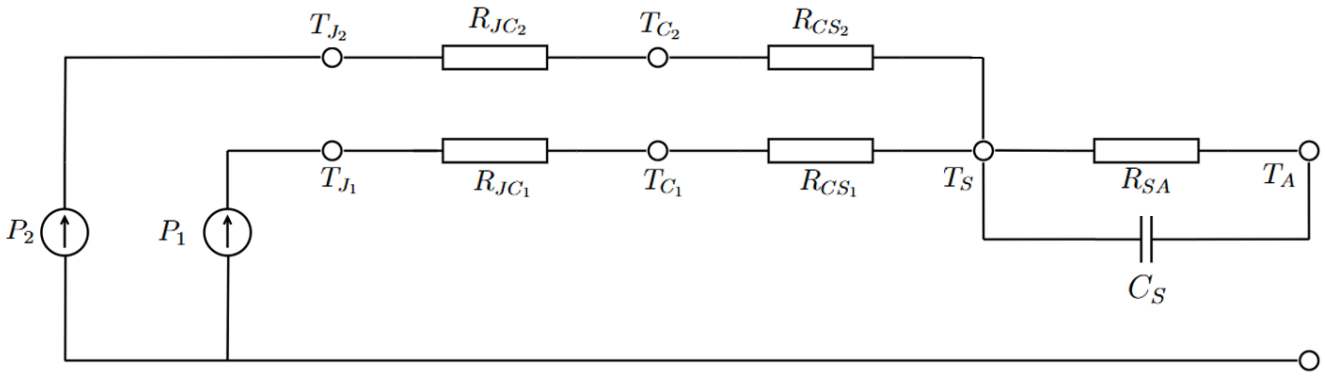

Figure 1: Thermal Circuit Diagram

The parameters for this circuit are given from the coursework brief document. These are reiterated and conveniently summarised in Table 1 where the units have their usual meanings.

Variable Name	Symbol	Value	Units
Power Dissipated through Diode	P_1	7	W
Power Dissipated through IGBT	P_2	12	W
Ambient Temperature	T_A	40	$°C$
Heatsink to ambient thermal resistance	R_{SA}	3.2	$°C/W$
Diode case to heatsink resistance	R_{CS1}	1.5	$°C/W$
IGBT case to heatsink resistance	R_{CS2}	1.4	$°C/W$
Diode junction to case thermal resistance	R_{JC1}	0.9	$°C/W$
IGBT junction to case thermal resistance	R_{JC2}	0.6	$°C/W$
Heatsink thermal capacitance	C_s	280	$\frac{J}{°C}$

Table 1: Summary of parameters as given in the brief document

It is also noteworthy that the subscript ”2” denotes the components in the IGBT device, and ”1” is representative of the Diode elements. This arrangement was selected to provide distinction between the devices and its usefulness can be visualised in Figure 1 by the separation intro parallel branches.

q1a)ii) Calculation of Junction Temperatures

Performing nodal analysis of the schematic shown in Figure 1, the expressions for the temperatures at T_{J_2} and T_{J_1} is given as (1,2)

$$T_{J_2} = T_A + (P_1 + P_2)R_{SA} + P_2(R_{JC_2}) + P_2(R_{JC_2}) \tag{1}$$

$$T_{J_1} = T_A + (P_1 + P_2)R_{SA} + P_1(R_{JC_1}) + P_1(R_{JC_1}) \tag{2}$$

Using these equations, the junction temperatures for the Diode and IGBT can be computed using the parameters defined in Table 1.

$$T_{J_2} = 40 + (7 + 12) \times 3.2 + 12 \times (1.4) + 12 \times (0.6) = \underline{\mathbf{124.8}}°c \tag{3}$$

$$T_{J_1} = 40 + (7 + 12) \times 3.2 + 7 \times (1.5) + 7 \times (0.9) = \underline{\mathbf{117.6}}°c \tag{4}$$

q1a)iii) Calculation of heatsink temperature

The calculation of the heatsink's temperature three minutes after circuit de-energisation commences with the conversion of time t into seconds.

$$t = 3 \times 60 = 180s \tag{5}$$

Next, the time constant is calculated by finding the product of the heatsink to ambient thermal resistance and thermal capacitance of the heatsink.

$$\tau = RC = 3.2 \times 280 = 896J/W \tag{6}$$

The characteristic formula for a de-energising heatsink is given by (7) where the equation is modelled from a decaying exponential where $T_s(t)$ is the temperature as a function of time, weighted by the total power and thermal resistance of the heatsink.

$$T_s(t) = P_t R_{SA}(e^{\frac{-t}{\tau}}) + T_A \tag{7}$$

The temperature of the heatsink after 3 minutes can be calculated by substitution of the known parameters.

$$T_s(180) = 19 \times 3.2 \times (e^{\frac{-180}{896}}) + 40 = \underline{\mathbf{89.73}}°c \tag{8}$$

q1b) Buck Converter Switching Losses Investigation

q1b)i) Thermal Superposition Measurements

The Thermal Superposition method is a common technique used to simulate and estimate the switching losses present in converters. This method operates by calculating the overall temperature distribution by summing temperature rises from heat sources within the system. This generation of heat is assumed to be consistent across its area, thus the core equations are linear, and the criterion for superposition is met [1].

Two tests are required for this method. The first of which tests the converters under normal operating conditions to examine the behaviour of both switching and conduction losses in the system. The temperature rise of the switch is typically measured using thermal sensors [2]. In the second experiment, switching activity ceases and subsequently, only the conduction losses are present. Disabling the switches entails configuring the gate driver signal to switch the gate permanently open or closed. Superposition of the thermal temperature of the two experiments is exploited to calculate an estimation for the switching losses since both experiments have a common conduction loss contribution but only the first experiment contains switching losses.

Major advantages of the thermal superposition method include low set up complexity since high-speed electrical measurements are not required which results in cost savings from a time and equipment perspective. The simplicity of this solution makes it appealing for design engineers as it allows for an efficient and more streamlined testing process. Its dominance in industry is attributed to its ability to provide a detailed assessment of the long-term thermal performance of a converter during the continuous operating mode [3].

However, this major benefit of this technique proves also to be a limitation. Converter systems tend to have a low thermal response, and so dynamic testing is not suitable with this approach since the time taken for the component to each thermal equilibrium is too long. This makes this method unsuitable for capturing transient switching events where the temperature fluctuates rapidly over a short time period [4]. Such conditions are common in high-frequency power converters, like the buck converter. Furthermore, the linear thermal behaviour assumption is deemed an idealistic condition and may not hold true in all circumstances. This assumption can hinder the accuracy of thermal superposition switching loss calculations.

q1b)ii) Double-Pulse Testing

The Double-Pulse method is an alternative to the Thermal Superposition method and aims to simulate the switching events under realistic conditions. As alluded to by the name, two pulses are used: one to turn the device on, and the other to switch it off. The time interval between them is controlled using specific configuration of a signal generator. This method replicates the conditions of the power converter, in this case a buck converter philosophy, enabling the direct measurement of switching losses. More specifically, high-speed oscilloscopes are used to track the transient voltage and current waveforms so that the switching characteristics can be visualised. A simplified example of such is displayed in Figure 2.

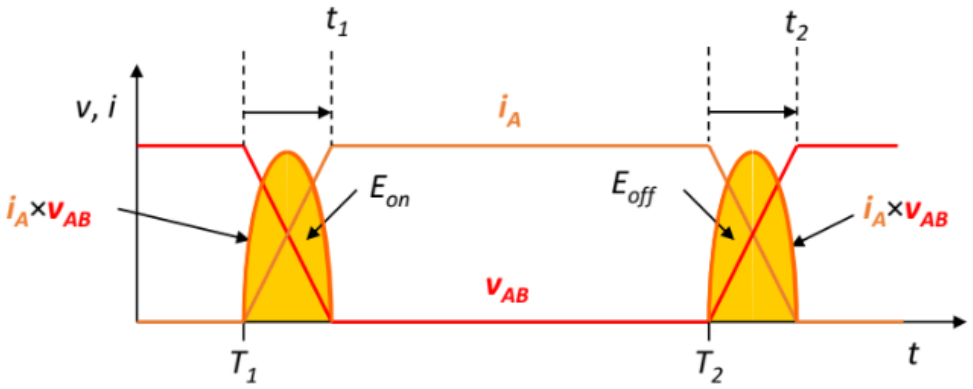

Figure 2: Idealistic Switching Loss Waveform [5]

The on and off transient response can be observed above with T_1 and T_2 marking the start times and t_1 and t_2 representing the duration of the transients. Calculation of the switching losses from the oscilloscope readings is simple and entails use of the following characteristic equations.

$$E_{on} = \int_{T_1}^{T_1+t_1} i_a v_{ab}\, dt \tag{9}$$

$$E_{off} = \int_{T_2}^{T_2+t_2} i_a v_{ab}\, dt \tag{10}$$

This method is deemed advantageous due to its realism when emulating normal operating conditions. This gives hyper-realistic measurements and is particularly useful for high-frequency switching applications, like the buck converter, since the short period transient responses are fully appreciated. These dynamic characteristics are critical for the understanding of high-speed power converters and the ability to capture these responses contributes to accurate predictions of the converter's efficiency and behaviour.

However, these significant benefits come with trade-offs. The testing arrangement is more complex due to the requirement of high-speed oscilloscope instrumentation which also hinders the cost of the method. Furthermore, Dual-Pulse testing only considers the short-term response of the system and is poor for analysis

in the steady-state domain. Since the method focusses on discrete switching events, the real-time or continuous operation is not simulated and the converter losses experienced under these circumstances may not be captured. Lastly, the high-speed testing could induce additional stress on the system with the potential of shortening the lifespan of the device.

q2 Question 2

q2a)

q2a)i) Ferrite and Nanocrystalline Materials in the Transformer of a Power Converter

Nanocrystalline cored materials are becoming increasingly popular in the application of Power Converters. By nature, they possess the high efficiency of ferrites and high permeability of amorphous materials. These reasons are attributed to their reduced power loss, material malleability, and excellent magnetic saturation level properties. The other contender is ferrite materials which are favoured for their high resistivity and cost effectiveness.

Cores made from Nanocrystalline exhibit around 80% lower losses compared to the conventional toroidal shapes and 67% less loss when compared to the same core but made from Nickel Supermalloy [6]. Less losses contributes to a higher system efficiency as more energy is conserved, and hence reduces excess heat generation. Malleability describes the ease of which the material can be moulded. This characteristic is particularly beneficial for the replacement of existing cores made from Supermalloy or ferrite materials as nanocrystalline can be formed into various shapes. Further experimentation in [6] reveals that cores made from nanocrystalline contributes to smaller transformer designs with a greater than 50% reduction in size, and 50% reduction in weight when compared ferrite-based counterparts.

On the contrary, the disadvantages associated with this material include higher cost and lower electrical resistivity. These metrics are dominated by the ferrite-based materials. Their popularity stems from high resistivity and cost. High resistivity is deemed beneficial as this reduces the eddy current losses, making them tremendously useful for high frequency applications like transformers in power electronics. Other advantages focus more closely on the practical side, where cost effectiveness and lightweight properties are apparent and can result in cleaner designs. However, the low saturation flux density of ferrites means that a larger core size is required to compensate for higher power levels.

q2a)ii) Application of Ferrite and Iron Power Core materials in the Choke of a Power Converter

The choke of a power converter serves the integral role of blocking high frequency signals, whilst allowing low frequency signals to pass. The design of a choke is simply an inductor which has an impedance that

can be modelled by (11)

$$X_L = 2\pi f L \tag{11}$$

where it is evidenced that lower frequencies are directly proportional to lower inductive reactance, and likewise for impedance.

With the current demand for devices with greater powers and switching frequencies, the conventional method of using ferrite materials is becoming obsolete and the search for a replacement is imminent. One solution is the utilisation of iron-powder based inductors as these meet the ever-challenging dynamic market demands.

The advantages of iron powdered based inductors include higher magnetic flux levels before saturation. This trait is positive for chokes used in power converters since stronger magnetic fields can be handled without reaching the saturation point. More precisely, the demand for the transition into electronic devices with higher current and lower voltage means that a higher current will drive a stronger magnetic field [7]. The saturation gradient is less steep and so the inductance does not drop as quickly, as it does with ferrite materials. However, a disadvantage of the iron powdered core is its lower permeability which is an issue as it degrades the efficiency of energy transfer [8].

The more traditional ferrite choke inductors have a higher resistivity which in turn, contributes to lower eddy currents and core losses [9]. The coercive force H_c in this instance is also lower which describes a smaller hysteresis loop. This subsequently reduces hysteresis losses since the journey travelled round the coercivity loop will be shorter which ultimately results in higher efficiency as the pathway is reduced per each cycle. The disadvantage of the ferrite material are the advantages of the iron powder as it has low saturation flux densities.

q2b) Thyristor Rectifier Circuit load current calculation

The half-wave rectifier is a method of AC-DC conversion and operates by blocking the negative voltage for half the period while allowing the positive half to pass. This is displayed in Figure 3.

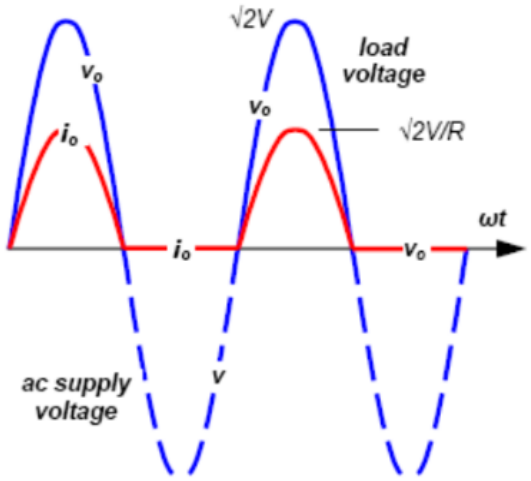

Figure 3: Half-Wave Rectifier Waveform [5]

Figure 4 displays a half-wave rectifier circuit configured with a thyristor. The source voltage is of a sinusoidal nature and is given by V_{ac}, the resistance through the load is R_{load}, and the current through the load is i_{laod}.

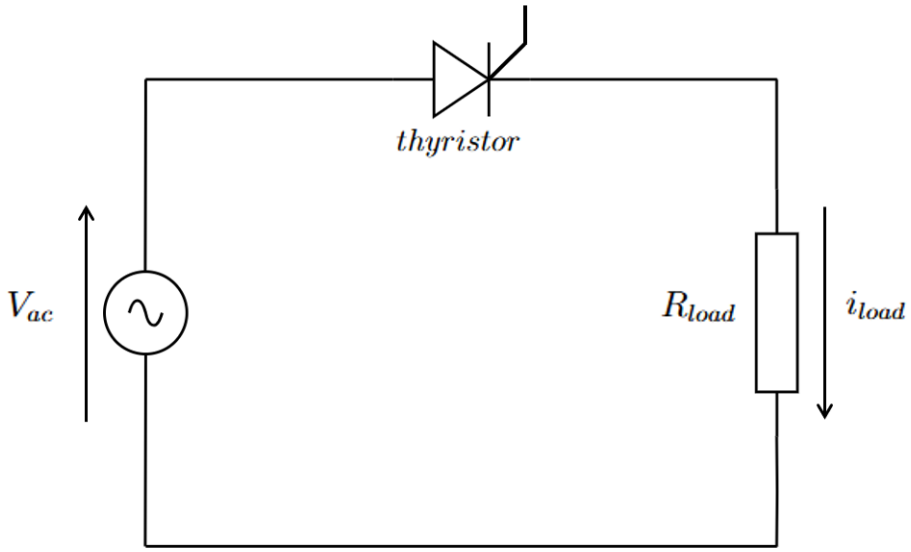

Figure 4: Thyristor Circuit

The derivation for the average voltage commences with an expression for the average value of a periodic waveform and is given by

$$V_{ave} = \frac{1}{T}\int_{\alpha}^{T} V_m \sin(\omega t)\, d\omega t \tag{12}$$

which can be modified for a half-wave rectifier where V_p is the peak voltage. The period of a sinusoid is given by 2π and the interval of evaluation is between π and α.

$$V_{ave} = \frac{V_p}{2\pi} \int_{\alpha}^{\pi} \sin(\omega t)\, d\omega t \tag{13}$$

Integrating yields

$$V_{ave} = \frac{V_p}{2\pi} \left[-\cos(\omega t) \right]_{\alpha}^{\pi} \tag{14}$$

and substitution of the upper and lower limits gives the following expression

$$V_{ave} = \frac{V_p}{2\pi} (1 + \cos(\alpha)) \tag{15}$$

where α is the thyristor triggering angle. Utilisation of the known parameters, the average voltage can be computed.

$$V_{ave} = \frac{325.27}{2\pi} (1 + \cos(65)) = 147.3V \tag{16}$$

Using this in alignment with Ohm's law, the average current through the resistive load i_{load} can be calculated

$$i_{load} = \frac{V_{ave}}{R_{load}} = \frac{147.3}{2 \times 500} = \underline{\mathbf{0.1473A}} \tag{17}$$

q2c) MOSFET Junction Temperature Calculation

An expression for the power dissipated across the MOSFET in the thermal domain is

$$P_{loss} = \frac{T_J - T_A}{R_\theta} \tag{18}$$

The same can be achieved in the electrical domain which commences with

$$P_{loss} = I_{rms}^2 R_{DS} \tag{19}$$

Aside, an equation for R_{DS} is generated as (20) and is modelled from the derivation in [10]. This article discusses the logic behind the ambient temperature selection for a MOSFET.

$$R_{DS} = R_{DS(on)20}[1 + k_\theta(T_J - T_{J_{SPEC}})] \tag{20}$$

Substitution of (20) into (21) forms the complete electrical expression for P_{loss}

$$P_{loss} = I_{rms}^2 R_{DS(on)20}[1 + k_\theta(T_J - T_{J_{SPEC}})] \tag{21}$$

Equating the electrical and thermal equivalent equations yields (22). This can be solved by inputting the parameters in Table 1, and solving for the junction temperature T_J. It is worth noting that in this instance that $T_{J_{SPEC}} = T_A$

$$\frac{T_J - T_A}{R_\theta} = I_{rms}^2 R_{DS(on)20}[1 + k_\theta(T_J - T_{J_{SPEC}})] \tag{22}$$

$$\frac{T_J - 20}{7} = 16^2 \times (25 \times 10^{-3}(1 + 0.011(T_J - 20)] \tag{23}$$

$$T_J = \underline{\mathbf{108.33}}^\circ c \tag{24}$$

This operation can be supported by a positive, closed-loop feedback system displayed in Figure 5. The operation nodes adopt the intuitive convention where multiplication signs indicate the product of two elements, and addition or subtraction denote the sum or difference.

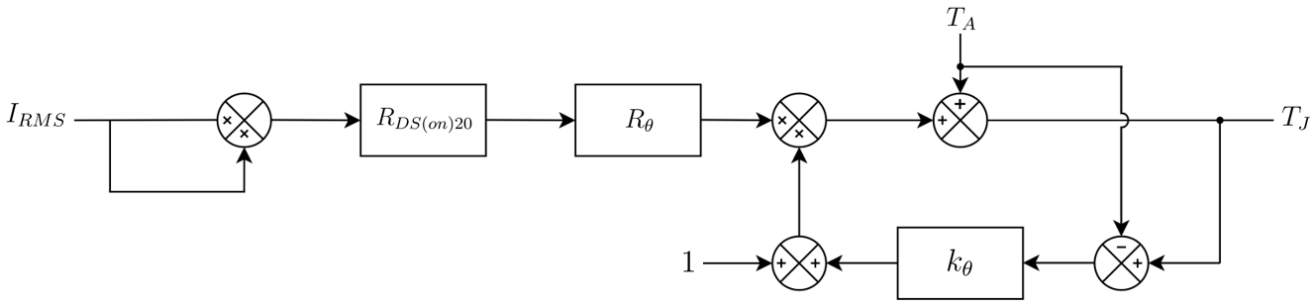

Figure 5: MOSFET Junction Temperature Control Diagram

The correctness of the system can be verified by deriving the input I_{rms} in terms of the block parameters and as a function of the junction temperature output T_J.

The derivation commences by analysis of the output, but specifically, its contribution to the feedback term. The expression builds with the following

$$T_J - T_A \tag{25}$$

which is fed into the coefficient rise block producing

$$k_\theta(T_J - T_A) \tag{26}$$

The feedback loop completes by adding one

$$1 + k_\theta(T_J - T_A) \tag{27}$$

Next, an expression for the other contribution looking at the node is computed by finding the product of all forward pass terms. This is represented as

$$I_{rms}^2 R_{DS(on)20} R_\theta \tag{28}$$

Lastly, this expression is multiplied by (27) and the resultant is summed with the ambient temperature to form the final expression for the junction temperature of the MOSFET.

$$T_J = I_{rms}^2 R_{DS(on)20} R_\theta (1 + k_\theta(T_J - T_A)) + T_A \tag{29}$$

which aligns with the form in (23), and hence finalising the correctness of the positive feedback, closed loop block diagram.

q3 Question 3

q3a) a

q3a)i) Operating Duty Factor calculation

The duty factor D for a circuit of this configuration is given by

$$D = \frac{V_{out}}{V_{in}} \times \frac{N_1}{N_2} \tag{30}$$

This can be simply solved using the parameters given in the question.

$$D = \frac{14}{48} \times \frac{32}{26} = \underline{\mathbf{0.359}} \tag{31}$$

q3a)ii) Minimum support voltage of Diode D_r

The equation for the minimum support voltage of diode D_r is shown in 32 and can be solved by inputting the necessary parameters.

$$D_r = \frac{N_2}{N_1} \times V_{in} \tag{32}$$

$$D_r = \frac{26}{32} \times 48 = \underline{\mathbf{39V}} \tag{33}$$

q3a)iii) Output Power for entrance into boundary conduction mode

Boundary Conduction Mode describes the medium between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The behaviour of the load current i_L, as a function of time, can be visualised in Figure 6 where the switches on time t_{on} and off time t_{off} are clearly labelled.

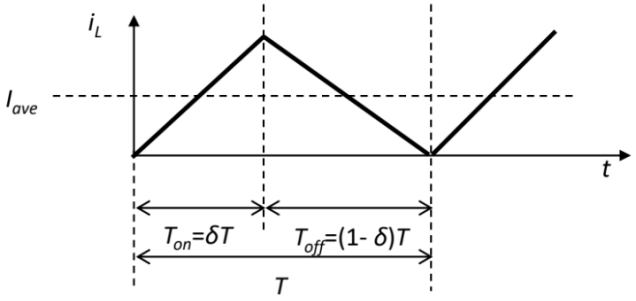

Figure 6: Inductor Current in Boundary Conduction Mode [5]

The characteristic equation that expresses the inductor voltage V_L in terms of the rate of current Δi can be rearranged to yield

$$i_{peak} = \frac{V_{out} \times DT}{L} = \frac{14 \times 0.359 \times \frac{1}{120 \times 10^3}}{180 \times 10^{-6}} = 0.4155A \tag{34}$$

It is known that in Boundary Conduction Mode, the average current is simply half the peak current.

$$i_{ave} = \frac{i_{peak}}{2} = \frac{0.4155}{2} = 0.2078A \tag{35}$$

Lastly, the power is calculated as

$$P = I_{ave}V = 0.2078 \times 14 = \underline{\mathbf{2.91W}} \tag{36}$$

q3a)iv) Flux Density Swing of Transformer's core material

An equation for the Flux Density Swing is taken from the Texas Instruments application report for MOSFET and IGBT Gate Drivers [11]. This can be rearranged for the flux density swing ΔB and solved in accordance with the parameters given in the question.

$$\Delta B = \frac{V_{in}DT}{N_1 A_e} = \frac{48 \times 0.359 \times \frac{1}{120\times10^3}}{32 \times 69 \times 10^{(-3)^2}} = \underline{\mathbf{65mT}} \tag{37}$$

q3a)v) Peak Magnetising Current drawn by the transformer

The calculation for the peak magnetising current i_m stems from the assumption that the airgap in the transformer is 0mm wide. This is justified since the transformers in forward converters are not required to store energy, hence the omission of an airgap. However, other configurations, like the fly-back converter do require energy storage and so a curve modelling the change in airgap length against the magnetising inductance would need to be plotted. Consequently, the EFD30/15/9-3C90 model was selected and to maximise the magnetising current, the error margin was set to -25%.

The expression for the magnetising current is taken from [12] and is displayed in (38).

$$I_m = \frac{V_b DT}{L_m} \tag{38}$$

From the feroxcube datasheet, the inductance per turn of the transformer coils is given as $A_L = 2100 \pm 5\%\, nH$ and is converted to inductance by the formula

$$L_m = A_L N_p^2 = 2100 \times 0.75 \times 10^{-9} \times 32^2 = 1.613 \times 10^{-3} H \tag{39}$$

This can be substituted into (38) to yield

$$I_m = \frac{48 \times 0.359 \times \frac{1}{120 \times 10^3}}{1.613 \times 10^{-3}} = \underline{\mathbf{89.03mA}} \tag{40}$$

q3b) Low Voltage Control Circuity

As stated in the assignment brief, driving the upper transistor TR1 can become problematic as the voltage source swings between 0 to 48V. The incorporation of a bootstrap diode, boostrap capacitor in a flying configuration, high-voltage level-shifting MOSFET, and driver IC to solve this problem is discussed in this section. The circuit diagram for this solution is displayed in Figure 7.

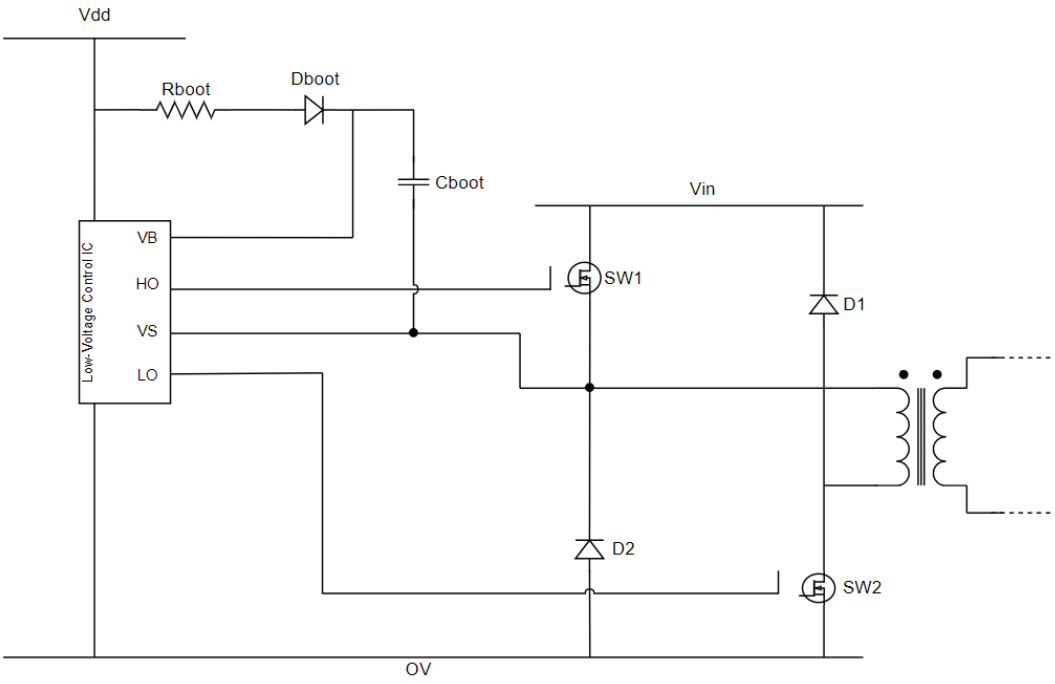

Figure 7: Level Shifting Circuit Implementation

The voltage level of the MOSFET SW1 is controlled in 3 phases. During the first phase, SW1 is open and SW2 is closed. This enables the subsequent charging of the flying capacitor which drains the current from Vdd until the capacitor voltage is equal to Vdd. This can be visualised in Figure 8.

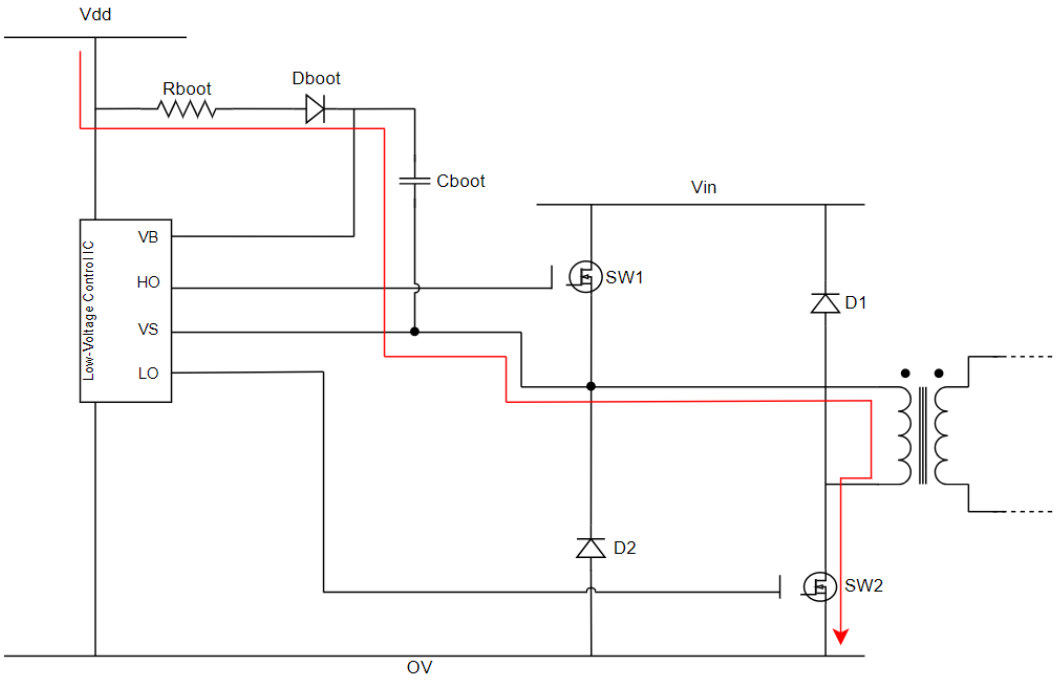

Figure 8: Level Shifting Stage 1 Current Flow

In the next stage, both switches are open and so the bootstrap diode is reversed biased to ensure that the current flowing back to Vdd is blocked. Switch 2 then closes, with Switch 1 remaining open, and allows the current to take the path shown in Figure 9.

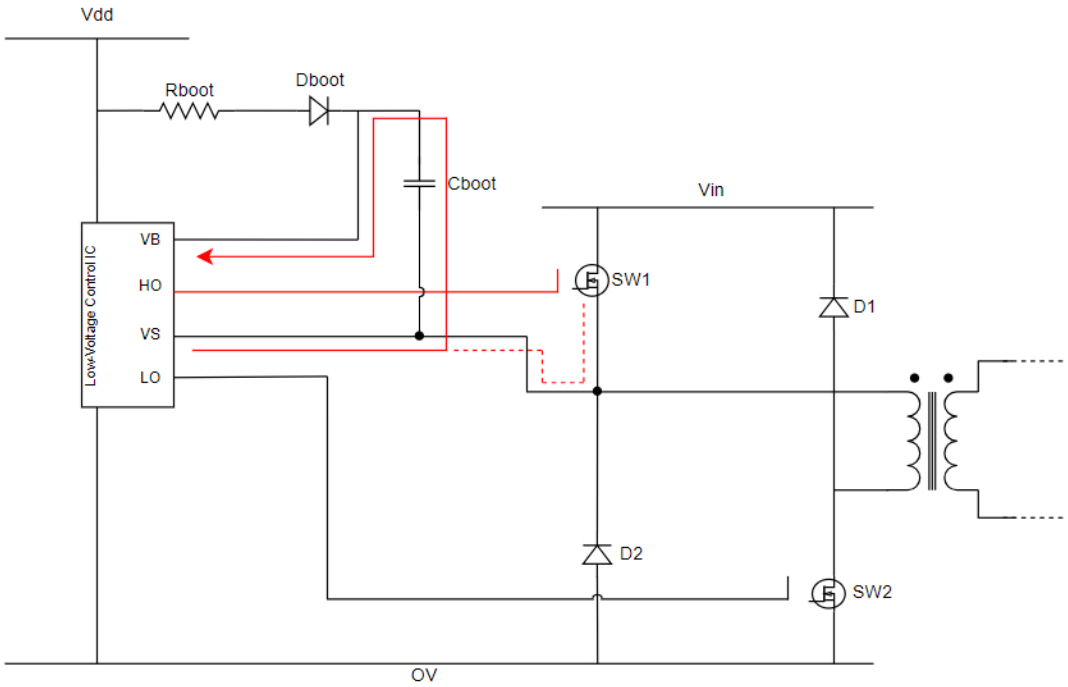

Figure 9: Level Shifting Stage 3 Current Flow

Thus, the voltage experienced by the MOSFET is between the gate and source, and can be controlled by

selection of an appropriate sized Vdd supply. This charging and discharging cycle must be implemented every time to switch the MOSFET. The main advantage of this design is that it solves the voltage swing from 0V to 48V using a relatively simple and low-cost design.

However, a drawback is that the capacitor needs to be charged and discharged every time the MOSFET activates and so the duty cycle of the dual switch forward converter is limited. Furthermore, negative voltage is observed at the source of the MOSFET during turn off which causes current to suddenly flow through SW2 as shown in Figure 10.

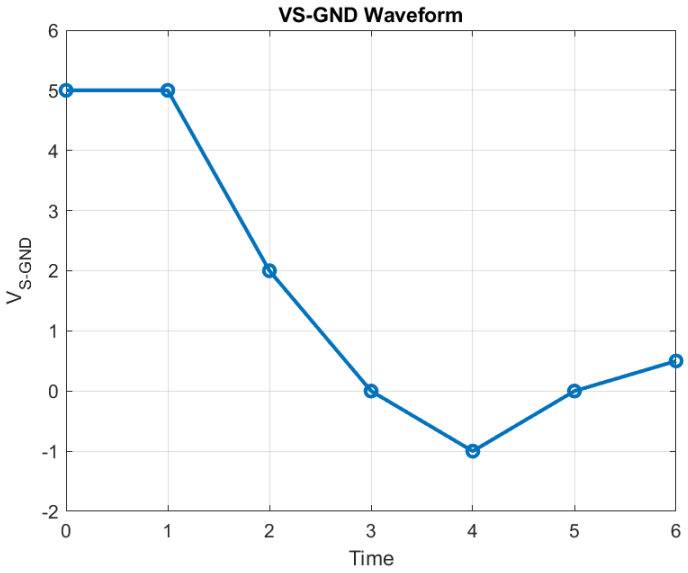

Figure 10: Voltage Waveform from Vs pin to Ground

This can be detrimental to the output stage of the gate driver since it has a direct impact on the VS pin of the level shifting control IC and may pull some internal circuitry below ground level.

Another issue that arises due to the negative voltage transient is the chance that an over-voltage condition is developed across the bootstrap capacitor. This is charged by the bootstrap diode from the Vdd source. Since Vdd is ground referenced, the maximum voltage across the capacitor is the sum of Vdd and the magnitude of the negative voltage transient - contributing to additional stress across the capacitor terminals.

q3c) Dual-switch Forward converter Synchronous Rectification

Synchronous rectification is achieved by replacing diodes D_r and D_f with MOSFETs. The two commonly used synchronous rectification philosophies are: Self-Driven and Control Driven. In this occasion, the Control Driven method was not implemented due to thoughts concerning the word count and reducing verbosity. To summarise concisely, this method describes controlling the switching of MOSFETs using an external controller that acts to precisely determine the ON and OFF times based on timing signals. Pulse Modulated Wave (PWM) signals learned from feedback loops are used to optimise timing and effectively minimise losses in a dynamic manner.

Self-Driven rectification operates by deriving the gate driving signal directly from the secondary side of the transformer rather than an external controller. A diagram showcasing the self-driven synchronous rectification concept in the context of a forward converter is displayed in Figure 11 where the black dots denote the mutual transformer inductance during primary switch on time, the red dots denote the reversed polarity mutual inductance during primary switch off time, and the MOSFET body diodes are considered internal to the MOSFET, hence their exclusion from the diagram.

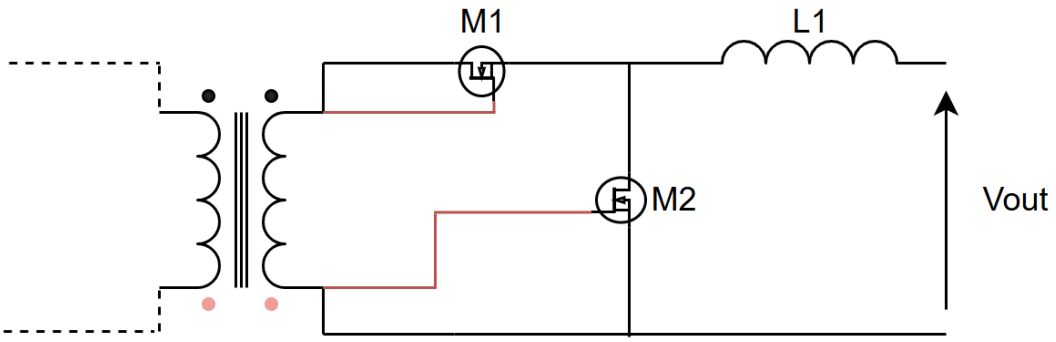

Figure 11: Self-Driven Synchronous Rectification of Dual-Switch Forward Converter

The operation of this MOSFET implementation is similar to using diodes with M_1 in forward operation and M_2 in freewheeling mode. During the on time, primary side switches TR1 and TR2 are closed, current from the source V_{in} interacts with the transformer, M1 is driven closed due to the polarity of the transformer voltage, M2 is open since the self-driven signal does not meet the gate threshold, and power is provided to the output and charge is stored in the inductor L_1. The primary side transistor switches then turn off, the transformer reverses polarity due to the back electromotive force (EMF) caused by the breakdown of the magnetic field in the transformers, subsequently reversing the polarity of the transformer voltages, hence changing the self-driven signals to cause M1 to open and M2 to close, and the output power is generated from the stored energy in L_1.

The main advantage with synchronous rectification with MOSFETs compared to a purely diode implementation is that the efficiency is improved tremendously due to diodes having greater conduction losses than MOSFETs. Subsequently, this contributes to reduced heat generation and hence improved thermal performance, with potential to lower the need for cooling. Furthermore, the conduction losses are controlled by the on-state resistance of the MOSFET due to $I^2R_{DS(ON)}$ losses. In theory, these losses can be controlled, with the tradeoff being cost, as larger MOSFETs tend to have lower on-state resistances [13]. However, this utilisation of MOSFETs is disadvantageous due to the switching losses present during on and off times. A plot of this relationship is displayed in Figure 12.

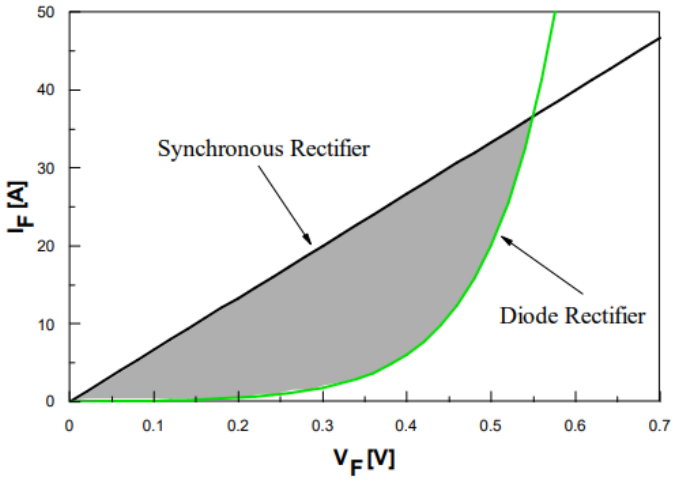

Figure 12: Diode vs Synchronous Rectifier Losses Comparison [14]

When compared to its IC controlled counterpart, the self-driven method can be regarded as superior in terms of cost, since an external gate driving component is not required. The simplicity of operation is also desired with the timing of gate driving signals aligning conveniently with the transformer activity, enabling the MOSFET gate to be driven directly from the transformer without any additional components required. On the other hand, having a controlled gate signal gives finer command on the timing of switching and often, does not switch on or off at the optimal moment. This can lead to dwell time during the off time of the primary switches (TR1, TR2), after the transformer has reset but before the primary switches turn back on. This exists since the reset time remains constant, while the duty cycle decreases when the input voltage increases, leading to a longer unused section of the switching cycle at greater voltages. This is illustrated in Figure 13 where the subscript R denotes the freewheeling device, F is the forward device, Q1 is the primary switch, DS is the drain to source voltage, and GS is the gate to source voltage [15].

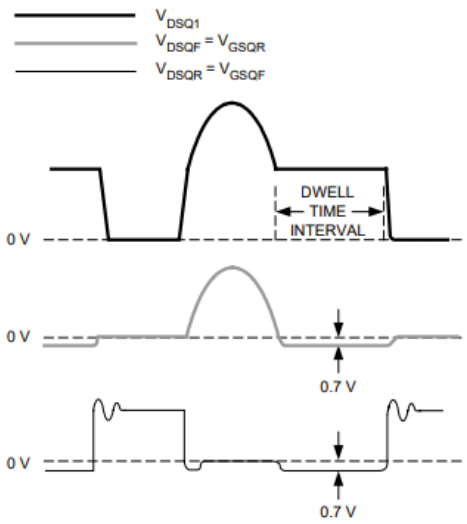

Figure 13: Self-driven Synchronous Forward Converter Waveform [15]

The convenience of the self-driven property also proves to be a downfall as the gate driving signal must be of sufficient magnitude to open and close the MOSFET switch. This means that the turns ratio of the transformer is heavily constrained as it must be specifically designed to provide a gate driving signal greater or equal to the gate switching threshold.

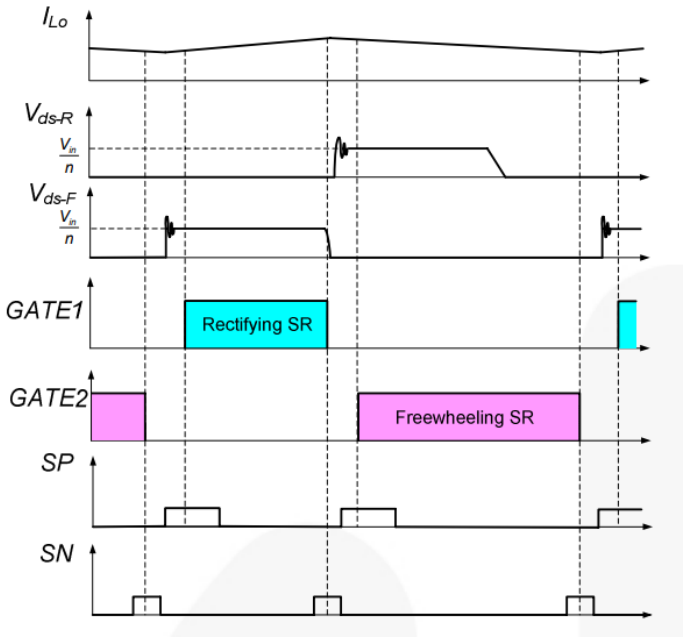

Figure 14: Continuous Conduction Mode Waveform Response [16]

The waveforms for the Continuous Conduction Mode (CCM) operation of the proposed rectifier design is displayed in Figure 14 where I_{LO} is the inductor current, V_{ds-R} and V_{ds-F} are the drain voltages of M1 and M2, Gate 1 and 2 are the gates of the MOSFETS, and SP and SN are the driving signals. The Discontinuous Current Mode (DCM) case is displayed in Figure 15.

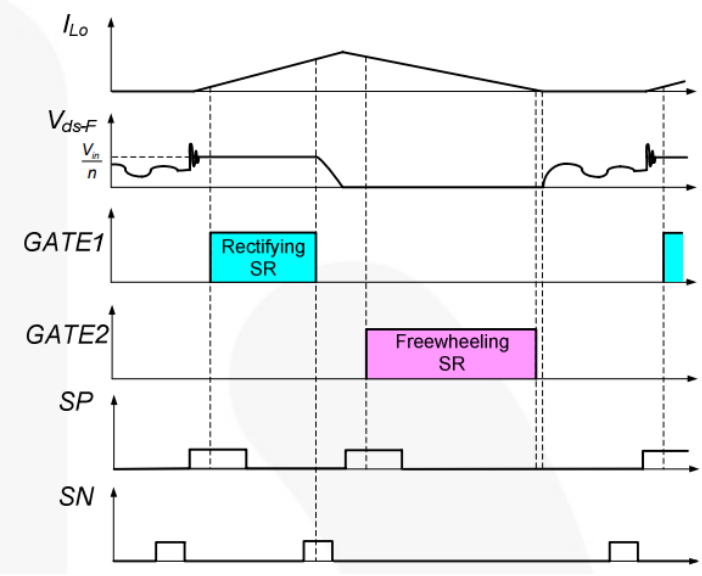

Figure 15: Discontinuous Conduction Mode Waveform Response [16]

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