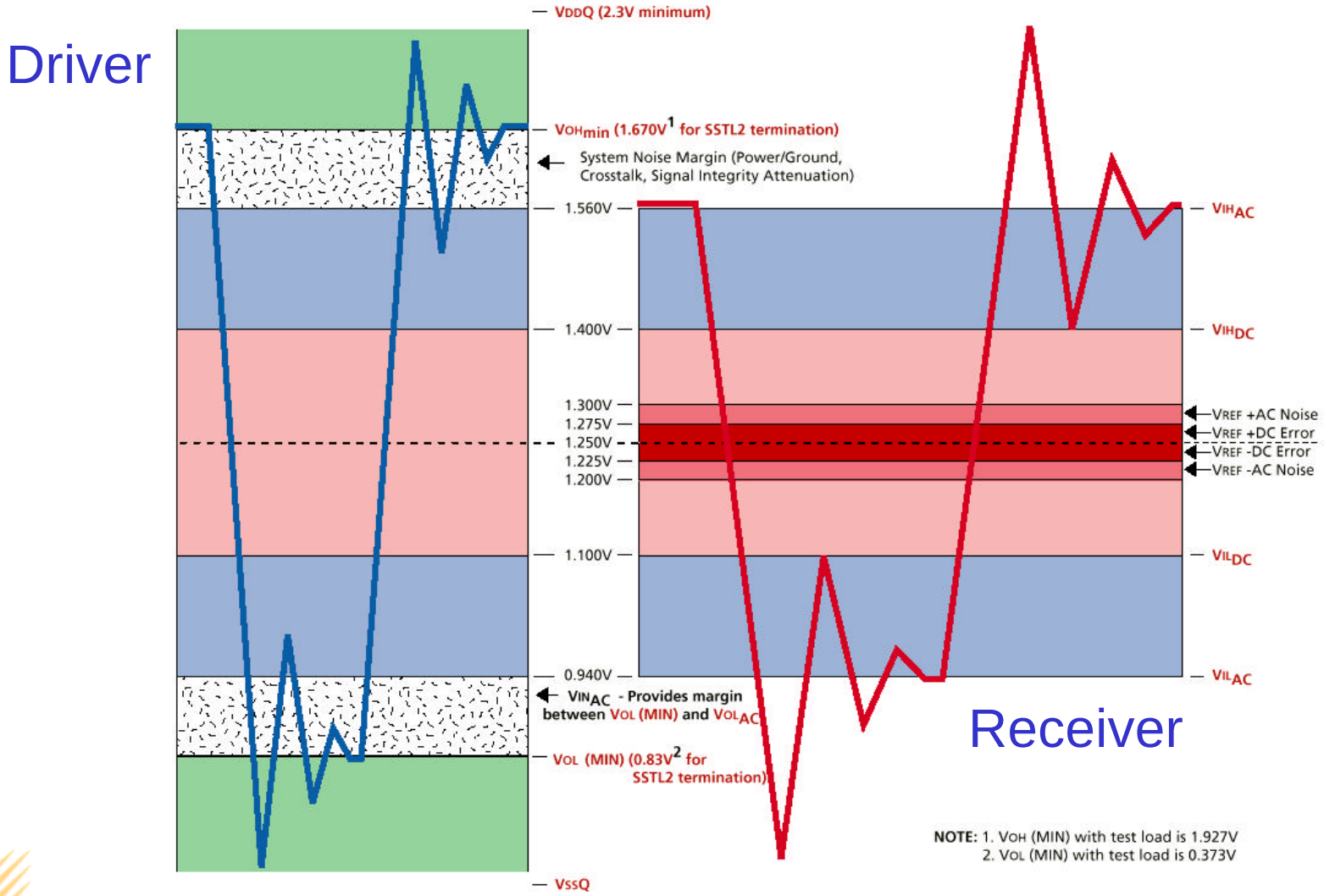
DDR System Design Considerations

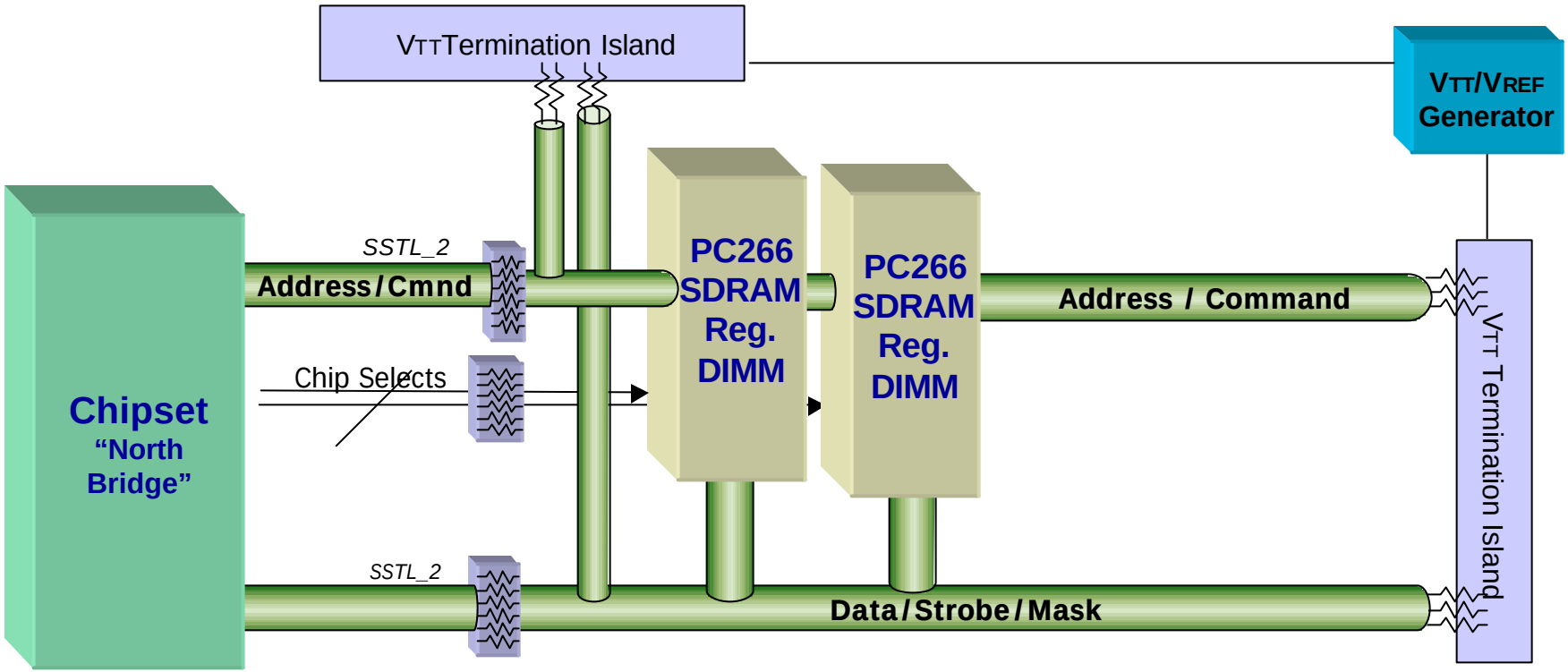
Integrated Technology Group
Micron

DDR Overview

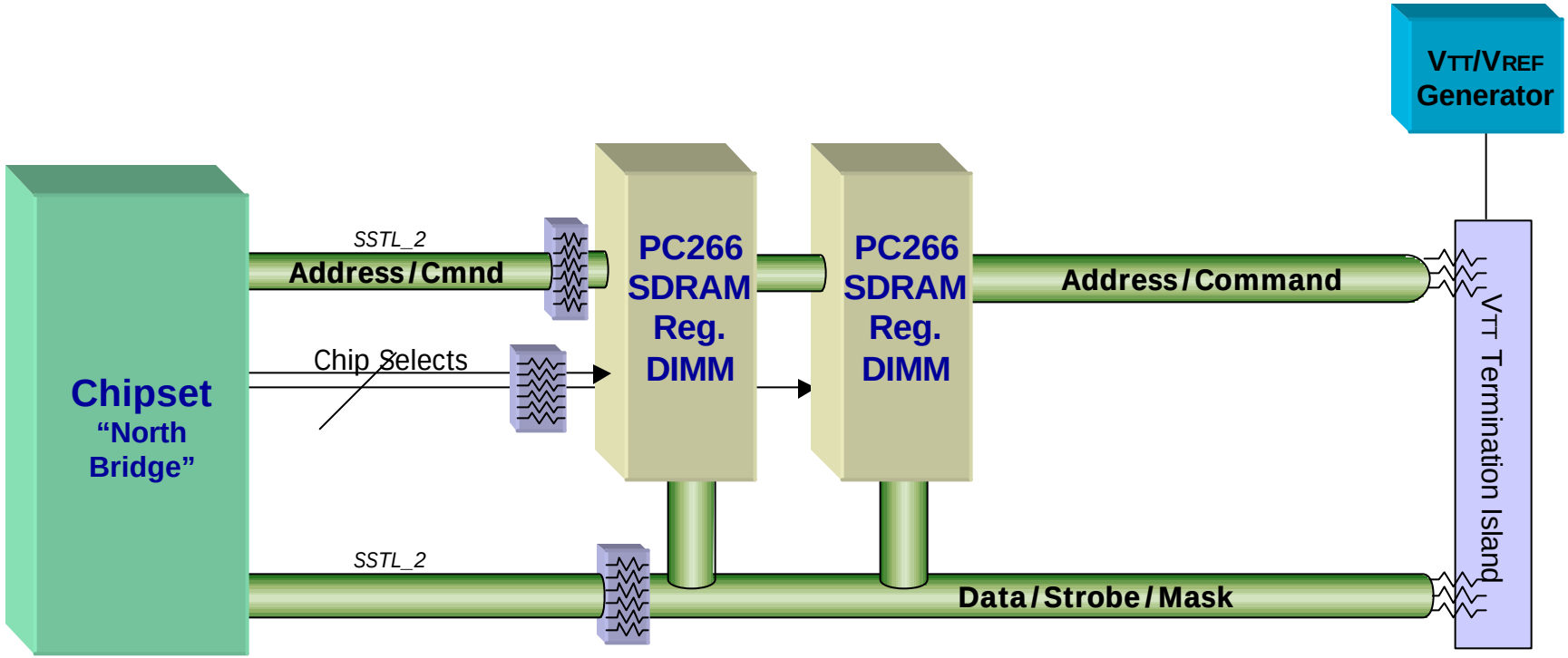
SSTL2 Signal Levels



SSTL2 Double Ended Termination



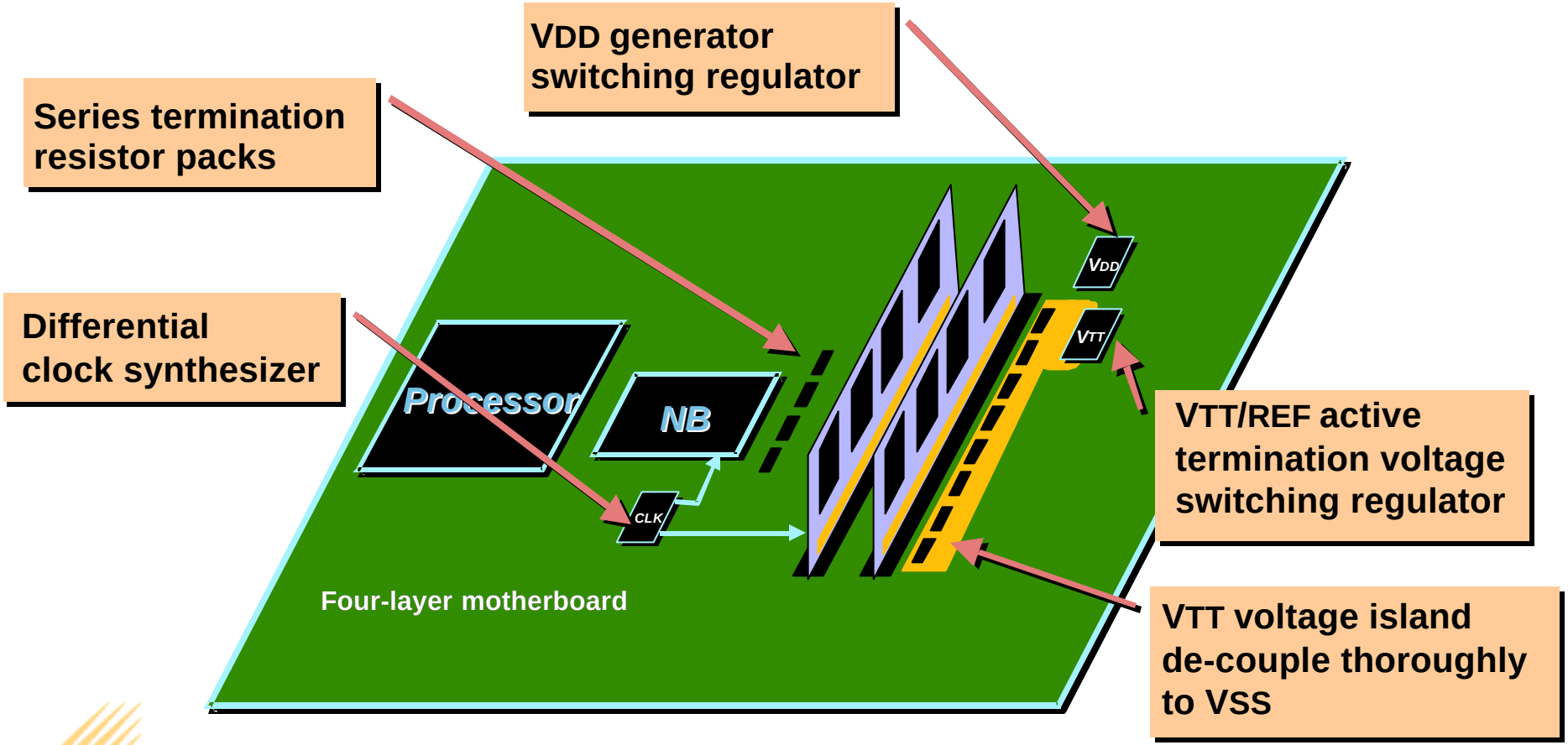
SSTL2 Single Ended Termination



Use Single Parallel Termination Resistor With Series Resistor

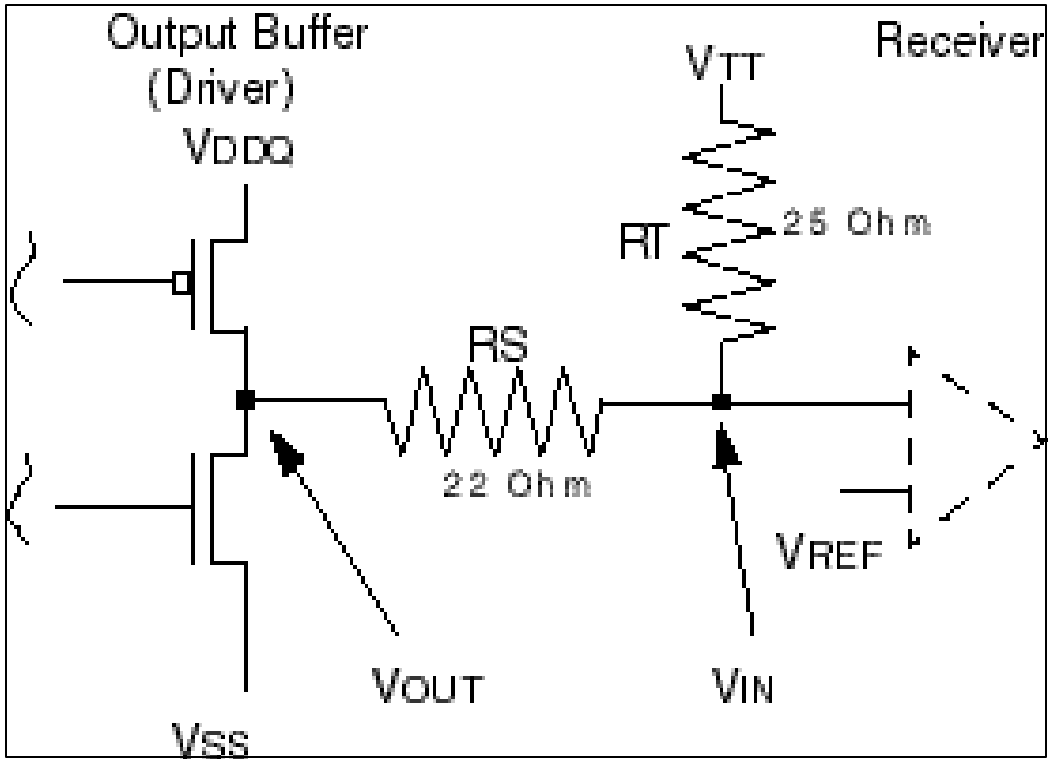
- Lower system cost
- Easier motherboard route
- Improved bandwidth
- Lower skew due to ISI
- Reduced skew due to crosstalk if done properly
  - Consider crosstalk effects in the connector pinout

Double Data Rate Motherboard Components



Typical Signaling for DDR Main Memory

- The values for the series and termination resistors vary depending on the system design



VTT/VREF Implementation

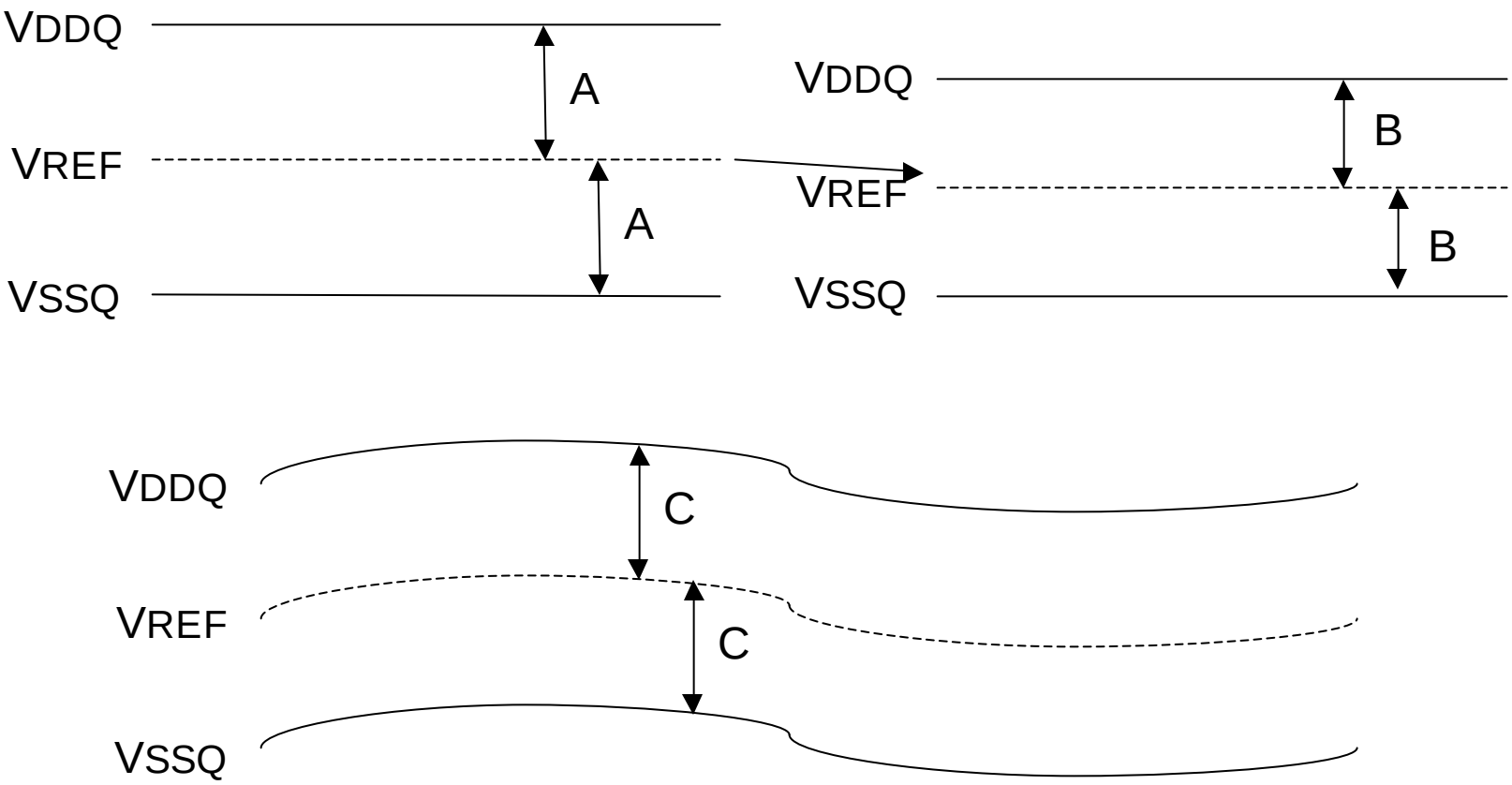
Goals of VTT and VREF Design

- Minimize timing skew due to
  - Asymmetric logic highs versus logic lows
  - Noise on VREF or VTT
  - Offset of VTT relative to VREF
  - Drift of VREF or VTT over voltage and temperature
  - External component mismatch
- Minimize cost
- Minimize power dissipation

VREF Requirements

- Track 50% of (V_{DDQ}-V_{SSQ}) over
  - Voltage
  - Temperature
  - Noise
- Supplies minimal DC current (input leakage only) and only small transient currents
  - Input to NFET gates of a differential pair

VREF Tracking to VDDQ

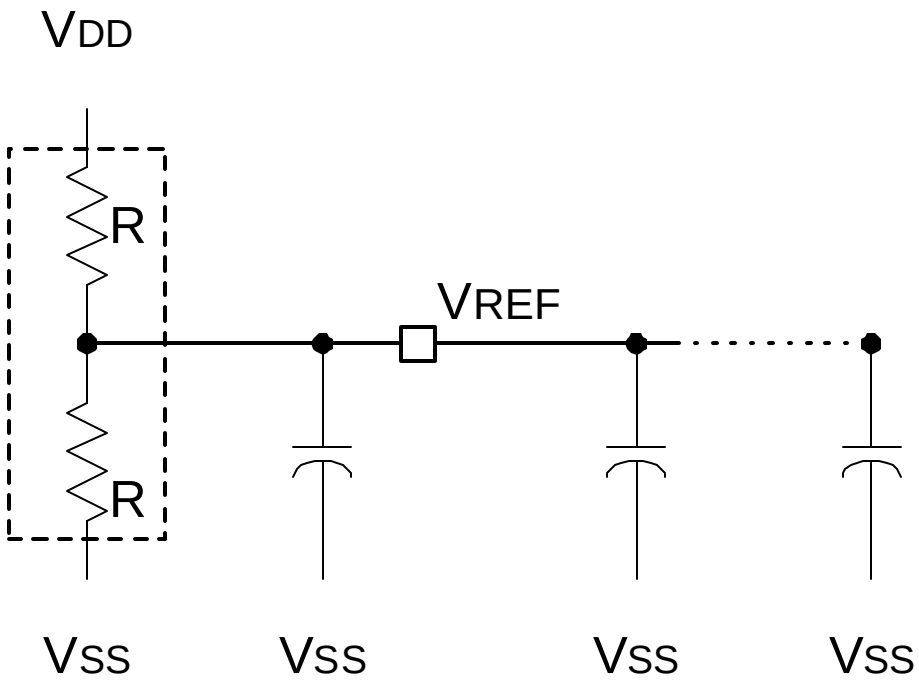


VREF Recommendations

- Use global V_{REF} distribution scheme
  - Eliminates variation and tracking of multiple generators
  - Best performance if kept clean
- Use simple resistor divider with 1% or better accuracy
  - Inexpensive to use
  - Tracks voltage and temperature well
- Use V_{REFOUT} pin of ML6554
  - Resistor divider is integrated on-chip
  - Fewer external components
  - Best accuracy and matching to V_{TT} due to trimming
  - Minimizes DC error caused by the load current of multiple device input leakage

VREF Generation

- **Example of VREF generation using a resistor divider**

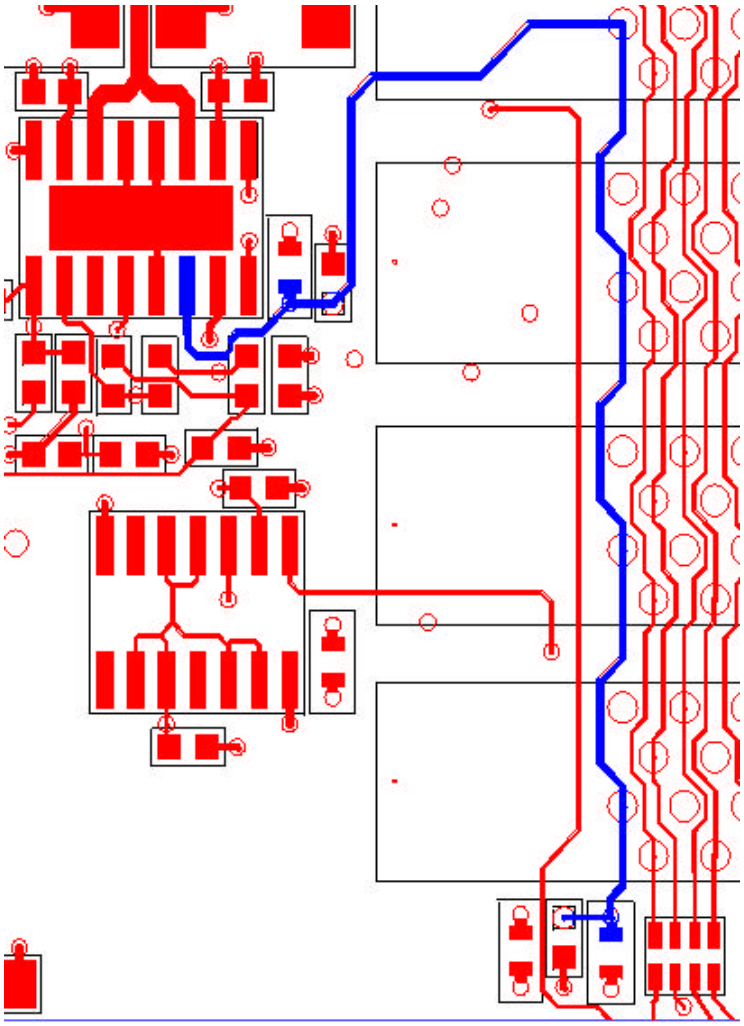


Discrete Resistors or VREF (OUT) of ML6654

VREF Layout Recommendations

- Maintain a 15-20 mil clearance from other nets
- Use distributed decoupling scheme
  - Minimizes capacitor ESL
  - Localizes transient currents and returns
- Simple implementation by routing on top signal layer trace
  - V_{REF} is at connector pin 1
  - Isolate V_{REF} and/or shield with V_{DDQ} and V_{SSQ}

VREF PCB Routing



VTT Requirements

- Track 50% of (V_{DDQ}-V_{SSQ}) over
  - Voltage
  - Temperature
  - Noise
- Maintain <40mV offset from V_{REF} over these conditions
- Source and sink DC current for signal termination
  - Absolute maximum current is 2.6-2.9A for a 64/72-bit channel

VTT Recommendations

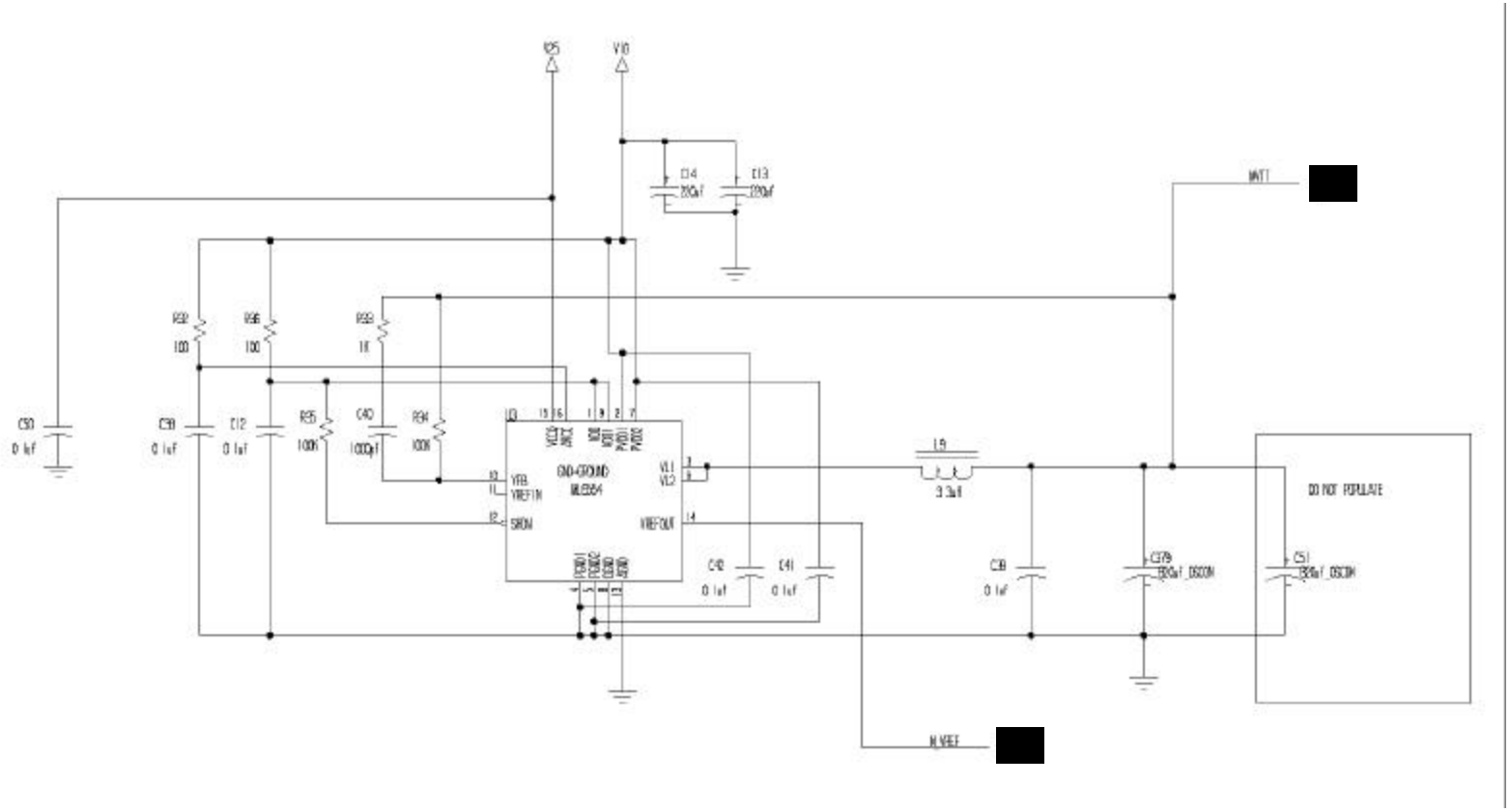
- Several solutions exist that are tradeoffs of cost, integration, and performance
  - Standard analog components (Motorola, National, Fairchild, etc.)
    - High current output, good accuracy
  - Switching regulator with discrete MOSFETs (such as LTC1430)
    - High current output (10A), good accuracy, semi-integrated
  - Switching regulator with integrated MOSFETs (such as ML6554)
    - Adequate current output (3A) and accuracy, highest integration, lowest cost

VTT Recommendations (continued)

- Use global VREF as input reference to minimize tracking error and offset
- Use high-quality filter components
  - Low Rs on filter inductor
  - Low ESR and ESL on filter capacitor to minimize DC and dynamic offset
    - Recommend the use of multiple parallel capacitors and/or Sanyo OS-CONs to minimize ESR and ESL

VTT Regulation Circuit

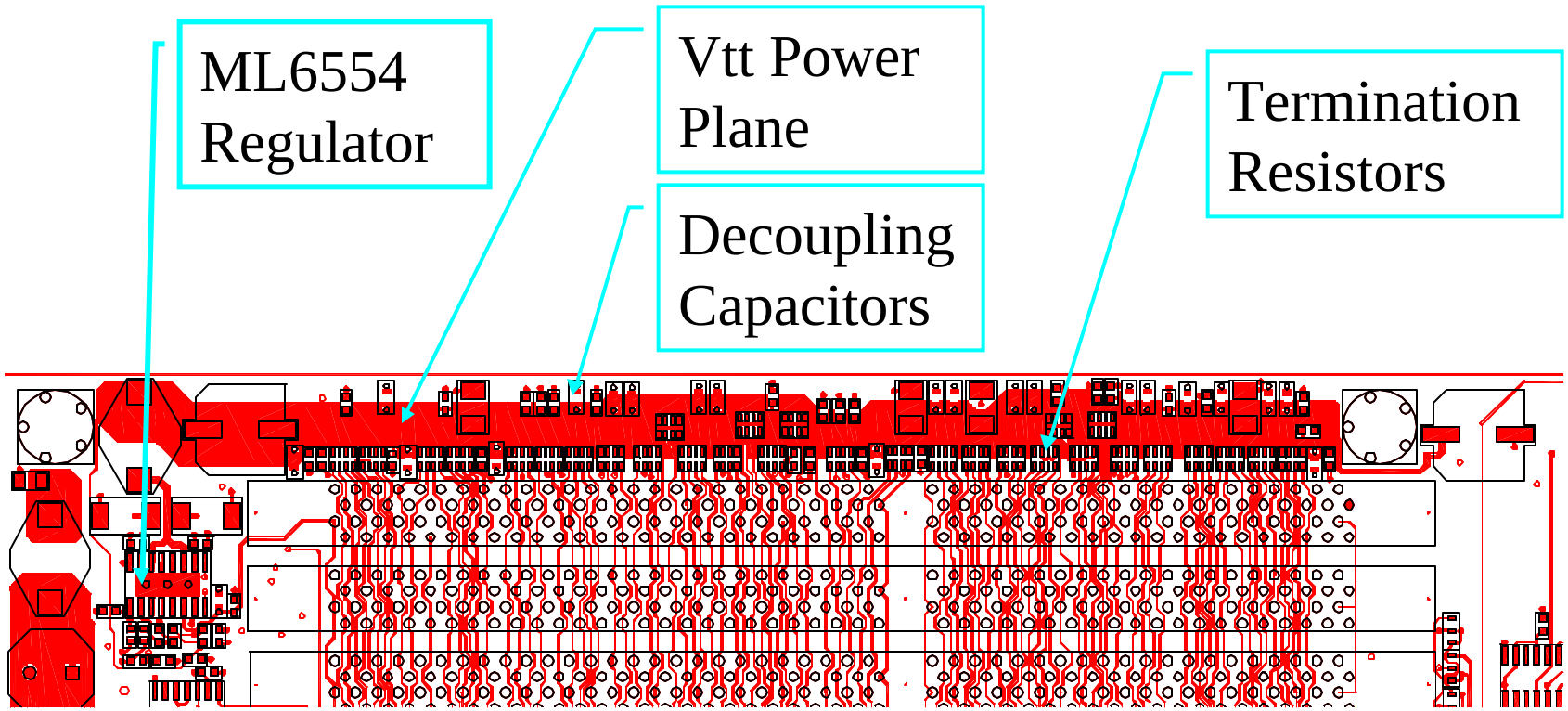
- VTT regulation circuit using Micro Linear ML6554



VTT Layout Recommendations

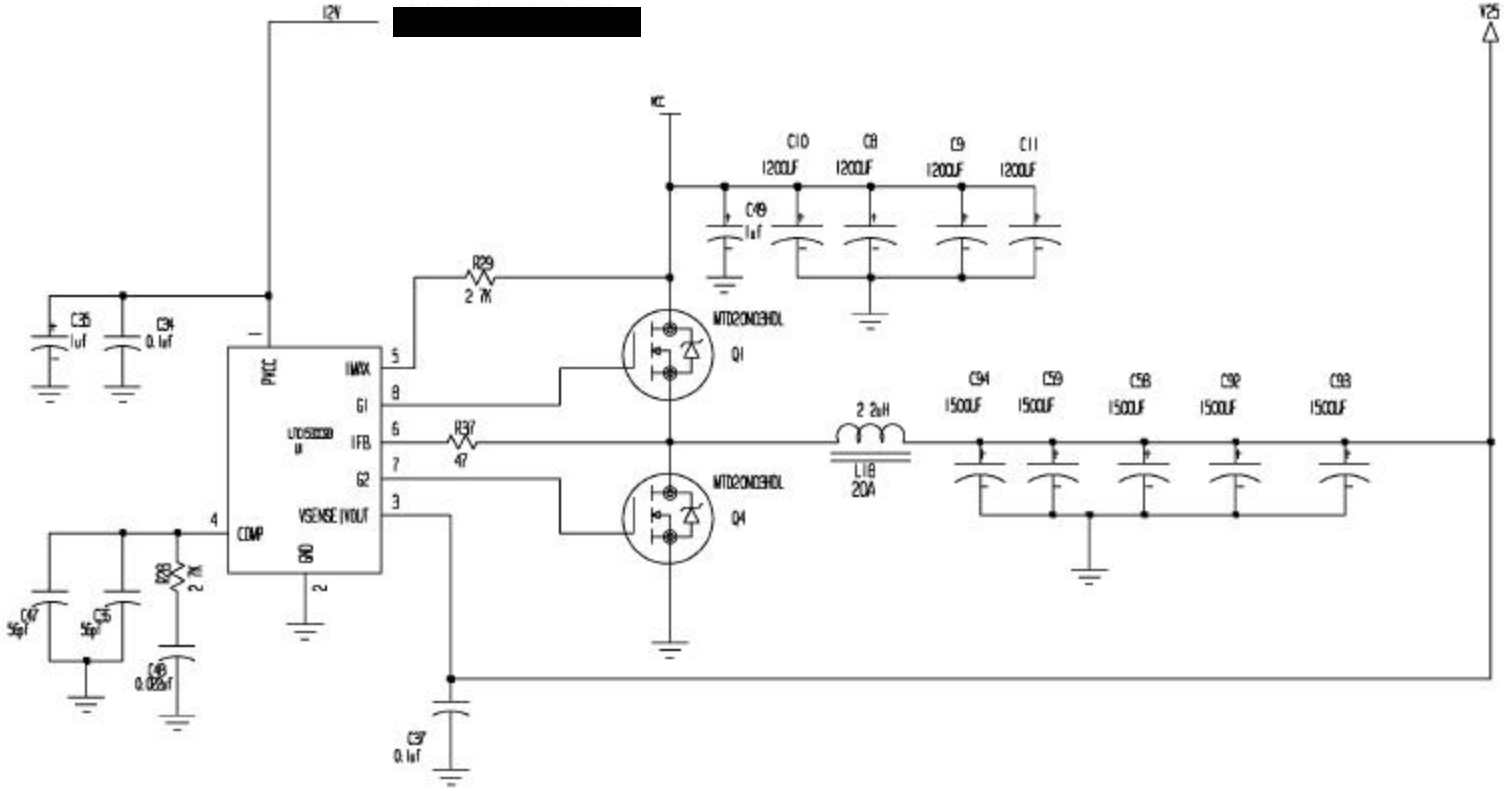
- Decouple to VSSQ
  - Decouple at both ends, and distribute decoupling across the island to localize transient currents and minimize ESL
- Place termination resistors on a top layer VTT island
  - Island is at the end of the bus and non-obstructing
  - Use wide-island trace for current capacity
  - Place VTT generator as close to termination resistors as possible to minimize impedance (inductance)

VTT Island PCB Layout



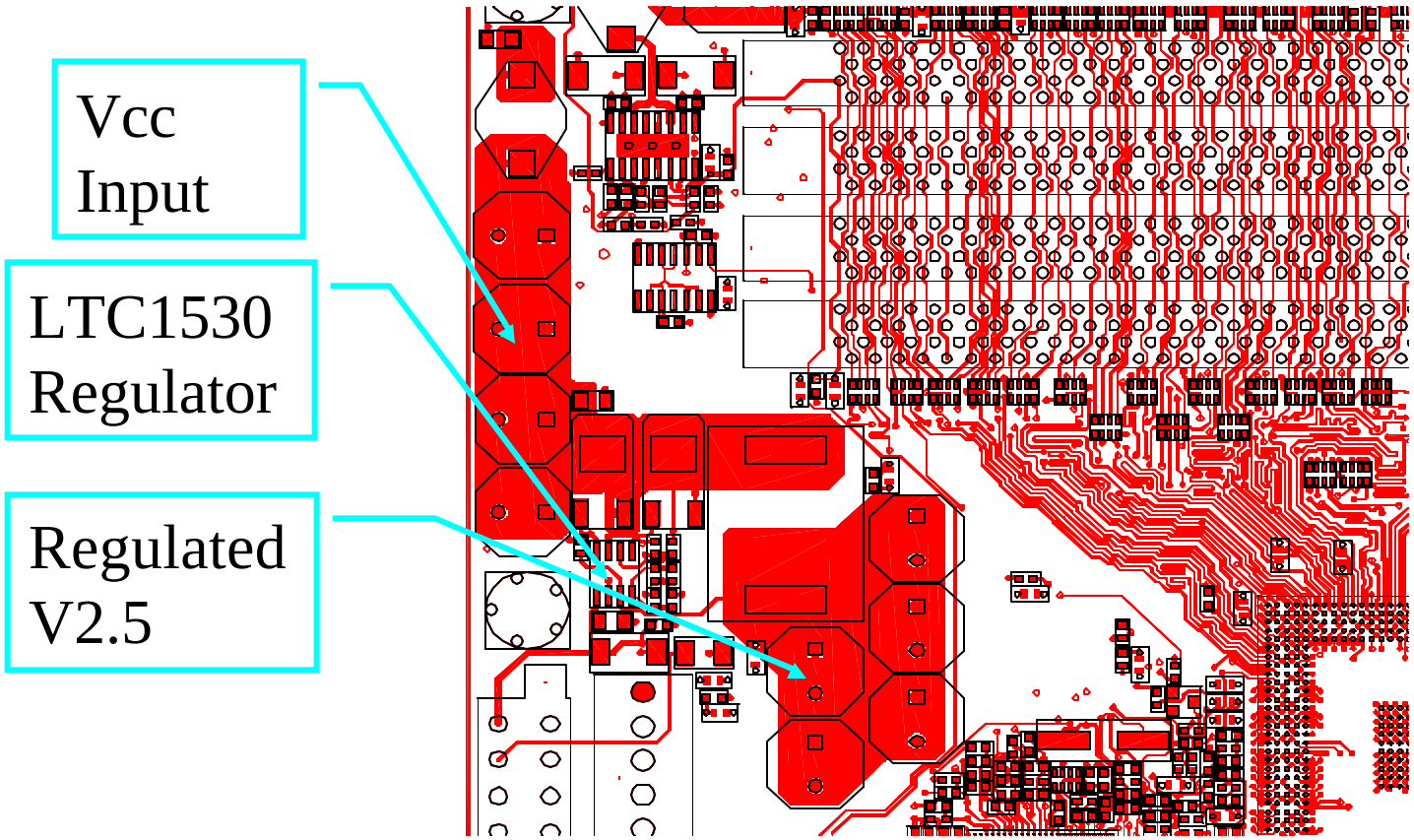
2.5 Volt Regulation

- 2.5 volt regulation circuit using Linear Technology LTC1530-2.5



2.5 Volt Regulation Layout

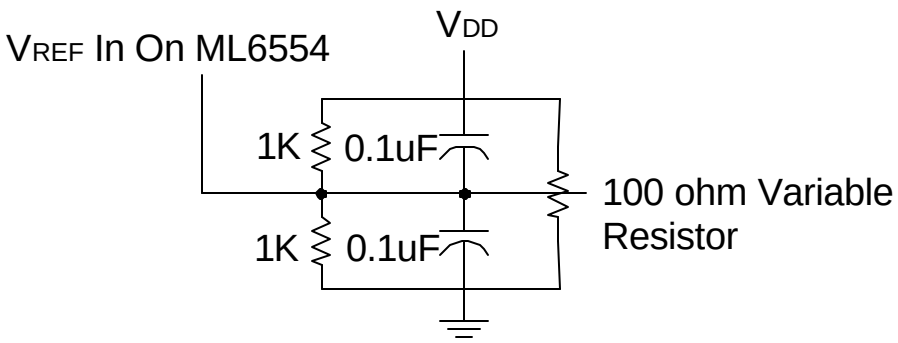
- **Regulated V2.5 ties to solid power plane under DIMM's and DRAM controller portion of Samurai DDR**



Voltage Margining

VREF/VTT Margining

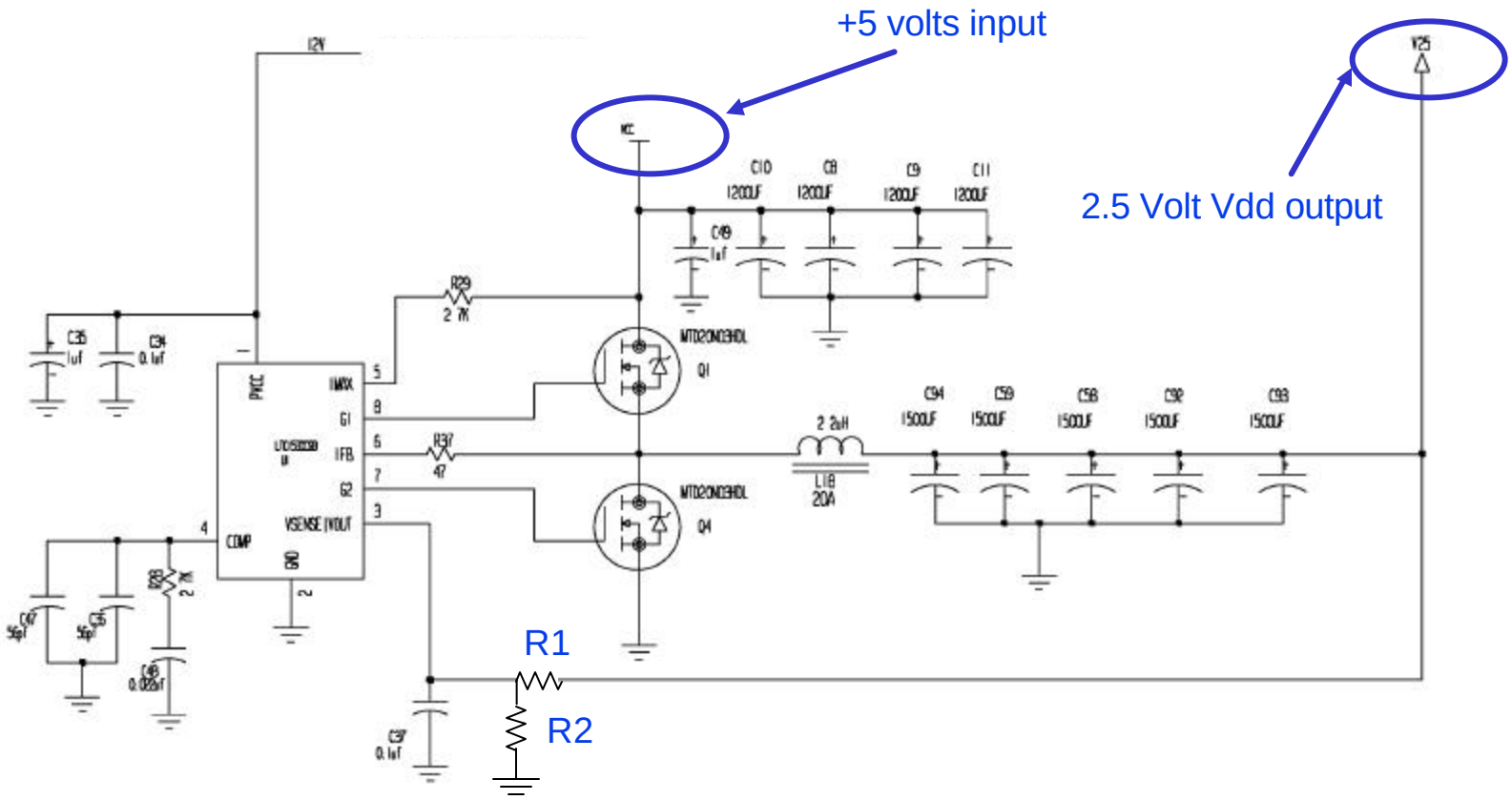
- Use the VREF In pin on the ML6554 to margin VREF and VTT
  - VTT and VREF out follow VREF In
- VREF specification is 0.49*VDD to 0.51*VDD
- VTT specification is VREF +/- 40mV
- Use simple resistor divider below connected to VREF In pin on ML6554



VDD Margining

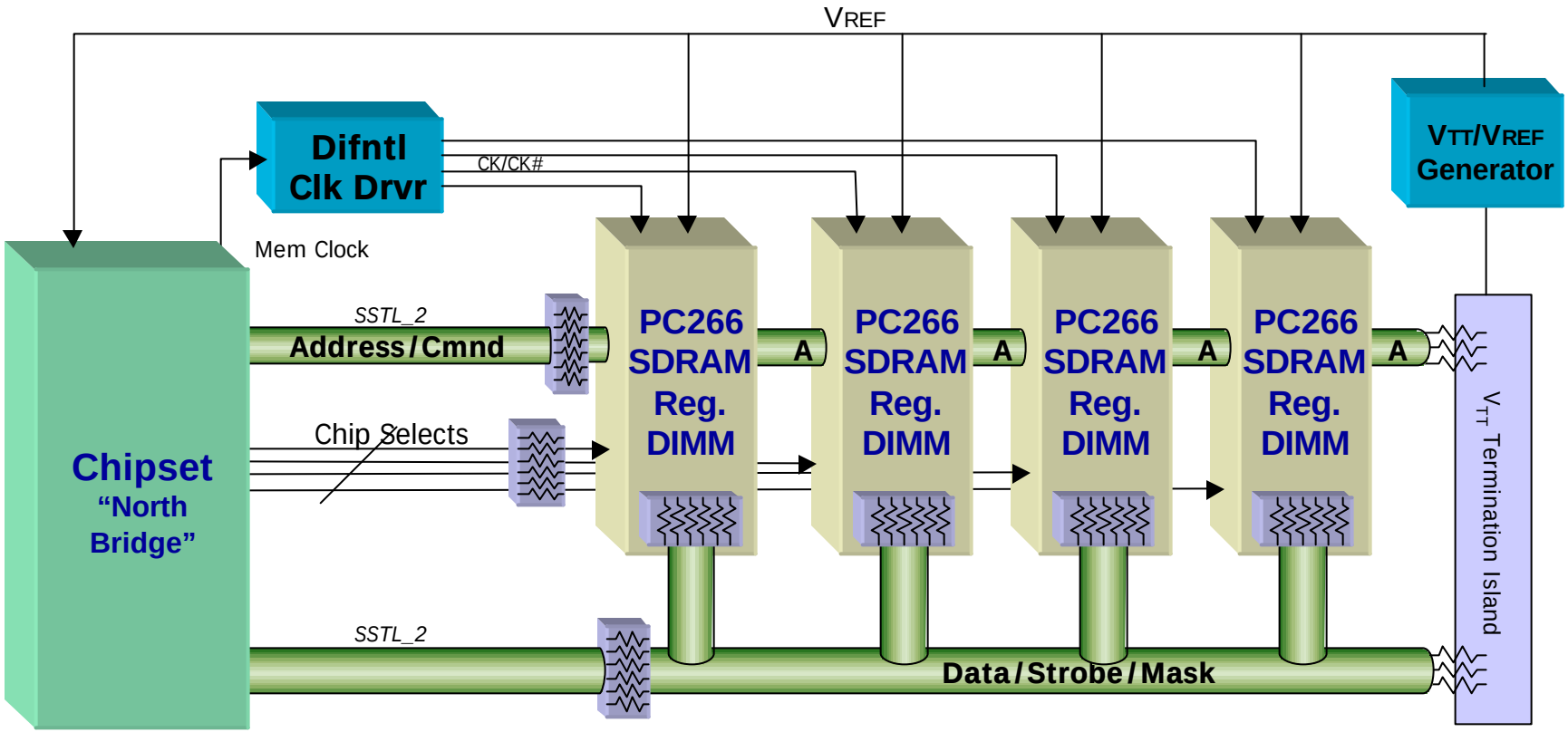
- VDD specification is 2.3 to 2.7 volts
- To margin VDD change LTC1530-2.5 to LTC1530-ADJ
- Adjust VDD with resistor divider R1/R2.

VDD Margining

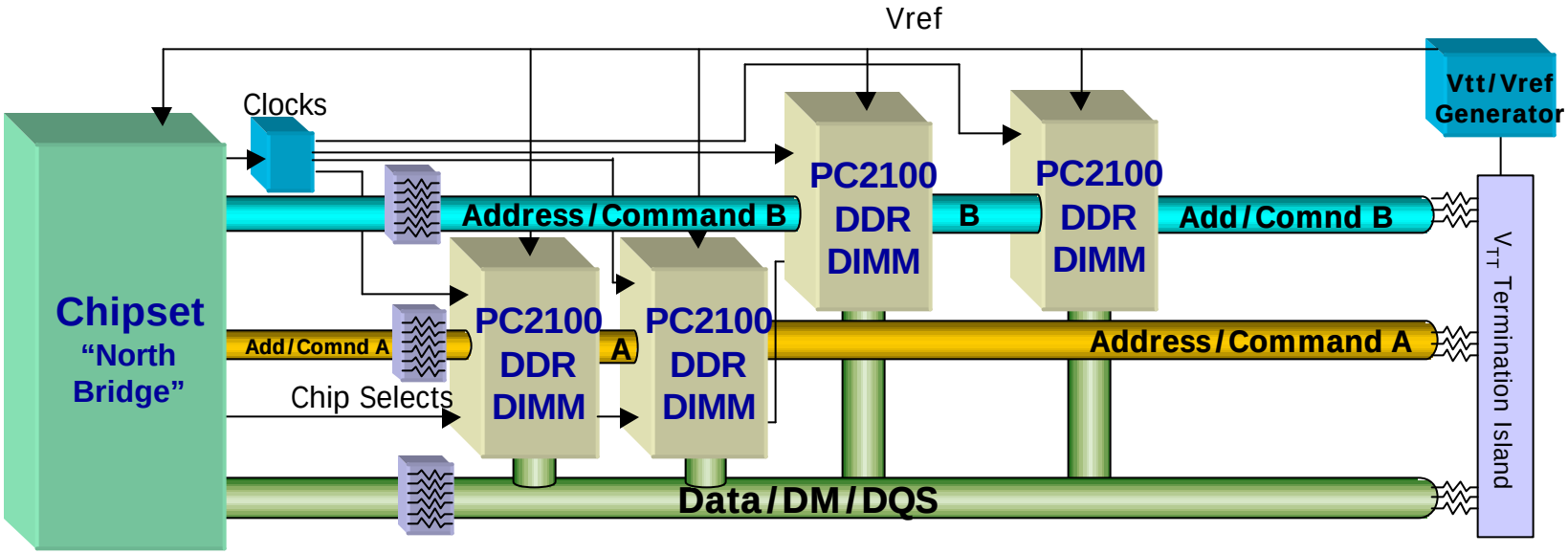


Board Implementation

Registered-Only Motherboard Topology



Unbuffered/Registered Motherboard Topology



PCB Considerations

- PC2100 DDR can be implemented in a low-cost PCB (standard PC100 motherboard technology)
- Standard pad, anti-pad and via sizes can be used
- No additional PCB test requirements relative to PC100

PCB Routing

- DDR channel can be implemented in a 2S 2P board
  - Controller BGA ballout determines whether a four-layer board can be used, not the memory channel
  - Two signal layers to get from controller to series resistor
  - The channel can be routed on one signal layer from the series termination resistor out, with the exception of point-to-point signals

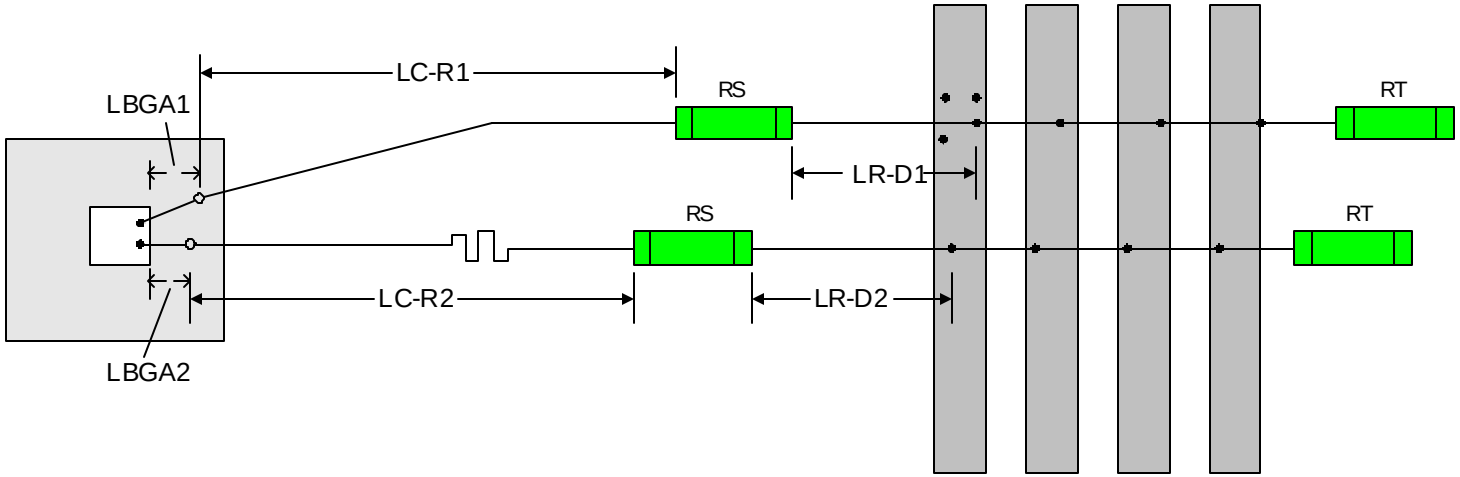
Reference Motherboard Routing

- Maintain signal reference through DDR channel
  - Route signals on layers adjacent to a common reference plane.
  - Route each data group (8 x DQ + DQS + DM) on same layer to match propagation delays and minimize skew.
  - Address and control matching is less critical.
  - Separate data and control nets to minimize crosstalk.
- Routing Rules
  - 5 mil trace/15 mil space on all in group SSTL nets
  - Connector rules: 5 mil trace, 2 mil space from antipad, 7 mils from trace

Micron Samurai DDR
Trace length matching rules

- Match trace lengths for each data group (8 x DQ + DQS + DM) to 0.1 inch from controller to first DIMM.
- Match trace lengths to +/- 500 mils across the entire channel.
- Match composite length from controller bond pad to first DIMM pad
  - $L_{BGA} + L_{controller\text{-}R} + L_{R\text{-}DIMM}$ = matched
- Length matching from last DIMM pad to parallel termination resistor is less critical

Length Matching from Controller to 1st DIMM Pin

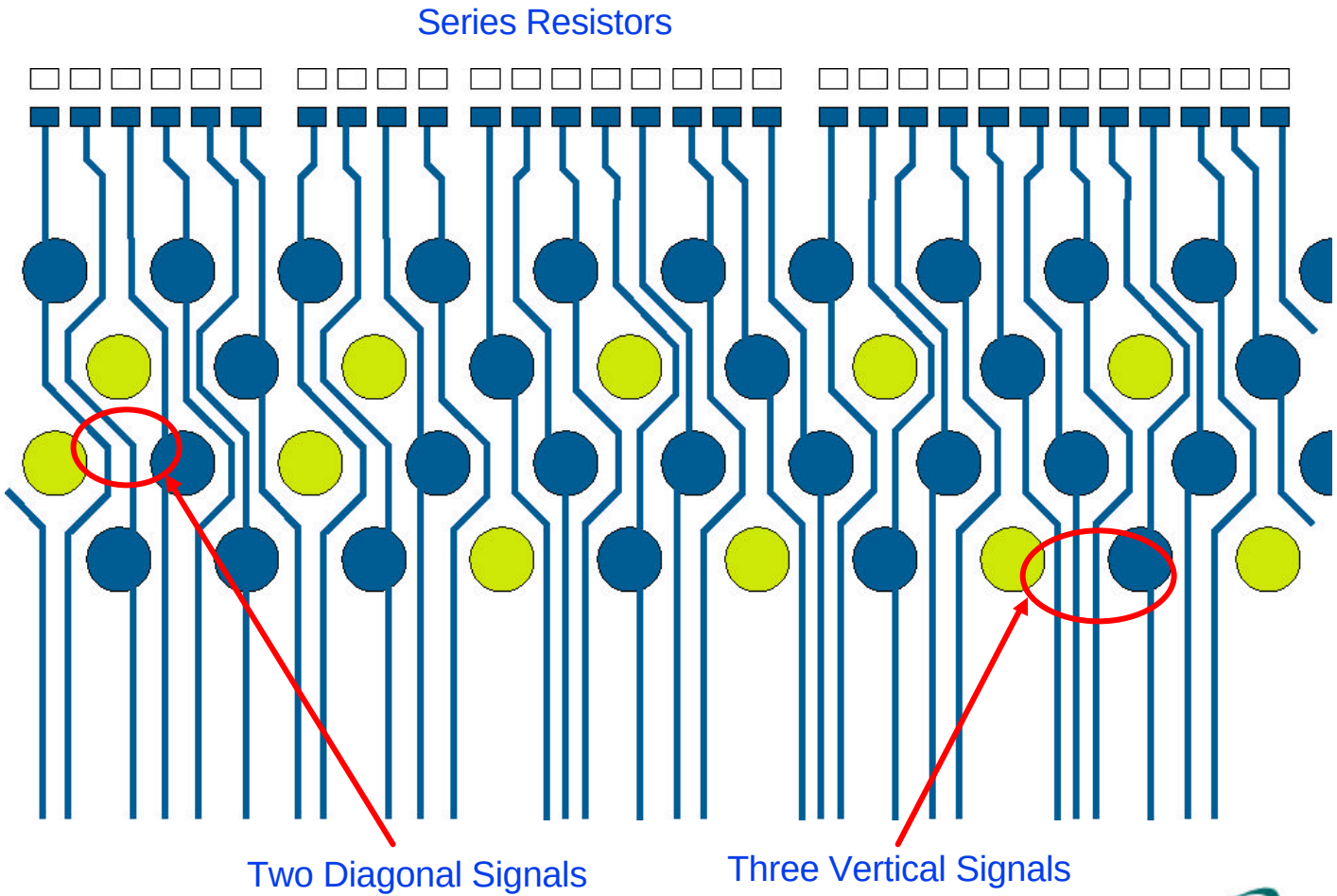


$$L_{BGA1} + L_{C\text{-}R1} + L_{R\text{-}D1} = L_{BGA2} + L_{C\text{-}R2} + L_{R\text{-}D2}$$

PCB Channel Routing Through the DIMMs

- A 5-mil width / 7-mil space board will yield:
  - Three vertical signal-routing channels
  - Two diagonal signal-routing channels
  - Second layer void except for point-to-point signals
  - Lowest skew due to propagation-velocity mismatch between different signal layers

Routing Through DIMMs

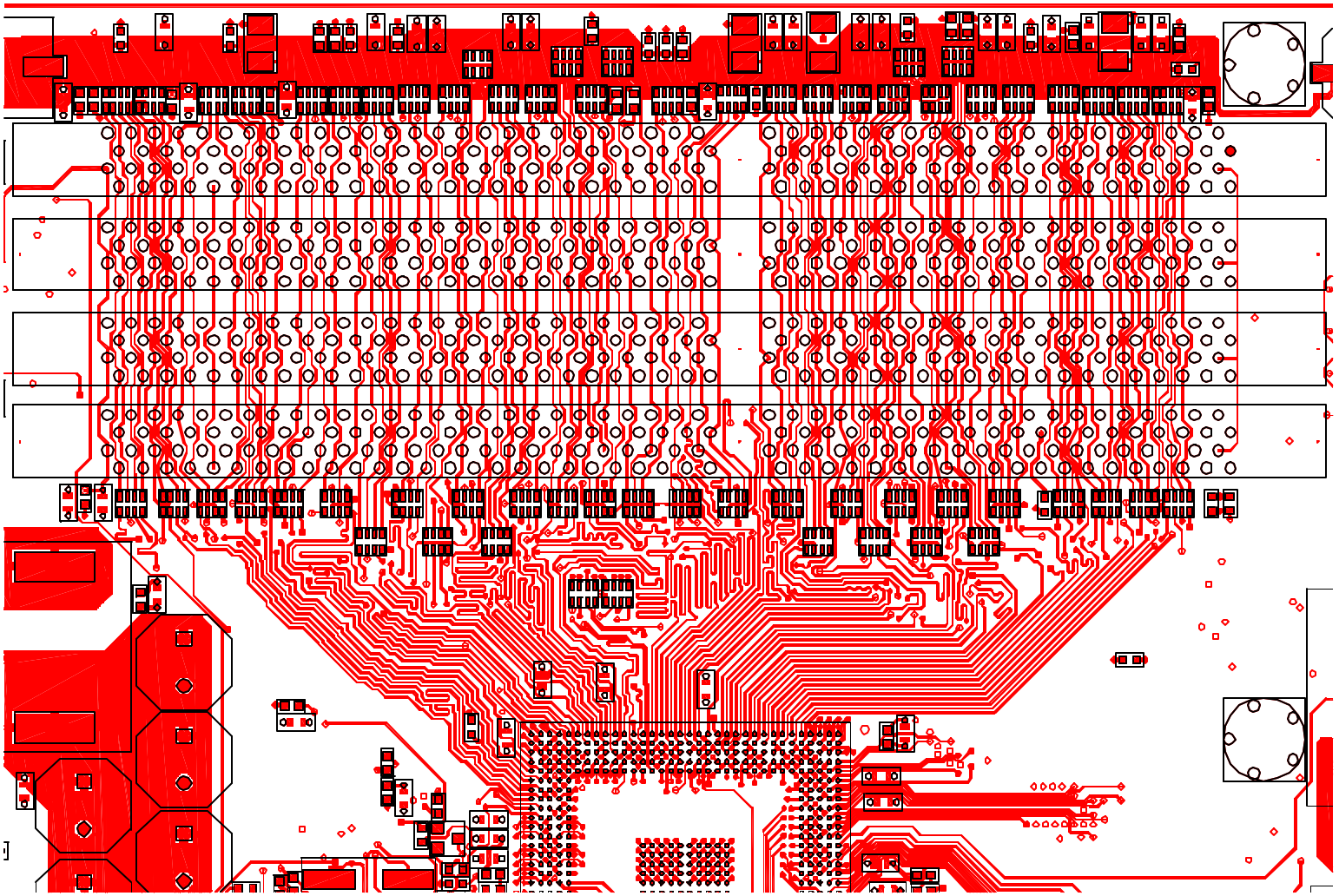


Termination Resistor Placement

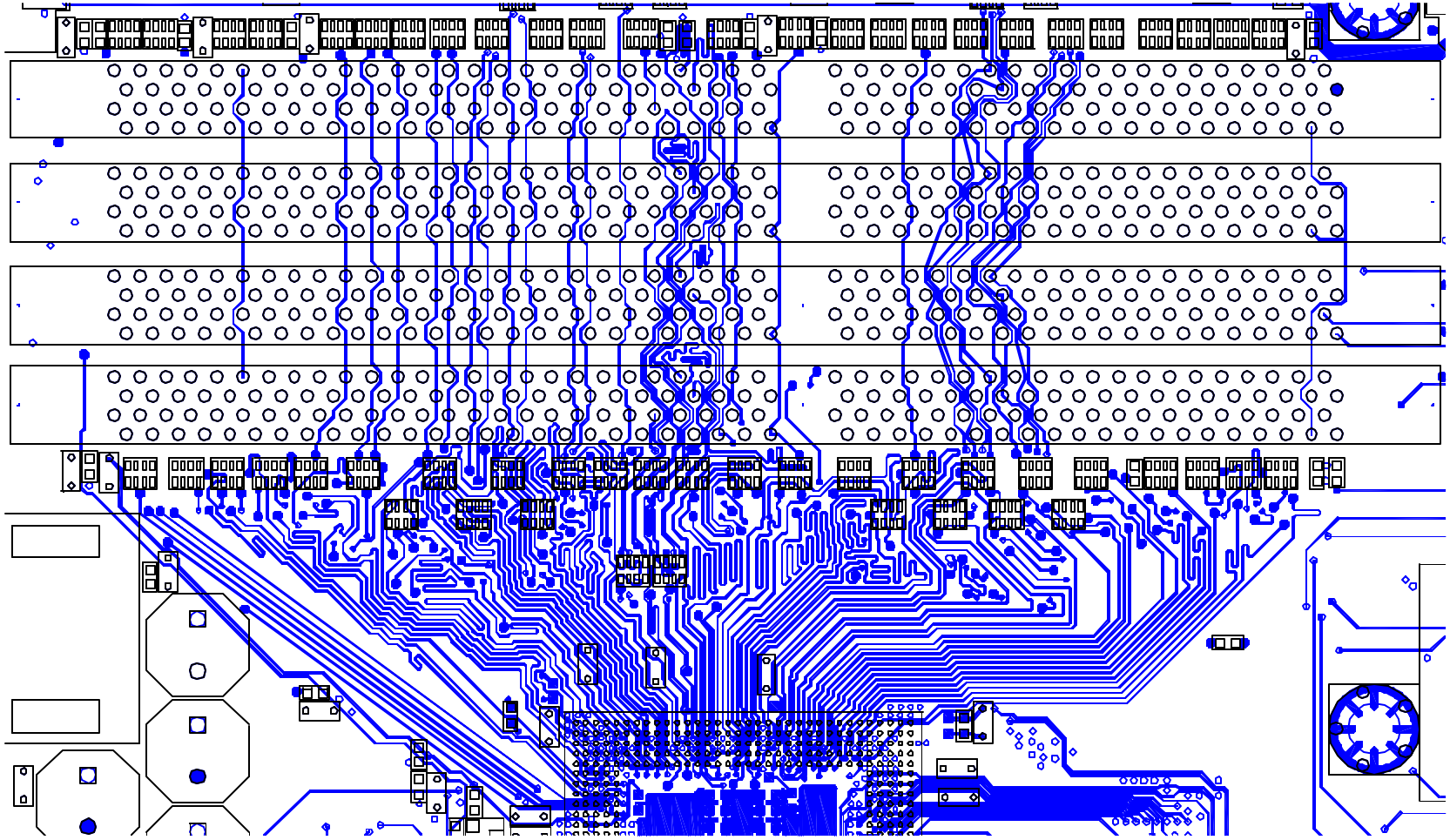
- Motherboard series resistors should be close to the first DIMM
  - Best performance for READ from last module
    - Limiting case
  - Simplifies routing and controller congestion

System Design Examples

DDR Memory Route 1st Layer

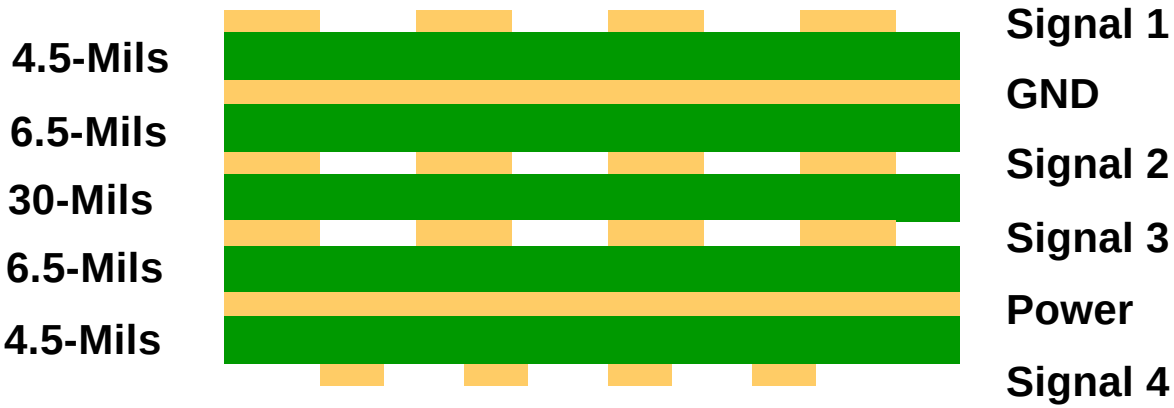


DDR Memory Route
2nd Layer



Reference Motherboard Stack-Up

- Reference board stack-up
  - 6 Layer Board



Questions and Answers