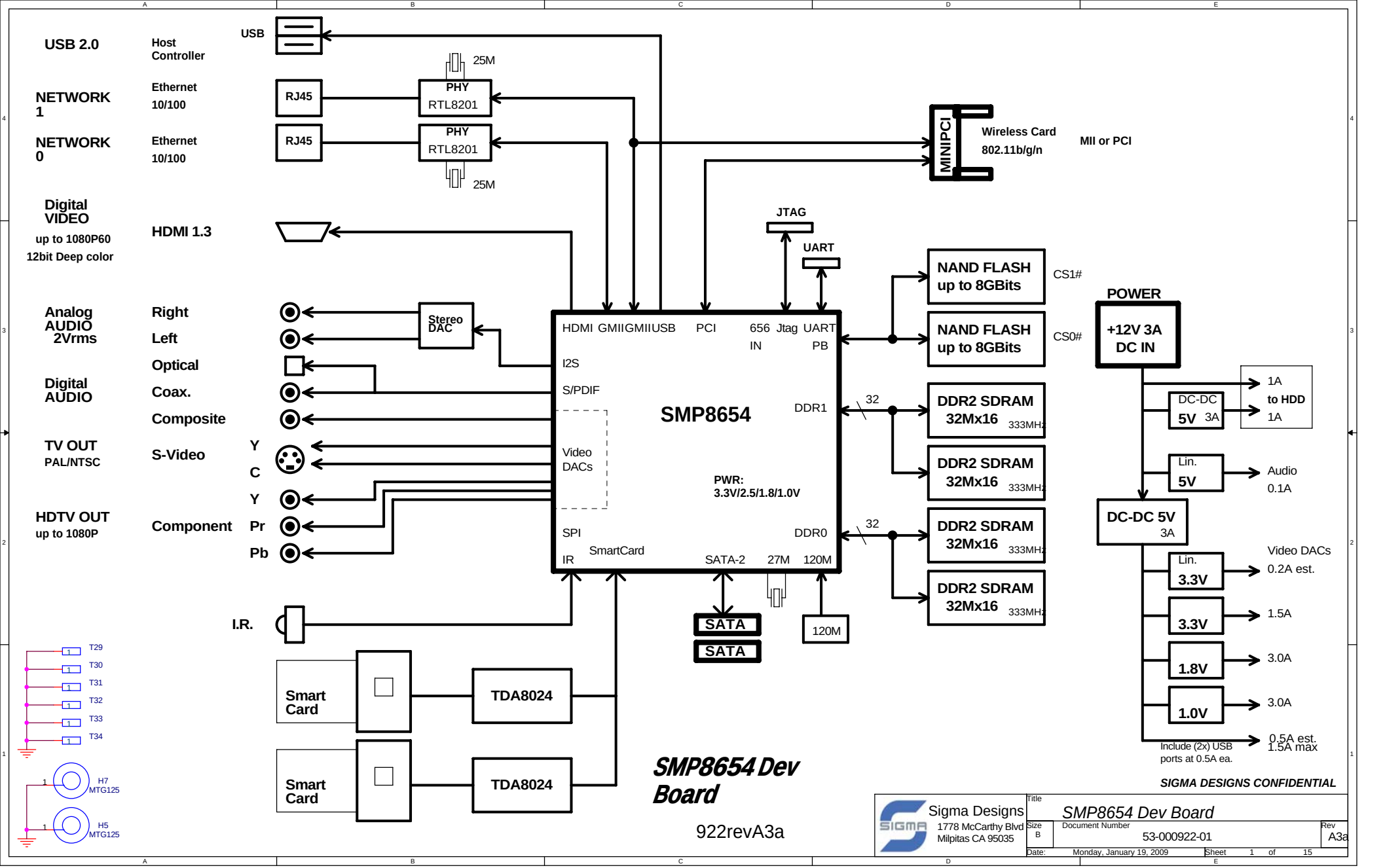
USB 2.0
Host Controller
USB
NETWORK 1
Ethernet 10/100
RJ45
PHY RTL8201
25M
NETWORK 0
Ethernet 10/100
RJ45
PHY RTL8201
25M
MINIPCI
Wireless Card 802.11b/g/n
MII or PCI
Digital VIDEO
up to 1080P60
12bit Deep color
HDMI 1.3
JTAG
UART
NAND FLASH up to 8GBits
CS1#
NAND FLASH up to 8GBits
CS0#
POWER
+12V 3A DC IN
Analog AUDIO 2Vrms
Right
Left
Stereo DAC
Optical
Digital AUDIO
Coax.
Composite
HDMI GMII GMII USB PCI 656 IN Jtag UART PB
I2S
S/PDIF
SMP8654
DDR1
32
DDR2 SDRAM 32Mx16 333MHz
DDR2 SDRAM 32Mx16 333MHz
Video DACs
PWR: 3.3V/2.5/1.8/1.0V
TV OUT
PAL/NTSC
S-Video
Y
C
HDTV OUT
up to 1080P
Component
Y
Pr
Pb
SPI
DDR0
32
DDR2 SDRAM 32Mx16 333MHz
DDR2 SDRAM 32Mx16 333MHz
IR
SmartCard
SATA-2
27M
120M
SATA
SATA
120M
I.R.
DC-DC 5V 3A
1A to HDD 1A
Lin. 5V
Audio 0.1A
DC-DC 5V 3A
Lin. 3.3V
Video DACs 0.2A est.
3.3V
1.5A
1.8V
3.0A
1.0V
3.0A
0.5A est. 1.5A max
Include (2x) USB ports at 0.5A ea.
Smart Card
TDA8024
Smart Card
TDA8024
T29
T30
T31
T32
T33
T34
H7 MTG125
H5 MTG125
SMP8654 Dev Board
922revA3a
SIGMA DESIGNS CONFIDENTIAL
Sigma Designs
1778 McCarthy Blvd
Milpitas CA 95035
Title
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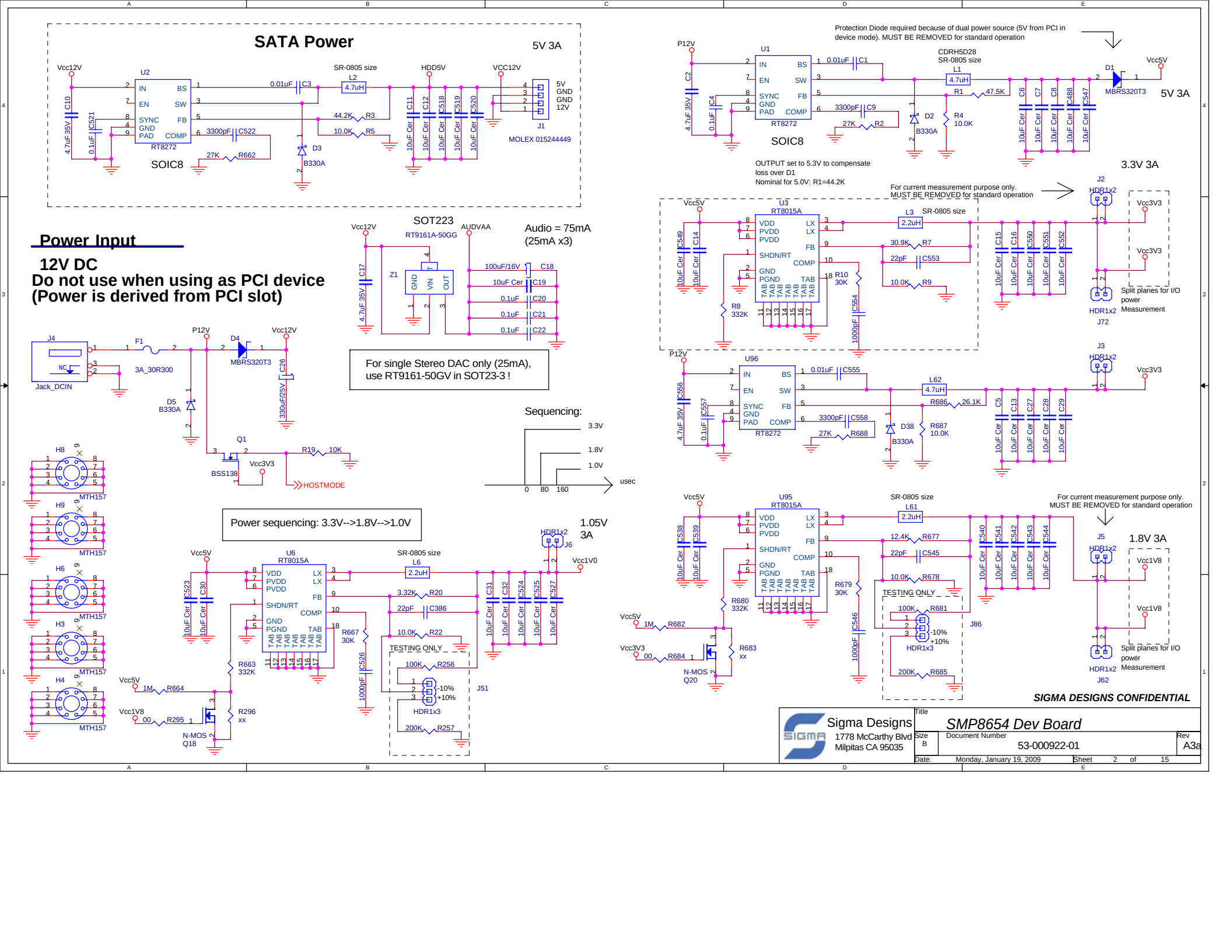
SATA Power
5V 3A
Vcc12V
U2
IN
BS
EN
SW
SYNC
FB
GND
PAD
COMP
RT8272
SOIC8
SR-0805 size
L2
4.7uH
0.01uF C3
44.2K R3
10.0K R5
3300pF C522
27K R662
D3
B330A
HDD5V
VCC12V
C10
C521
4.7uF 35V
0.1uF
C11
C12
C518
C519
C520
10uF Cer
J1
MOLEX 015244449
5V
GND
GND
12V
Power Input
12V DC
Do not use when using as PCI device
(Power is derived from PCI slot)
J4
NC
Jack_DCIN
F1
3A_30R300
P12V
D4
MBRS320T3
Vcc12V
C26
330uF/25V
D5
B330A
Q1
BSS138
R19
10K
Vcc3V3
HOSTMODE
H8
H9
H6
H3
H4
MTH157
SOT223
RT9161A-50GG
AUDVAA
Audio = 75mA
(25mA x3)
Z1
GND
VIN
OUT
C17
4.7uF 35V
100uF/16V
C18
10uF Cer
C19
0.1uF
C20
C21
C22
For single Stereo DAC only (25mA),
use RT9161-50GV in SOT23-3 !
Sequencing:
3.3V
1.8V
1.0V
0
80
160
usec
Power sequencing: 3.3V-->1.8V-->1.0V
U6
RT8015A
VDD
PVDD
LX
FB
SHDN/RT
COMP
GND
PGND
TAB
Vcc5V
C523
C30
10uF Cer
SR-0805 size
L6
2.2uH
3.32K R20
22pF C386
10.0K R22
TESTING ONLY
100K R256
-10%
+10%
HDR1x3
200K R257
J51
R667
30K
C526
1000pF
R663
332K
1M R664
00 R295
Vcc1V8
R296
xx
N-MOS
Q18
HDR1x2
J6
1.05V
3A
Vcc1V0
C31
C32
C524
C525
C527
Protection Diode required because of dual power source (5V from PCI in
device mode). MUST BE REMOVED for standard operation
U1
CDRH5D28
SR-0805 size
L1
4.7uH
R1
47.5K
0.01uF C1
3300pF C9
27K R2
D2
B330A
R4
10.0K
D1
MBRS320T3
5V 3A
C2
C4
C6
C7
C8
C488
C547
OUTPUT set to 5.3V to compensate
loss over D1
Nominal for 5.0V: R1=44.2K
3.3V 3A
For current measurement purpose only.
MUST BE REMOVED for standard operation
J2
HDR1x2
U3
RT8015A
L3
2.2uH
SR-0805 size
30.9K R7
22pF C553
10.0K R9
R10
30K
R8
332K
C554
10000pF
C549
C14
C15
C16
C550
C551
C552
Vcc3V3
Split planes for I/O
power
Measurement
J72
U96
RT8015A
0.01uF C555
L62
4.7uH
R686
26.1K
3300pF C558
27K R688
D38
B330A
R687
10.0K
C556
C557
C5
C13
C27
C28
C29
J3
1.8V 3A
U95
RT8015A
L61
2.2uH
SR-0805 size
12.4K R677
22pF C545
10.0K R678
TESTING ONLY
100K R681
-10%
+10%
HDR1x3
200K R685
J86
R679
30K
R680
332K
C546
10000pF
1M R682
00 R684
N-MOS
Q20
R683
xx
C538
C539
C540
C541
C542
C543
C544
J5
J62
For current measurement purpose only.
MUST BE REMOVED for standard operation
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Sigma Designs
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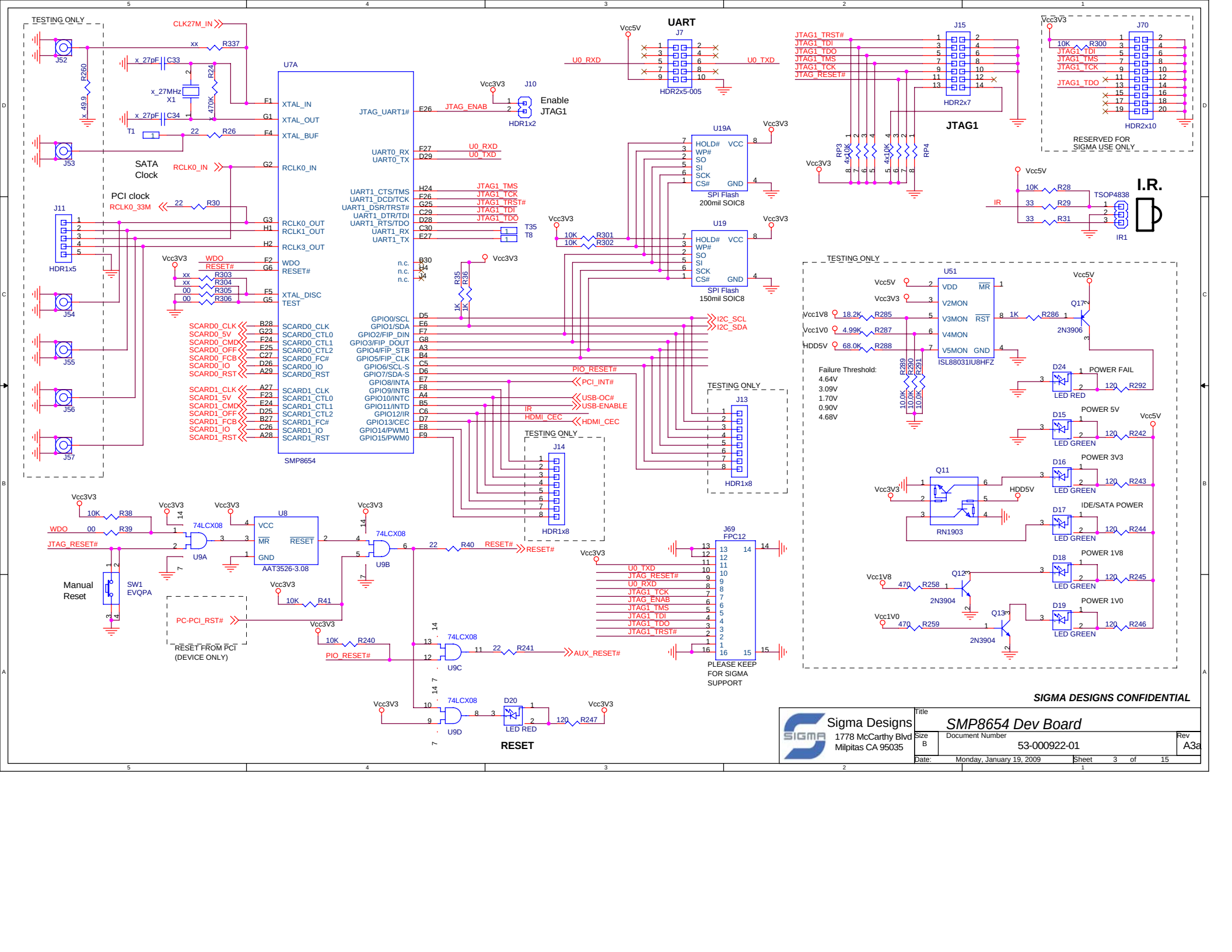
TESTING ONLY
CLK27M_IN
J52
R337
x_27pF C33
x_27MHz X1
x_27pF C34
R260
R24
T1
R26
J53
SATA Clock
RCLK0_IN
PCI clock
RCLK0_33M
R30
J11
HDR1x5
J54
J55
J56
J57
U7A
XTAL_IN
XTAL_OUT
XTAL_BUF
RCLK0_IN
RCLK0_OUT
RCLK1_OUT
RCLK3_OUT
WDO
RESET#
XTAL_DISC
TEST
SCARD0_CLK
SCARD0_5V
SCARD0_CMD
SCARD0_OFF
SCARD0_FCB
SCARD0_IO
SCARD0_RST
SCARD1_CLK
SCARD1_5V
SCARD1_CMD
SCARD1_OFF
SCARD1_FCB
SCARD1_IO
SCARD1_RST
JTAG_UART1#
UART0_RX
UART0_TX
UART1_CTS/TMS
UART1_DCD/TCK
UART1_DSR/TRST#
UART1_DTR/TDI
UART1_RTS/TDO
UART1_RX
UART1_TX
n.c.
GPIO0/SCL
GPIO1/SDA
GPIO2/FIP_DIN
GPIO3/FIP_DOUT
GPIO4/FIP_STB
GPIO5/FIP_CLK
GPIO6/SCL-S
GPIO7/SDA-S
GPIO8/INTA
GPIO9/INTB
GPIO10/INTC
GPIO11/INTD
GPIO12/IR
GPIO13/CEC
GPIO14/PWM1
GPIO15/PWM0
SMP8654
JTAG_ENAB
Vcc3V3
J10
HDR1x2
Enable JTAG1
U0_RXD
U0_TXD
JTAG1_TMS
JTAG1_TCK
JTAG1_TRST#
JTAG1_TDI
JTAG1_TDO
T35
T8
R35
R36
1K
PIO_RESET#
PCI_INT#
USB-OC#
USB-ENABLE
IR
HDMI_CEC
I2C_SCL
I2C_SDA
TESTING ONLY
J14
HDR1x8
J13
HDR1x8
UART
J7
HDR2x5-005
U19A
U19
HOLD#
WP#
SO
SI
SCK
CS#
VCC
GND
SPI Flash 200mil SOIC8
SPI Flash 150mil SOIC8
R301
R302
10K
J15
HDR2x7
JTAG1
JTAG1_TRST#
JTAG1_TDI
JTAG1_TDO
JTAG1_TMS
JTAG1_TCK
JTAG_RESET#
RP3
RP4
4x10K
J70
HDR2x10
R300
RESERVED FOR SIGMA USE ONLY
I.R.
TSOP4838
IR1
R28
R29
R31
33
Vcc5V
TESTING ONLY
U51
ISL88031IU8HFZ
VDD
MR
V2MON
V3MON
RST
V4MON
V5MON
GND
Vcc1V8
Vcc1V0
HDD5V
18.2K
4.99K
68.0K
R285
R287
R288
R286
Q17
2N3906
Failure Threshold:
4.64V
3.09V
1.70V
0.90V
4.68V
R289
R290
R291
10.0K
D24
POWER FAIL
LED RED
R292
D15
POWER 5V
LED GREEN
R242
D16
POWER 3V3
R243
Q11
RN1903
D17
IDE/SATA POWER
R244
D18
POWER 1V8
R245
Q12
2N3904
R258
470
D19
POWER 1V0
R246
Q13
R259
U8
AAT3526-3.08
74LCX08
U9A
U9B
U9C
U9D
Manual Reset
SW1
EVQPA
RESET FROM PCI (DEVICE ONLY)
PC-PCI_RST#
R38
R39
R40
R41
R240
R241
RESET#
AUX_RESET#
J69
FPC12
PLEASE KEEP FOR SIGMA SUPPORT
D20
LED RED
R247
RESET
SIGMA DESIGNS CONFIDENTIAL
Sigma Designs
1778 McCarthy Blvd
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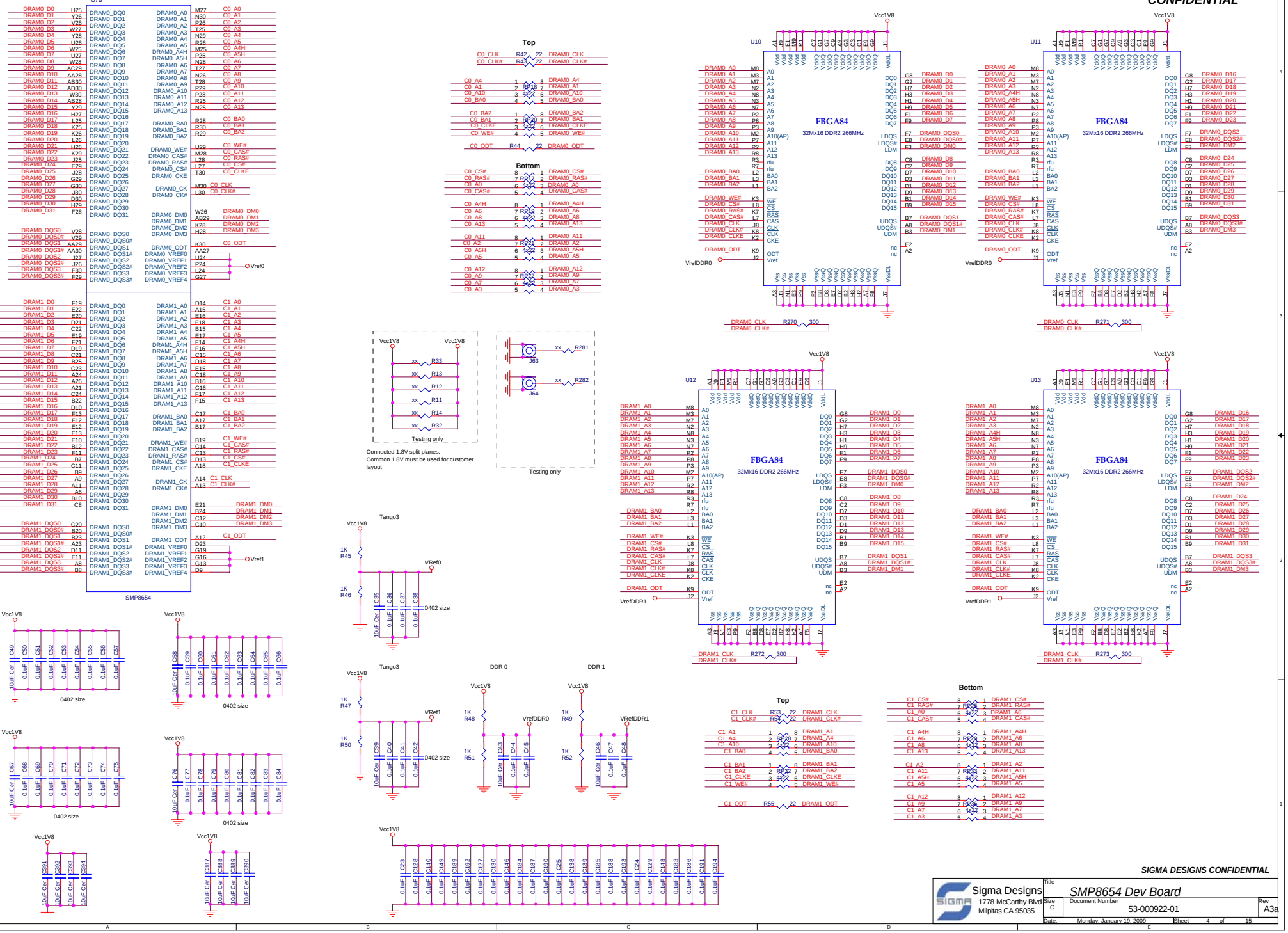

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Title	SMP8654 Dev Board		
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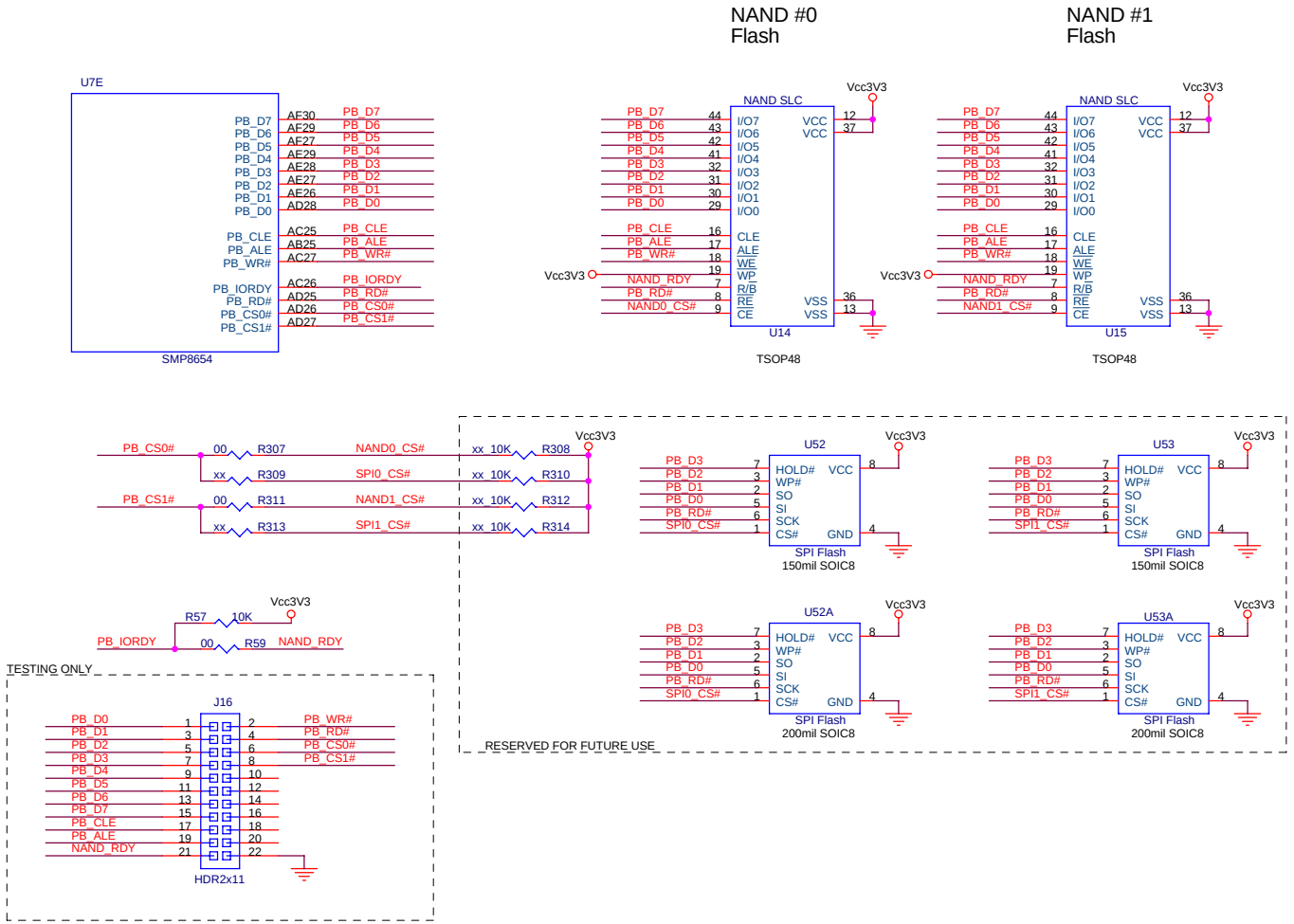
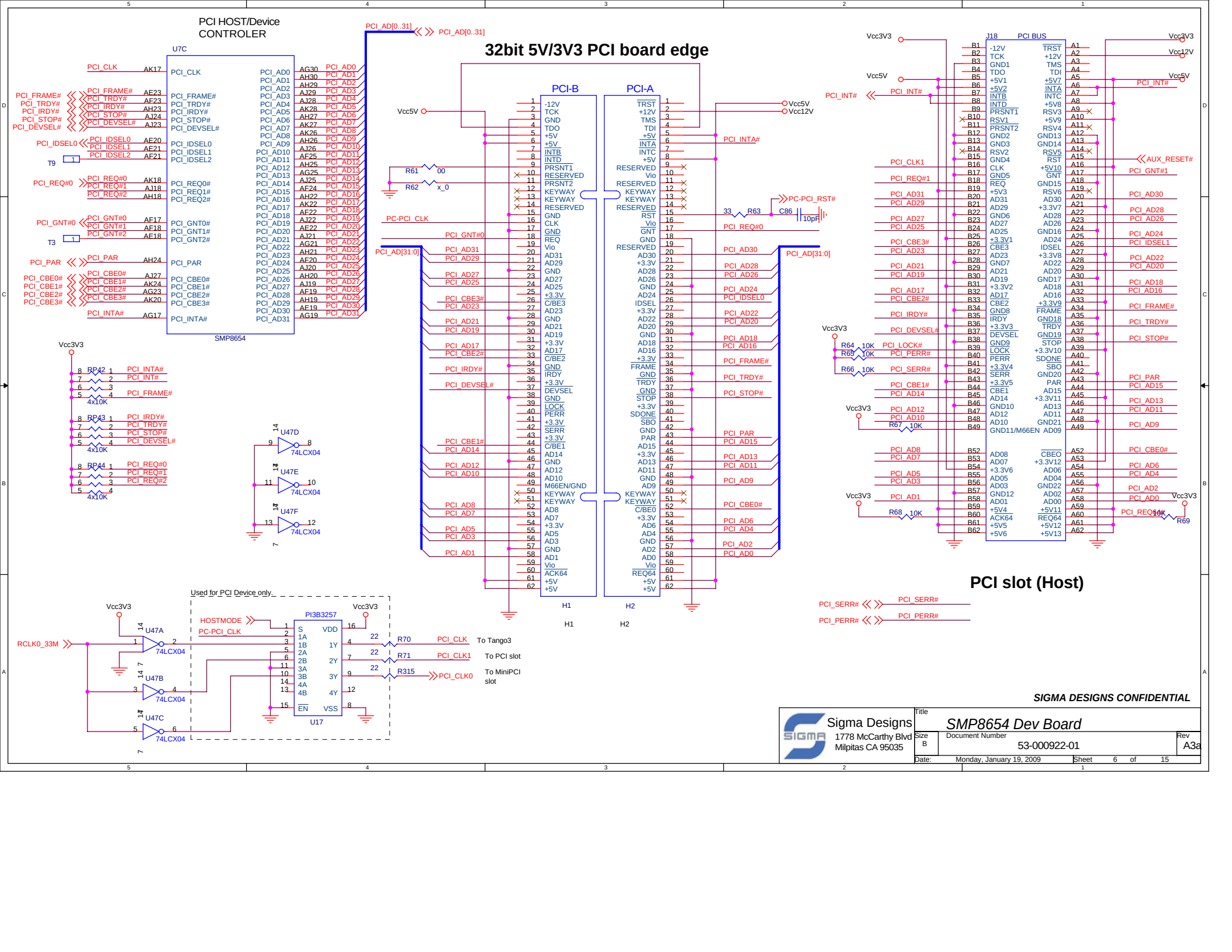


SIGMA DESIGNS CONFIDENTIAL

Sigma Designs 1778 McCarthy Blvd Milpitas CA 95035	Title: *SMP8654 Dev Board*		
	Size: B	Document Number: 53-000922-01	Rev: A3a
	Date: Monday, January 19, 2009	Sheet 5 of 15	


PCI HOST/Device CONTROLER
U7C
SMP8654
32bit 5V/3V3 PCI board edge
PCI-B
PCI-A
H1
H2
PCI slot (Host)
J18
PCI BUS
Used for PCI Device only.
PI3B3257
U17
To Tango3
To PCI slot
To MiniPCI slot
SIGMA DESIGNS CONFIDENTIAL
Sigma Designs
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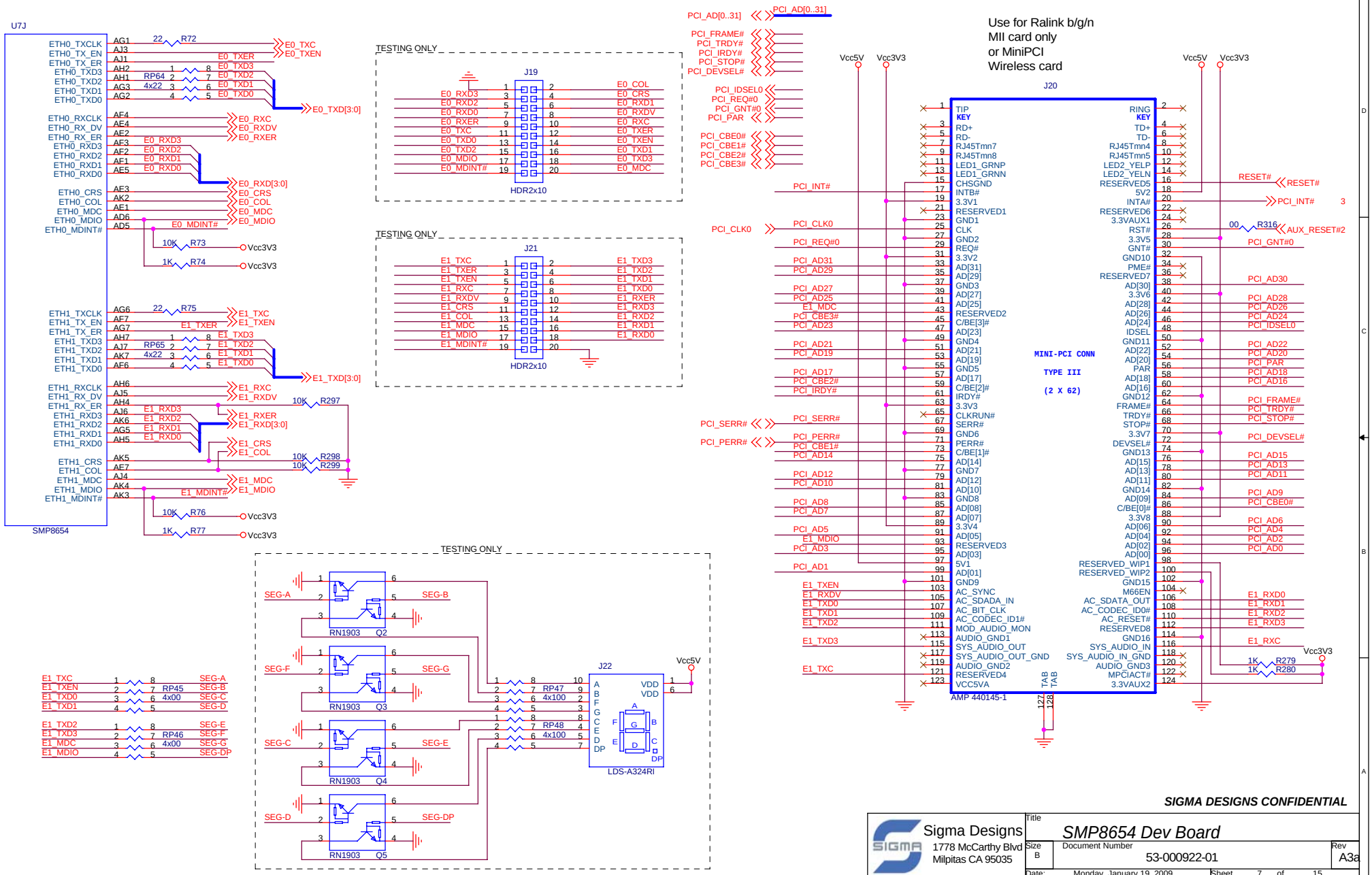
U7J
SMP8654
TESTING ONLY
J19
HDR2x10
TESTING ONLY
J21
HDR2x10
TESTING ONLY
RN1903 Q2
RN1903 Q3
RN1903 Q4
RN1903 Q5
J22
LDS-A324RI
Use for Ralink b/g/n
MII card only
or MiniPCI
Wireless card
J20
MINI-PCI CONN
TYPE III
(2 X 62)
AMP 440145-1
SIGMA DESIGNS CONFIDENTIAL
Sigma Designs
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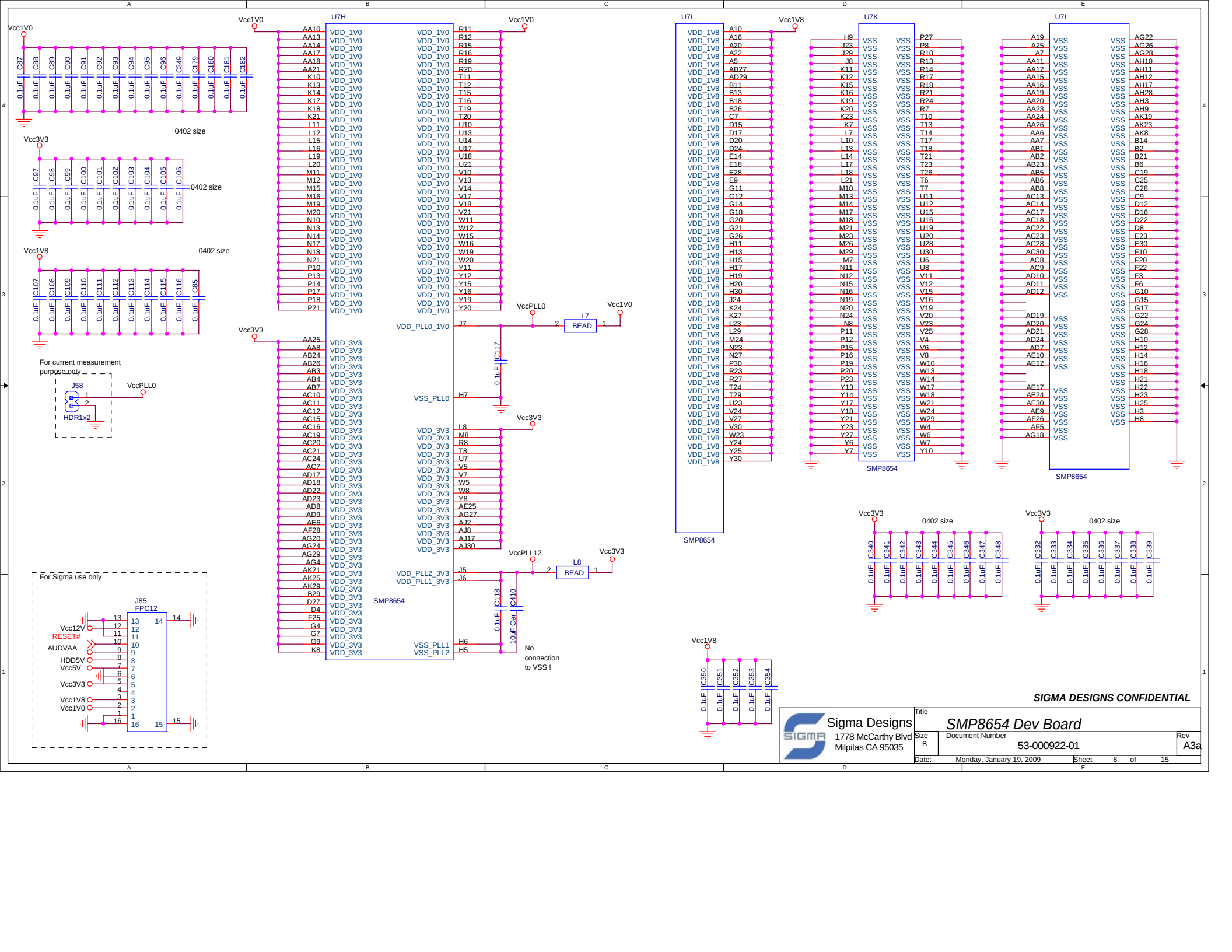
U7H
SMP8654
U7L
SMP8654
U7K
SMP8654
U7I
SMP8654
Vcc1V0
Vcc3V3
Vcc1V8
VccPLL0
VccPLL12
0402 size
For current measurement purpose only
J58
HDR1x2
For Sigma use only
J85
FPC12
RESET#
AUDVAA
HDD5V
Vcc5V
Vcc12V
L7
L8
BEAD
No connection to VSS !
SIGMA DESIGNS CONFIDENTIAL
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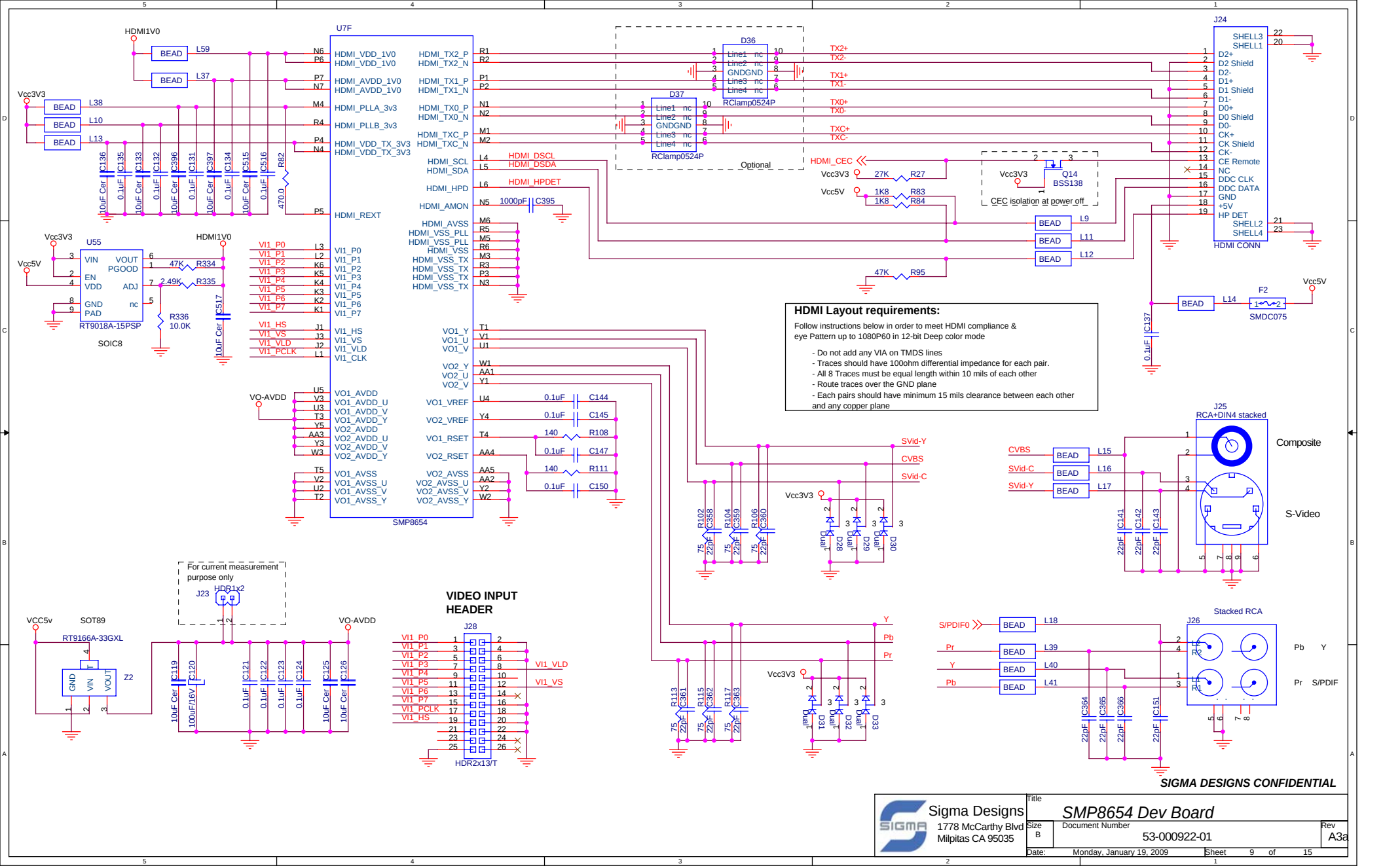
HDMI1V0
U7F
SMP8654
HDMI_VDD_1V0
HDMI_AVDD_1V0
HDMI_PLLA_3v3
HDMI_PLLB_3v3
HDMI_VDD_TX_3V3
HDMI_REXT
HDMI_TX2_P
HDMI_TX2_N
HDMI_TX1_P
HDMI_TX1_N
HDMI_TX0_P
HDMI_TX0_N
HDMI_TXC_P
HDMI_TXC_N
HDMI_SCL
HDMI_SDA
HDMI_HPD
HDMI_AMON
HDMI_AVSS
HDMI_VSS_PLL
HDMI_VSS
HDMI_VSS_TX
VI1_P0
VI1_P1
VI1_P2
VI1_P3
VI1_P4
VI1_P5
VI1_P6
VI1_P7
VI1_HS
VI1_VS
VI1_VLD
VI1_CLK
VO1_Y
VO1_U
VO1_V
VO2_Y
VO2_U
VO2_V
VO1_AVDD
VO1_AVDD_U
VO1_AVDD_V
VO1_AVDD_Y
VO2_AVDD
VO2_AVDD_U
VO2_AVDD_V
VO2_AVDD_Y
VO1_VREF
VO2_VREF
VO1_RSET
VO2_RSET
VO1_AVSS
VO1_AVSS_U
VO1_AVSS_V
VO1_AVSS_Y
VO2_AVSS
VO2_AVSS_U
VO2_AVSS_V
VO2_AVSS_Y
HDMI_DSCL
HDMI_DSDA
HDMI_HPDET
1000pF C395
D36
D37
RClamp0524P
Optional
TX2+
TX2-
TX1+
TX1-
TX0+
TX0-
TXC+
TXC-
HDMI_CEC
Vcc3V3
Vcc5V
27K R27
1K8 R83
1K8 R84
47K R95
Q14 BSS138
CEC isolation at power off
J24
HDMI CONN
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL1
SHELL2
SHELL3
SHELL4
U55
RT9018A-15PSP
SOIC8
VIN
VOUT
PGOOD
EN
VDD
ADJ
GND
nc
PAD
47K R334
2.49K R335
R336 10.0K
F2
SMDC075
HDMI Layout requirements:
Follow instructions below in order to meet HDMI compliance & eye Pattern up to 1080P60 in 12-bit Deep color mode
- Do not add any VIA on TMDS lines
- Traces should have 100ohm differential impedance for each pair.
- All 8 Traces must be equal length within 10 mils of each other
- Route traces over the GND plane
- Each pairs should have minimum 15 mils clearance between each other and any copper plane
SVid-Y
CVBS
SVid-C
J25
RCA+DIN4 stacked
Composite
S-Video
For current measurement purpose only
J23
HDR1x2
VCC5v
SOT89
RT9166A-33GXL
Z2
VO-AVDD
VIDEO INPUT HEADER
J28
HDR2x13/T
S/PDIF0
Pr
Y
Pb
J26
Stacked RCA
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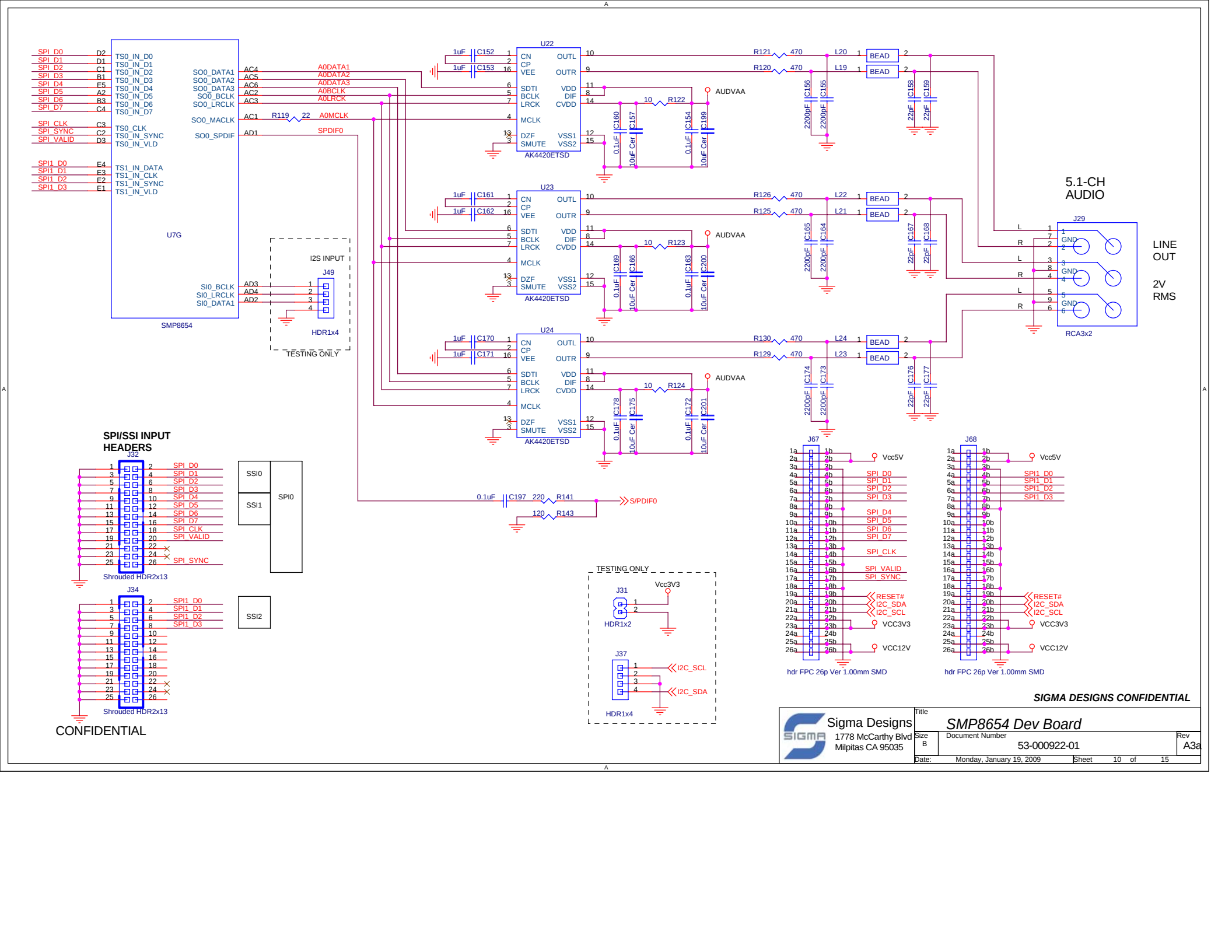
SMP8654
U7G
TS0_IN_D0
TS0_IN_D1
TS0_IN_D2
TS0_IN_D3
TS0_IN_D4
TS0_IN_D5
TS0_IN_D6
TS0_IN_D7
TS0_CLK
TS0_IN_SYNC
TS0_IN_VLD
TS1_IN_DATA
TS1_IN_CLK
TS1_IN_SYNC
TS1_IN_VLD
SO0_DATA1
SO0_DATA2
SO0_DATA3
SO0_BCLK
SO0_LRCLK
SO0_MACLK
SO0_SPDIF
SI0_BCLK
SI0_LRCLK
SI0_DATA1
A0DATA1
A0DATA2
A0DATA3
A0BCLK
A0LRCK
A0MCLK
SPDIF0
I2S INPUT
J49
HDR1x4
TESTING ONLY
U22
U23
U24
AK4420ETSD
AUDVAA
5.1-CH AUDIO
LINE OUT
2V RMS
J29
RCA3x2
SPI/SSI INPUT HEADERS
J32
Shrouded HDR2x13
J34
SSI0
SSI1
SSI2
SPI0
CONFIDENTIAL
J67
J68
hdr FPC 26p Ver 1.00mm SMD
Vcc5V
VCC3V3
VCC12V
J31
HDR1x2
J37
Vcc3V3
S/PDIF0
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Sigma Designs
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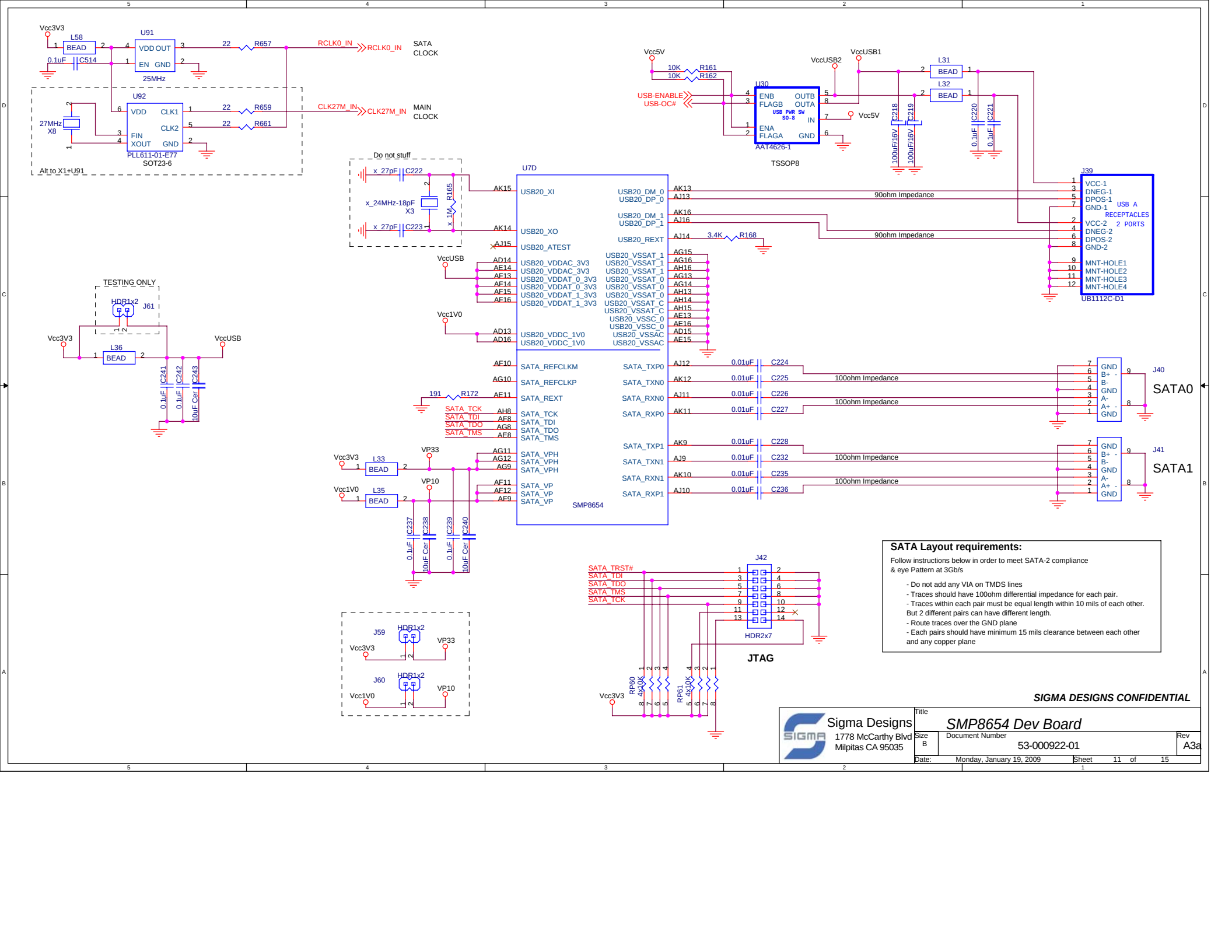
Vcc3V3
L58
BEAD
0.1uF
C514
U91
VDD OUT
EN GND
25MHz
22
R657
RCLK0_IN
SATA CLOCK
U92
VDD CLK1
CLK2
FIN
XOUT GND
27MHz
X8
PLL611-01-E77
SOT23-6
22
R659
22
R661
CLK27M_IN
MAIN CLOCK
Alt to X1+U91
TESTING ONLY
HDR1x2
J61
L36
VccUSB
C241
C242
C243
0.1uF
10uF Cer
Do not stuff
x 27pF
C222
x_24MHz-18pF
X3
R165
x 1M
C223
U7D
SMP8654
USB20_XI
USB20_XO
USB20_ATEST
USB20_VDDAC_3V3
USB20_VDDAT_0_3V3
USB20_VDDAT_1_3V3
USB20_VDDC_1V0
SATA_REFCLKM
SATA_REFCLKP
SATA_REXT
SATA_TCK
SATA_TDI
SATA_TDO
SATA_TMS
SATA_VPH
SATA_VP
USB20_DM_0
USB20_DP_0
USB20_DM_1
USB20_DP_1
USB20_REXT
USB20_VSSAT_1
USB20_VSSAT_0
USB20_VSSAT_C
USB20_VSSC_0
USB20_VSSAC
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
SATA_TXP1
SATA_TXN1
SATA_RXN1
SATA_RXP1
191
R172
3.4K
R168
90ohm Impedance
100ohm Impedance
0.01uF
C224
C225
C226
C227
C228
C232
C235
C236
J40
SATA0
J41
SATA1
GND
B+
B-
A-
A+
L33
L35
VP33
VP10
C237
C238
C239
C240
J59
J60
Vcc1V0
Vcc5V
VccUSB1
VccUSB2
10K
R161
10K
R162
USB-ENABLE
USB-OC#
U30
ENB OUTB
FLAGB OUTA
USB PWR SW
SO-8
IN
ENA
FLAGA GND
AAT4626-1
TSSOP8
L31
L32
C218
C219
C220
C221
100uF/16V
0.1uF
J39
VCC-1
DNEG-1
DPOS-1
GND-1
USB A
RECEPTACLES
VCC-2
2 PORTS
DNEG-2
DPOS-2
GND-2
MNT-HOLE1
MNT-HOLE2
MNT-HOLE3
MNT-HOLE4
UB1112C-D1
J42
HDR2x7
JTAG
SATA_TRST#
SATA_TDI
SATA_TDO
SATA_TMS
SATA_TCK
RP60
RP61
4.10K
SATA Layout requirements:
Follow instructions below in order to meet SATA-2 compliance & eye Pattern at 3Gb/s
- Do not add any VIA on TMDS lines
- Traces should have 100ohm differential impedance for each pair.
- Traces within each pair must be equal length within 10 mils of each other. But 2 different pairs can have different length.
- Route traces over the GND plane
- Each pairs should have minimum 15 mils clearance between each other and any copper plane
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53-000922-01
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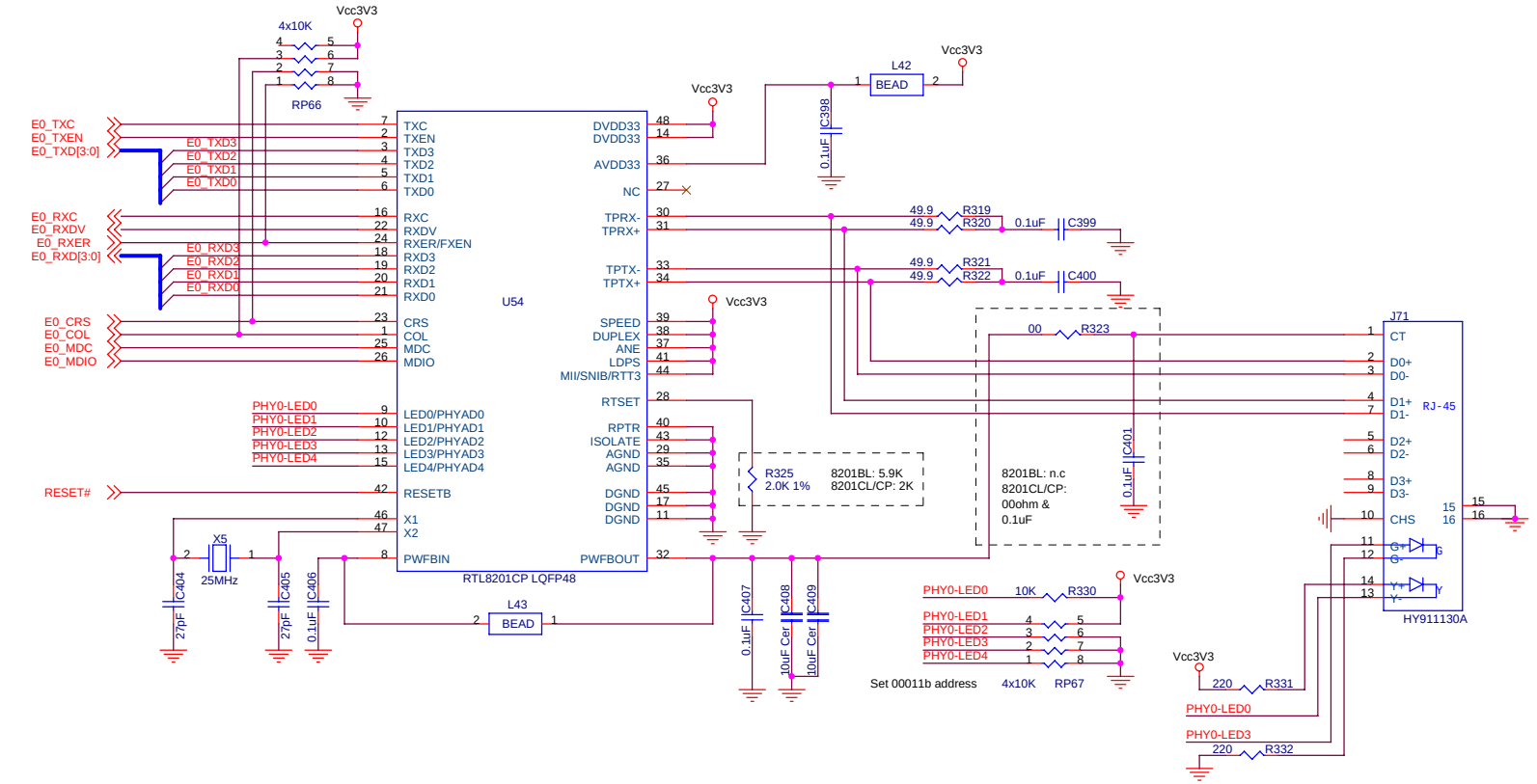

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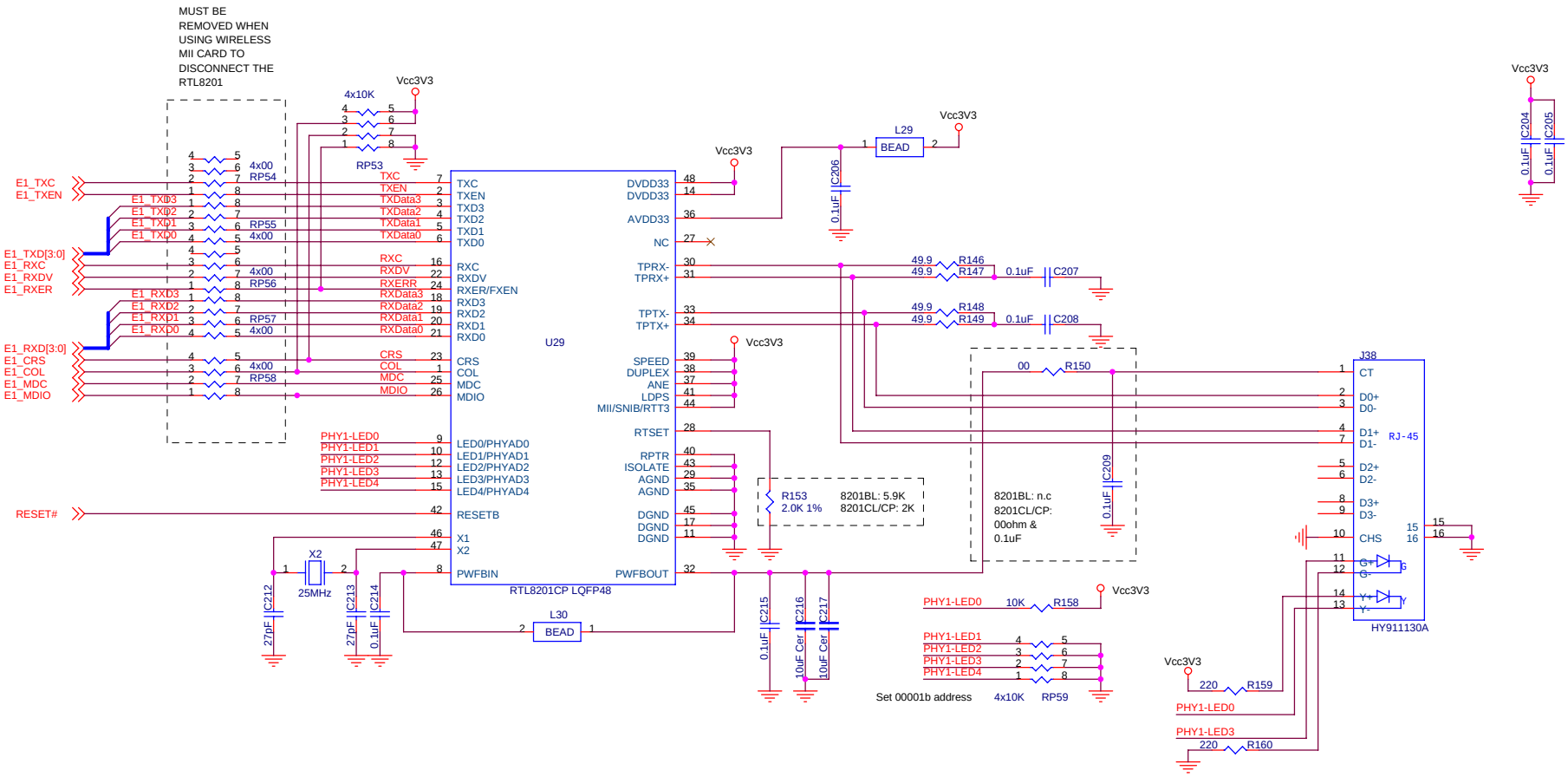

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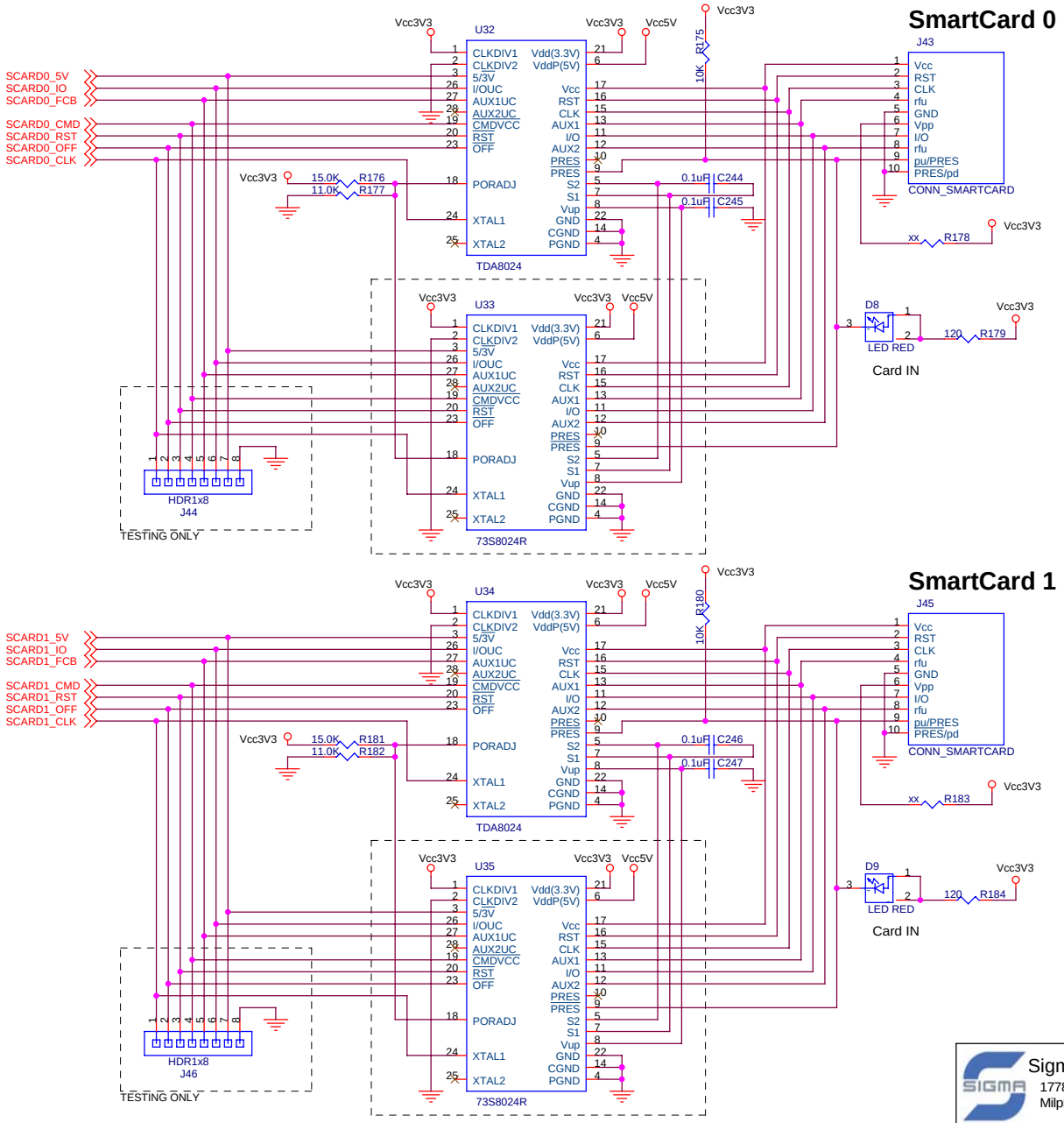

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Boards for SMP8654 Engineering Samples

Changes from Rev E1 --> Rev E2:

- Correct HDMI 1.3 video input pins mapping
- Fix IDE & PCI reset (AUX_RESET# duplicate)
- Correct connection to Marvell PHY

Changes from Rev E2 --> Rev E3:

- Remove DDR series resistors
- Improve PLL decoupling (Cap location)
- Change Gigabit PHY to RTL8211BG
- Change Audio DAC to AK4420
- Remove 2.5V power (unused)
- Add SMA conn on clocks
- Isolate DDR I/O for power measure
- Remove video output buffers

Changes from Rev E3 --> Rev E4:

- Fix SMP8654 pinout on SPI-0 input
- Minor Updates on RTL8211BG page (EMI)
- Re-add series resistors on DDR address lines only
- Add termination on DDR clocks
- Change core & DDR power supply to 2A
- Add additional 10uF caps to DDR
- Add connection to USB power pin AE13
- Add U49 Alternate SATA clock
- Add Ralink MII Wireless card support

Boards for SMP8654 Production IC (Integrated HDMI)

Changes from Rev E4 --> Rev A1:

- Update SMP8654 pinout related to HDMI section
- Remove SII9134 and Sil9002 ICs, replace with internal HDMI circuit

Changes from Rev A1 --> Rev A1a:

- SMP8654 ballout UPDATE:
  - USB section
  - Del GND ball AD15, AD16, AE14, AE15
  - Del 3V3 ball AD13, AD14
- Added GND test points and SMA Conn.

Changes from Rev A1a --> Rev A1b:

- Swapp U & V connection on Video DAC outputs
- Add optional power sequencing
- Change AAT1153 back to AAT1112, update current data
- Short power jumpers
- Add RP64,65 accidentally deleted on A1a

Changes from Rev A1b --> Rev A1c:

- Add Connector for ATSC/DVB-T tuner board
- Fix MiniPCI MII pinout

Changes from Rev A1c --> Rev A2:

- Correct symbol n/c balls J4,H4,B30
- Add VSS ball L7
- Replace Gigabit PHY with 10/100 PHY
- Fix JTAG new pinout (TDI)
- Add SPI Flash (GPIO2..5 and Flash Bus)
- Add support for Bist test (Sigma use only)
- Added decoupling on 1.8V
- Added ESD protection on video outputs (dig & analog)

Changes from Rev A2 --> Rev A2a:

- Update PLL 1&2 power connection

Changes from Rev A2a --> Rev A2b:

- Update HDMI power & layout
- Change HDMI RSET connection
- Add 200mils SOIC footprint for SPI flash
- Add 25MHz to RCLK0 for SATA Clock

Changes from Rev A2b --> Rev A2c:

- Replace RJ45s with external Transf. with integrated unit

Changes from Rev A2c --> Rev A3:

- Upgrade core power to 3A
- Upgrade DDR power to 3A
- Upgrade HDMI1V0 regulator
- Update 5V and HDD5V regulator
- Update AUDVAA regulator
- Update 3.3V Video DACs regulators
- Remove 120MHz clock UNUSED
- Correct 27MHz input to XTAL_IN

Changes from Rev A3 --> Rev A3a:

- Change 3.3V source from 12V (alternate)

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