DDR II

Outline

- DDRI vs. DDRII
- Functional Block Diagram
- Simplified State Diagram
- Action of Functional signal Description

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Different points

DDR v.s. DDR2

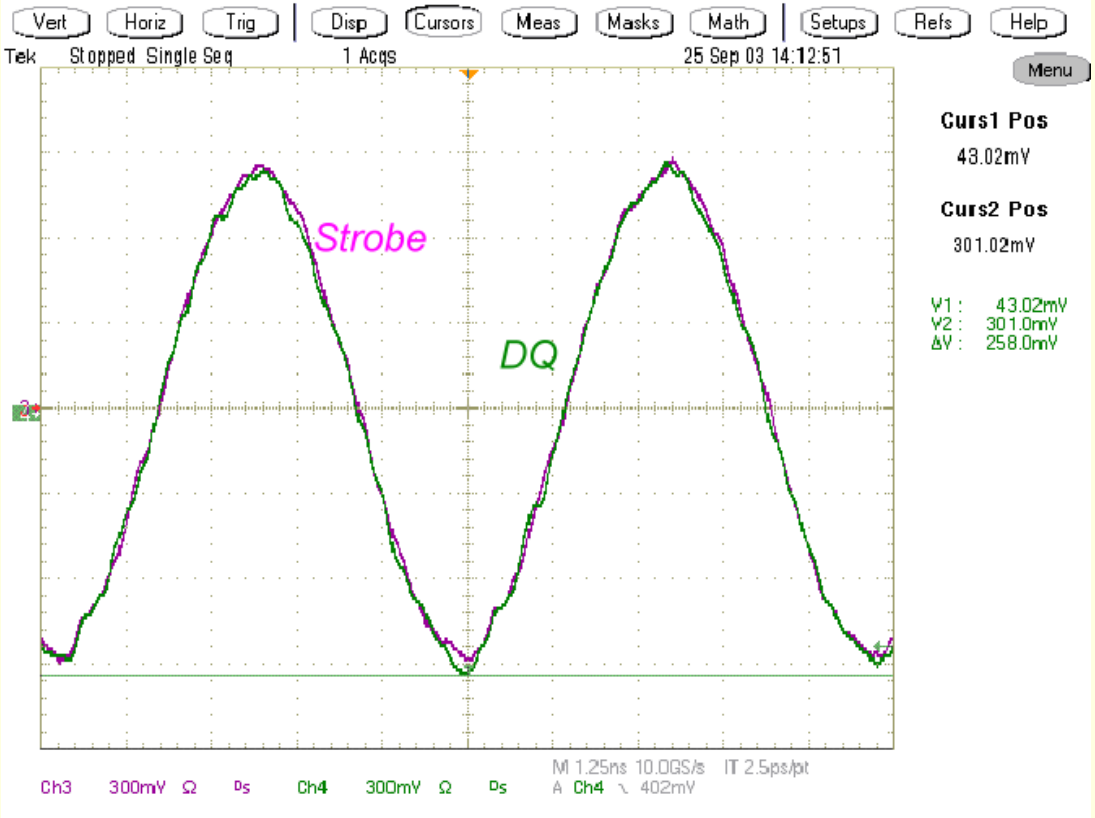
Memory Type	DDR	DDR2
Core Voltage(VDD)	2.5V	1.8V
I/O Voltage (VDDQ)	SSTL_2(2.5V)	SSTL_1.8(1.8)
Data Rate	200/266/333/400Mbps	400/533/667/800Mbps
Bus Frequency	100/133/166/200MHz	200/266/333/400MHz
Core Frequency	100/133/166/200MHz	100/133/166/200MHz
Pre-fetch	2-bit	4-bit
Burst Length	2/4/8	4/8
Data Strobe	Single DQS	Differential DQS, /DQS
Write Latency	1 clock	(Read Latency-1) clock
CAS Latency	1.5, 2, 2.5	3, 4, 5
Package	x4/x8/x16: 66-pin TSOP(II) x4/x8/x16: 60-ball FBGA	x4/x8: 60 ball FBGA x16: 84 ball FBGA
New Features		OCD ODT Posted CAS

Power Improvement

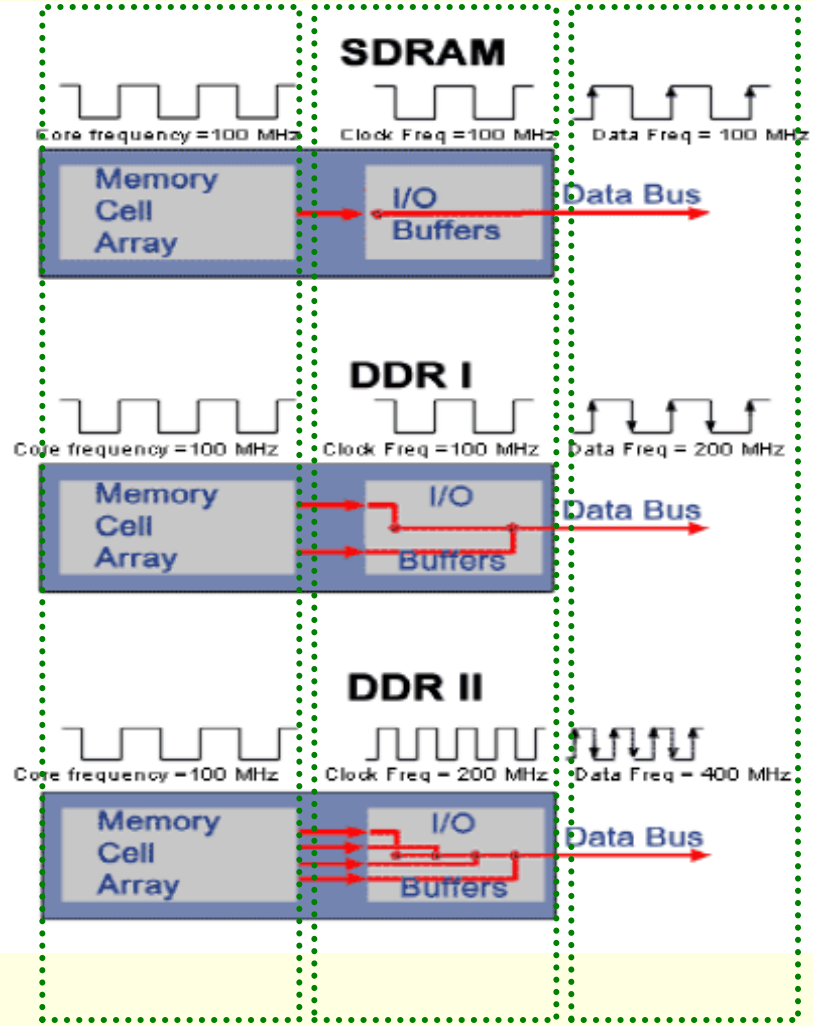
- Reduced operating voltage allows power saving
- Reduced voltage swing allows higher frequency
- Support for disabling DLL during Power Down Mode
- Less power to activate sense amps

DLL (Delay Lock Loop)

- DLL aligns DQ and DQS transitions with CK transitions

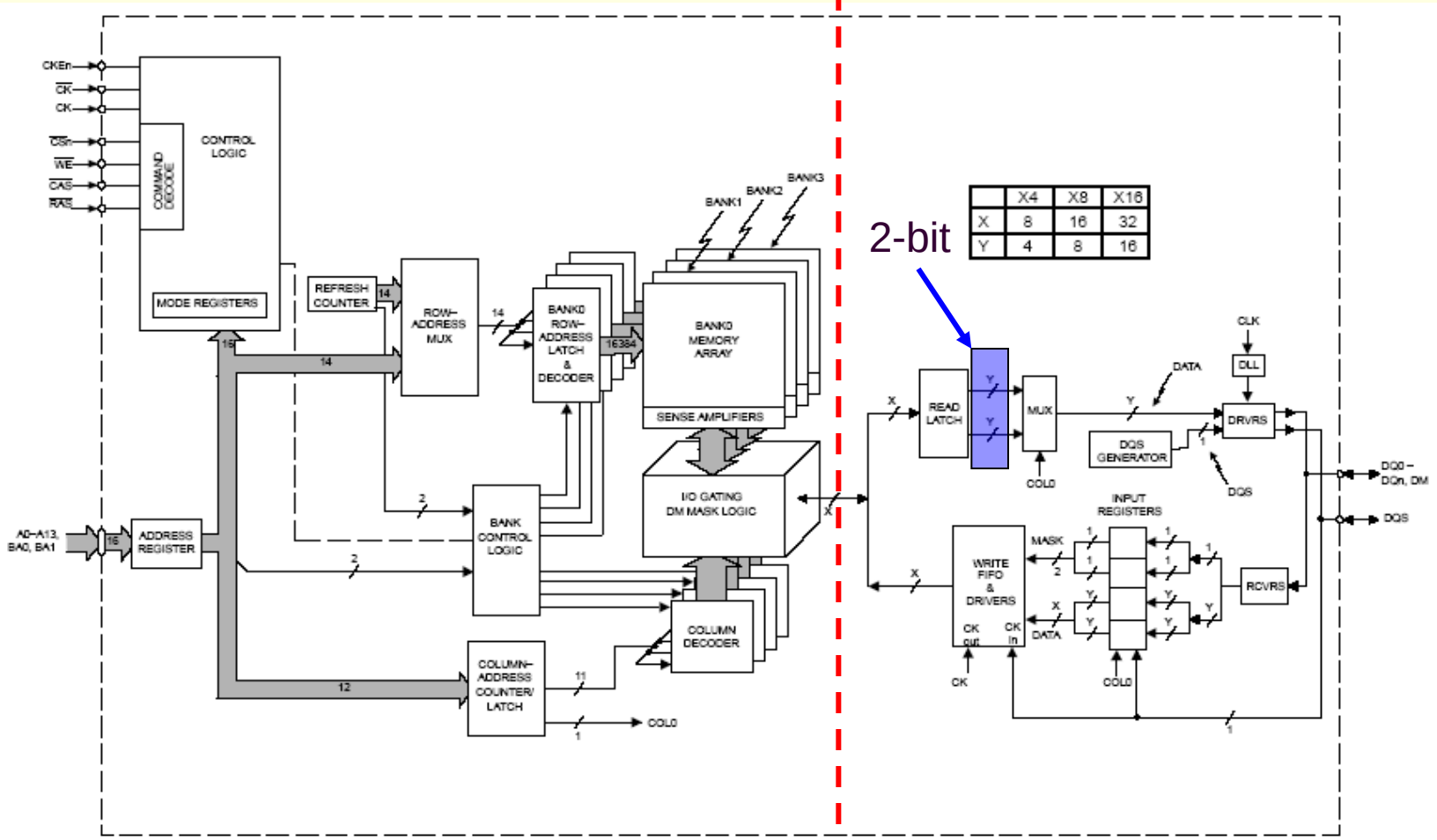


SDR, DDR and DDR2 clock comparison

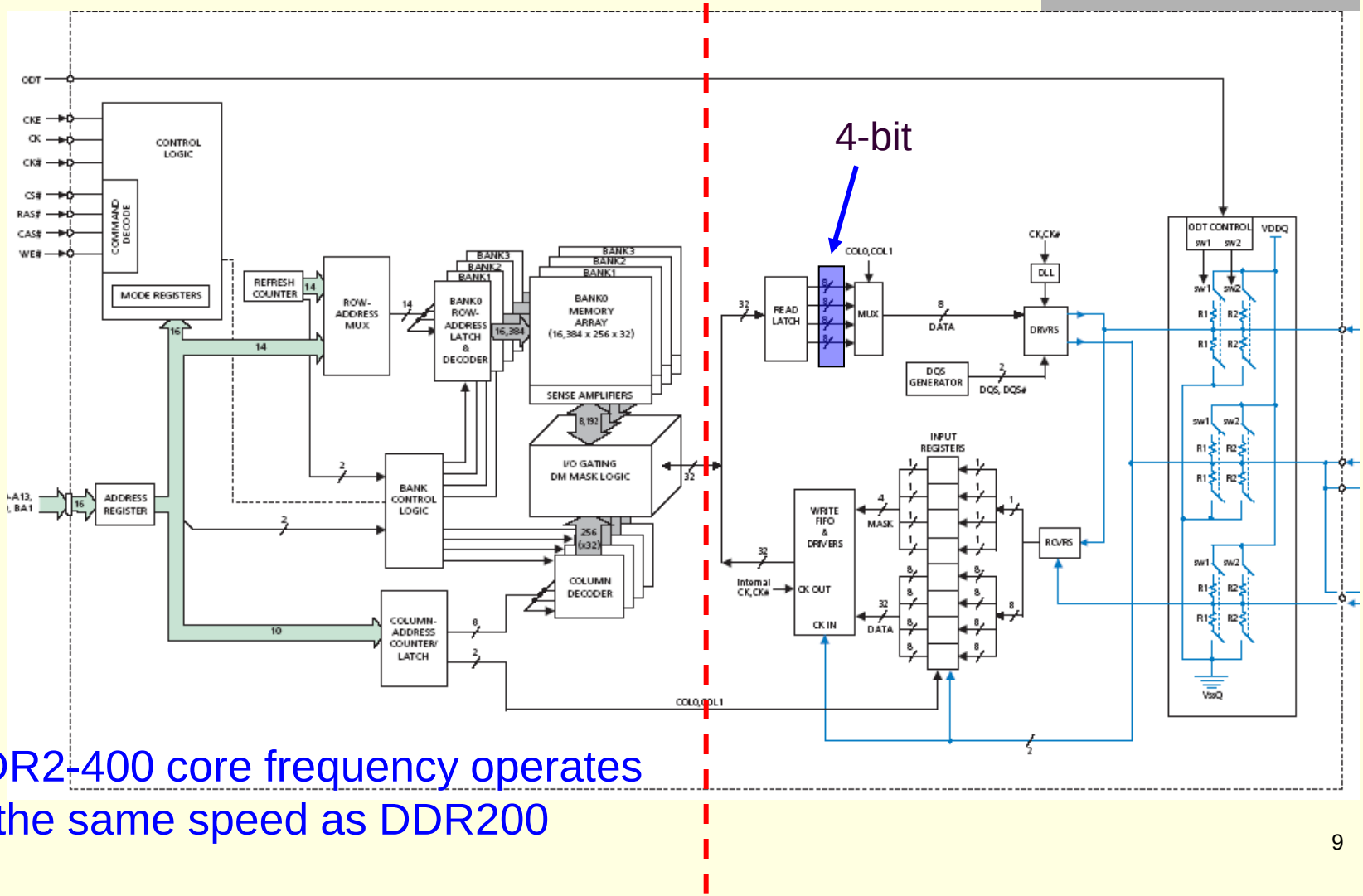


Item	DDR2 SDRAM	DDR SDRAM	SDR SDRAM
Prefetch	4 bit	2 bit	1 bit
Internal bus operating frequency	100MHz	100MHz	100MHz
External clock frequency	200MHz	100MHz	100MHz
Data bus speed	400Mbps	200Mbps	100Mbps

DDRI 2-bit Pre-fetch



DDRII 4-bit Pre-fetch



DDR2-400 core frequency operates at the same speed as DDR200

Burst Length

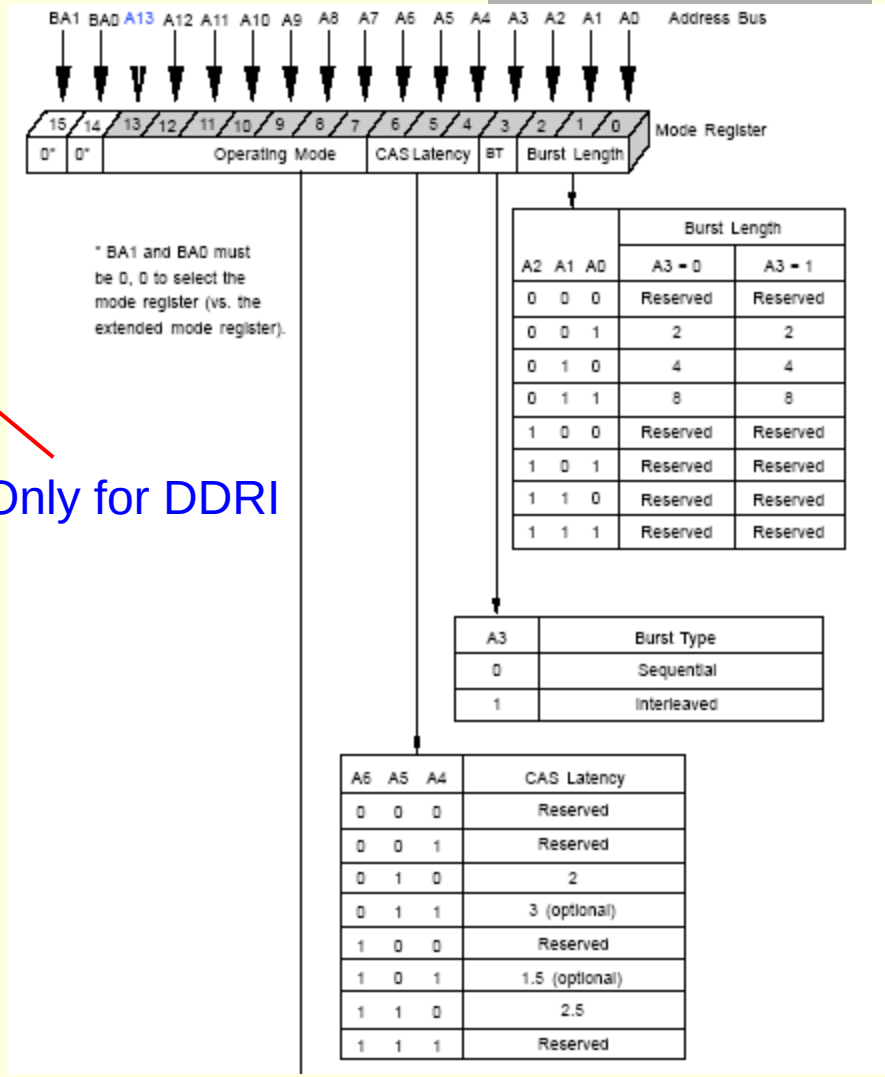
- Burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

Burst Length

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0–1	0–1
			1	1–0	1–0
4		A1	A0		
		0	0	0–1–2–3	0–1–2–3
		0	1	1–2–3–0	1–0–3–2
		1	0	2–3–0–1	2–3–0–1
		1	1	3–0–1–2	3–2–1–0
8	A2	A1	A0		
	0	0	0	0–1–2–3–4–5–6–7	0–1–2–3–4–5–6–7
	0	0	1	1–2–3–4–5–6–7–0	1–0–3–2–5–4–7–6
	0	1	0	2–3–4–5–6–7–0–1	2–3–0–1–6–7–4–5
	0	1	1	3–4–5–6–7–0–1–2	3–2–1–0–7–6–5–4
	1	0	0	4–5–6–7–0–1–2–3	4–5–6–7–0–1–2–3
	1	0	1	5–6–7–0–1–2–3–4	5–4–7–6–1–0–3–2
	1	1	0	6–7–0–1–2–3–4–5	6–7–4–5–2–3–0–1
	1	1	1	7–0–1–2–3–4–5–6	7–6–5–4–3–2–1–0

Only for DDRI



DDR2 Features

- Power Improvement
  - Reduced operating voltage allows power saving
  - Reduced voltage swing allows higher frequency
- Signal Integrity Improvement
  - Off Chip Driver (OCD) Calibration
  - On Die Termination (ODT)
- Posted CAS Mode
- 4bit Pre-fetch Architecture
  - Transfer four data word per clock cycle at the I/O pins
  - Core frequency run at the same speed as DDR

OCD (Off-Chip Driver) Calibration

- The I/O driver resistance is set to adjust the voltage to equalize the pull-up/pull-down resistance.

OCD (Off-Chip Driver) Calibration

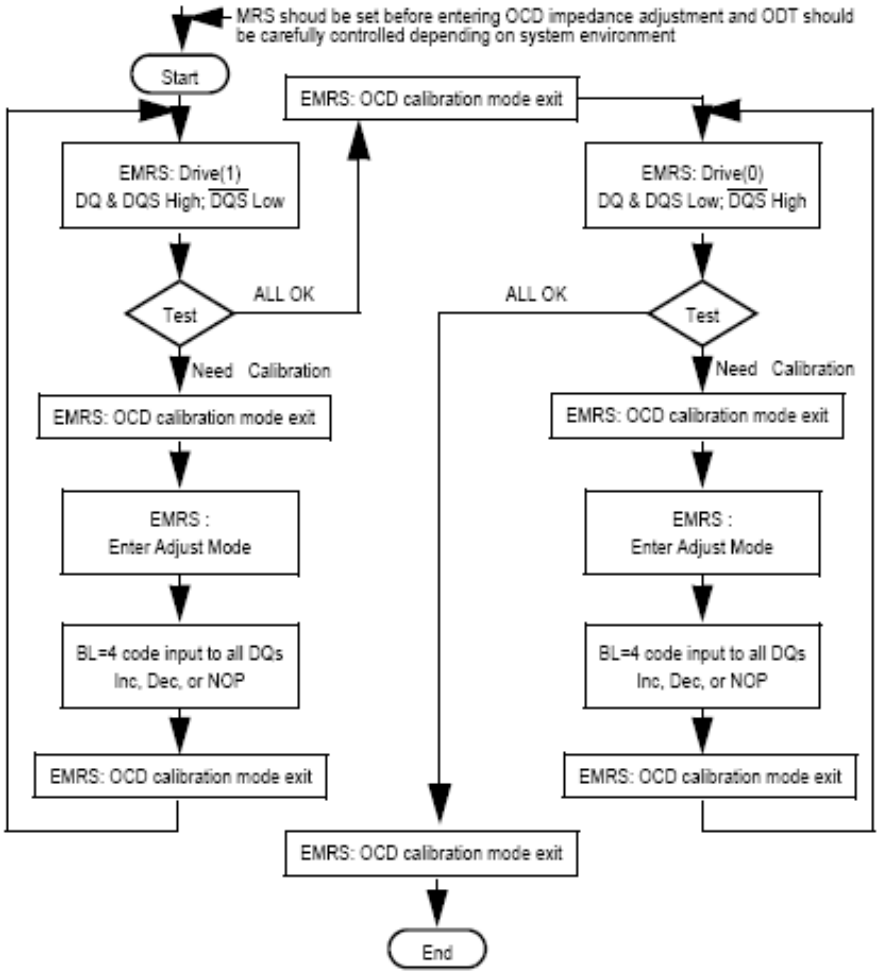
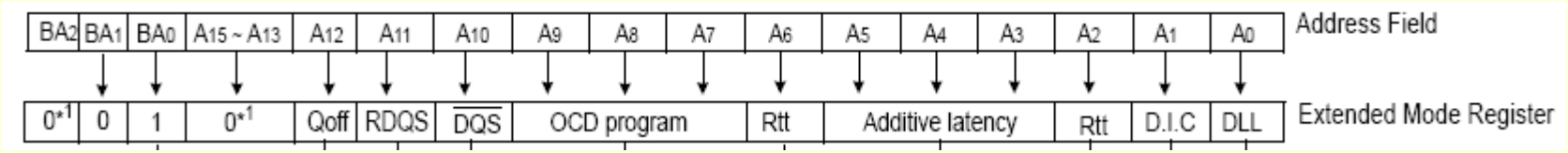


Figure 12 — OCD impedance adjustment

OCD (Off-Chip Driver) Calibration



A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$ low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and $\overline{DQS}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

OCD (Off-Chip Driver) Calibration

- Drive Mode is used for controllers to measure DDR2 SDRAM Driver impedance.

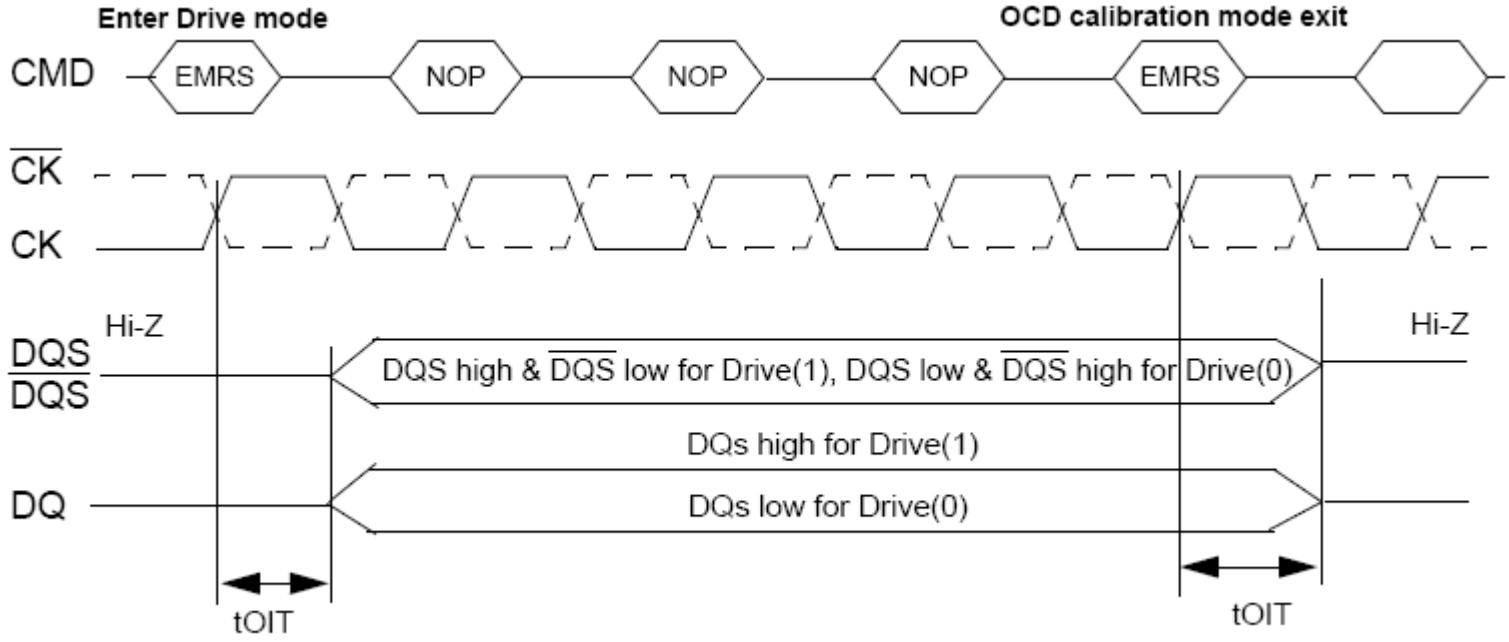
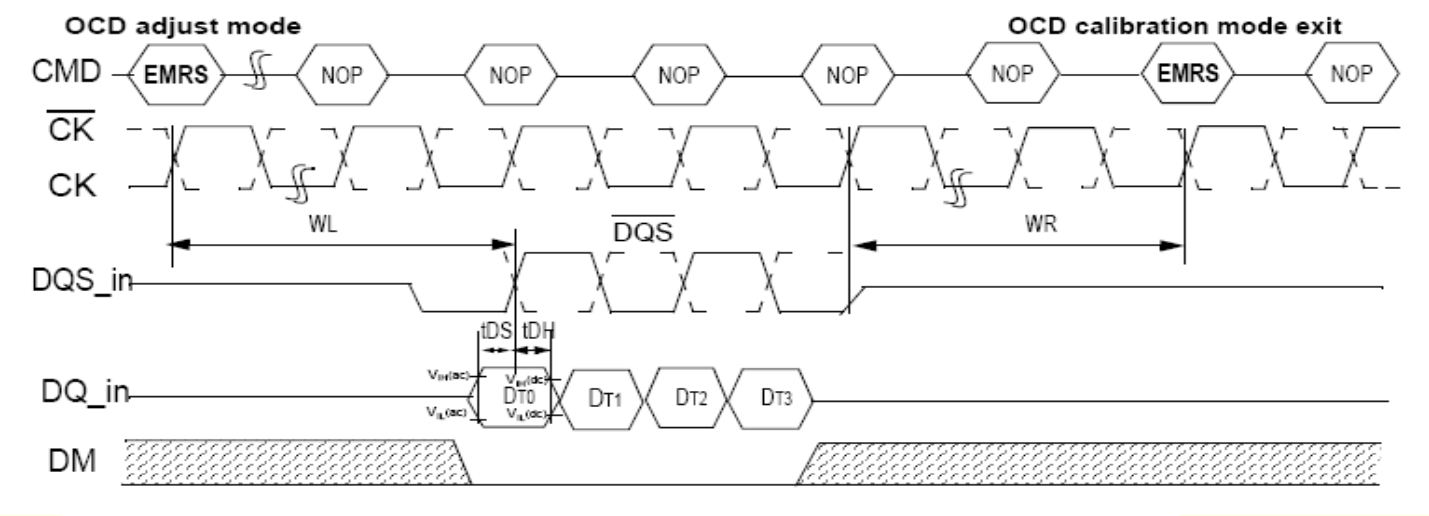


Figure 14 — OCD drive mode

OCD (Off-Chip Driver) Calibration

- Adjust Mode is used to adjust output driver impedance.



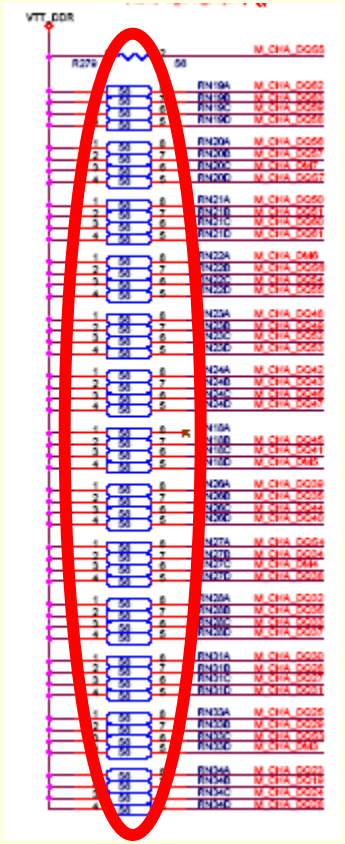
4bit burst code inputs to all DQs				Operation	
D_{T0}	D_{T1}	D_{T2}	D_{T3}	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

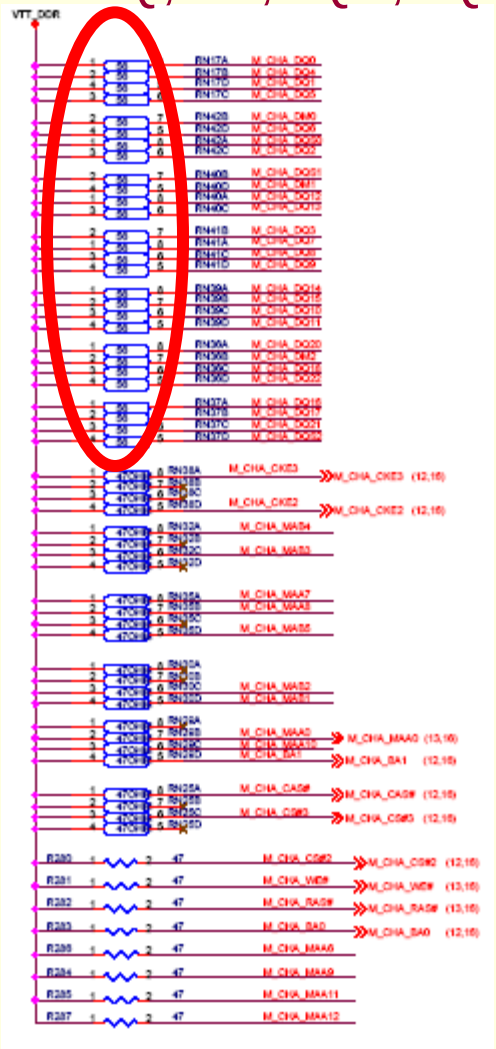
On Die Termination (ODT)

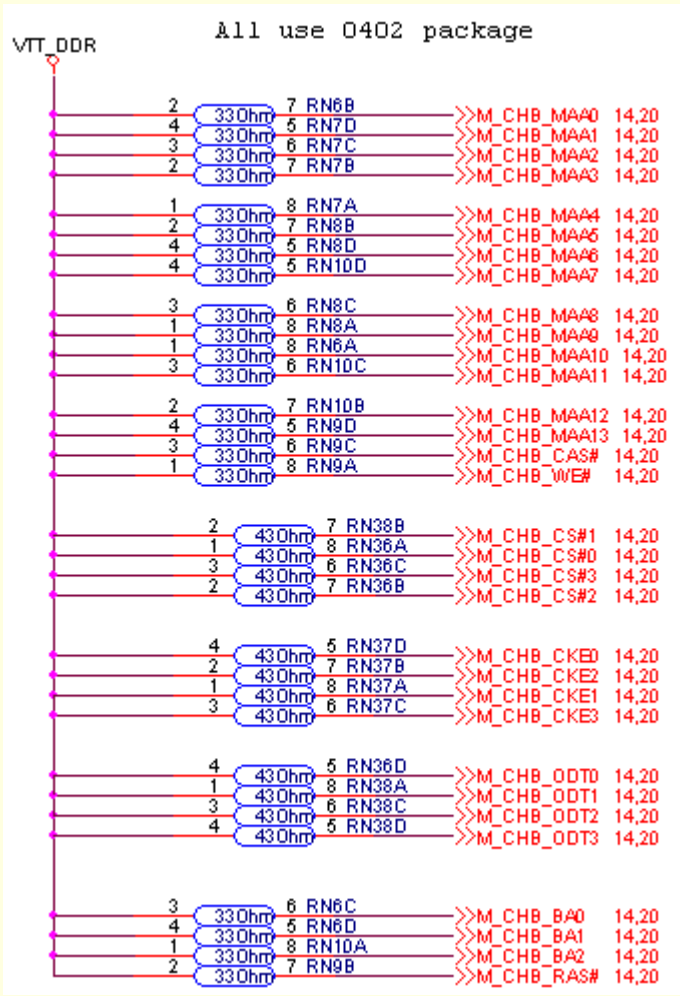
- Improved signal integrity
  - Control reflected noise on the transfer line
- Reduction of parts cost
  - Reduce the parts counts on the mother board
- Easier system design
  - Eliminate the complicated placement and routing for termination

On Die Termination (ODT)

DDRI DQ,DM,DQS,DQS# DDRII

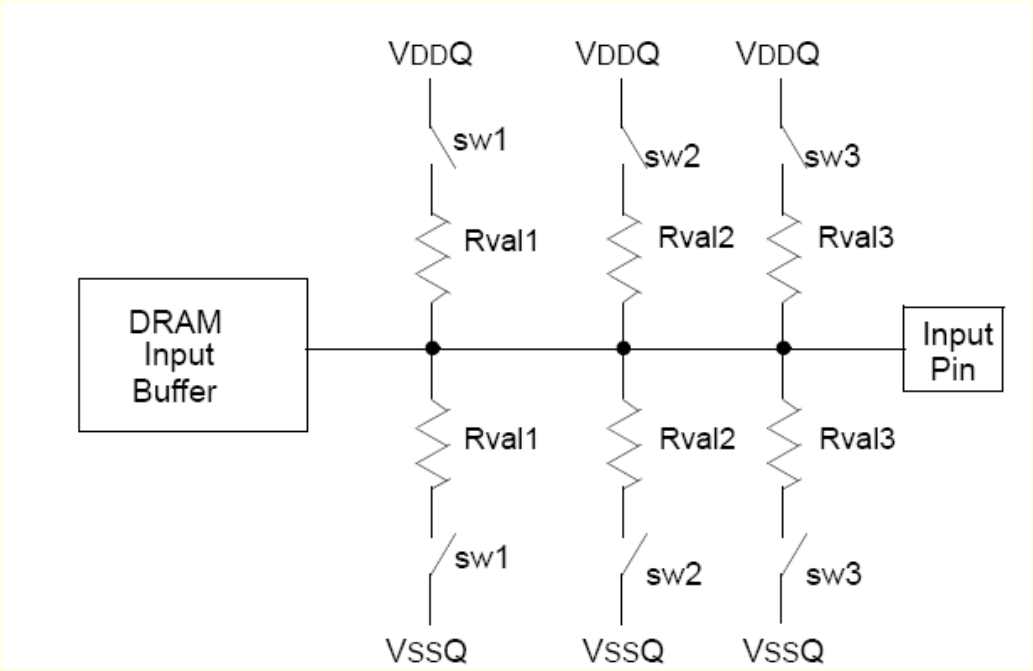


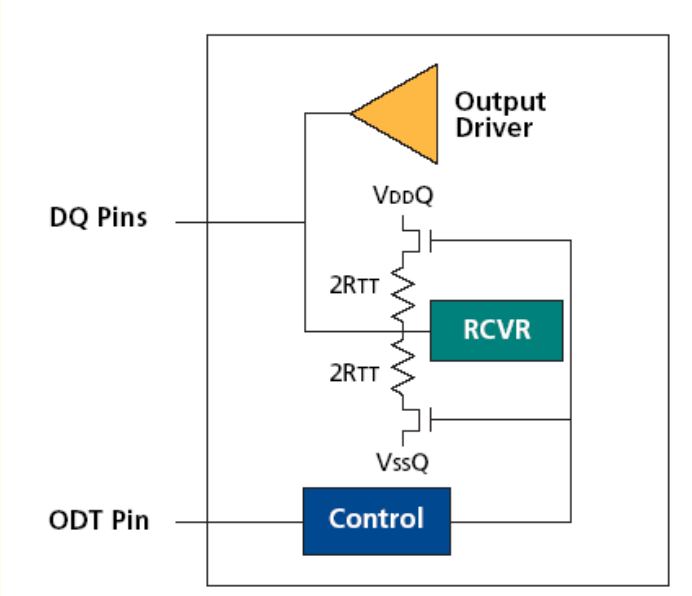




On Die Termination (ODT)

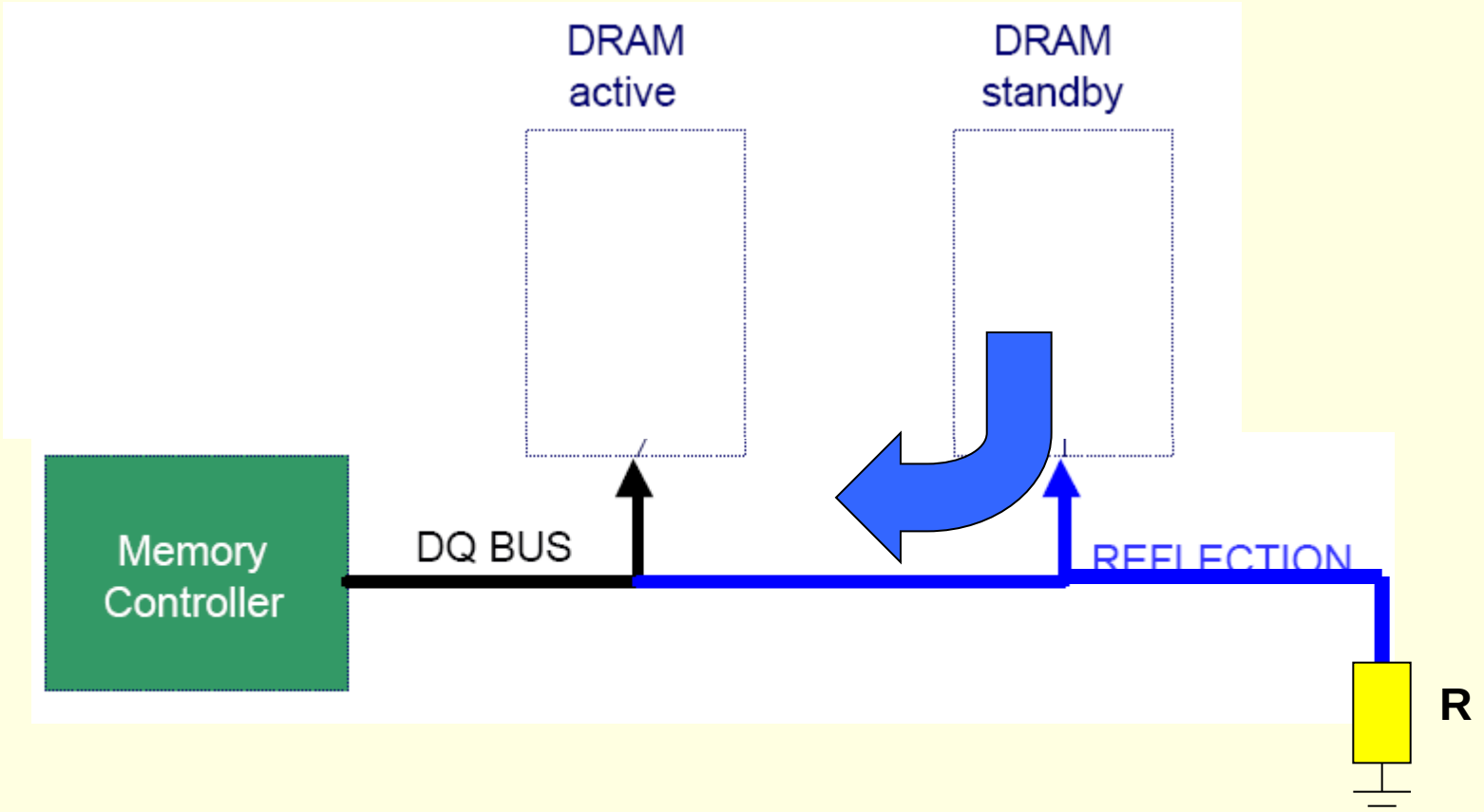
- On Die Termination (ODT) allows a DRAM to turn on/off termination resistance for each DQ,DQS/DQS#, RDQS/RDQS#, and DM signal.





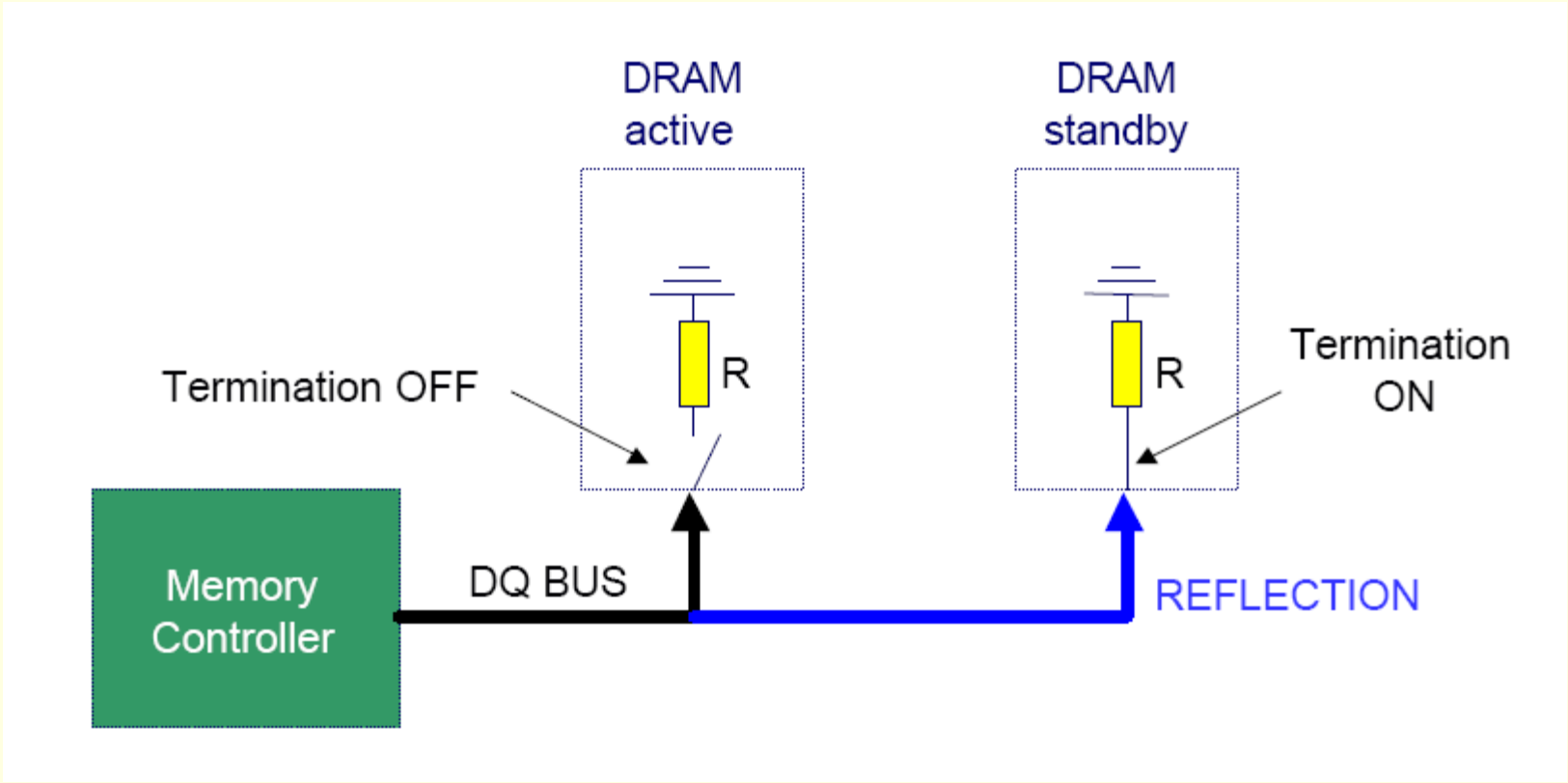
On Die Termination (ODT)

- DDRI

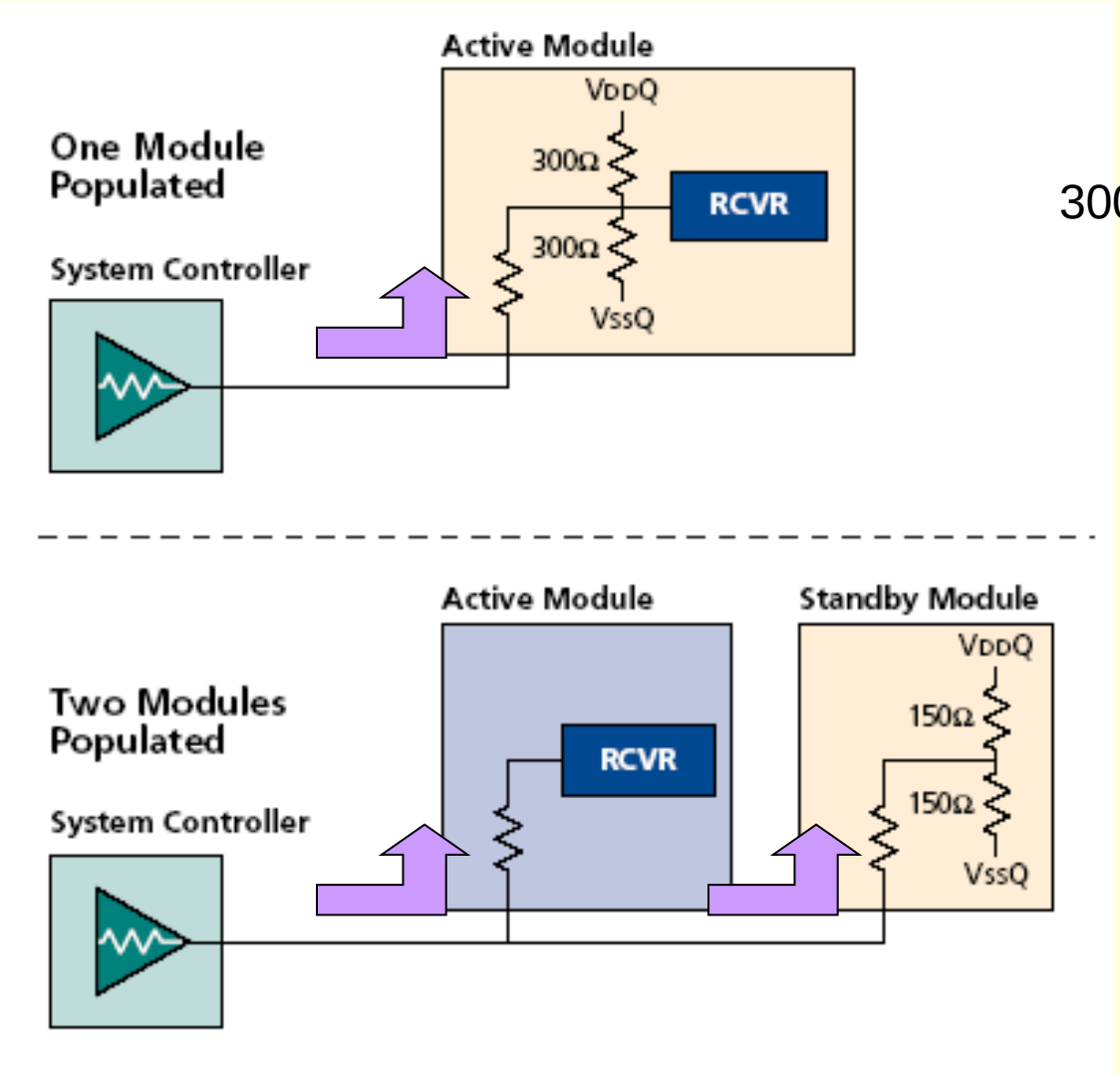


On Die Termination (ODT)

- DDRII



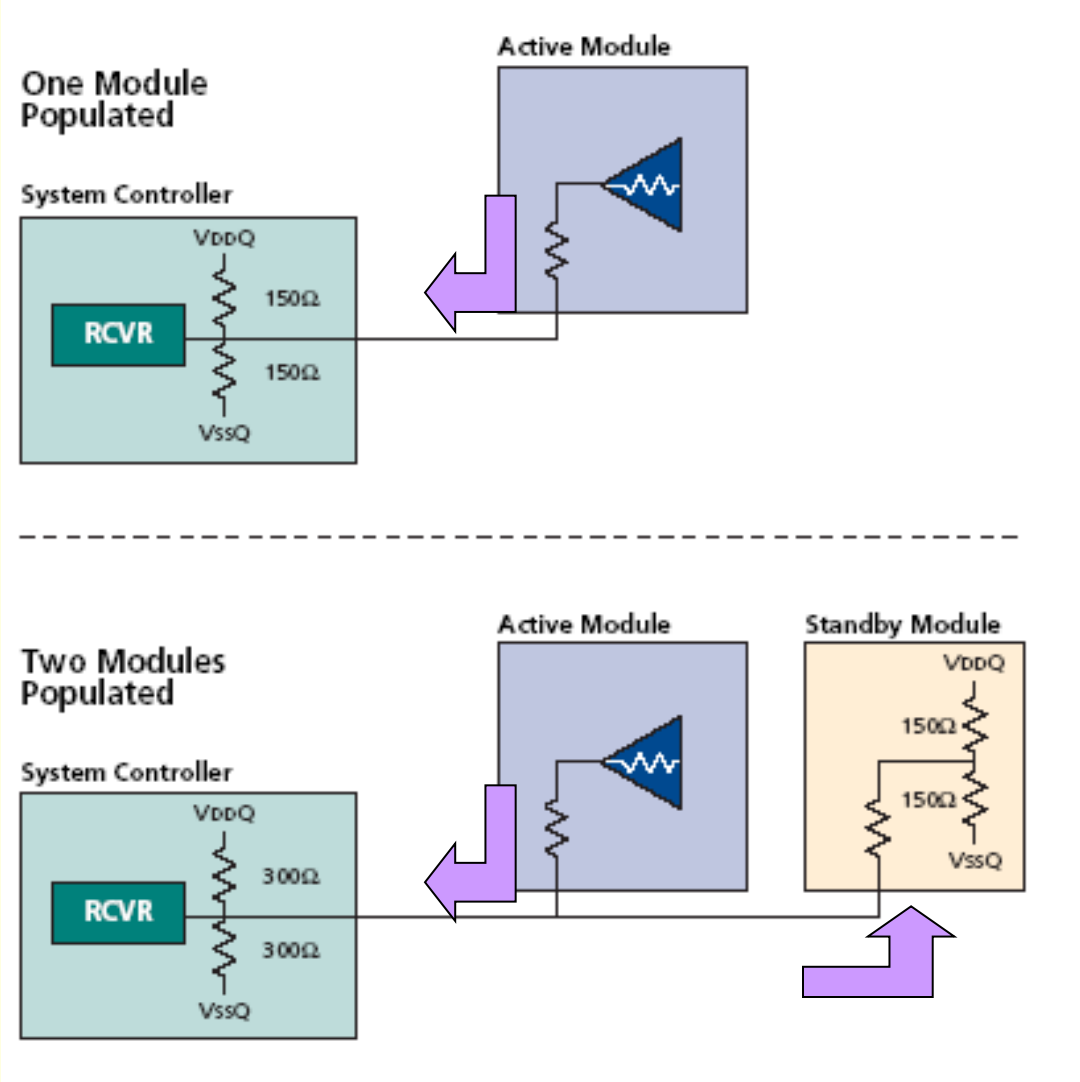
ODT WRITE



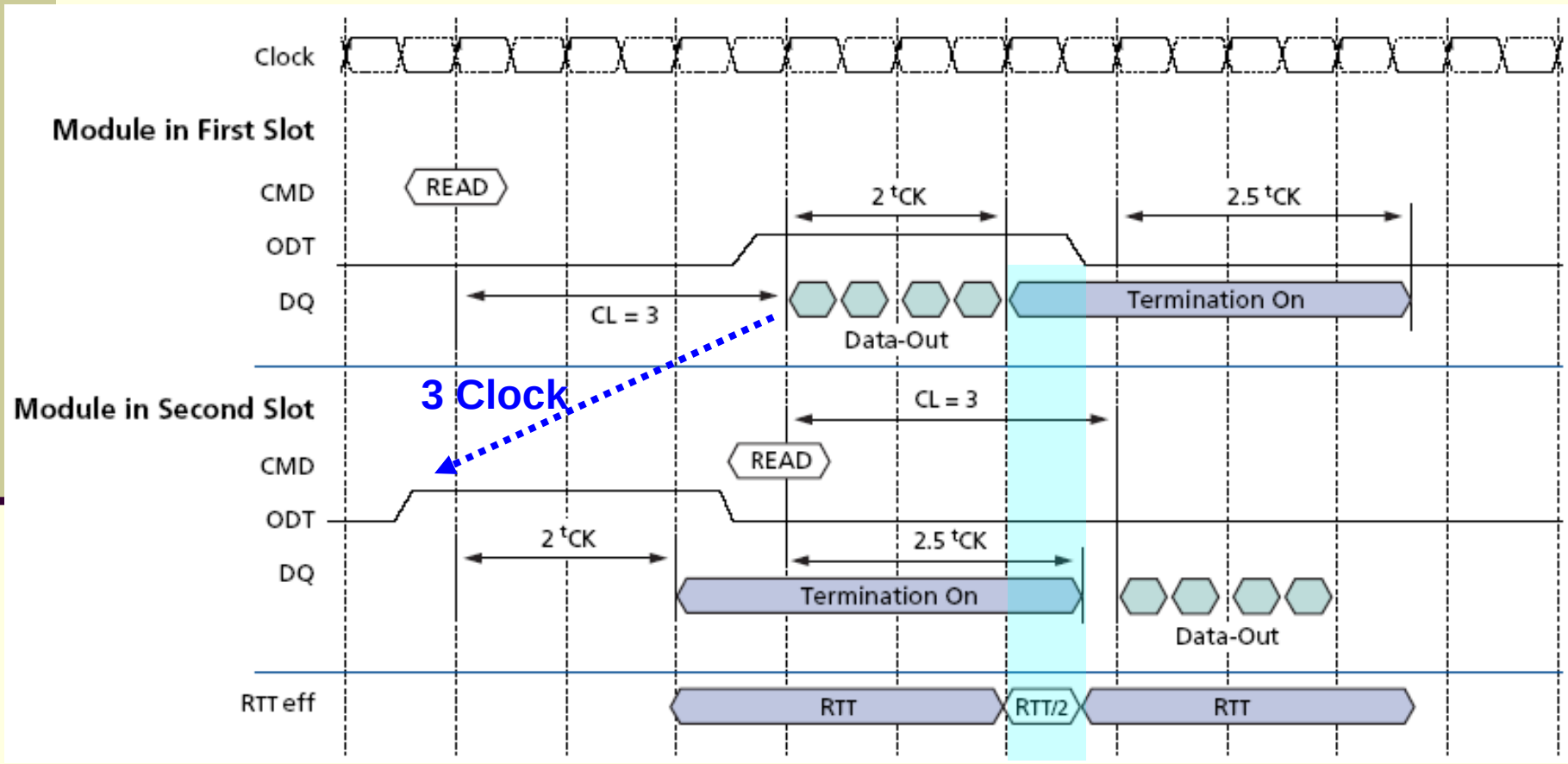
300//300ohm=150ohm

150//150ohm=75ohm

ODT READ

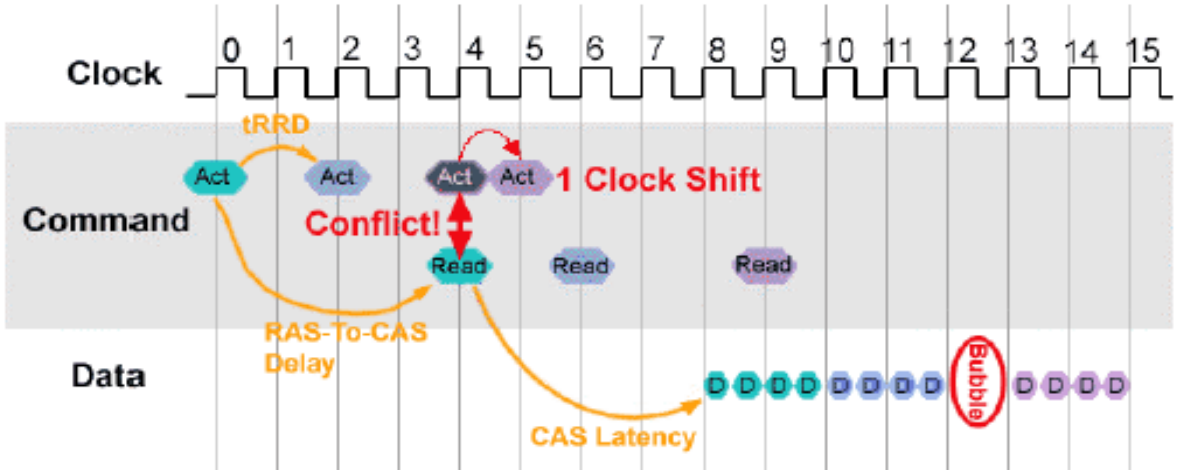

One Module Populated
Active Module
System Controller
VDDQ
150Ω
RCVR
150Ω
VSSQ
Two Modules Populated
Active Module
Standby Module
System Controller
VDDQ
300Ω
RCVR
300Ω
VSSQ
VDDQ
150Ω
150Ω
VSSQ

Rank-to-Rank ODT Control – READs

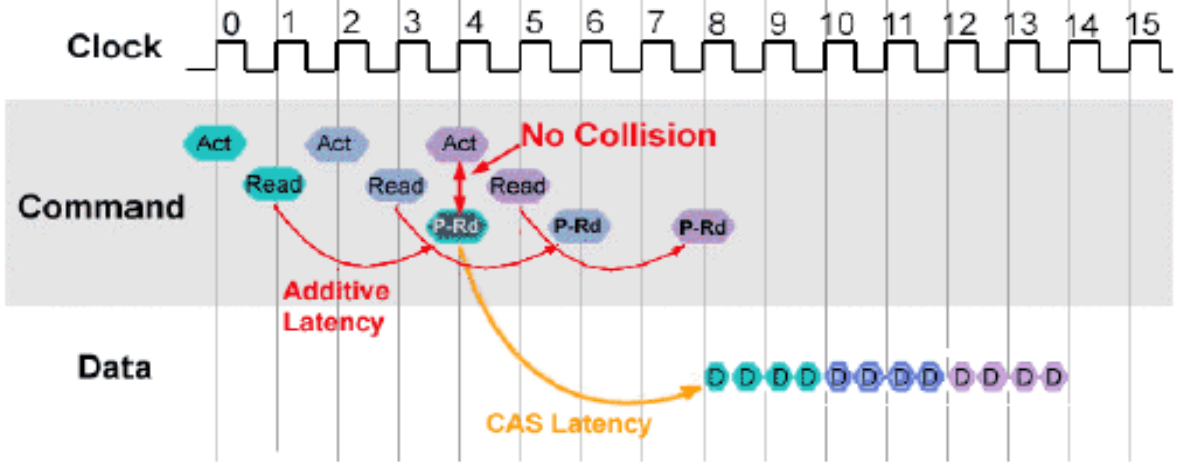


Posted CAS Mode

Conventional command



Posted CAS mode



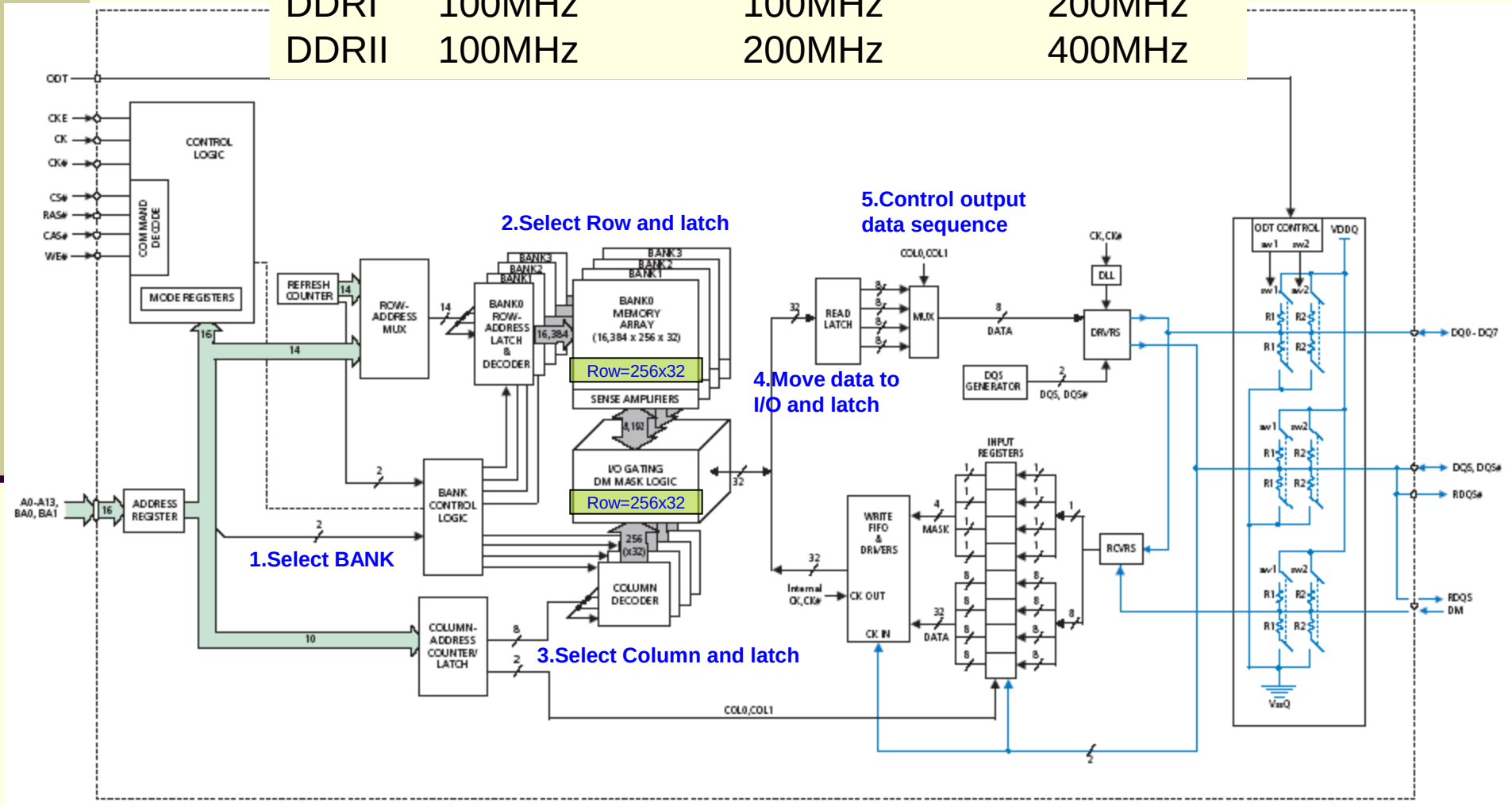
Act: Bank activate command
Read: Read Command
P-Rd: Posted Read / Posted CAS
D: data output
Green, Blue and Purple:
represent different bank access

Outline

- DDRI vs. DDRII
- Functional Block Diagram
- Simplified State Diagram
- Action of Functional signal Description

Functional Block Diagram (64 Meg x 8)

	Internal	External	Data bus
DDRI	100MHz	100MHz	200MHz
DDRII	100MHz	200MHz	400MHz



Pin Descriptions

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.

Pin Descriptions

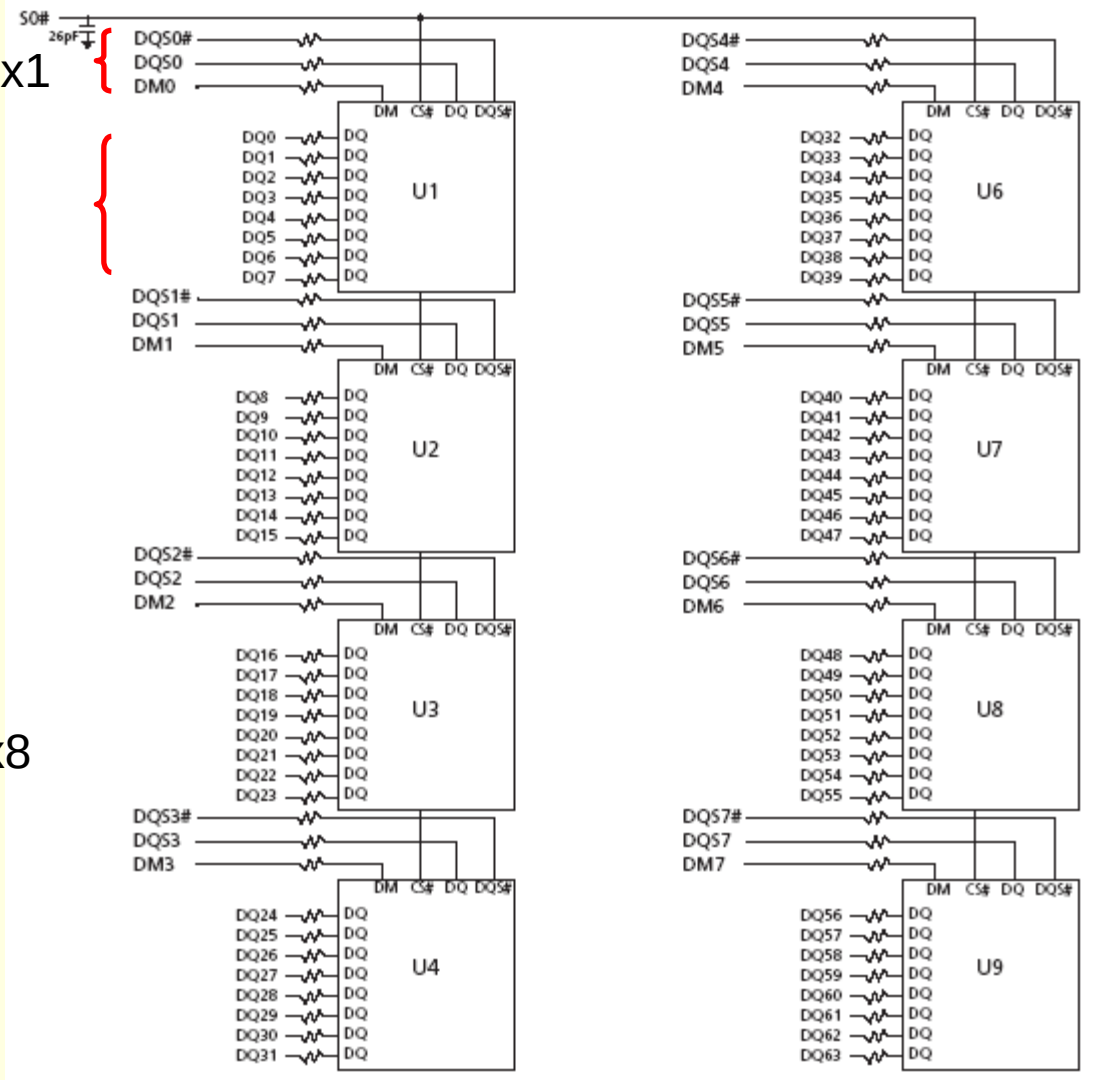
BA0 - BA2	Input	**Bank Address Inputs:** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied (For 256Mb and 512Mb, BA2 is not applied). Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0 - BA2. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{\text{DQS}}$) (UDQS), ($\overline{\text{UDQS}}$) (LDQS), ($\overline{\text{LDQS}}$) (RDQS), ($\overline{\text{RDQS}}$)	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{\text{DQS}}$, $\overline{\text{LDQS}}$, $\overline{\text{UDQS}}$, and $\overline{\text{RDQS}}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals. In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMRS(1) x4 DQS/$\overline{\text{DQS}}$ x8 DQS/$\overline{\text{DQS}}$ if EMRS(1)[A11] = 0 x8 DQS/$\overline{\text{DQS}}$, RDQS/$\overline{\text{RDQS}}$, if EMRS(1)[A11] = 1 x16 LDQS/$\overline{\text{LDQS}}$ and UDQS/$\overline{\text{UDQS}}$ "single-ended DQS signals" refers to any of the following with A10 = 1 of EMRS(1) x4 DQS x8 DQS if EMRS(1)[A11] = 0 x8 DQS, RDQS, if EMRS(1)[A11] = 1 x16 LDQS and UDQS
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**

SDRAM Slot (x8)

DQS/# x1

DQ x8

Total:
DQS/# x8
DQ x64



Pin Descriptions

Address are for all chips

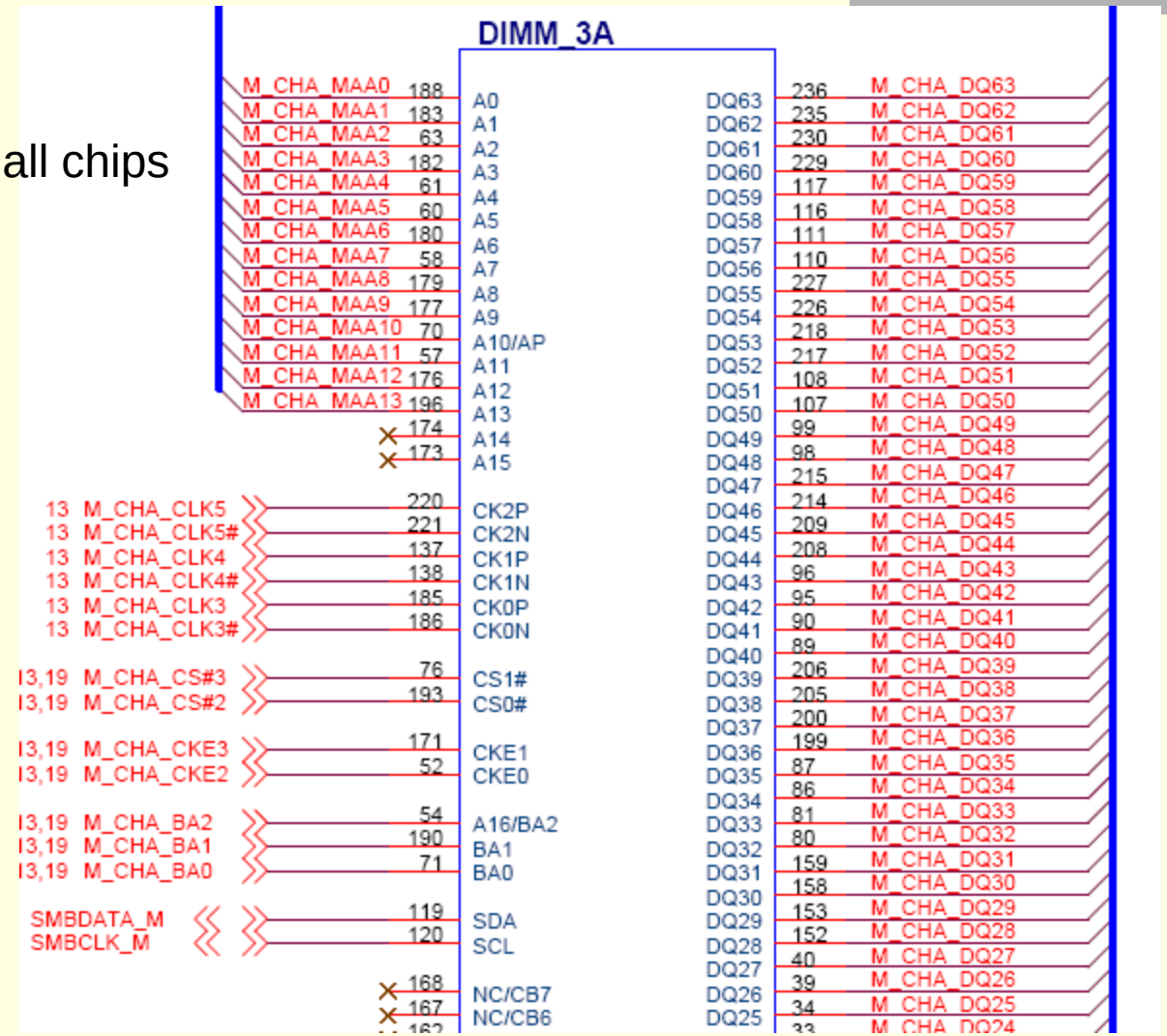
18/3

Chip select:
for Rank selection

X8,4bank need 2pin
X16,8bank need 3pin

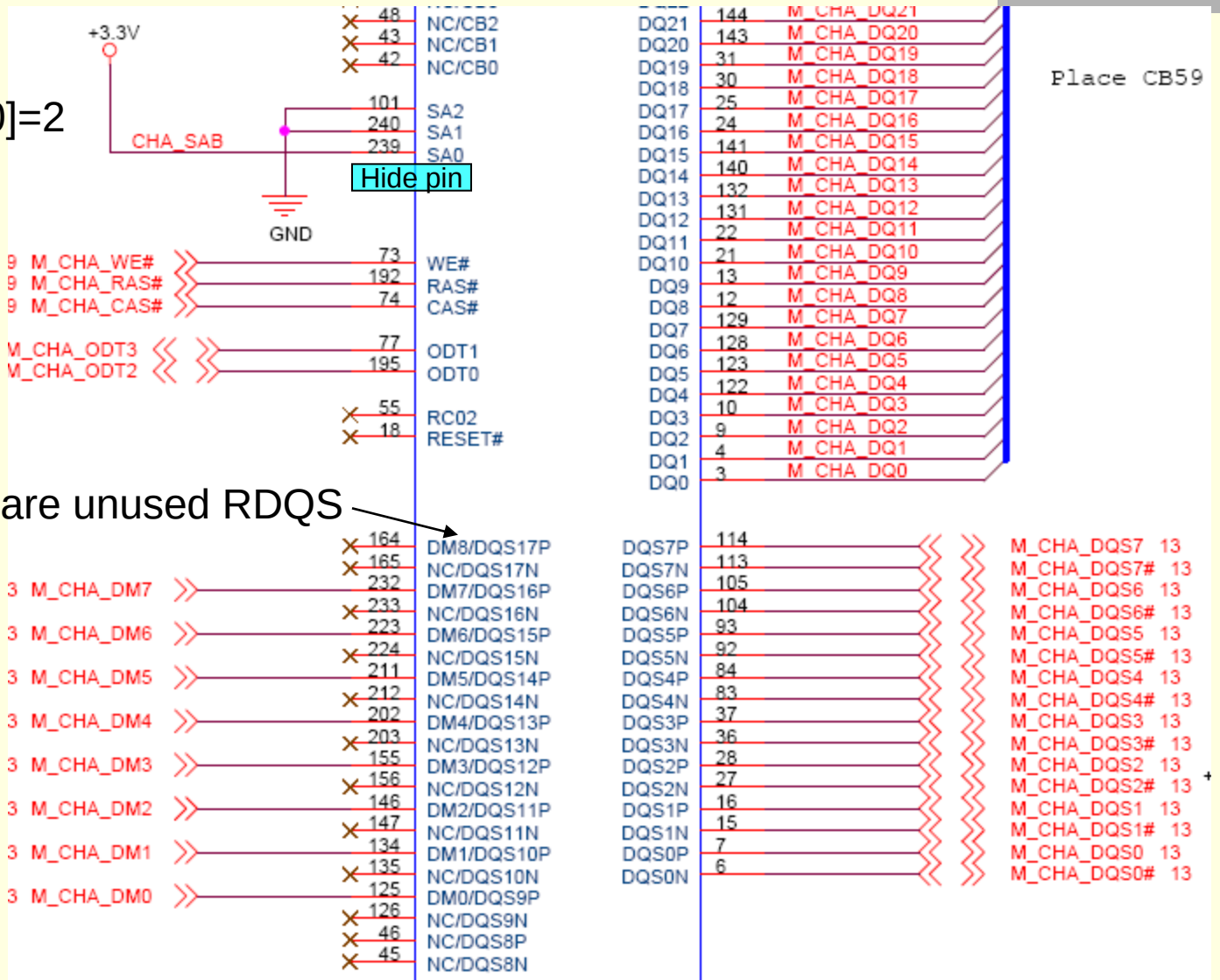
SMBus

7~1	0

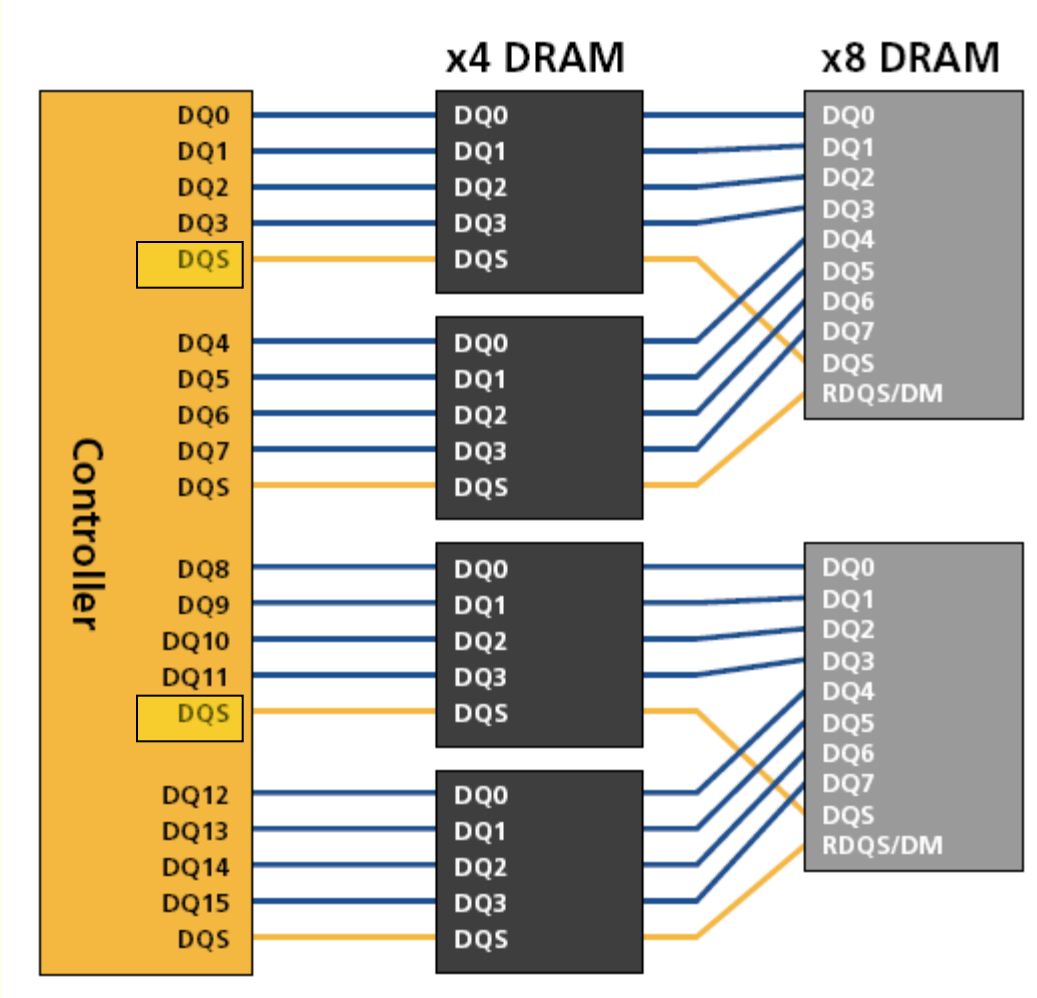


Pin Descriptions

Read
[0 0 1 0]=2
Write
2+1=3



RDQS: Redundant DQS



*Controller must support X4 DRAM

Outline

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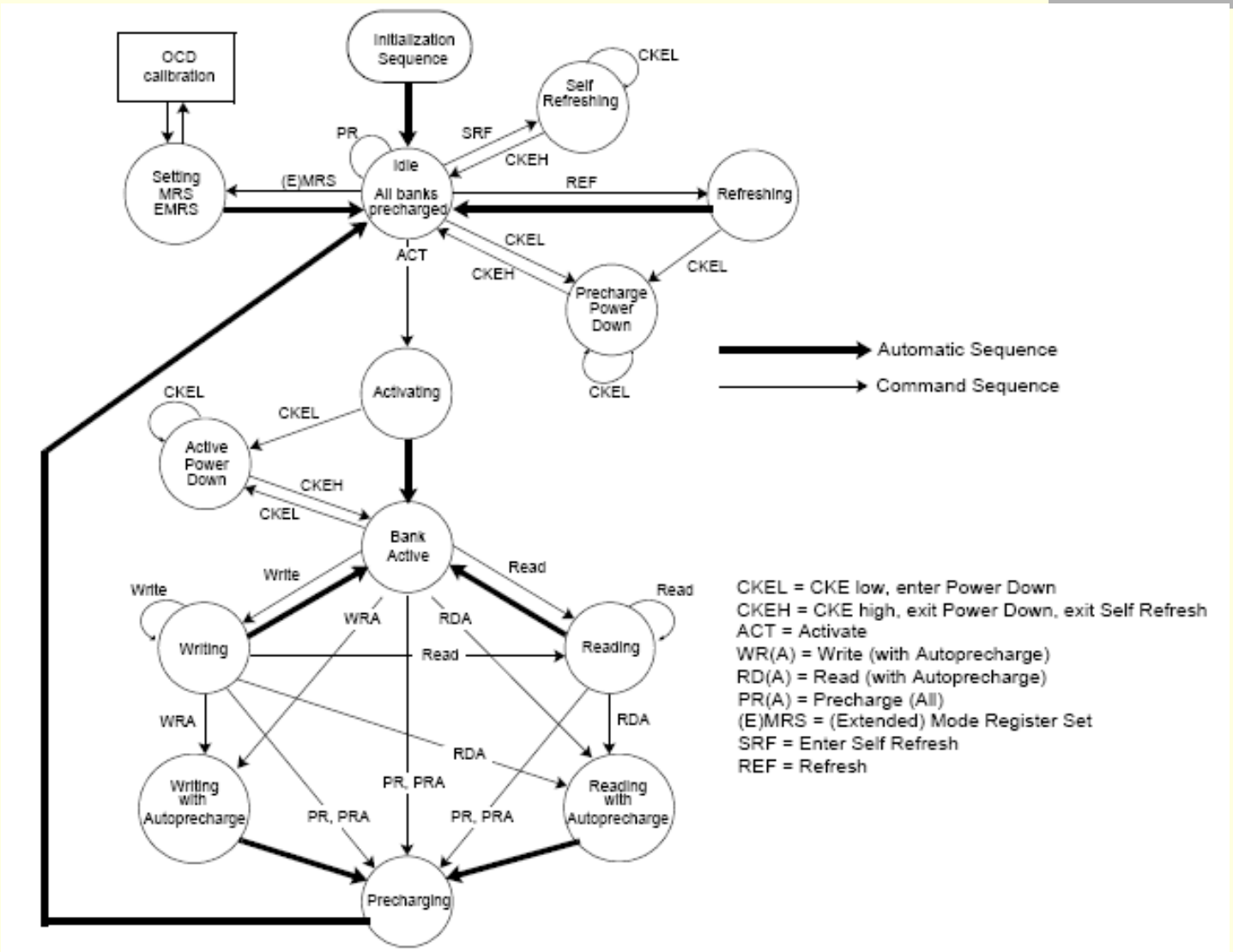
Simplified State Diagram



Outline

- DDRI vs. DDRII
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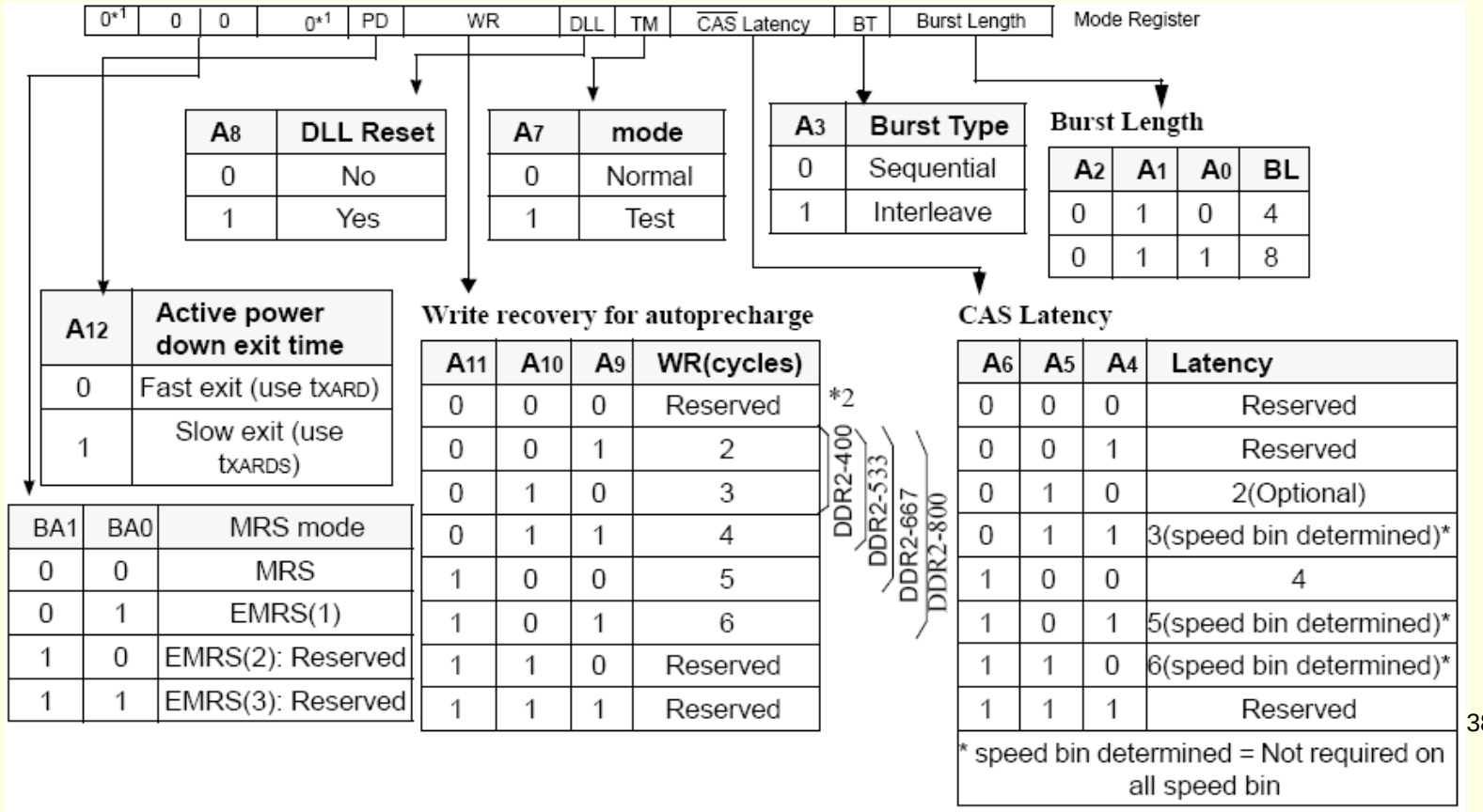
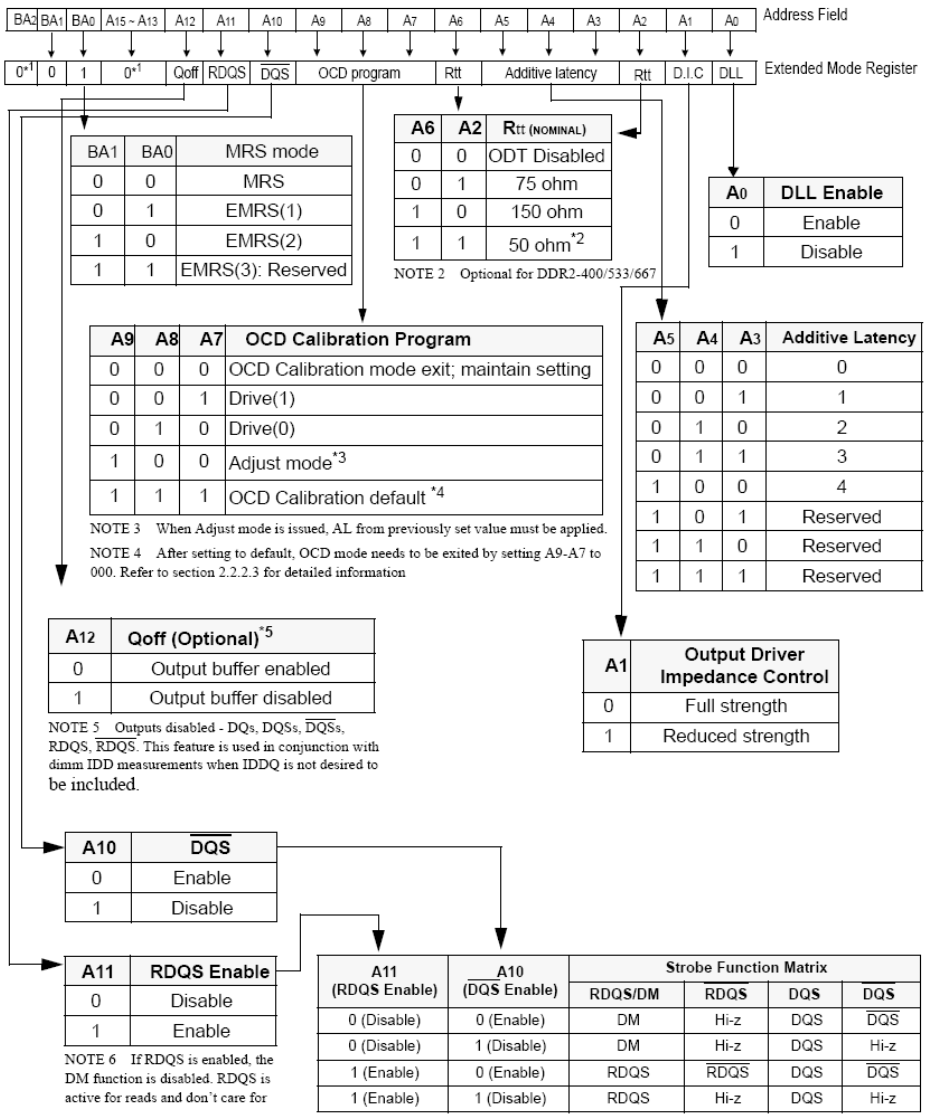
Mode Register Set (MRS)

- Control CAS latency, burst length, burst sequence, test mode, DLL reset, tWR



Extended Mode Register Set (EMRS)

- Stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, DQS disable, OCD program, RDQS enable.



Bank Active Command

- The bank addresses BA0 ~ BA2 are used to select the desired bank.
- The row address A0 through A15 is used to determine which row to activate in the selected bank.
- Once a bank has been activated it must be precharged.

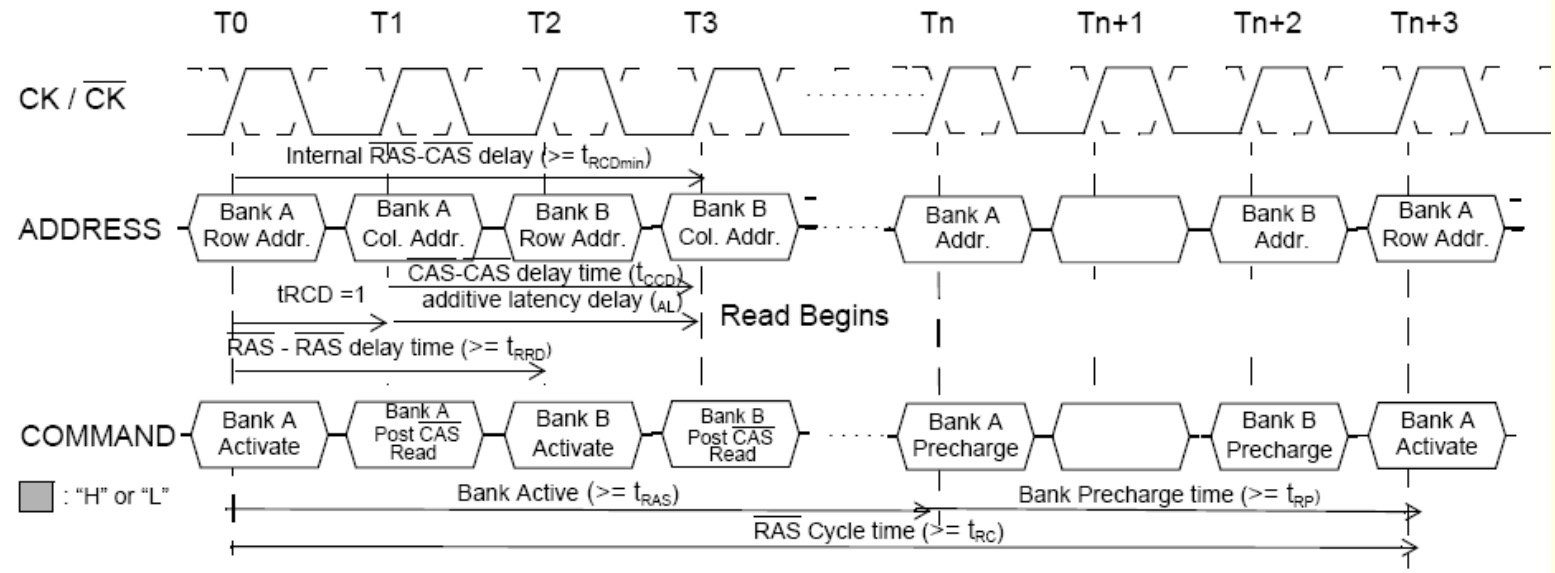
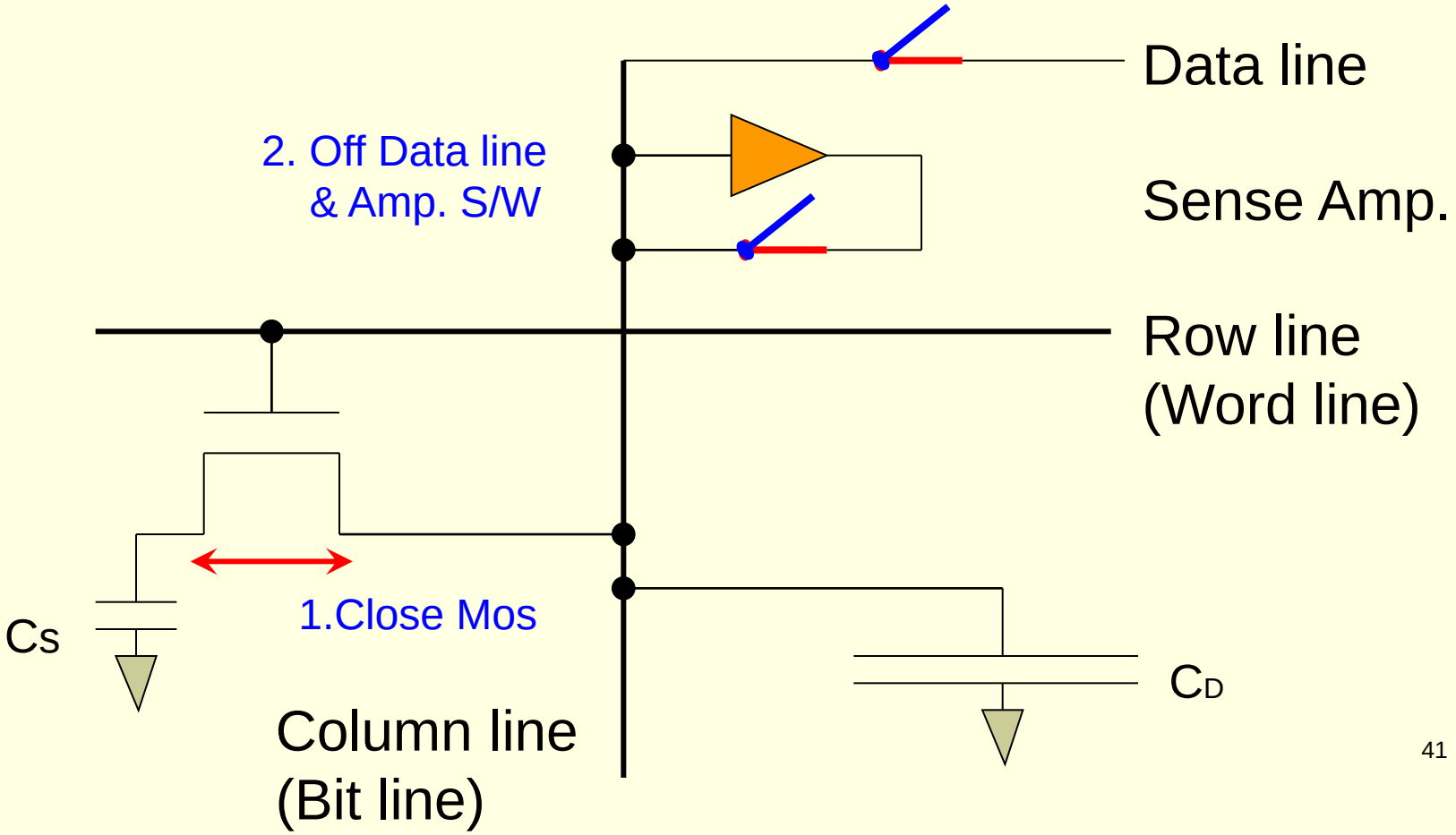


Figure 20 — Bank activate command cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2

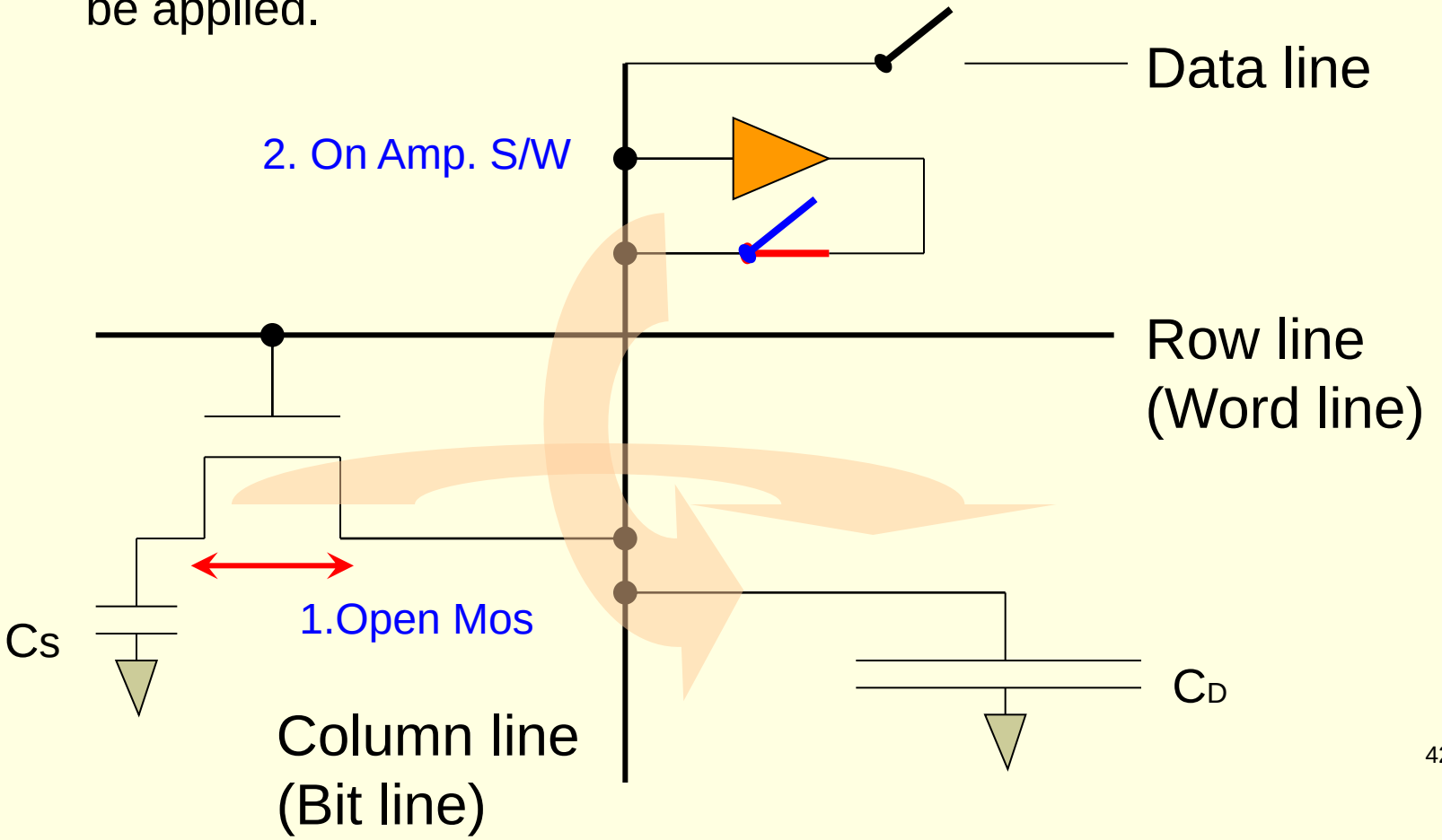
Precharge

- Precharge Command is used to precharge or close a bank that has been activated.



Refresh

- All banks must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied.



Refresh Command

- All banks must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied.

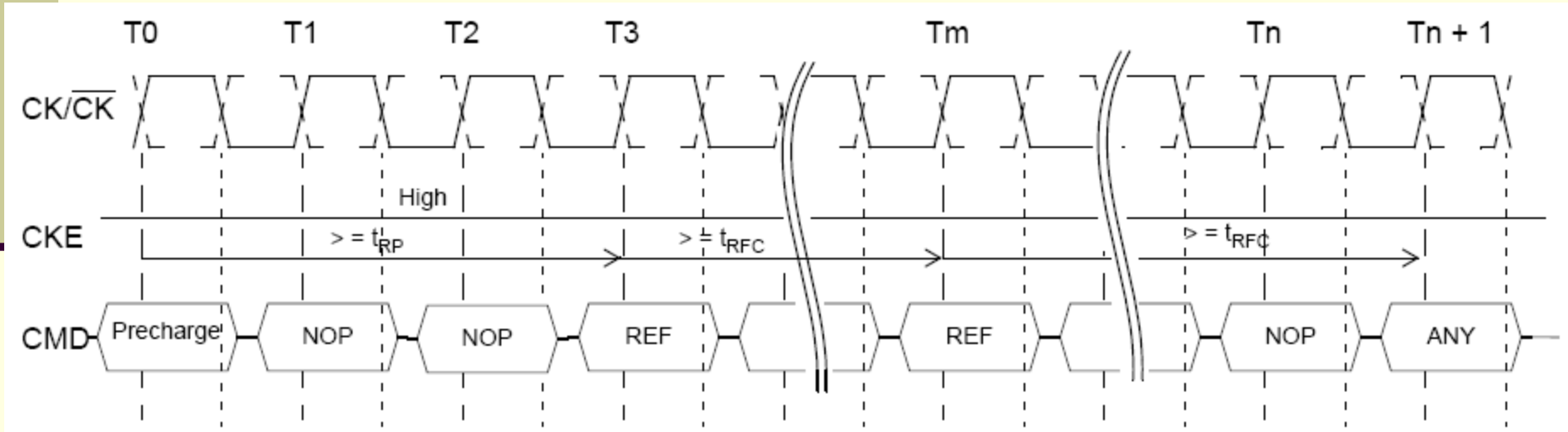
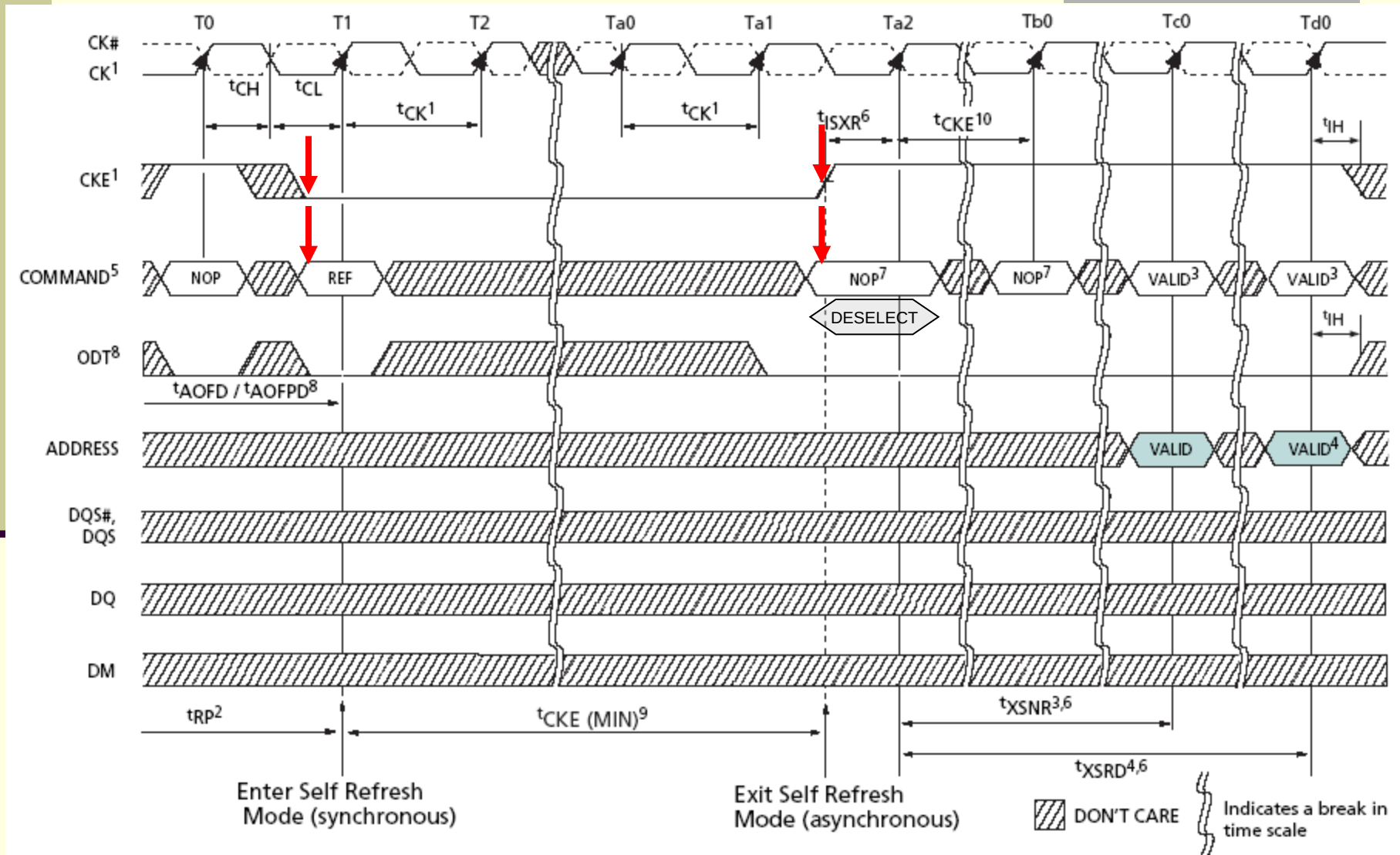


Figure 49 — Refresh command

Self Refresh Operation



Burst Read Command

- RL=AL+CL
- When AL=2

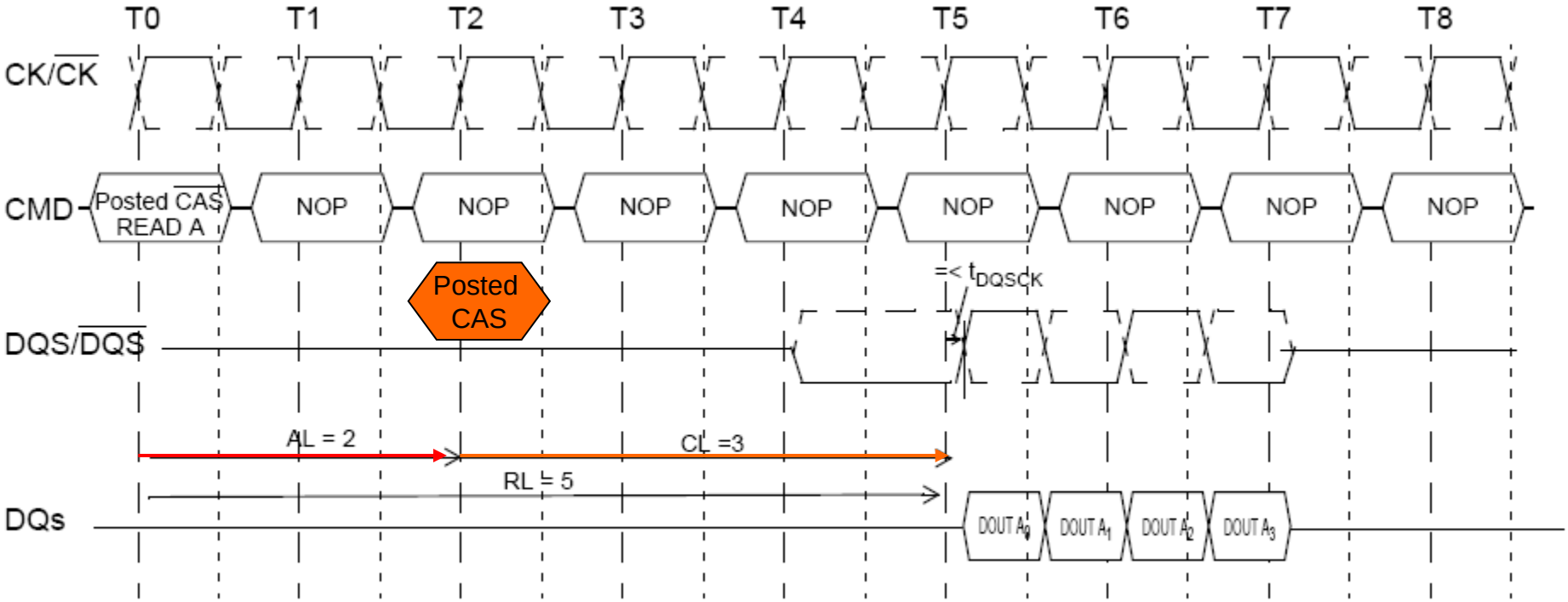


Figure 24 — Burst read operation: RL = 5 (AL = 2, CL = 3, BL = 4)

Burst Read Command

- When AL=0

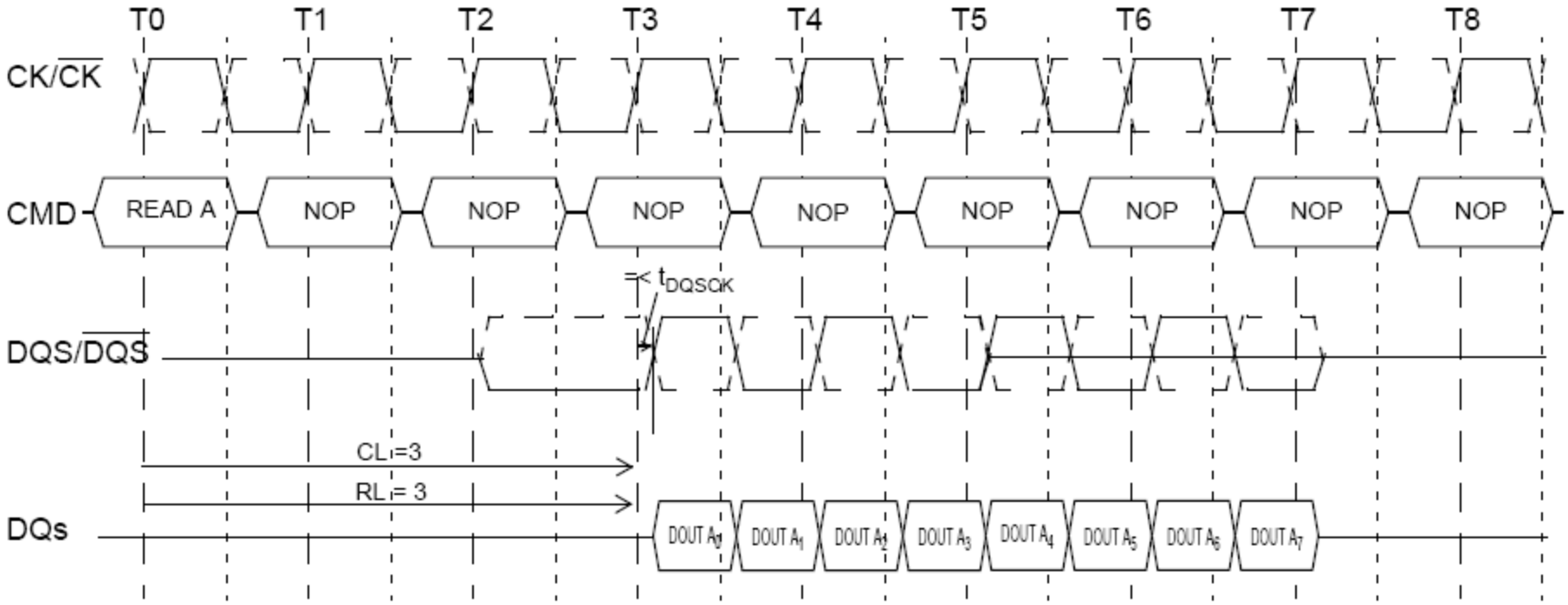


Figure 25 — Burst read operation: RL = 3 (AL = 0 and CL = 3, BL = 8)

Burst Write Command

- WL=RL-1

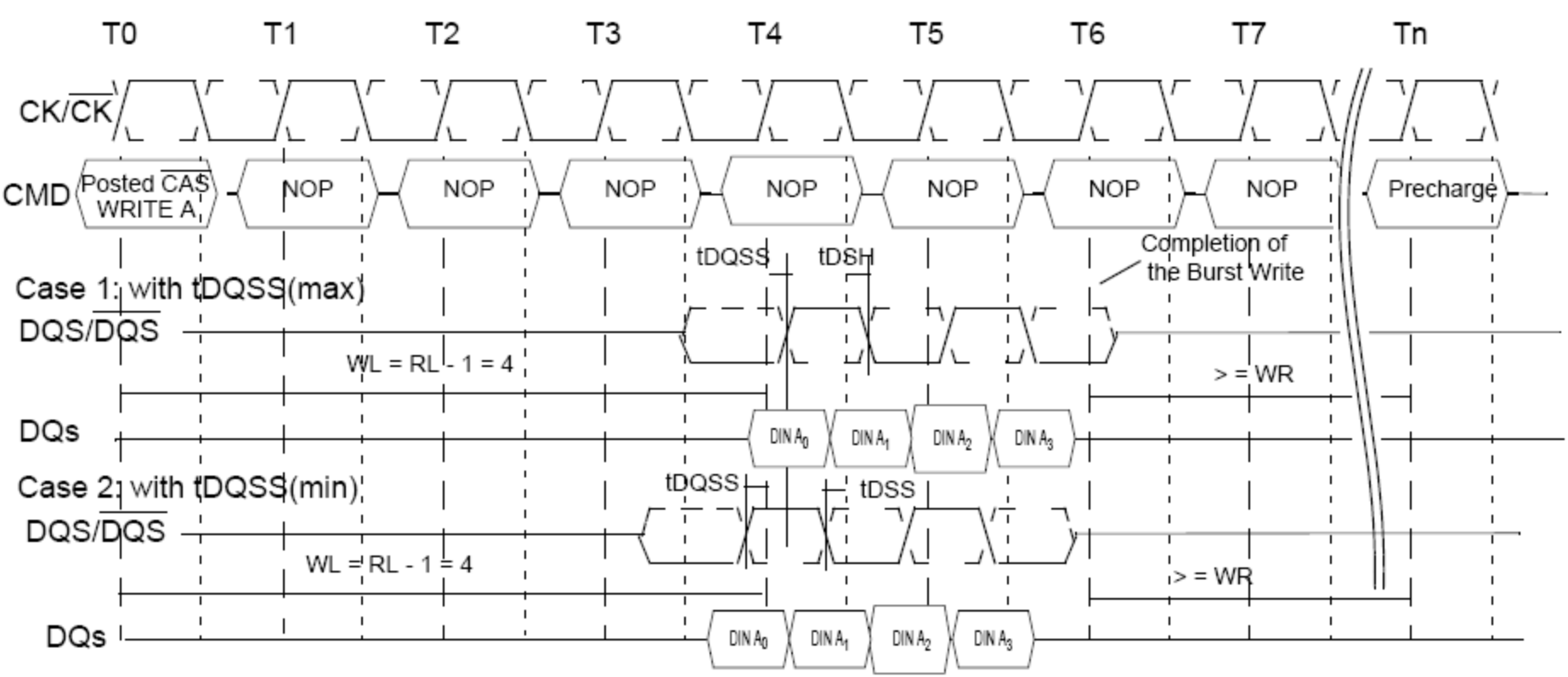


Figure 30 — Burst write operation: RL = 5 (AL=2, CL=3), WL = 4, WR = 3, BL = 4

*tDQSS: First DQS latching transition to associated clock edge

Burst Read followed by Burst Write

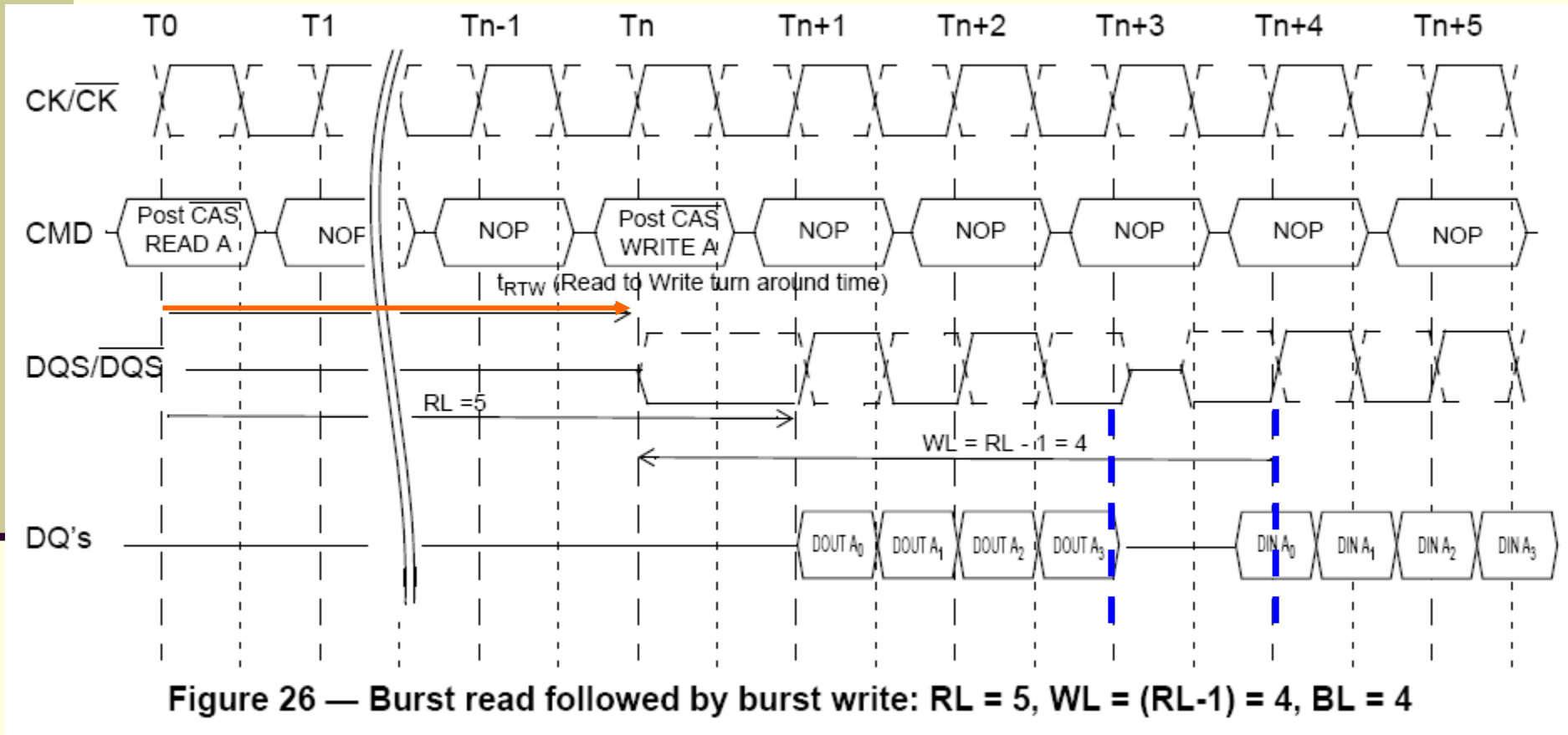
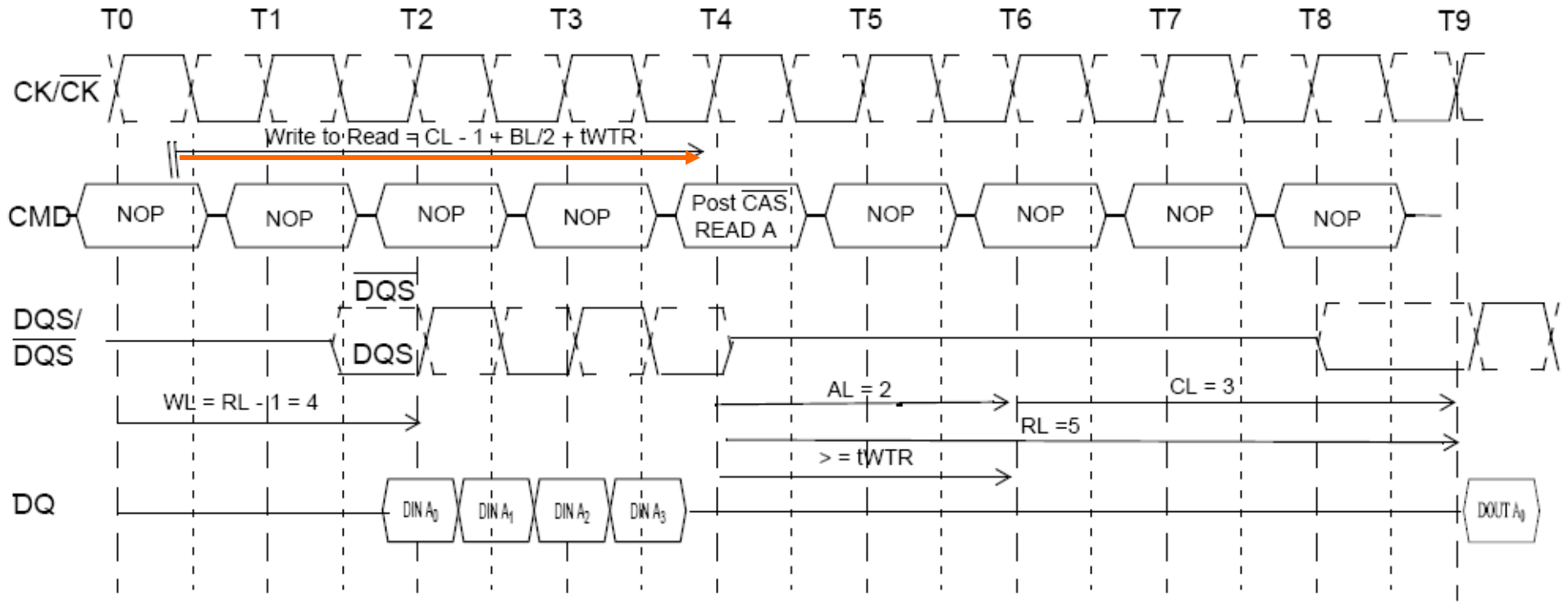


Figure 26 — Burst read followed by burst write: RL = 5, WL = (RL-1) = 4, BL = 4

*t_{RTW}: Read to Write turn around time

Burst Write followed by Burst Read



NOTE The minimum number of clock from the burst write command to the burst read command is [CL - 1 + BL/2 + tWTR]. This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array. tWTR is defined in AC spec table of this data sheet.

Figure 32 — Burst write followed by burst read: RL = 5 (AL=2, CL=3), WL = 4, tWTR = 2, BL = 4

Burst Read operation followed by Precharge

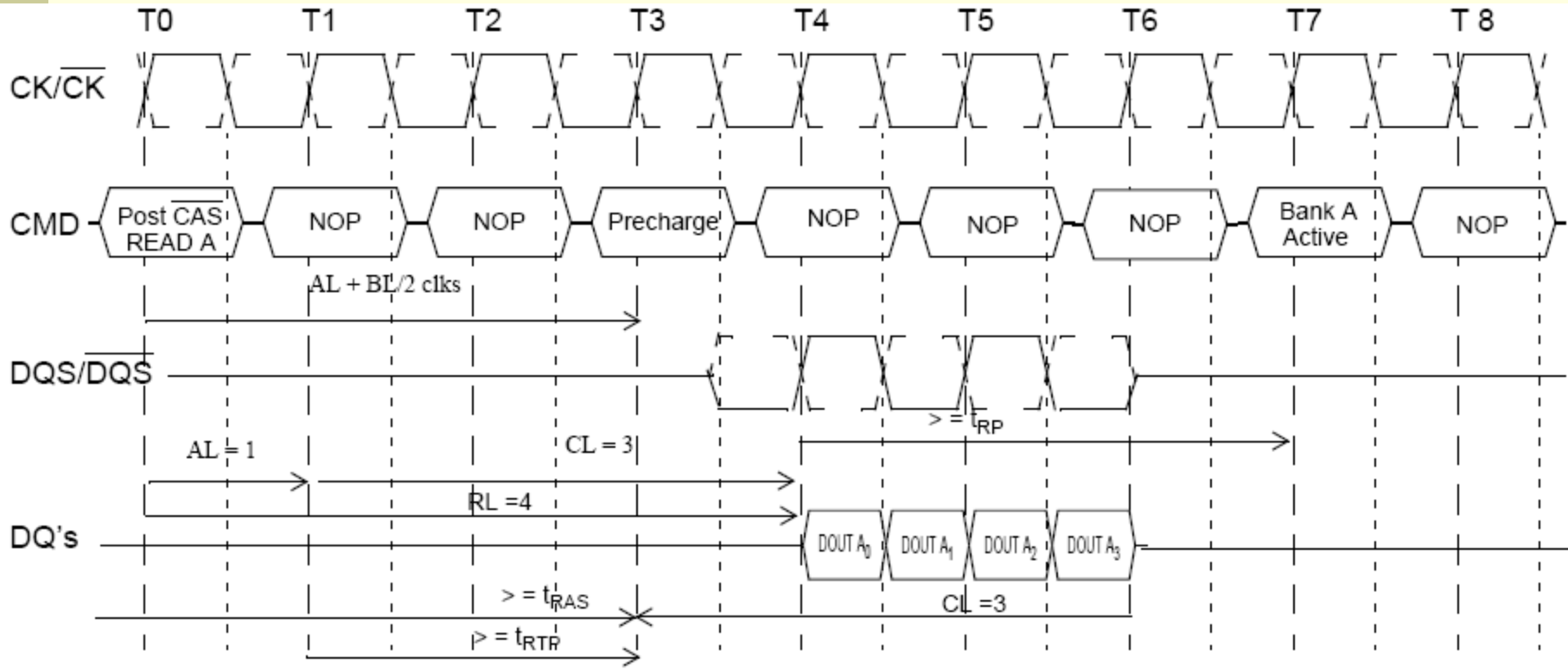


Figure 36 — Example 1: Burst read operation followed by precharge: RL = 4, AL = 1, CL = 3, BL = 4, t_{RTP} <= 2 clocks

Burst Write operation followed by Precharge

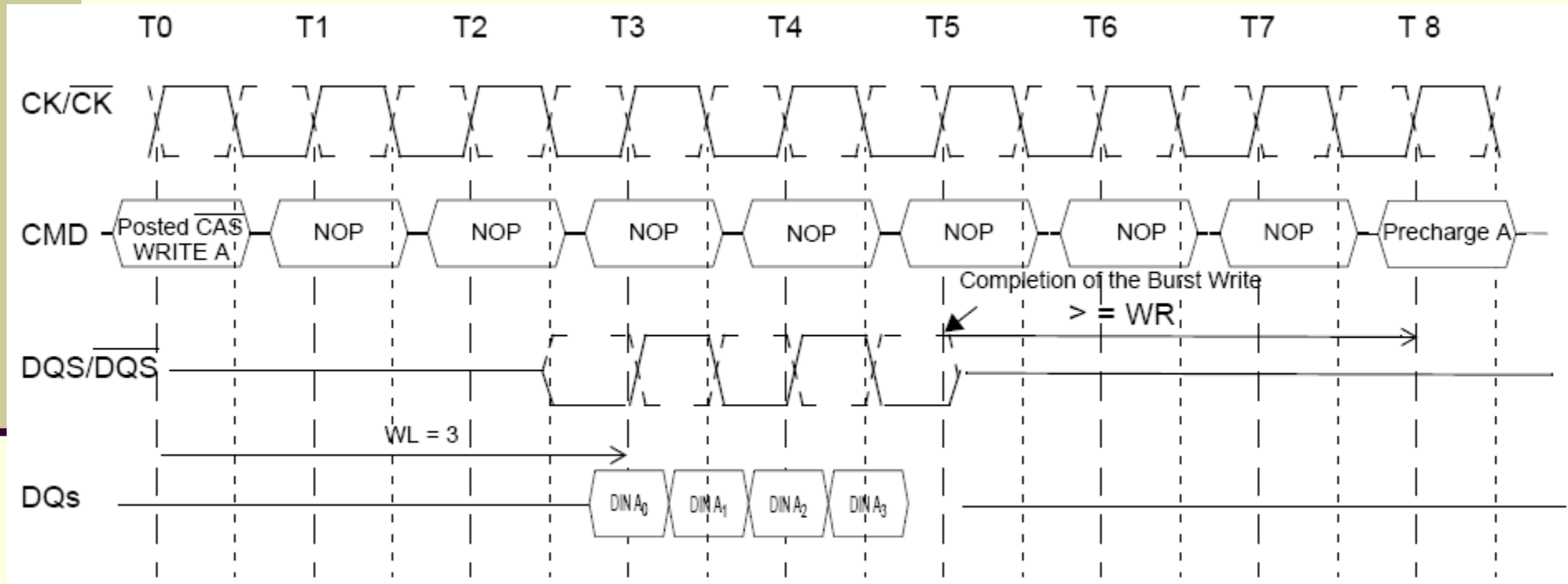


Figure 41 — Example 1: Burst write followed by precharge: WL = (RL-1) =3

Burst Read operation with Auto Precharge

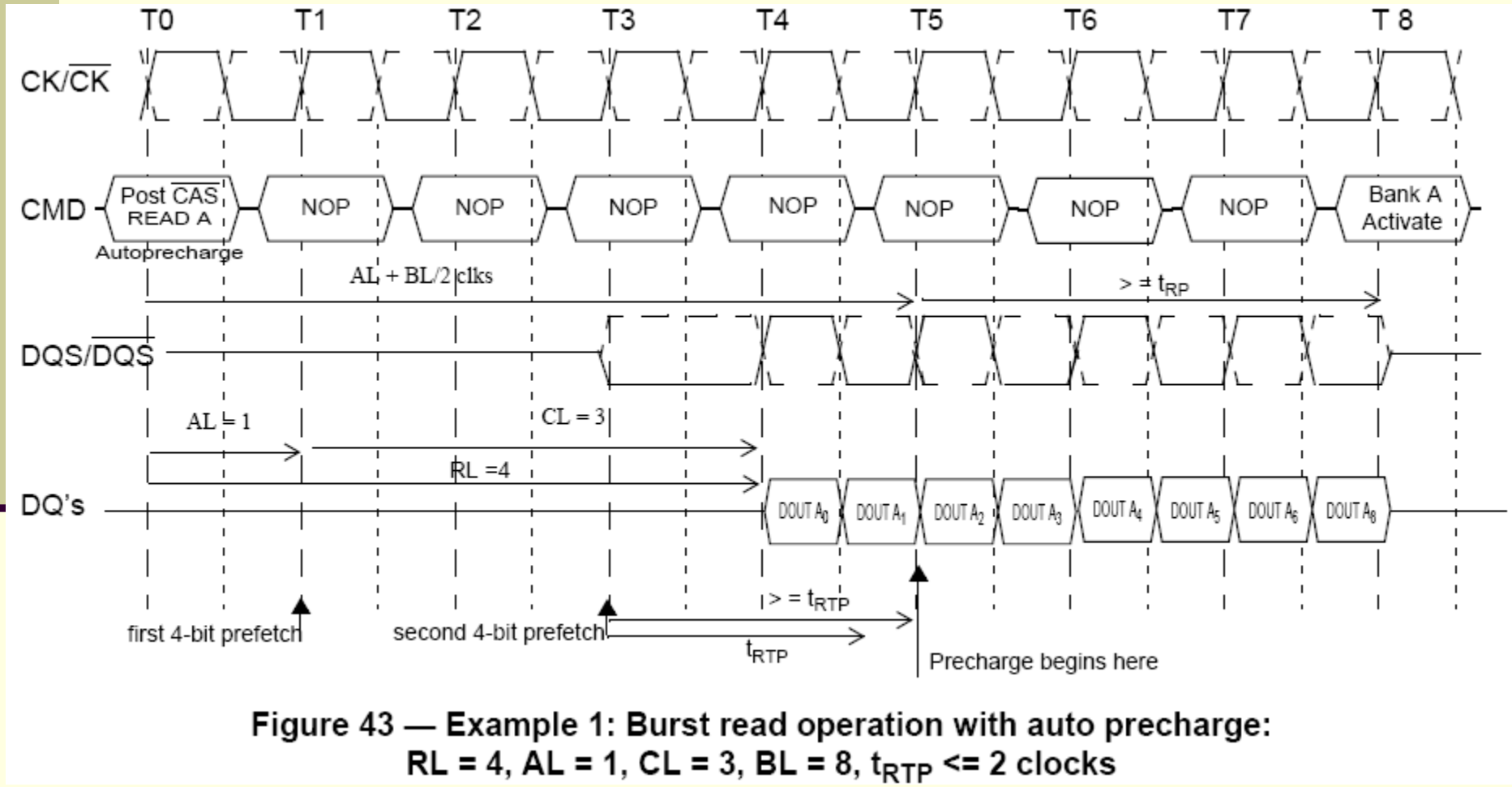


Figure 43 — Example 1: Burst read operation with auto precharge: RL = 4, AL = 1, CL = 3, BL = 8, t_{RTP} <= 2 clocks

Burst Write with Auto Precharge

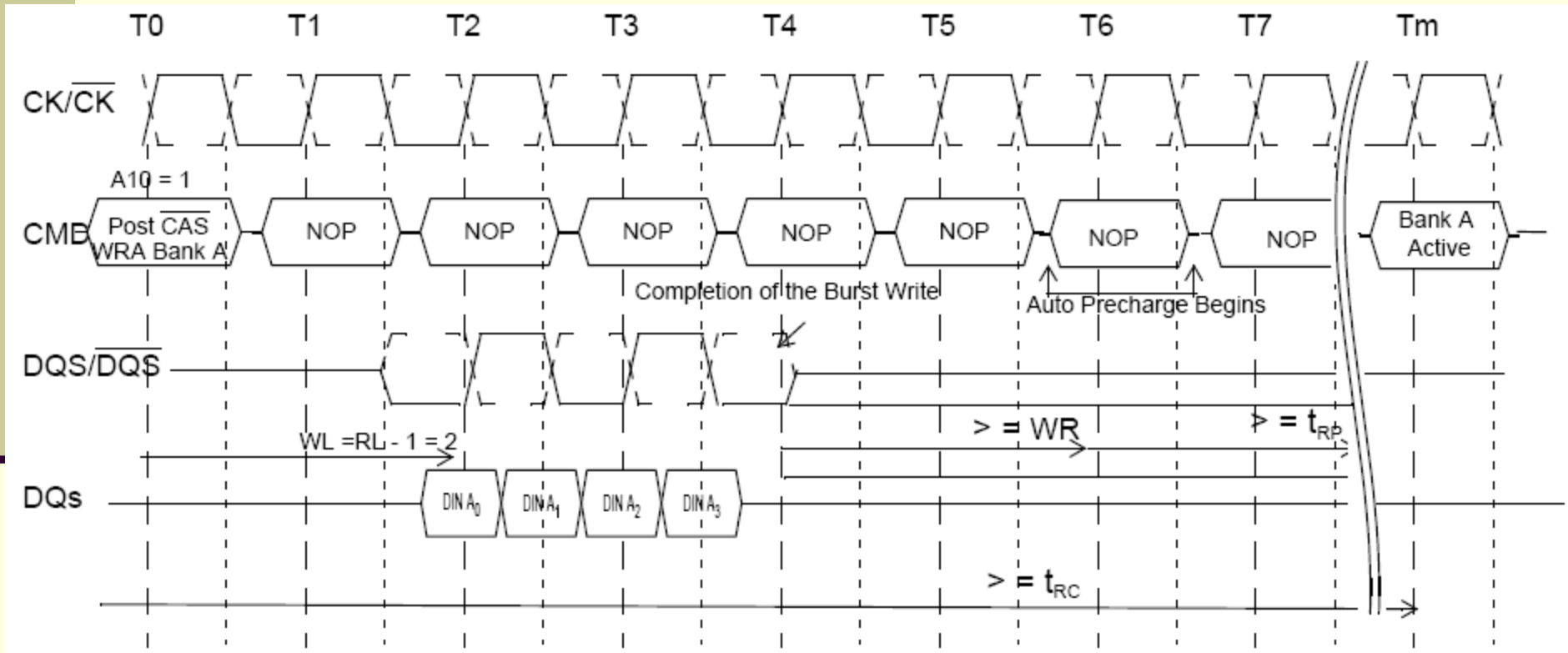
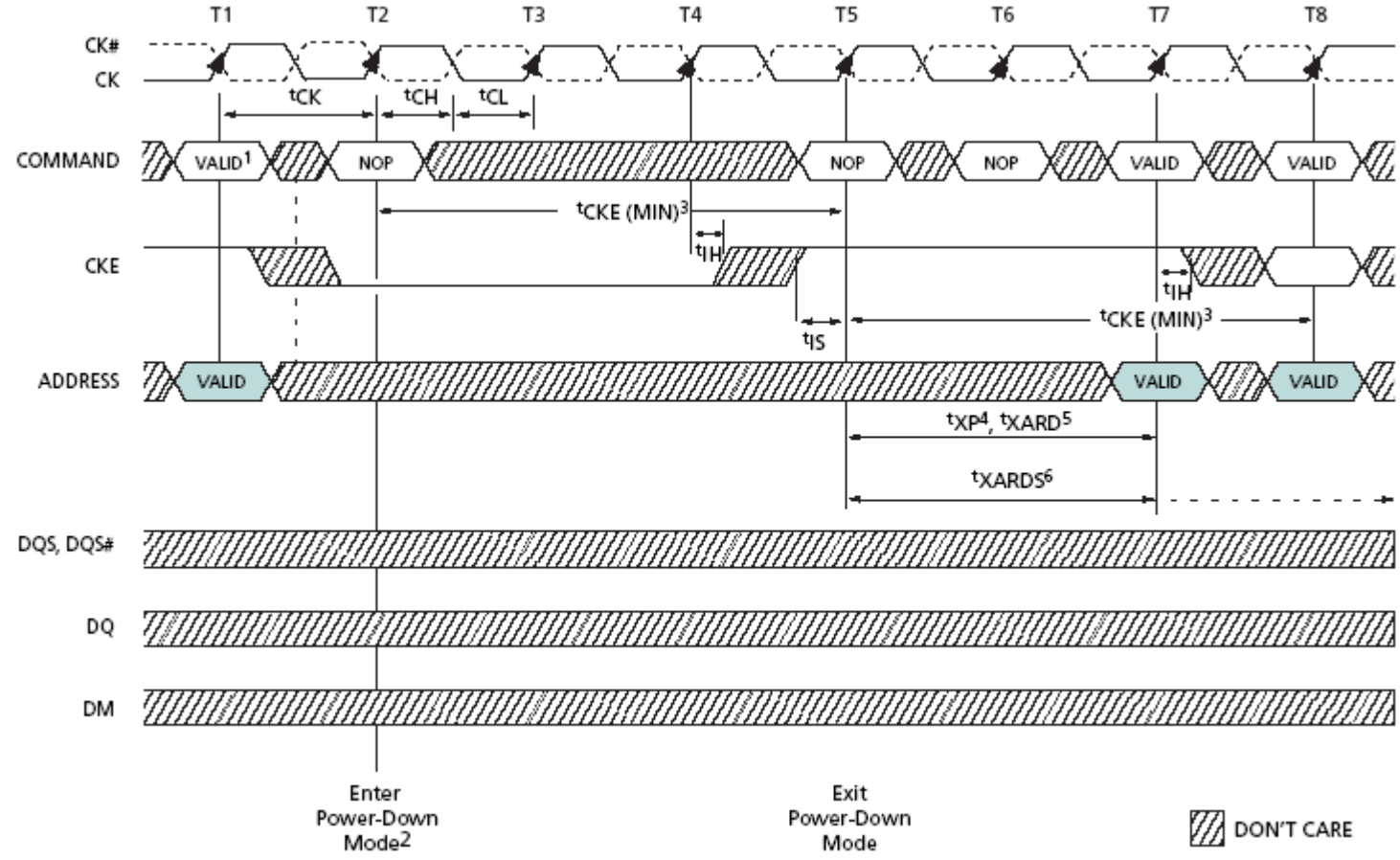


Figure 47 — Burst write with auto-precharge (tRC Limit): WL = 2, tWR =2, BL = 4, tRP=3

Power-Down Mode

- Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, CKE and DLL.



Command Truth Tables

Function	CKE		CS#	RAS#	CAS#	WE#	BA1 BA0	A12 A11	A10	A9–A0	Notes
	Previous Cycle	Current Cycle									
LOAD MODE	H	H	L	L	L	L	BA	OP Code			2
REFRESH	H	H	L	L	L	H	X	X	X	X	
SELF REFRESH Entry	H	L	L	L	L	H	X	X	X	X	
SELF REFRESH Exit	L	H	H	X	X	X	X	X	X	X	7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	2
All Banks PRECHARGE	H	H	L	L	H	L	X	X	H	X	
Bank Activate	H	H	L	L	H	H	BA	Row Address			
WRITE	H	H	L	H	L	L	BA	Column Address	L	Column Address	2, 3
WRITE with Auto Precharge	H	H	L	H	L	L	BA	Column Address	H	Column Address	2, 3
READ	H	H	L	H	L	H	BA	Column Address	L	Column Address	2, 3
READ with Auto Precharge	H	H	L	H	L	H	BA	Column Address	H	Column Address	2, 3
NO OPERATION	H	X	L	H	H	H	X	X	X	X	
Device DESELECT	H	X	H	X	X	X	X	X	X	X	
POWER-DOWN Entry	H	L	H	X	X	X	X	X	X	X	4
			L	H	H	H					
POWER-DOWN Exit	L	H	H	X	X	X	X	X	X	X	4
			L	H	H	H					