Rong-jian Liang

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AREA OF INTEREST: AI for EDA (Electronic Design Automation), EDA for AI

WORKING EXPERIENCE

NVIDIA **01/2022-now**
- Job Title: *Research Scientist*
  Conduct research on VLSI design automation, especially on AI for EDA

NXP Semiconductors **05/2021-08/2021**
- Job Title: *Digital Designer Intern*
  Developed a machine learning-based solution for fast estimation of dynamic voltage drop

IBM Thomas J. Watson Research Center **06/2020-08/2020**
- Job Title: *Research Intern*
  Developed an automatic multi-stage EDA flow parameter tuner

IBM Thomas J. Watson Research Center **05/2019-08/2019**
- Job Title: *Research Intern*
  Applied machine-learning techniques to design-rule-violation prediction at cell placement stage

SRC (Semiconductor Research Corporation) Research Scholars Program **01/2019/-12/2021**
- Job Title: *Research Scholar*
  Conducted research on applying machine learning to fast and high-fidelity design prediction

EDUCATION

Texas A&M University (US) **09/2018-12/2021**
- Major: Computer engineering Degree: ***Doctor*** of Philosophy

Tsinghua University (China) **09/2014-07/2017**
- Major: Control Science and Engineering Degree: ***Master*** of Engineering

Beihang University (China) **09/2010-07/2014**
- Major: Detection Guidance and Control Technology Degree: ***Bachelor*** of Engineering
- The Second Grade Scholarship for Academic Excellence in 2013

AWARD

ISPD 2021 Contest – Wafer Scale Physical Modeling **1st place**
- Description: Developed a compiler that maps a 3-D finite element model onto a 2-D grid of processing elements in the supercomputer Cerebras System CS-1. The objectives were to maximize performance and accuracy, while minimizing interconnect length. This involved partitioning and placement algorithms.

RESEARCH EXPERIENCE

Generative Machine Learning Framework for Scalable Buffering 02/2022-08/2022
- Developed a generative ML framework for buffering consisting of (1) a clustering-based generation process, (2) a transformer-based decision-making neural network and (3) a teach enforcing-based training scheme. To our best knowledge, it is the first successful attempt at generative ML-based buffering, a critical EDA problem.

Analytical Co-optimization of CNN Hardware and Dataflow 09/2021-12/2021
- Developed an analytical performance model for CNN hardware and dataflow in a matrix form;
- Proposed a two-stage analytical optimization scheme. At stage I, the problem is relaxed to continuous non-linear optimization, which is further cast as neural network training and solved through a deep learning toolkit with parallel computing and automatic gradient propagation. Stage II is to obtain an integer solution through parallel local search;
- To our best knowledge, it is the first deep learning toolkit-accelerated approach for CNN hardware and dataflow co-optimization and achieves better solutions than state-of-the-art methods with 6.2X speedup of optimization runtime.

DRV (Design Rule Violation) Density Prediction Considering the Non-determinism in Routing 03/2021-11/2021
- Modeled the stochastic spatial distribution of DRVs via a LGC (Log Gaussian Cox) process;
- Developed a deep learning framework – LGC-Net, which is a realization of LGC process on a deep neural architecture;
- To our best knowledge, it is the first attempt to combine deep learning and stochastic modelling for solving the non-determinism in VLSI design prediction.

Multi-Stage EDA Flow Tuner Exploiting Knowledge Transfer 06/2020-05/2021
- Developed a cooperative co-evolutionary-based framework for multi-stage EDA flow parameter tuning. The high-dimensional flow tuning problem was decomposed into a set of more tractable sub-problems: parameter tuning for each design stage, and the tuning of multiple design stages were orchestrated in an interactive and cooperative manner to achieve the best final quality of results;
- Mathematically defined and automatically extracted three types of parameter knowledge, i.e., parameter importance,

parameter bias and parameter interaction, and transferred the knowledge to accelerate the tuning on new designs;
- Proposed a novel flow jump-start technique, which actively exploits reusable synthesis results, and a flow early-stop technique, which employs a branch-and-bound strategy to reduce runtime.

Routing-free Crosstalk Prediction 10/2019-05/2020
- Extracted net physical information, electrical and logical features, which affect crosstalk-induced noise and delay;
- Developed machine learning-based models to identify crosstalk-critical nets at the cell placement stage.

DRC (Design Rule Checking) Hotspot Prediction at Placement Stage 01/2019-09/2019
- Formulated DRC hotspot prediction, i.e., to tell whether or not there exists DRV in each routing region, as an image segmentation-based classification problem;
- Proposed to extract high-resolution pin configuration images, which capture pin shape patterns, as well as low resolution tile-based feature maps, which capture routing congestion patterns, at placement stage as input to predict DRC hotspot.
- Proposed a customized convolutional neural network, J-Net, to address mixed-resolution input and output.

PUBLICATIONS

Books and Book Chapters:
- **Liang, R.,** Xie, Z., Barboza, E. C., & Hu, J. "Net-Based Machine Learning-Aided Approaches for Timing and Crosstalk Prediction" in Machine Learning Applications in Electronic Design Automation, pp.63-84, Springer, 2022.
- Xie, Z., Pan, J., Chang, C. C., **Liang, R**., Barboza, E. C., & Chen, Y. "Net-Based Machine Learning-Aided Approaches for Timing and Crosstalk Prediction" in Machine Learning Applications in Electronic Design Automation, pp.35-61, Springer, 2022.

Journal Articles:
- Xie, Z., **Liang, R**., Xu, X., Hu, J., Chang C., Pan J. and Chen, Y., "Pre-Placement Net Length and Timing Estimation by Customized Graph Neural Network". IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2022.
- **Liang, R.**, et al. "Design Rule Violation Prediction at Sub-10nmProcess Nodes Using Customized Convolutional Networks." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2021.
- Chen, Z., Wang, Z., **Liang, R.**, Liang, B., & Zhang, T. "Virtual-joint based motion similarity criteria for human–robot kinematics mapping". Robotics and Autonomous Systems, 2020.
- Wang, L., Zhang, T., & **Liang, R.** "A small-sized locating message for cooperative localization under communication constraint". International Journal of Advanced Robotic Systems, 2016.

Conference Papers:
- **Liang, R.**, et al. "CircuitOps: An ML Infrastructure Enabling Generative AI for VLSI Circuit Optimization." Proceedings of International Conference on Computer-Aided Design (ICCAD), 2023 (To appear)
- **Liang, R.**, et al. "Late Breaking Results: Test Selection for RTL Coverage by Unsupervised Learning from Fast Functional Simulation." Proceedings of Design Automation Conference (DAC), 2023
- **Liang, R.**, et al. "BufFormer: A Generative ML Framework for Scalable Buffering." Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), 2023.
- **Liang, R.**, et al. "Deep Learning Toolkit-Accelerated Analytical Co-optimization of CNN Hardware and Dataflow." Proceedings of International Conference on Computer-Aided Design (ICCAD), 2022.
- **Liang, R.**, et al. "A Stochastic Approach to Handle Non-Determinism in Deep Learning-Based Design Rule Violation Predictions." Proceedings of International Conference on Computer-Aided Design (ICCAD), 2022.
- Lin, Y., **Liang, R**., Li, Y., Hu, H., & Hu, J., "Mapping Large Scale Finite Element Computing onto Wafer-Scale Engines". Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), 2022
- **Liang, R.**, et al. "A Multi-Stage EDA Flow Tuner Exploiting Parameter Knowledge Transfer." Proceedings of International Conference on Computer-Aided Design (ICCAD), 2021.
- Xie, Z., **Liang, R**., Xu, X., Hu, J., Duan, Y. and Chen, Y., "Net^2: A Graph Attention Network Method Customized for Pre-Placement Net Length Estimation". Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), 2021.
- **Liang, R**., et al. "Routing-free Crosstalk Prediction." Proceedings of International Conference on Computer-Aided Design (ICCAD), 2020.
- **Liang, R**., et al. "DRC Hotspot Prediction at Sub-10nm Process Nodes Using Customized Convolutional Network." Proceedings of International Symposium on Physical Design (ISPD), 2020.
- **Liang, R**., et al. "A unified predictive display scheme for teleoperation systems with multi-time-delay multi-rate measurements and missing data". Proceedings of Chinese Control Conference (CCC), 2017.

Patents:
- **Liang, R**., et al, "DRC (Design Rule Check) Heatmap Prediction Considering the Non-determinism in Routing." US patent filed
- **Liang, R**., et al, "BufFormer: A Generative ML Framework for Buffering." US patent filed
- GJ Nam, J Jung, AY Lvov, LN Reddy H Xiang, **R Liang**, "Multi-stage electronic design automation parameter tunning." US patent filed

SERVICES

ISPD'24 TPC member, reviewer for TCAD, TODAES, IFAC WC'23 and ISCAS'22