vcs常用的命令选项如下：  
-cm line|cond|fsm|tgl|obc|path 　设定coverage的方式  
+define+macro=value+ 　　　　　预编译宏定义  
-f filename 　　　　　　　　　　　 RTL文件列表  
+incdir+directory+ 　　　　　　　 添加include 文件夹  
-I　　　　　　　　　　　　　　　　 进入交互界面  
-l 　　　　　　　　　　　　　　　　logfile文件名  
-P pli.tab　　　　　　　　　　　　  定义PLI的列表(Tab)文件  
+v2k 　　　　　　　　　　　　　　 使用推荐的标准  
-y 　　　　　　　　　　　　　　　  定义verilog的库  
-notice 　　　　　　　　　　　　　 显示详尽的诊断信息  
-o 　　　　　　　　　　　　　　　  指定输出的可执行文件的名字,缺省是simv  
+ nospecify 　　　　　　　　　　　不对SPECIFY 模块进行时序检查和路径延时计算  
+ notimingcheck 　　　　　　　　  不进行时序检查；但是还是把path延时加入仿真中  
   
Summary of vcs compile options:  
-ASFLAGS 　　　　"opts" pass 'opts' to the assembler  
-B 　　　　　　　　generate long call instructions in native assembly code (HP only)  
-CC 　　　　　　　"opts" pass 'opts' to C compiler  
-CFLAGS 　　　　　"opts" pass 'opts' to C compiler  
-LDFLAGS 　　　　"opts" pass 'opts' to C compiler on load line only  
-I 　　　　　　　　enable interactive/postprocessing debugging capabilities  
-ID 　　　　 　　　get host identification information  
-M 　　　　 　　　 enable incremental compilation (see manual)  
-Mupdate 　　 　　enable incremental compilation and keep the Makefile up-to-date  
-Marchive[=N] 　　create intermediate libs to reduce link line length; N objs per lib  
-P plitab 　　　　　compiles user-defined pli definition table 'plitab'  
-PP 　　　　　　 　　enable optimizer postprocessing capabilities for vcd+  
-R 　　　　　　 　　after compilation, run simulation executable  
-RI 　　　　　　　　after compilation, run simulation under xvcs (Implies -I)  
-RIG 　　　　　　　　run simulation under xvcs without compiling (executable has to exist)  
-RPP 　　　　　　　　run xvcs in postprocessing mode (requires file created by vcdpluson)  
-V[t] 　　　　  　　　verbose mode; with 't', include time information  
-as 　　　　　　　　　foo use foo as the assembler  
-cc 　　　　　　　　　foo use foo as the C compiler  
-cpp 　　　　　　　　foo use foo as the C++ compiler  
-e 　　 specify the name of your main() routine. (see manual section 7-11 for more details).  
-f file 　　　　　　　　 reads 'file' for other options  
-gen\_c 　　　　 　　 　generate C code (for HP and Sun, default is -gen\_obj)  
-gen\_asm 　　　　　　generate native assembly code (HP and Sun only)  
-gen\_obj 　　　　　　 generate native object code (HP and Sun only)  
-ld 　　　　　　　　　　foo use foo as the linker. (refer vcs manual for compatibility with -cpp option)  
-line 　　　　　　　　 　enable single-stepping/breakpoints for source level debugging  
-lmc-swift 　　　　　　 include lmc swift interface  
-lmc-hm 　　　　　　　include lmc hardware modeler interface  
-vera 　　 　　　　　　 add VERA 4.5+ libraries  
-vera\_dbind 　　　　　add VERA 4.5+ libraries for dynamic binding  
-location 　　　　　　 display full pathname to vcs installation for this platform.  
-vhdlobj 　　 generate a vhdl obj for simulating in a vhdl design  
-mixedhdl 　　　　　　 include MixedHDL-1.0 interface  
-mhdl 　　　　　　　　 include MixedHDL-2.0 interface and library  
-q 　　　　　　　　　　 quiet mode  
-platform. 　　　　　　 display name of vcs installation subdirectory for this platform.  
-syslib 　　　　　　　　'libs' specify system libraries (placed last on the link line) eg -lm  
-o 　　　　　　　　　　exec name the executable simulation model 'exec' (default is 'simv')  
-u 　　　　　　　　　　 treat all non text string characters as uppercase  
-v file 　　　　　　　　 search for unresolved module references in 'file'  
-y libdir 　　　　　　　　　search for unresolved module references in directory 'libdir'  
+acc 　　　　　　　　　　enable pli applications to use acc routines (see manual)  
+ad 　　　　　　　　 　　 include anlog simulation interface and library  
+adfmi="files" 　　　　　ADFMI support for vcs-ace  
+cliedit 　　　　　　 　　 enable command line edit/recall (see doc/readline.ps)  
+cli 　　　　　　　　 　　 enable command line interactive debugging (see manual)  
+cmod 　　　　　　 　　 Enabling cmodule feature  
+cmodext+cmodext 　　 Changing cmodule extension to cmodext  
+cmodincdir+cmoddir 　　 Cmodule Include directory  
+cmoddefine+macro 　　 define cmodule source 'macro' in the form. of XX=YY  
+define+macro 　　　　 　define hdl source 'macro' to have value "macro"  
+plusarg\_save 　　　　 　hardwire the plusargs, which follow this flag, into simv  
+plusarg\_ignore 　　　　 turn off +plusarg\_save  
+prof 　　　　　　　　 　tells vcs to profile the the design and generate vcs.prof file  
+race 　　　　　　　　 tells vcs to generate a report of all race conditions and write this report in the race.out file  
+rad+1 　　　　　　 　　 enable level 1 radiant optimizations (See Release Notes)  
+rad+2 　　　　　　 　　 enable level 2 radiant optimizations (See Release Notes)  
+libext+lext 　　　　 　　 use extension 'lext' when searching library directorys  
+librescan 　　　　 　　 search from beginning of library list for all undefined mods  
+incdir+idir 　　　　 　　 for `include files, search directory 'idir'  
+nospecify 　　　　 　　 suppress path delays and timing checks  
+notimingchecks 　　 　suppress timing checks  
+optconfigfile+foo 　　use 'foo' as the optimization config file (See Release Notes)  
+vcsd 　　　　　　　　 enable the VCS Direct sim kernel interface  
-cmhelp 　　　　　　 　enable CoverMeter help  
-cm 　　　　　　　　　enable VCS to first run cmSource to instrument the Verilog source files on the command line  
-cm\_all 　　　　 enable VCS to link CoverMeter into the VCS executable in a way that enables all coverages

-cm\_lineonly　　enable VCS to link CoverMeter into the VCS executable in a way that only enables line coverage

### **vcs常用的命令选项**

vcs常用的命令选项:  
  -cm line|cond|fsm|tgl|obc|path     设定coverage的方式  
   
  +define+macro=value+       预编译宏定义

  -f filename             RTL文件列表

  +incdir+directory+         添加include 文件夹

  -I                 进入交互界面

  -l                 logfile文件名

  -P pli.tab             定义PLI的列表(Tab)文件

  +v2k                 使用推荐的标准

  -y                 定义verilog的库

  -notice               显示详尽的诊断信息

  -o                 指定输出的可执行文件的名字,缺省是sim.v

  + nospecify 不对 SPECIFY 模块进行时序检查和路径延时计算

  + notimingcheck 不进行时序检查；但是还是把path延时加入仿真中

Summary of vcs compile options:  
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-ASFLAGS "opts"    pass 'opts' to the assembler  
-B                 generate long call instructions in native assembly code (HP only)  
-CC "opts"         pass 'opts' to C compiler  
-CFLAGS "opts"     pass 'opts' to C compiler  
-LDFLAGS "opts"    pass 'opts' to C compiler on load line only  
-I                 enable interactive/postprocessing debugging capabilities  
-ID                get host identification information  
-M                 enable incremental compilation (see manual)  
-Mupdate           enable incremental compilation and keep the Makefile up-to-date  
-Marchive[=N]      create intermediate libs to reduce link line length; N objs per lib  
-P plitab          compiles user-defined pli definition table 'plitab'  
-PP                enable optimizer postprocessing capabilities for vcd+  
-R                 after compilation, run simulation executable  
-RI                after compilation, run simulation under xvcs (Implies -I)  
-RIG               run simulation under xvcs without compiling (executable has to exist)  
-RPP               run xvcs in postprocessing mode (requires file created by vcdpluson)  
-V[t]              verbose mode; with 't', include time information  
-as foo            use foo as the assembler  
-cc foo            use foo as the C compiler  
-cpp foo           use foo as the C++ compiler  
-e <new\_name>      specify the name of your main() routine.  
                   (see manual section 7-11 for more details).  
-f file            reads 'file' for other options  
-gen\_c             generate C code (for HP and Sun, default is -gen\_obj)  
-gen\_asm           generate native assembly code (HP and Sun only)  
-gen\_obj           generate native object code (HP and Sun only)

-ld foo            use foo as the linker. (refer vcs manual for compatibility with -cpp option)  
-line              enable single-stepping/breakpoints for source level debugging  
-lmc-swift         include lmc swift interface  
-lmc-hm            include lmc hardware modeler interface

-vera              add VERA 4.5+ libraries  
-vera\_dbind        add VERA 4.5+ libraries for dynamic binding  
-location          display full pathname to vcs installation for this platform  
-vhdlobj <name>    generate a vhdl obj for simulating in a vhdl design  
-mixedhdl          include MixedHDL-1.0 interface  
-mhdl              include MixedHDL-2.0 interface and library  
-q                 quiet mode  
-platform          display name of vcs installation subdirectory for this platform  
-syslib 'libs'     specify system libraries (placed last on the link line) eg -lm  
-o exec            name the executable simulation model 'exec' (default is 'simv')  
-u                 treat all non text string characters as uppercase  
-v file            search for unresolved module references in 'file'  
-y libdir          search for unresolved module references in directory 'libdir'  
+acc               enable pli applications to use acc routines (see manual)  
+ad                include anlog simulation interface and library  
+adfmi="files"     ADFMI support for vcs-ace  
+cliedit           enable command line edit/recall (see doc/readline.ps)  
+cli               enable command line interactive debugging (see manual)  
+cmod              Enabling cmodule feature  
+cmodext+cmodext   Changing cmodule extension to cmodext  
+cmodincdir+cmoddir   Cmodule Include directory  
+cmoddefine+macro  define cmodule source 'macro' in the form of XX=YY  
+define+macro      define hdl source 'macro' to have value "macro"  
+plusarg\_save      hardwire the plusargs, which follow this flag, into simv  
+plusarg\_ignore    turn off +plusarg\_save  
+prof              tells vcs to profile the the design and generate vcs.prof file

+race              tells vcs to generate a report of all race conditions during simulation  
                   and write this report in the race.out file  
+rad+1             enable level 1 radiant optimizations (See Release Notes)  
+rad+2             enable level 2 radiant optimizations (See Release Notes)  
+libext+lext       use extension 'lext' when searching library directorys  
+librescan         search from beginning of library list for all undefined mods  
+incdir+idir       for `include files, search directory 'idir'  
+nospecify         suppress path delays and timing checks  
+notimingchecks    suppress timing checks  
+optconfigfile+foo use 'foo' as the optimization config file (See Release Notes)  
+vcsd              enable the VCS Direct sim kernel interface  
   
-cmhelp            enable CoverMeter help. CoverMeter should be installed  
                   and environment variable CM\_HOME should be set.  
-cm                enable VCS to first run cmSource to instrument the  
                   Verilog source files on the command line, and then to  
                   compile the instrumented source files  
-cm\_all            enable VCS to link CoverMeter into the VCS executable in a  way that enables line, condition, and FSM coverage and establishes the direct link. Enabling all types of coverage and the direct link is the default condition when you  include the -cm option so you can omit this option  
-cm\_lineonly       enable VCS to link CoverMeter into the VCS executable in a way that only enables line coverage when it also establishes the direct link. Use this option for faster simulation and when you only need line coverage