Lab 3 – Circuit Equivalence Checking

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For two combination circuits, we identify pairs of corresponding outputs then XOR them. The XOR gate outputs are ORed to produce one single output. If any pair of the outputs is not equivalent, the XOR output = 1 and produce the output of the OR gate = 1. Otherwise, if the final output = 0, then the two circuits are not equivalent. If the result circuit is satisfiable, the two circuits are not equivalent. Otherwise, they are equivalent.

First, I add the "Lab3" module which has been provided, make a true table and simply the Boolean equation by using Kmap. Then I implement this simplified Boolean formula with "Lab3_eq" module. Next, I connect these two modules "Lab3" and "Lab3_eq" in "top" module to check whether the "top" module is satisfiable or not. XORing "Out1" and "Out2" will give "eq" = 0 meaning that the formula is not satisfiable, so the circuits are equivalent.

The three testbenches, "Lab3_tb", "Lab3_eq_tb" and "top_tb" will test all 32 possible combinations of inputs A, B, C, D, E and show the value of the outputs "Out1", "Out2", and "eq". Since, the two circuits are equivalent, values of "eq" in any cases will always equal to 0.

Truth Table

	A	**B**	**C**	**D**	**E**	**Out**
0	0	0	0	0	0	1

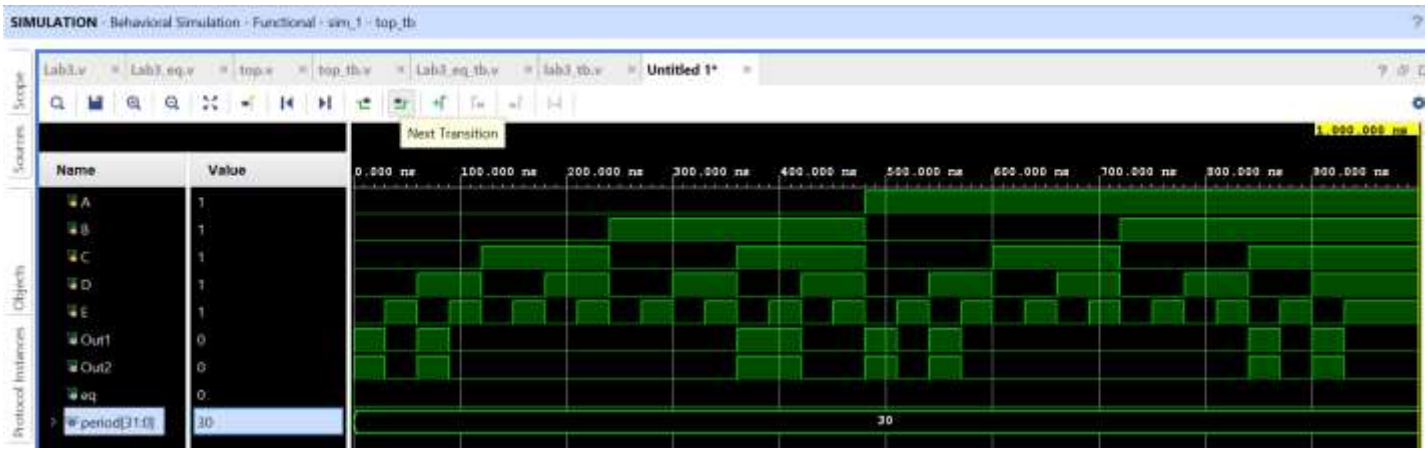
1	0	0	0	0	1	0
2	0	0	0	1	0	1
3	0	0	0	1	1	0
4	0	0	1	0	0	0
5	0	0	1	0	1	0
6	0	0	1	1	0	0
7	0	0	1	1	1	0
8	0	1	0	0	0	0
9	0	1	0	0	1	0
10	0	1	0	1	0	0
11	0	1	0	1	1	0
12	0	1	1	0	0	1
13	0	1	1	0	1	1
14	0	1	1	1	0	0
15	0	1	1	1	1	0
16	1	0	0	0	0	1
17	1	0	0	0	1	0
18	1	0	0	1	0	1
19	1	0	0	1	1	0
20	1	0	1	0	0	0
21	1	0	1	0	1	0
22	1	0	1	1	0	0
23	1	0	1	1	1	0
24	1	1	0	0	0	0
25	1	1	0	0	1	0
26	1	1	0	1	0	0
27	1	1	0	1	1	0
28	1	1	1	0	0	1
29	1	1	1	0	1	0
30	1	1	1	1	0	1

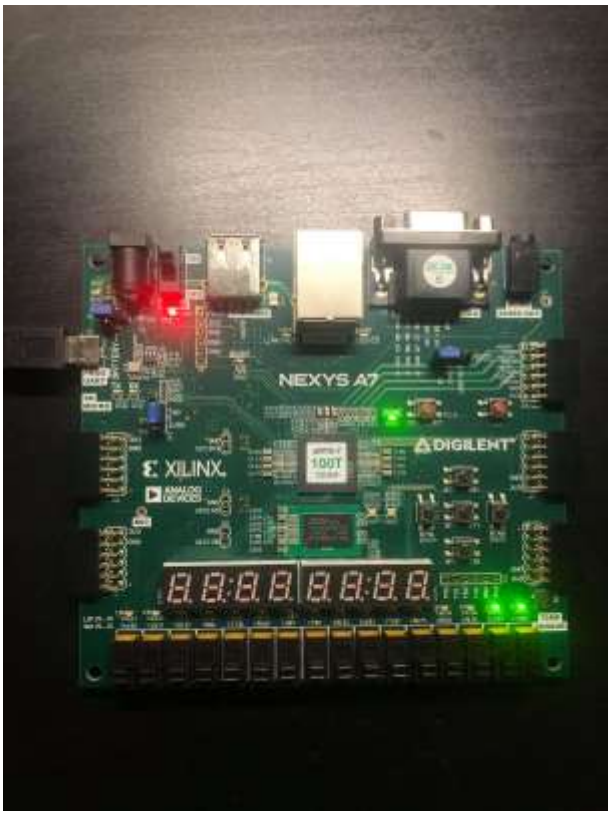
31	1	1	1	1	1	0

K-Map

Abc/de	**00**	**01**	**11**	**10**
000	1	0	0	1
001	0	0	0	0
011	1	1	0	0
010	0	0	0	0
100	1	0	0	1
101	0	0	0	0
111	1	0	0	1
110	0	0	0	0

Out = B'C'E' + A'BCD' + ABCE'

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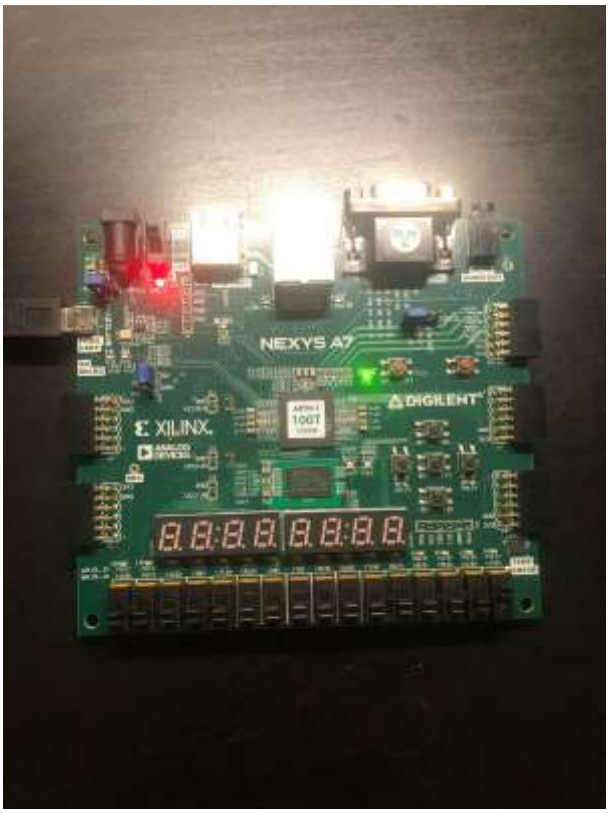
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