Design and Implementation of Digital Clock with Timer and Stopwatch on Xilinx FPGA

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***Abstract*— The goal of this project is to implement a configurable digital clock on an FPGA. The main components of this project will be a Verilog module that will output to the board to show the time in either military or standard format and a seven-segment display which is built into the FPGA Nexys A7 100T will show the time on the board. Using the features of the FPGA, the clock will switch from standard to military time or vice versa, flash LEDs, set the time, and have stopwatch and timer functions.**

Keywords*— *Digital Clock; Standard Time; Military Time; Stopwatch; Timer

I. Introduction

A digital clock uses numerals and other symbols to display the time in hours: minutes: seconds. The field-programmable gate array (FPGA) has a seven-segment display implementation that will be used to output the digital clock [1]. The clock will show 00:00:00 as soon as the FPGA is turned on.

Applying the components of the FPGA to the clock will allow it to have more features. Such features would include using a switch to change the time from standard to military or vice versa, using a button and the on-board switches to set a desired time on the board, a blue LED that will flash every hour, a timer function that will flash red LED when the time reaches 0, and a stopwatch function.

The on-board clock of the FPGA will generate the timing signals needed to increment or decrement the time shown on the seven-segment display. A 100 MHz clock is used to generate each real-time second [2].

II. Design Overview

The system design mainly performs three functions: digital clock, stopwatch and timer. The functions are implemented using counter, stopwatch, timer and display function.

The design of this digital clock will allow us to display total hours, minutes and seconds with a frequency of 100MHz [1].

Counter module includes seconds, minutes, and hours. The counter is updated by the internal clock signal. Internal clock signal is generated upon completion of each counter and it will be updated by the preceding counter.

The Stopwatch module displays for up to 24 hours. It has distinct clarity and a stop switch [3]. Similar to Stopwatch, the Timer module can also display up to 24 hours and has its input to start the timer.

Display module displays seven segment common anode. A switch is to select between Counter, Stopwatch and Timer modules. Figure 1 shows the module view of the design where four outputs of counter module, timer module and stopwatch modules are multiplexed. Switch offers selection of desired output on a seven segment display between counter, stopwatch and timer.

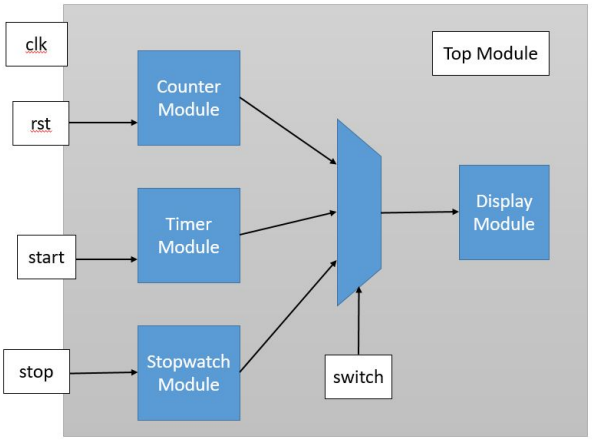

Fig.1. Module view of design.

Beside those features, the design digital clock will be able to change the time from standard to military or vice versa, set the time and make the blue LED flashing every new hour for one minute (one second on and one second off) and flashing red whenever the timer reaches zero.

III. Implementation

A. Software Implementation

Software implementation and prototype verification of digital clock using FPGA are Vivado 16.2 design tool and Verilog HDL. With Vivado 16.2, we can enhance design implementation with place and route tools that optimizes for multiple and concurrent design metrics. Verilog HDL is used to describe hardware design and document electronic systems. It allows us to describe the design at different levels of abstractions within a design, such as Behavior, RTL, Gate, and Switch level. Verilog modules are basic building blocks in hierarchy [1].

One second signal is generated using the global clock, and this second lock will be used to generate the timing signals [2]. There are a total of six digits including two digits of seconds (second and second1), two digits of

minutes (minute2 and minute1), and two digits of hours (hour2 and hour1). When second1 is 9 and second2 is 5, then second2 and second1 values are made to zero, and so minute1 is incremented. If minute2 is 5 and minute1 is 9, and then minute2 and minute1 values are made to zero, and hour1 is incremented. If hour2 is 2 and hour1 is 4, then hour2 and hour1 are made to zero, then the count will continue. The flow chart for the digital clock has shown in Figure 2.

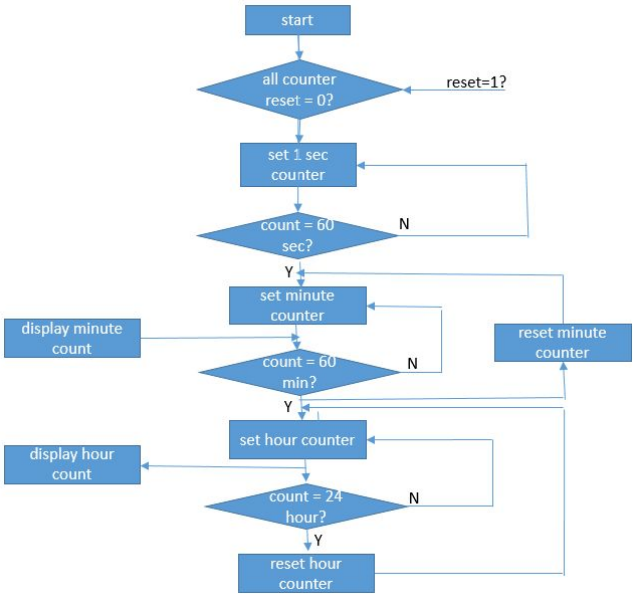

Fig.2. Design flow of digital clock.

Clock format allows us to switch from 24-hour military time to 12-hour American standard time by enabling the input, or vice versa [4].

Stopwatch can only be displayed in standard format. Stopwatch function can count up from 0 to 24 hours. One second pulse from the counter module is derived and fed as an input to the initial stopwatch. It starts counting as the switch is activated, and counts up 24 hours [3].

Also, timers can only be displayed in standard format. When the switch for timer is activated, a specified time should be set, and the timer function will count down from the setting time to zero.

Display module is performing counting. Six general seven segment display anode is used for display purposes. For every millisecond, each screen will be refreshed by a multiplexer.

B. Hardware Implementation

FPGA board offers a wide range of features making it suitable for use in laboratory environments, to perform various designs and development of digital systems. The Artix-7 FPGA is optimized for high performance logic, provides more capacity, high performance and more logic resources compared to earlier designs [1].

As soon as the FPGA board is switched on, the clock will start, and the FPGA and on board clock will generate the timing signals [1]. The clock time, stopwatch and timer can be set using the dip switches and push buttons on the board. The digital operations include counting, incrementing, decrementing and comparing. We can use the button to set the specified minutes and hours as desired, then adjust the digits by switches.

Nexys4 board contains two conventional six-digit anode seven-part LED displays, arranged to function like a single eight-digit display. Each of the eight-digits is made up of seven piece segments with an LED installed in each section [6]. The circuit controls the anode flags and compares the cathode examples of every digit in a continuous, repetitive process at a refresh rate faster than a human's eye can discern. Each digit only lights up for an eight of the time and the eye cannot see the obscured digit before it lights up again, the displayed digit continuously lights up [1].

Initially, a second clock is generated by using a global clock and according to that clock, a second pulse is increased and when it reaches 59, it will be set to zero, and a minute pulse is incremented. And similarity, the hour pulse will be increased when it reaches 60 minutes. The time can be set using load switch and set_H1, set_H0, set_M1, set_M0. With load enabled, we can set the current time, stopwatch and timer. When the clock_format switch is set, the time will be displayed in military time, otherwise, it will show in standard time. To access the features of design, a separate switch is assigned.

There are four buttons used to control the feature of a digital clock. Reset button is used to set the time to the input hour and minute and the second to 00. Load_counter button should be held to increase the number of the specified digit of the clock. Stop button is provided to stop the stopwatch, and the start button is to start the timer.

IV. RESULT

The proposed digital clock design displays the time on the seven segment display of the FPGA board. The functional blocks are designed using Verilog Hardware Description language. The digital clock is able to display minutes and 12 or 24 hours with timer and stopwatch displaying up to 24 hours, they all functioned according to the design, the results are exactly as we expected.

Figure 3 is a picture of the working board showing the real time on board is 04:00:36, and blue LED is on when the new hour is updated (the blue LED is blinking until the seconds count up to 59).

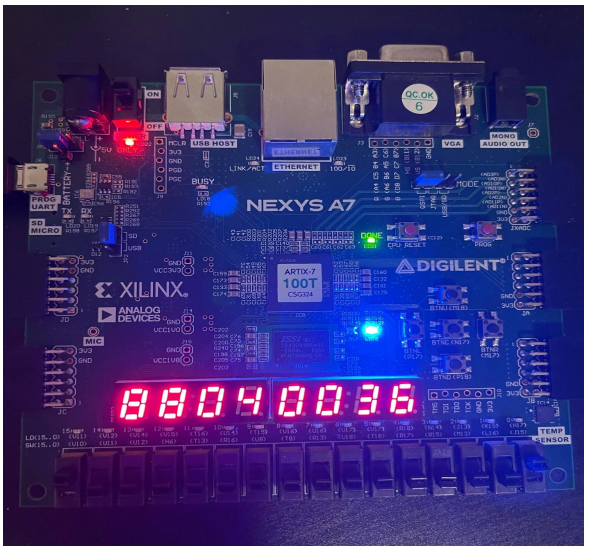

Fig3. Development board when every new hour is updated.

As shown in figure 4 below, when the timer is set to a specified time and counts down to zero, a red LED will blink every one second. It will not stop blinking until the timer is turned off.

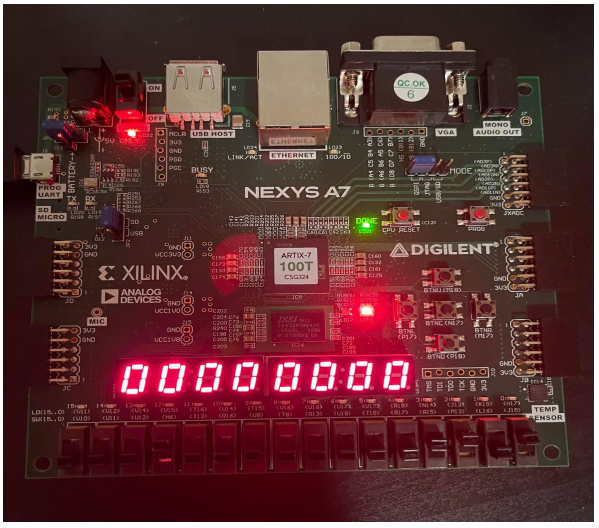

Fig.4. Development board when timer reaches zero.

The multiplexers are used with a common select switch for selection of display. Figure 5 shows the block diagram of the top module - Digital Clock.

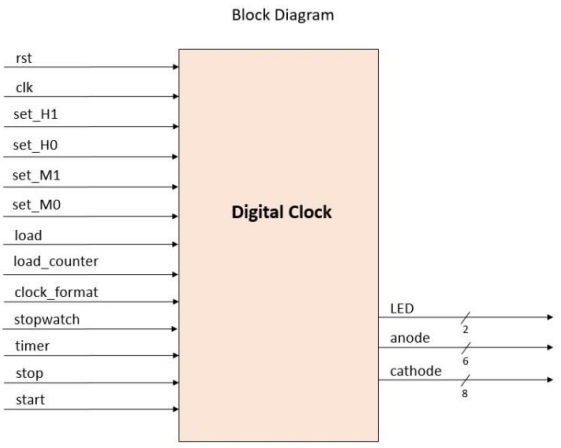

Fig.5. Block diagram of the Digital Clock.

V. Conclusion

This project helps develop a better understanding of digital systems. The design of a digital clock can be expanded further if adding more features to it, such as adding date, month and year calendar. Counter with possible stop and go functions can be implemented in substantial quantities to project a form of time keeping.

There were many obstacles we encountered, such as implementing input and output timing signals based on system clock frequency, and determining the order of the overall design stages and implementation of additional features. The most challenging obstacle for us in this project was the Timer feature. The code for the timer is a lot more complex than we originally thought because we had to implement two buttons and five switches. Once we figured out the Timer, it was easier for us to do the Stopwatch code as well.

We intended to implement a test-bench to our Digital Clock, however time did not allow extensive simulation testing. Ideally, creating a separate test-bench to test each feature of the digital clock would have allowed us to verify the functionality of each feature, observe behavior of each signal and potentially catch bugs in the code before implementation on the board. The project was tested mainly on the board due to time restriction and difficulties with designing the test-benches.

References

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