

CECS 346 Fall 2020 Project 1

Traffic Light Controller

By

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10/30/2020

Design a traffic light controller for the intersection of two equally busy one-way streets. The goal is to maximize traffic flow, minimize waiting time at a red light, and avoid accidents.

Introduction

The project including four major objectives: the understanding and implementing of indexed data structures; learning how to create a segmented software system; the study of real time synchronization by designing a finite state machine controller; learn how to use edge-trigger interrupt. We will define data structure for FSM, create fixed-time delays using the SysTick timer, and debugging real-time systems.

We design a traffic controller for the intersection of two equally busy one-way streets which are labeled as South and West. There are three inputs to LaunchPad, two are car sensors, and one is a pedestrian sensor.

We will interface 6 LEDs that represent the two Red-Yellow-Green traffic lights, and we will use the PF3 green LED for the "walk" light and the PF1 red LED for the "don't walk" light. The walk sequence should be showing three separate conditions: "walk", "hurry up" (LED flashing every 0.25s) and "don't walk".

Operation

https://youtu.be/iNQFdyHOl-w

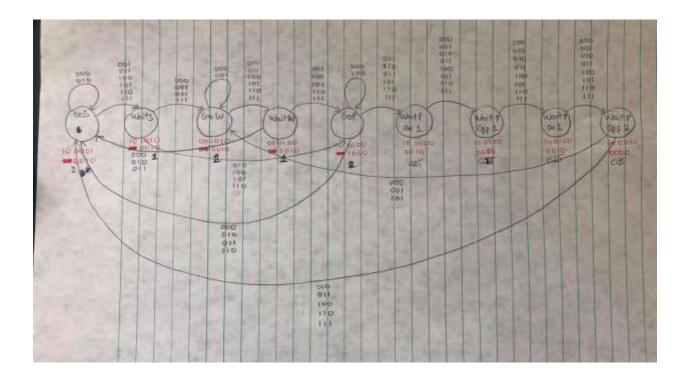
Theory

State table for the Moore FSM

State	000	001	010	011	100	101	110	111
GoS	goS	waitS	goS	waitS	waitS	waitS	waitS	waitS
WaitS	goW	goW	goP	goW	goP	goP	goW	goW
GoW	goW	goW	waitW	waitW	waitW	waitW	waitW	waitW
WaitW	goS	goP	goS	goS	goP	goP	goP	goP
GoP	goP	waitPOn1	waitPOn1	waitPOn1	goP	waitPOn1	waitPOn1	waitPOn1
WaitPOn1	waitPOff1							
WaitPOff1	waitPOn2							
WaitPOn2	waitPOff2							
WaitPOff2	goW	goW	goS	goS	goS	goW	goS	goS

Input: P,S,W

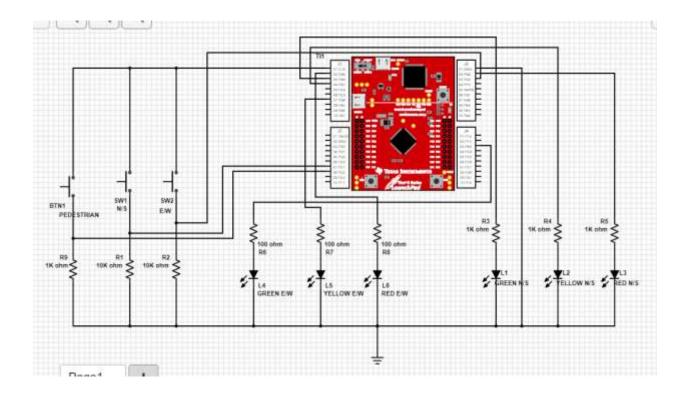
State diagram for the Moore FSM

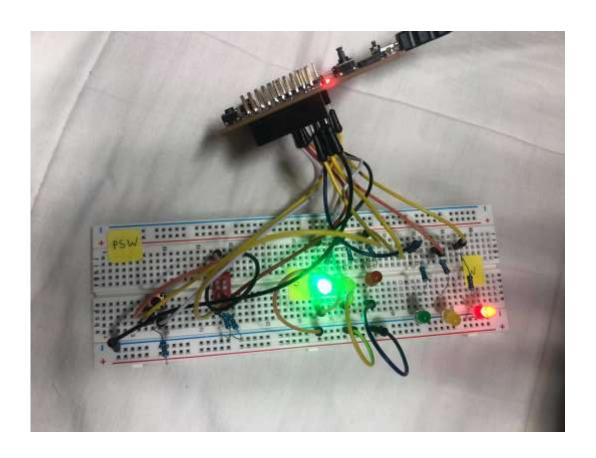


When none of the three sensors is true, stay in current state or finish transition to green. If one sensor is true, turn on the green for traffic light of that direction or "walk" for pedestrian and stay on as long as that sensor is true and no other sensor is true. If there are more than one sensor are true: cycle through the requests servicing them in a round robin fashion.

The time duration for green/walk 2 seconds, yellow/hurry 1 seconds. Red/don't walk 3 seconds. We will implement a Moore machine and use SysTick timer to wait a prescribed amount of time. The state graph defines exactly what the system does in a clear and unambiguous fashion.

Hardware design





Software design

```
startup.i ____ main.c
                                                                                                                                    (*((volatile unsigned long *) 0x49014414))

(*((volatile unsigned long *) 0x49014410))

(*((volatile unsigned long *) 0x49014404))

(*)((volatile unsigned long *) 0x49014400))

(*)((volatile unsigned long *) 0x49014410))

(*((volatile unsigned long *) 0x49014410))
                      #define GPIO PORTE RIS H
                    Adefine GPIO PORTE FOR B
#define GPIO PORTE IS R
#define GPIO PORTE IS B
#define GPIO PORTE ICR B
#define GPIO PORTE ICR B
#define GPIO PORTE ICR B
         30
         31
         32
         23
        35
       36
                      // user button connected to PEI (increment counter on falling edge)
        38
                     #define NVIC ENG B
                                                                                                                                     (*([volatile unsigned long *)OMEGODE[GG]) // INQ 0 to 31 Set Enable Register
(*)[volatile unsigned long *)OMEGODE(GG)) // INQ 3 to 7 Priority Register
                                                                                                                                   (*((volatile unsigned long *)0x40018018)) // hits 3,1
(*((volatile unsigned long *)0x40018400))
(*((volatile unsigned long *)0x40018400))
(*((volatile unsigned long *)0x40018400))
(*((volatile unsigned long *)0x40018400))
(*((volatile unsigned long *)0x40018410))
(*((volatile unsigned long *)0x40018510))
(*((volatile unsigned long *)0x40018520))
(*((volatile unsigned long *)0x40018520))
(*((volatile unsigned long *)0x40018520))
         40
                    #define P_LIGHT
#Jefine GFIO PORTF DIR R
#define GFIO PORTF ISE R
#define GFIO PORTF ISE R
#define GFIO PORTF ISV R
#define GFIO PORTF ISV R
#define GFIO PORTF RIS R
#define GFIO PORTF RIS R
         42
         43
         45
         47
                    #define GPIO PORTF RIS B
#define GPIO PORTF ASSE R
#define GPIO PORTF PUR B
#define GPIO PORTF PUR B
#define GPIO PORTF PUR B
#define GPIO PORTF DEN B
#define GPIO PORTF DEN R
#define GPIO PORTF AMSEL R
#define GPIO PORTF BCIL B
         SD
        52
        53
        35
                    #define GPIO PORTF LOCK R
                                                                                                                                     (*((volatile unsigned long *)0x40025520))
(*((volatile unsigned long *)0x40025524))
        58
57
                  Sdefine SYSCEL BOSCS B
                                                                                                                                      (*!(volstile unsigned long *)OuROGFE100))
```

```
56 fortue SPIO PORTF LOCK B
57 #Jorline SPIO PORTF CR B
                                                                      (*((volatile unsigned long *)0x40025520))
                                                                      (*((volatile unsigned long *)(x40025524))
                                                                      (*((volutile unsigned long *)Oscodffilm))
             #ORTION SYSCYL BOGGZ R
              #dafine SYSCTL RCGCI GRICK
#dafine SYSCTL RCGCI GRICK
#define SYSCTL RCGCI GRICK
                                                                     Om00000010 // purt E Clock Sating Control
Om00000001 // purt E Clock Sating Control
Om00000000 // purt F Clock Sating Control
       100
              // Punction Prototypes - Each subroutine defined
               void Forth Init (void) ;
              veid FortE Init (weid) /
veid FortE Init (weid) /
       26
              void SysTick Mair(woid);
void SysTick Wair(unsigned long delay);
void SysTick Wair(Oms(unsigned long delay);
       69
              extern void EnableInterrupts(void); // Enable interrupts
extern void WaitForInterrupt(void); // low power mode
               unsigned press = 0;
               // FSH state Hate structure
       TO Figure State |

10 Figure State |

10 uint30 t T Out;

11 uint30 t F Out;

12 double Time;

13 uint32 t Mext[0];
       24
            typedef const struct State SType
```

```
startup.s ____ main.r.
                                      // Constants definitions
                                      #define goS 0
                89
                BT
                                      #define goM
                                      #define waitW
                                      #define goF
                                      #dofine WaitPOnl
                85
                                      #define waitFoffi
                                     #define waitPOn2
                                      #define waitFOffI #
                99 [ STyp FSH[ 9] = [
                                             [0x21,0x02,2,(goS,wait5,goS,wait5,wait5,wait5,wait5,wait5)],
                                            (OM22, OMD2, 1, (goW, goW, goP, goW, goP, goP, goP, goP, goW)),
(OMDC, OMD2, 2, (goW, goW, waitW, waitW, waitW, waitW, waitW, waitW)),
           191
           192
                                            (OHI4, OROJ, 1, 1905, goP, goS, goF, goF, goP, goP, goP)), (OHI2, OXOB, J, 190F, WHITPOH), WHITP
           104
                                              (0x24, 0x02, 0.25, (waitPOff), waitPOff), waitPOff), waitPOff), waitPOff), waitPOff), waitPOff), waitPOff)
             105
                                             (0x24,0x00,0,25,(waitF0n2,waitF0n2,waitF0n2,waitF0n2,waitF0n2,waitF0n2,waitF0n2,waitF0n2,waitF0n2))
           106
                                              (0x24, 0x02, 0.25, (waitPOff2, waitPOff2, wa
           108
                                            [0x26, 0x00, 0.25, (goW, goW, goS, goS, goS, goW, goS, goS)]);
           110 // global variable visible in Watch window of debugger
                                      // increments at least once per bottom press volatile unsigned long FallingEdges = 0;
           112
                                            roid EdgeCounter_Init(void)(
                                               SYSCTI ROCCE R |= 0800000010; // (a) activate clack for port E FallingEdges = 0; // (b) initialize counter OPIO PORTE DIR R = -0807; // (c) hake f2,1,0 output OPIO PORTE AFSER R = -0807; // disable alt funct on FEI-0 GPIO PORTE DEN R |= 0807; // enable digital I/O on FEI-0
           114
           116
           118
                                                                                                                                                                                                                                                   enable digital I/O on FEI-0
```

```
___ startup.t ___ man.c
    109
    110 // global variable visible in Watch window of debugges
           // increments at least once per button press
    112 volatile unsigned long FallingEdges = 0;
113 = void EdgeCounter_Init(void)(
              SYSCTL RCGC2 R (= 0x000000010; // (a) activate clock for port E
FallingEdges = 0; // (b) initialize counter
GPIO FORTE DIR R 4= -0x07; // (c) make E3,1,0 output
    118
    116
    117
              GPIO PORTE AFSEL R 4=-0\pi07; // disable alt funct on FE2-0 GPIO PORTE DEN R 1=0\pi07; // enable digital 1/0 on FE2-0 GPIO PORTE PCTL R 4=-0\pi000000FFF; // configure PE2-0 as GPIO
    118
    119
                                                       // disable analog function
// enable weak pull-up on FE2
              GPIO PORTE AMSEL R 4= -GMO7;
GPIO PORTE PUR R 1= URD4;
GPIO PORTE IS R 4= -0x94;
    120
                                                                       disable shalog functionality on PE2-0
    121
                                                        // (d) FE2 is edge-sensitive
             123
    124
    126
    127
                                                                                                           (portE: bit 4 -> 0001 0000 -> 0x10)
    129
    138
    131 Byoid GPIOPortE_Handler(void) (
              GPIO PORTE ICR R |= 0x04; / FallingEdges = FallingEdges + 1;
                                                         // acknowledge flag3: 06001000
    332
    133
    134
    135
    136
    137 | int main(void) (
              uint32 t S; // index to the current state
uint32 t Input;
    138
    139
    140
```

```
135
137 Bins main (word) (
         uint32 t S; // index to the current state uint32 t Input;
138
139
140
         PortB_Init();
141
142
         PortE_Init();
143.
        PortF Init();
144
         volatile unsigned long delay;
SysTick_Init(); // Program 10.2
EnableInterrupts();
145
146
147
148
         EdgeCounter_Init():
                                              // initialize GPIO Fort F interrupt
149
                                             // FSM start with green on north,
        S = goS:
150
                                             // also provide time for activating port E4B clock
151
152
153 @ while(1) (
           T_LIGHT = FSM[5].T_Out; // set traffic lights
F_LIGHT = FSM[5].F_Out; // set walk lights for pedestrians
154
155
            Systick Wattions(FSM[5].Time*100); // isec = 10ma*100
Input = SENSOR; // read sensors
156
           Input = SENSOR: // read mensors
Input = SENSOR | (press<<2): //PSM : PE2,1,0
157
158
           S = F5M[S].Next[Input]:
159
          1f(5 == goP)(
press = 0;
160 🗎
161
162
163
164 1
165
166 Twoid PortB Init (wold) (
```

```
______ startup.s ______ main.c
           GPIO_PORTF_CR_R |= 0 \times 0 A;

GPIO_PORTF_AMSEL_R i= -0 \times 0 A; // Disable snalog function on PF3,1

GPIO_PORTF_PCTL_R i= -0 \times 0 A; // Disable regular GPIO

GPIO_PORTF_PCTL_R i= -0 \times 0 A; // Disable regular GPIO_PS1.1
 190
 191
           GPIO PORTF DIR R |= 0x0A; // Outputs on PF3,1
GPIO PORTF_AFSEL R += -0x0A; // Regular function on PF3,1
 193
 194
           GPIC PORTF DEN R |= 0x0A;
                                                   // Enable digital signals on FF3,1
 195
 196
 197
 198 // Initialise SysTick with busy wait running at bus clock 199 [ world SysTick_Init(void) (
           NVIC ST CTRL R = 0;
NVIC ST CTRL R = 0x000000005;
 200
                                                          // disable SysTick during setup
                                                          // enable SysTick with core clock
 202
 203
         // The delay parameter is in units of the 80 MHz core clock. (12.5 ms)
 204
 105 -void SysTick Wait (unsigned long delay) (
           NVIC_ST_RELOAD_R = delay-1; // number of counts to wait
NVIC_ST_CURRENT_R = 0; // any value written to CURRENT clears
 208 D while ((NVIC_ST_CTRL_R&0x00010000) == 0) ( // wait for count flag
 209
 210
 211
 212 // 10000us equals 10mm
 213 Dwoid SysTick WaitlOms (unsigned long delay) (
          unsigned long is
 215 [] for (1=0; 1cdelay; 1++) [
                                                 // wait 10mm
 216
              SysTick Mait (160000);
          1
 217
       1
 218
 319
 220
```

Conclusion

My success in this project is better understand and implement of indexed data structures, learn how to create a segmented software system including linked data structures, creating fixed time delay using SysTick time, and debugging real time systems by designing a state machine.

I think the hardest part of this project is designing the correct finite state machine. I had a lot of errors on the fsm with the older lab description version. However, with the newer version, it is so much clearer to follow the rules and as to give the fair chances for each participant. The next part that I also had many troubles on was the interrupt to implement the pedestrian button.