74AHC30; 74AHCT30

8-input NAND gate Rev. 03 — 26 June 2009

Product data sheet

General description 1.

The 74AHC30; 74AHCT30 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC30; 74AHCT30 provides an 8-input NAND function.

Features 2.

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - ◆ For 74AHC30: CMOS level
 - ◆ For 74AHCT30: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

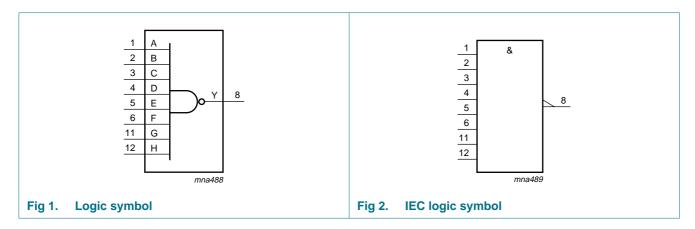
3. Ordering information

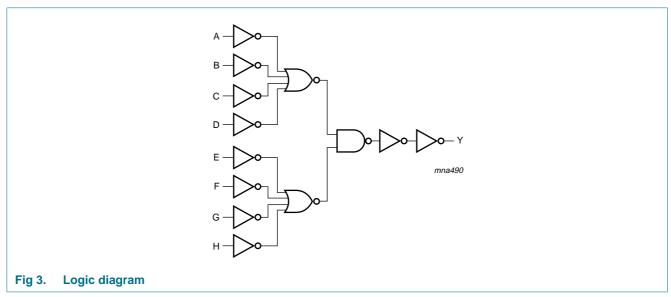
Ordering information Table 1.

Type number	Package				
	Temperature range	Name	Description	Version	
74AHC30D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1	
74AHCT30D			body width 3.9 mm		
74AHC30PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1	
74AHCT30PW			body width 4.4 mm		
74AHC30BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very	SOT762-1	
74AHCT30BQ	_		thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm		



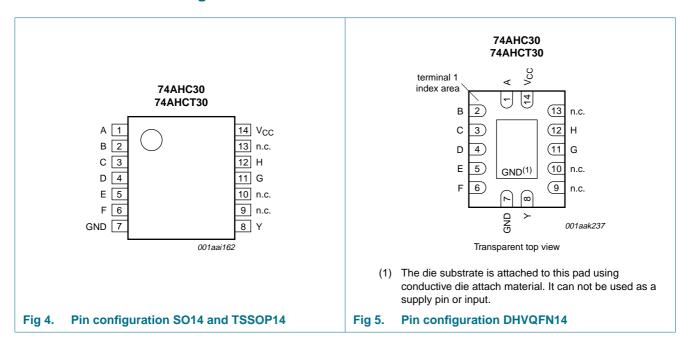
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A	1	data input
В	2	data input
С	3	data input
D	4	data input
E	5	data input
F	6	data input
GND	7	ground (0 V)
Υ	8	data output
n.c.	9	not connected
n.c.	10	not connected
G	11	data input
Н	12	data input
n.c.	13	not connected
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table [1]

Input								Output
Α	В	С	D	E	F	G	Н	Y
L	Χ	Χ	X	X	X	Χ	X	Н
Χ	L	Χ	Χ	Χ	Χ	Χ	Χ	Н
Χ	Χ	L	Χ	Χ	Χ	Χ	Χ	Н
Χ	Χ	Χ	L	Χ	Χ	Χ	Χ	Н
Χ	Χ	Χ	Χ	L	Χ	Χ	Χ	Н
Χ	Χ	Χ	Χ	Х	L	Χ	Χ	Н
Χ	Χ	Χ	Χ	Χ	Χ	L	Χ	Н
X	Χ	Х	Х	Х	Х	Χ	L	Н
Н	Н	Н	Н	Н	Н	Н	Н	L

^[1] H = HIGH voltage level;

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_{I}	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_1 < -0.5 \text{ V}$	<u>[1]</u> –20	-	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> –20	+20	mA
I _O	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I_{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[2] _	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For TSSOP14 packages: above 60 $^{\circ}\text{C}$ the value of Ptot derates linearly at 5.5 mW/K.

For DHVQFN14 packages: above 60 $^{\circ}\text{C}$ the value of Ptot derates linearly at 4.5 mW/K.

L = LOW voltage level;

X = don't care.

^[2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	•	74AHC30)	7	Unit		
			Min	Тур	Max	Min	Тур	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	and fall rate	V_{CC} = 3.3 V \pm 0.3 V	-	-	100	-	-	-	ns/V
ć		V_{CC} = 5.0 V \pm 0.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC3	0					'			"	
V_{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	$V_{CC} = 3.0 \text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	$V_{CC} = 3.0 \text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_{O} = -50 \mu A$; $V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu A$; $V_{CC} = 3.0 \text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_O = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 50 \mu A$; $V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A$; $V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	$V_I = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
Cı	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	–40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
Co	output capacitance		-	4	-	-	-	-	-	pF
74AHCT	30									
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	-	8.0	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_{O} = -50 \ \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
0_	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_O = 50 \mu A$	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	$V_I = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other pins at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		25 °C		–40 °C to	o +85 °C	–40 °C to	Unit	
				Typ[1]	Max	Min	Max	Min	Max	
74AHC3	0									
pu .	propagation delay	A, B, C, D, E, F, G, H to Y; see <u>Figure 6</u> and <u>7</u>	<u>!]</u>							
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		C _L = 15 pF	-	5.0	9.5	1.0	11.0	1.0	12.0	ns
		$C_L = 50 pF$	-	6.7	12.0	1.0	14.5	1.0	15.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		C _L = 15 pF	-	3.6	6.5	1.0	7.5	1.0	8.0	ns
		$C_L = 50 pF$	-	4.9	8.0	1.0	9.5	1.0	10.5	ns

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 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions			25 °C		–40 °C to	o +85 °C	-40 °C to	Unit	
					Typ[1]	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$		-	10	-	-	-	-	-	pF
74AHCT30; V _{CC} = 4.5 V to 5.5 V											
t _{pd}	propagation delay	A, B, C, D, E, F, G, H to Y; see <u>Figure 6</u> and <u>7</u>	[2]								
		C _L = 15 pF		-	3.3	6.5	1.0	7.5	1.0	8.0	ns
		$C_{L} = 50 \text{ pF}$		-	4.7	8.5	1.0	9.5	1.0	10.5	ns
C_{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	[3]	-	12	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 5.0 \text{ V}$).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.

11. Waveforms

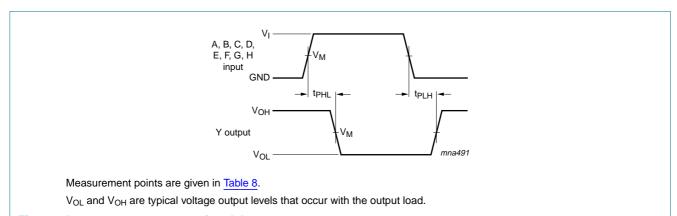
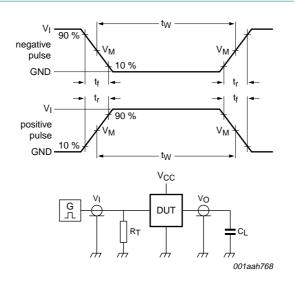


Fig 6. Input to output propagation delays

Table 8. Measurement points

Туре	Input	Output
	V _M	V _M
74AHC30	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT30	1.5 V	$0.5 \times V_{CC}$



Test data is given in Table 9.

Definitions for test circuit:

 R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

Fig 7. Load circuitry for measuring switching times

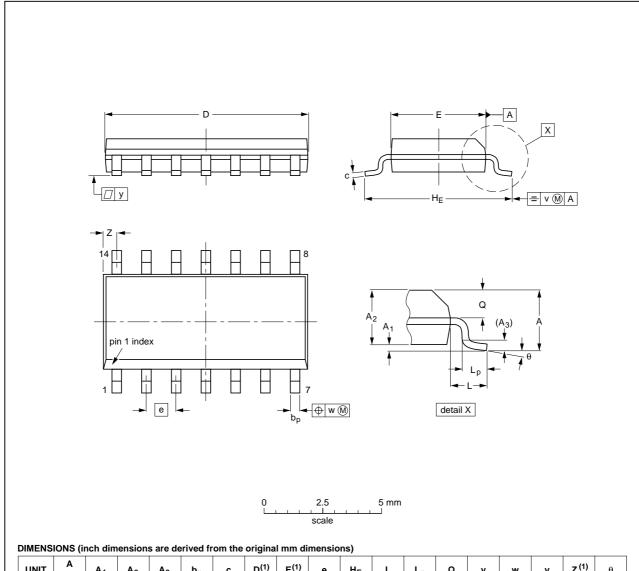
Table 9. Test data

Туре	Input		Load	Test
	VI	t _r , t _f	CL	
74AHC30	V _{CC}	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74AHCT30	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01	1	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

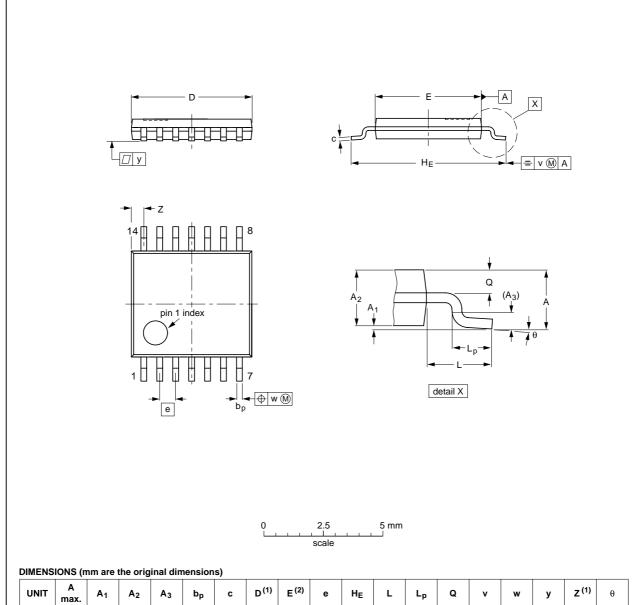
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



				,		-,												
UNIT	A max.	A ₁	A ₂	А3	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT402-1		MO-153				99-12-27 03-02-18	

Fig 9. Package outline SOT402-1 (TSSOP14)

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

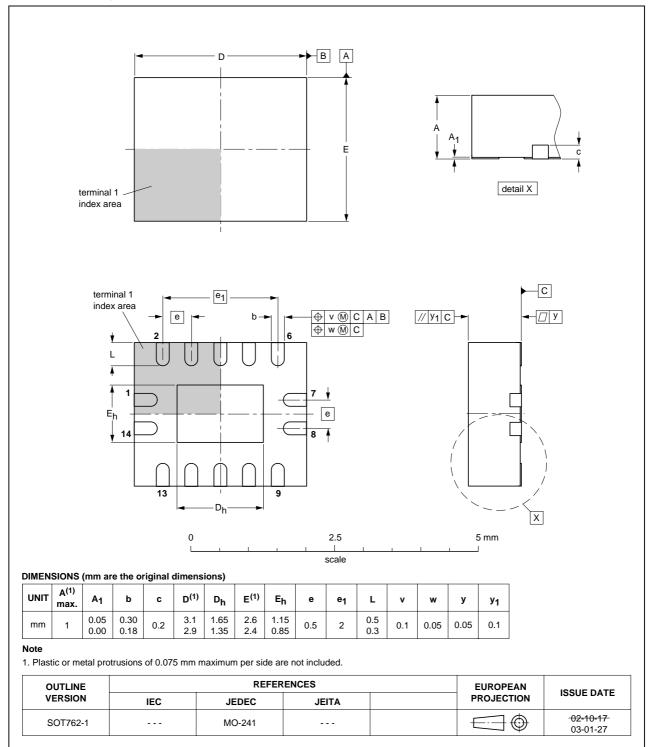


Fig 10. Package outline SOT762-1 (DHVQFN14)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT30_3	20090626	Product data sheet	-	74AHC_AHCT30_2
Modifications:	• Section 7:	DHVQFN14 package added derating values added for Dh outline drawing added for D	HVQFN14 package.	
74AHC_AHCT30_2	20080530	Product data sheet	-	74AHC_AHCT30_1
74AHC_AHCT30_1	19991130	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- [2] The term 'short data sheet' is explained in section "Definitions"
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