CAD Design

HW-1

Due Date: 15th February'2018

1.
    a. Explain the procedure of Doping (What do you mean by doping?) How does it affect the semiconductor? List the different kinds of doping materials. Name two methods of doping and explain the process.
    b. Go to "nanohub.com" and make a profile of yours, then access the software "Mobility and Resistivity". With this software take Silicon and GaAs wafer Dope the wafer with donor and acceptor with different carrier concentration of 5e+10, 1e+5, 1e+20 and take the snap shot of the results and include it in your homework. Discuss about the mobility and resistivity. What is your opinion about that?
2. From Question.1, you know about P-type and N-type material. If you connect one P-type material and N-type material and apply 0 voltage between N and P type material. How the device will act in equilibrium (Applying 0 volt).Explain it in terms of electric field direction and diffusion force direction (what will be the electric field force direction on holes and electrons, direction of diffusion force on holes and electrons in equilibrium)

3. From Question.2, explain the device behavior when it is in Forward bias and Reverse Bias. Include Charge density, Electric Field, Voltage plot in terms of space like EField Vs x, Q(Charge) Vs x and Voltage Vs x (where x is space)

4. NMOS and PMOS have four terminals: Source, gate, drain, body. For the case of NMOS, which terminal will have maximum voltage and which one will have minimum voltage. Write the equation of threshold voltage. Will threshold voltage V_t remain constant for all cases (different situation varying temperature)? Explain your opinion. Draw the I-V characteristic of NMOS.

5. For PMOS which terminal will have maximum voltage and which one will have minimum. Voltage? Draw the I-V characteristic of PMOS. Among PMOS and NMOS, which one is Pull Down Network (PDN) and which one is Pull UP Network (PUN). Explain your opinion.

6. Draw the schematic diagram of XOR, NAND and NOR gate and include the truth table of all the gates with PMOS and NMOS.