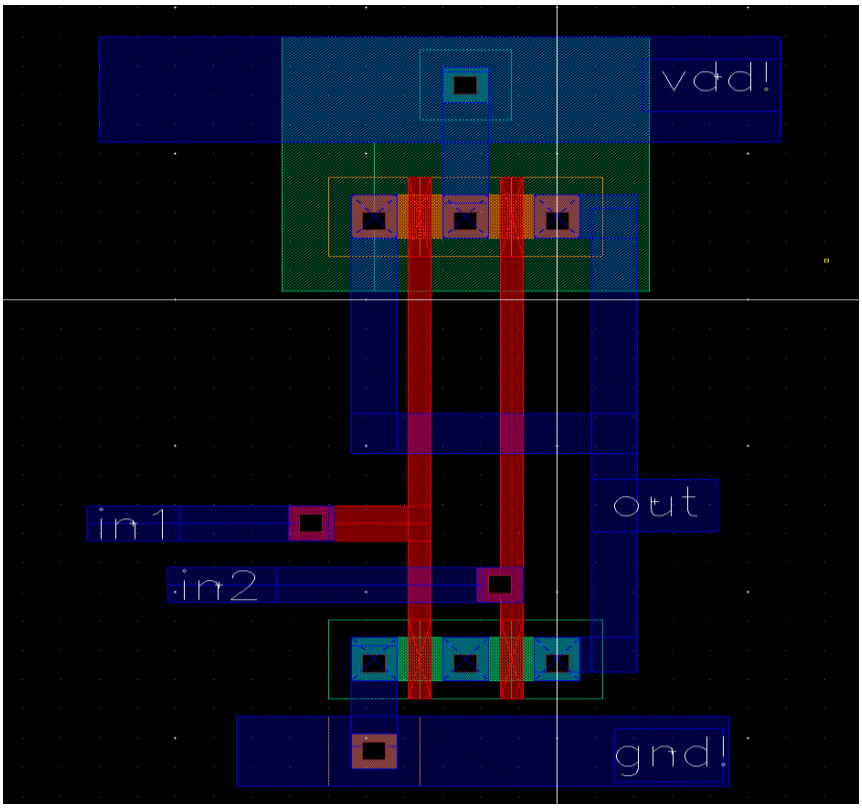
Tutorial 3: Cadence Layout

Objective:

To learn how to draw layout in Cadence Virtuoso Layout.

Tasks:

1. You will draw the layout for the NAND circuit that you design and simulate in the previous tutorial

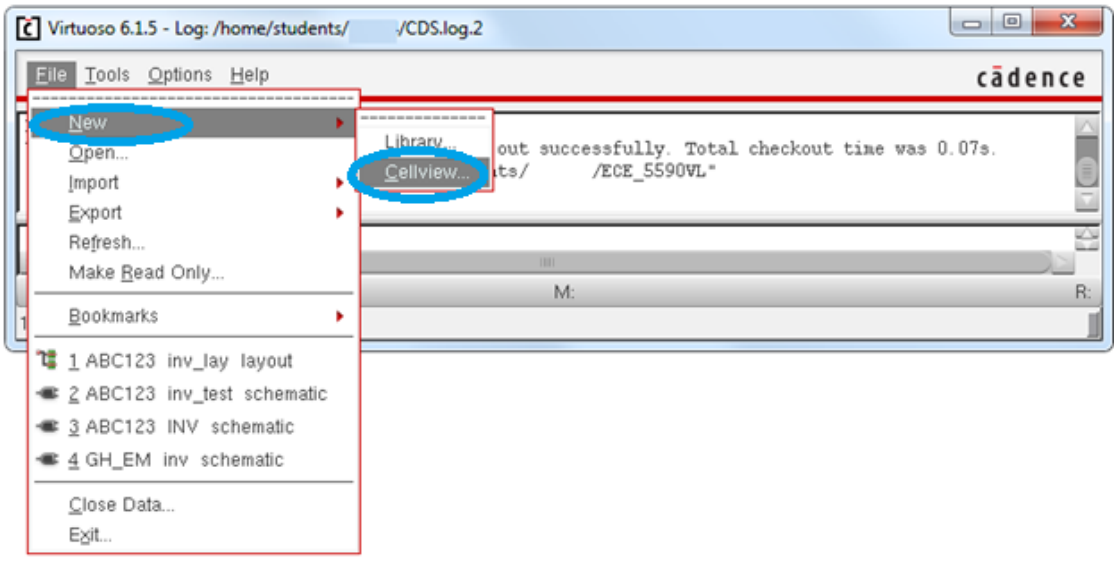


2. Test/Simulate you NAND layout in Analog Design Environment.

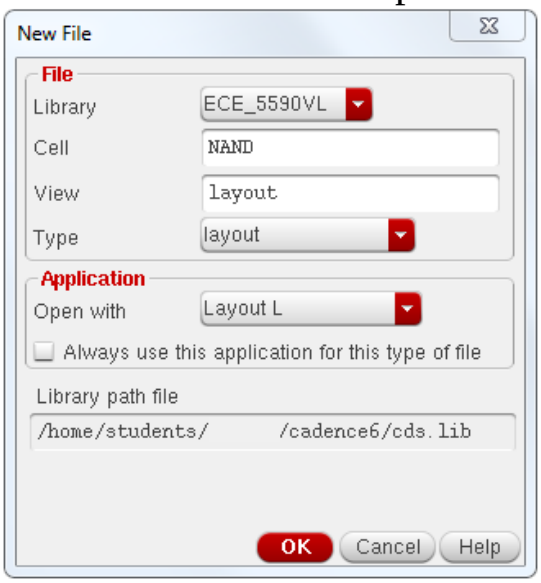
Procedure:

PART I: you will draw the layout of the circuit

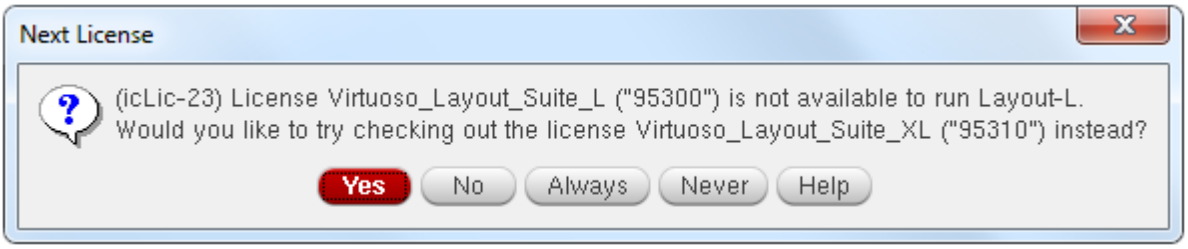
In the library manager (you should what is that) click on File → New → Cellview



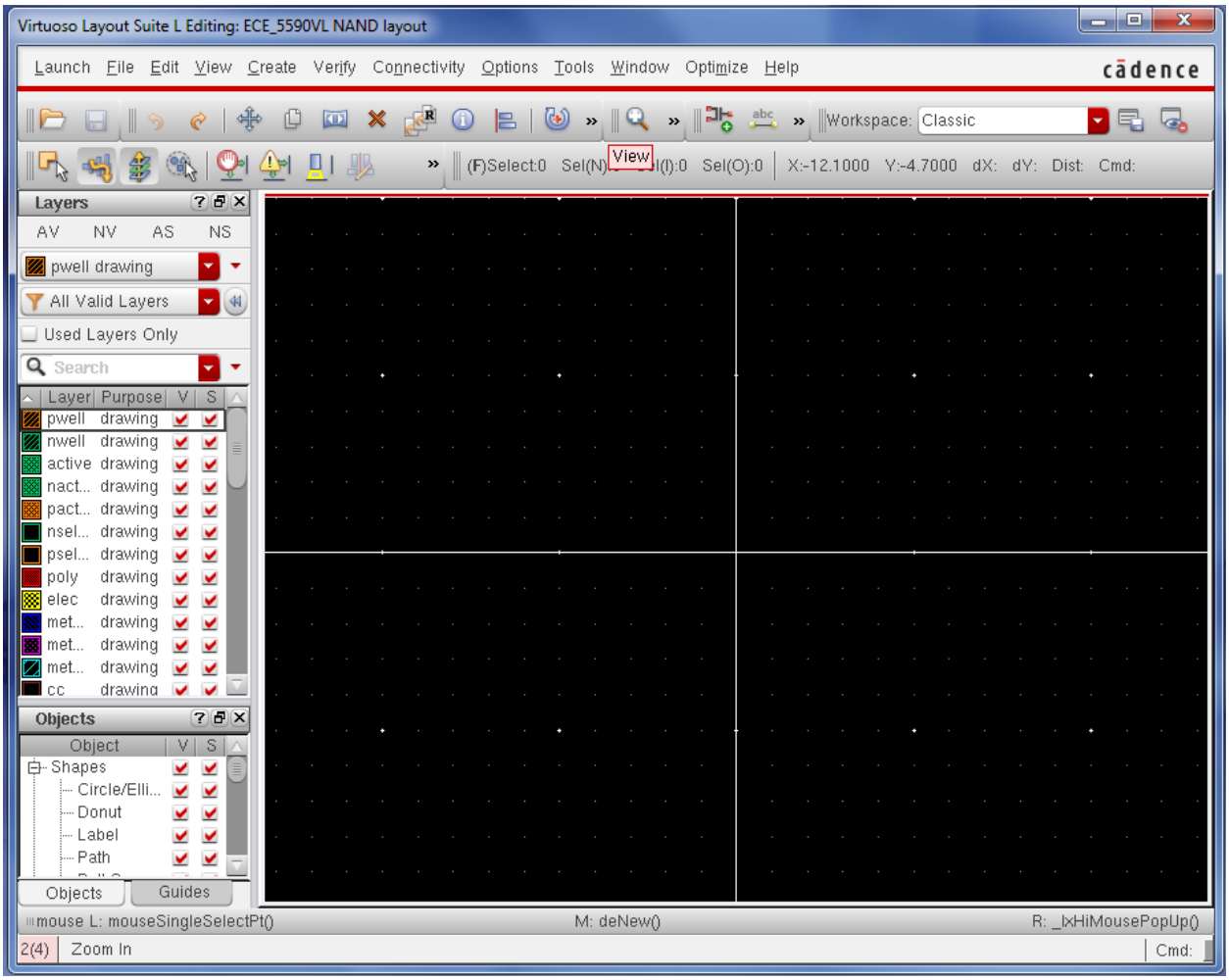
Then, on the following window type NAND for Cell file name. On the library button, scroll up and down to pick the right library name and click **ok**. Make sure to pick the **layout** option under the **Type** selection.



Then, the following window will appear. Click **Yes**.

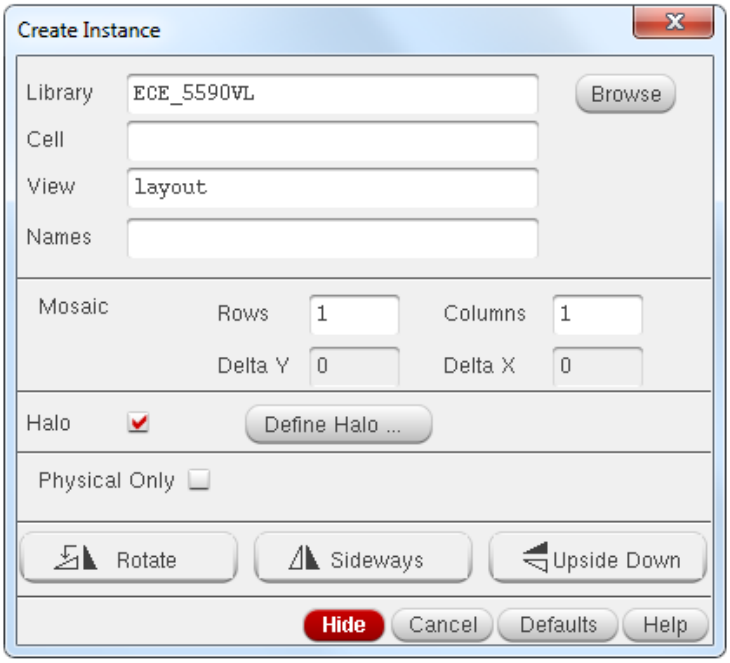


At this point, you should see virtuoso layout editor window as shown on the bottom.

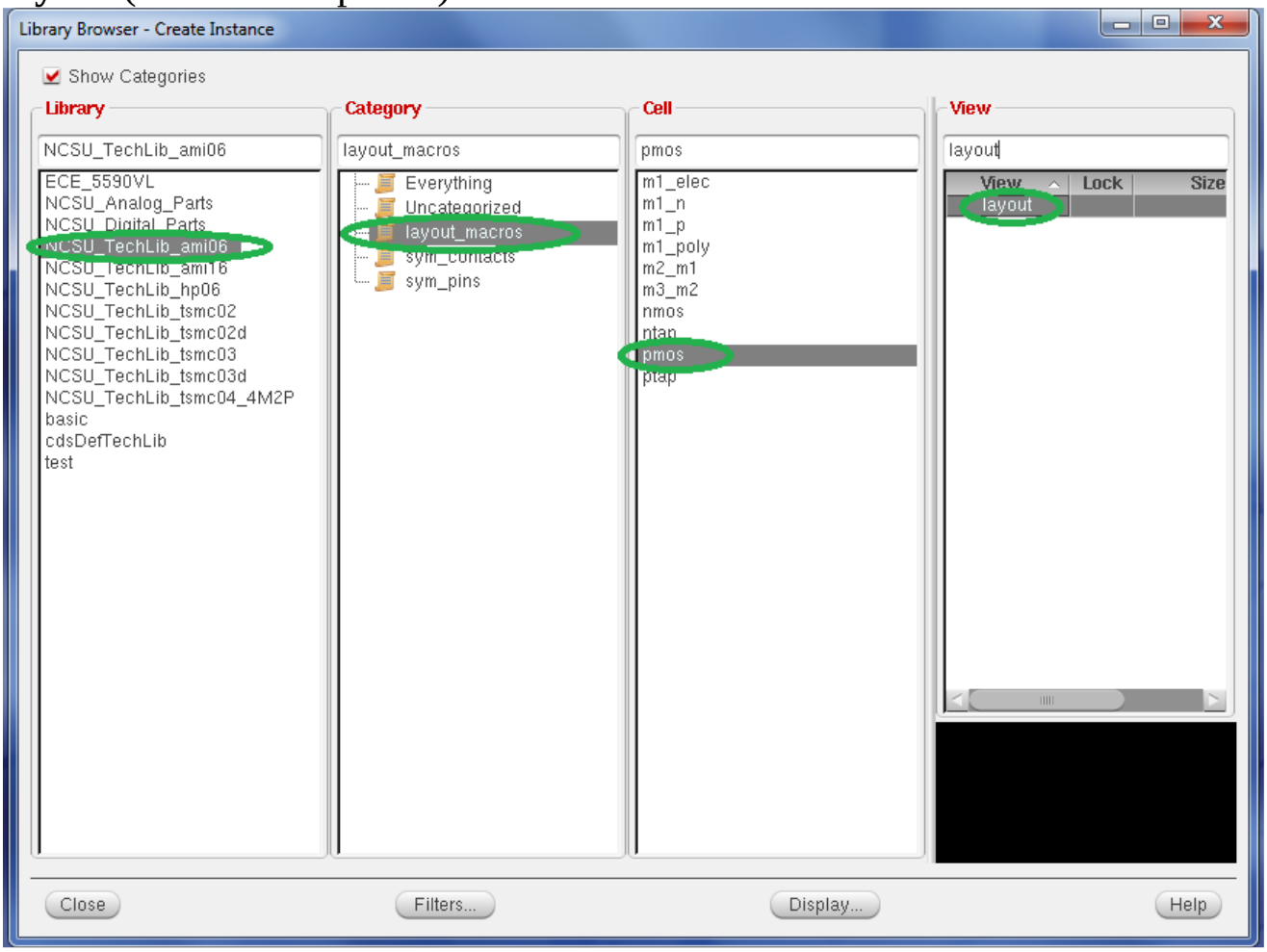


Now, we will be placing the PMOS and NMOS transistors on the layout-editing window.
Make sure that you the properties of the NMOS and PMOS are same as your schematic

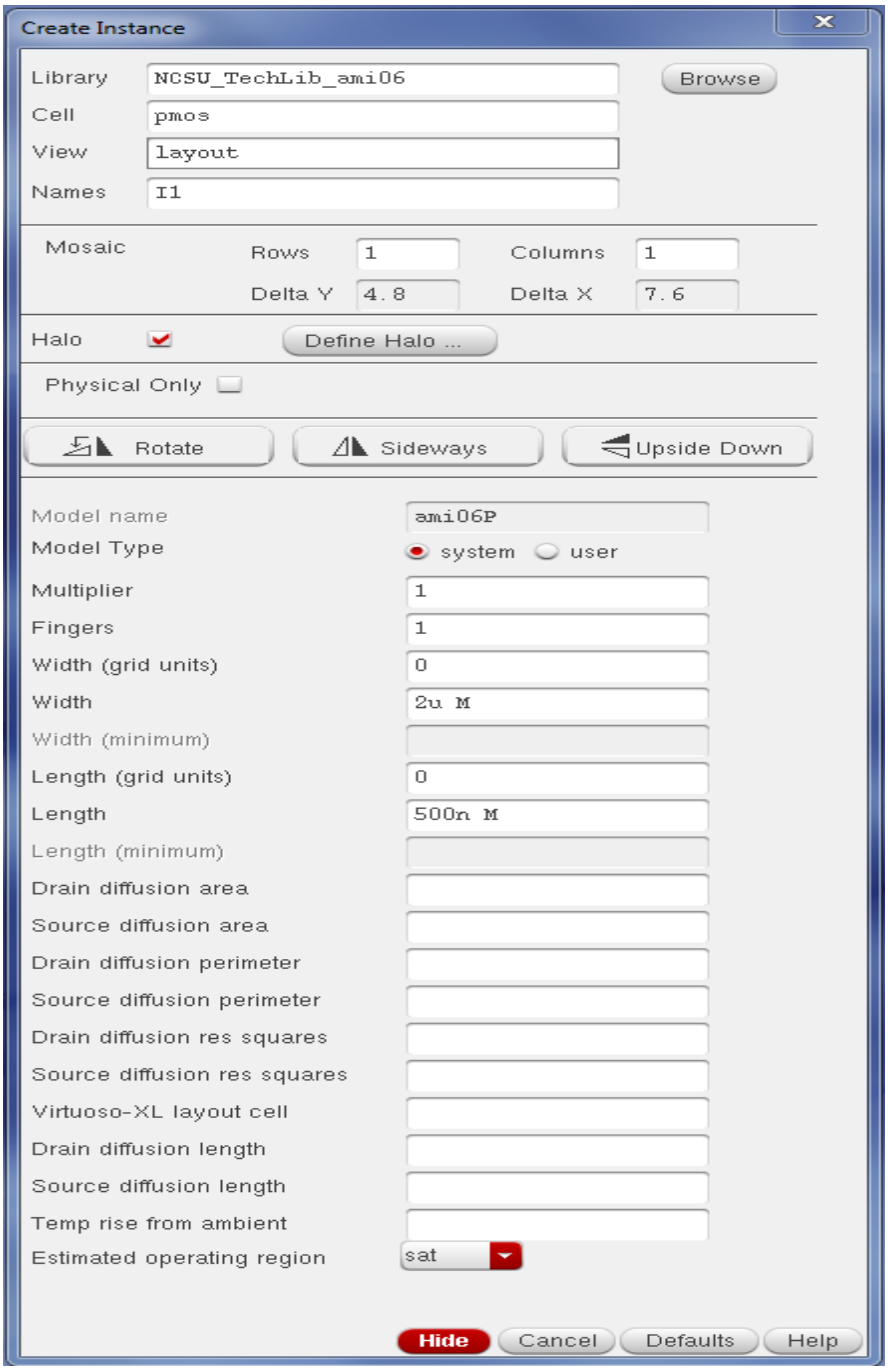
To place PMOS:
Create → Instance then the following window will come.



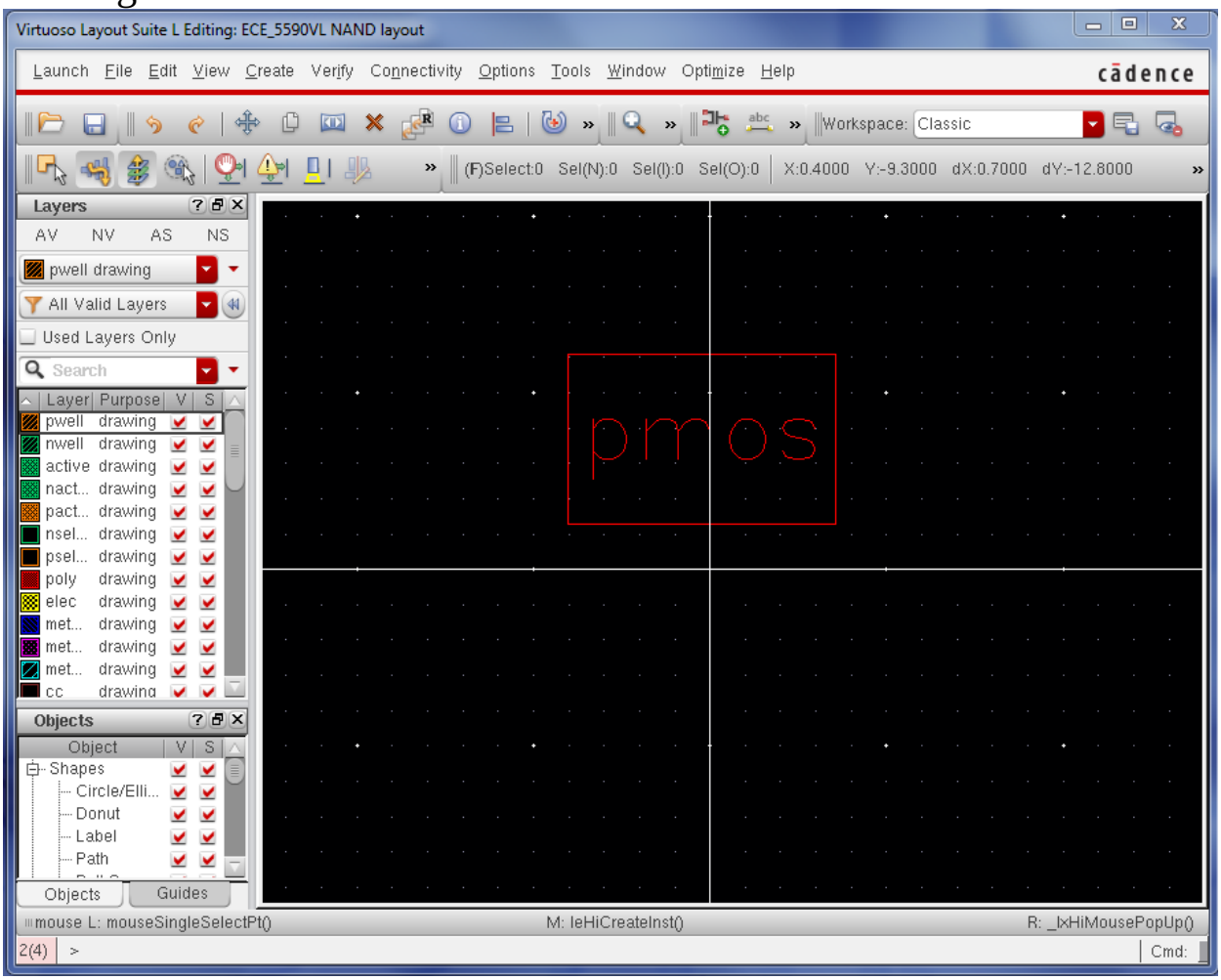
When you click on **Browse,** the library window will be opened. Select: **NCSU_TechLib_ami06** (from the Library options), **Layout_macros** (from category options), **pmos** (from Cell options), **layout** (from view options)



Then, when you click **Close,** the cursor will change to a red rectangle with pmos writing on it. Do not place the transistor yet. On the **Create Instance window,** make the changes shown on the bottom then click **hide**.

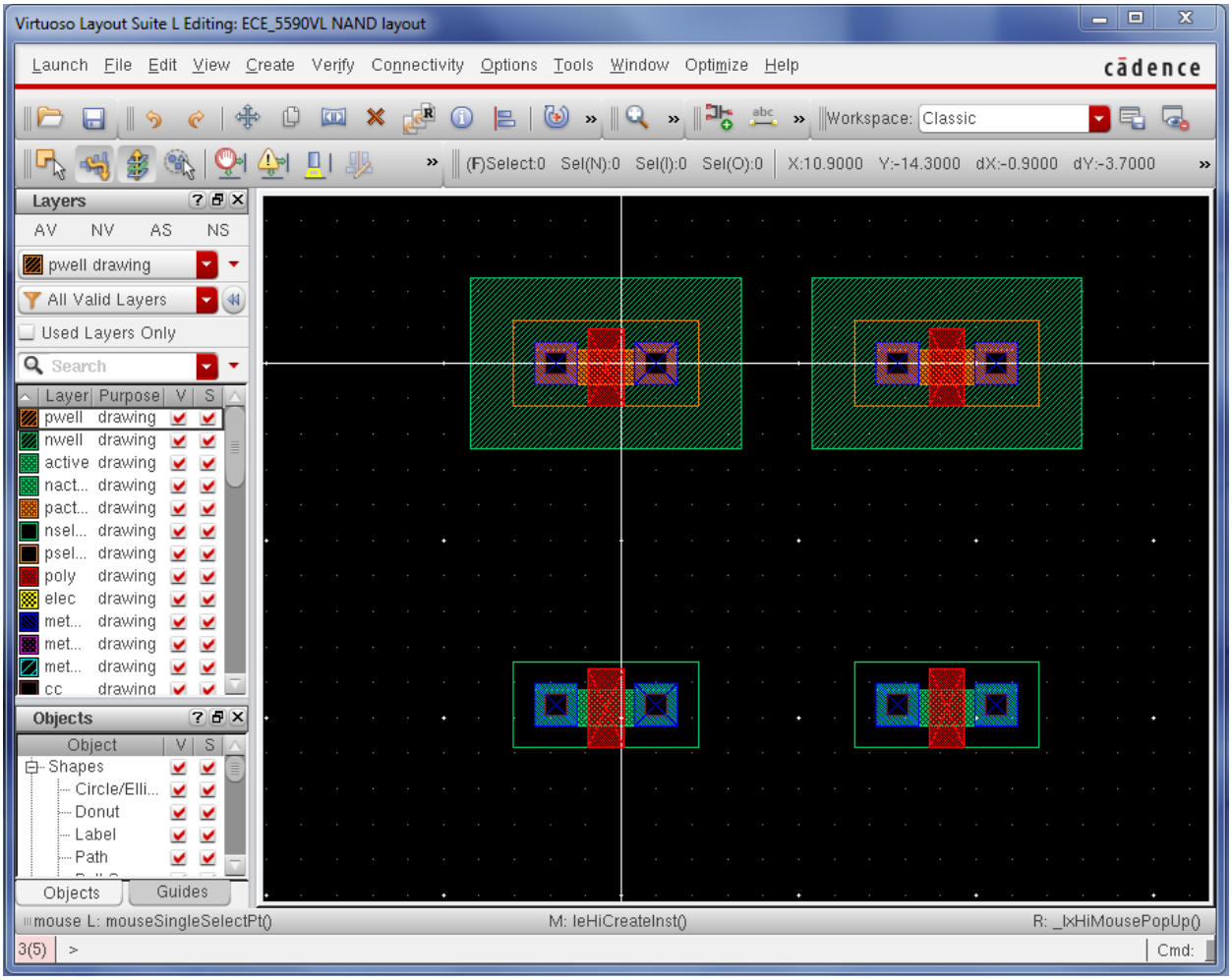


Place the **pmos** transistor on the virtuoso layout editor window by left clicking on the mouse.



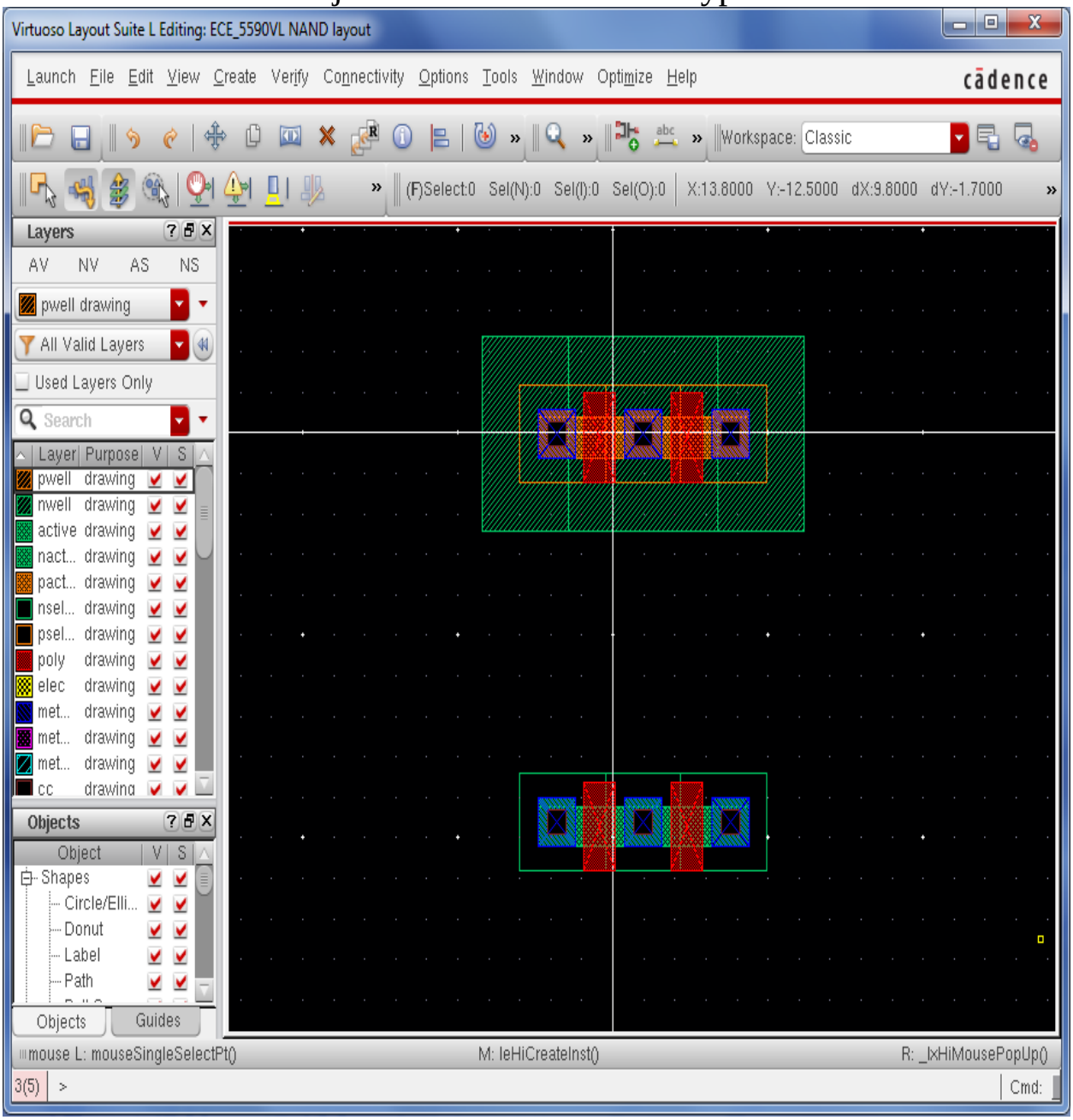
To place the second PMOS, left click on the PMOS and type **c (Copy)** then place it on the window. Repeat the same process for NMOS and click **OK**.

To go from the red rectangle box to transistor symbol press **shift + F**
To go back to the red rectangle press **Ctrl + F.**

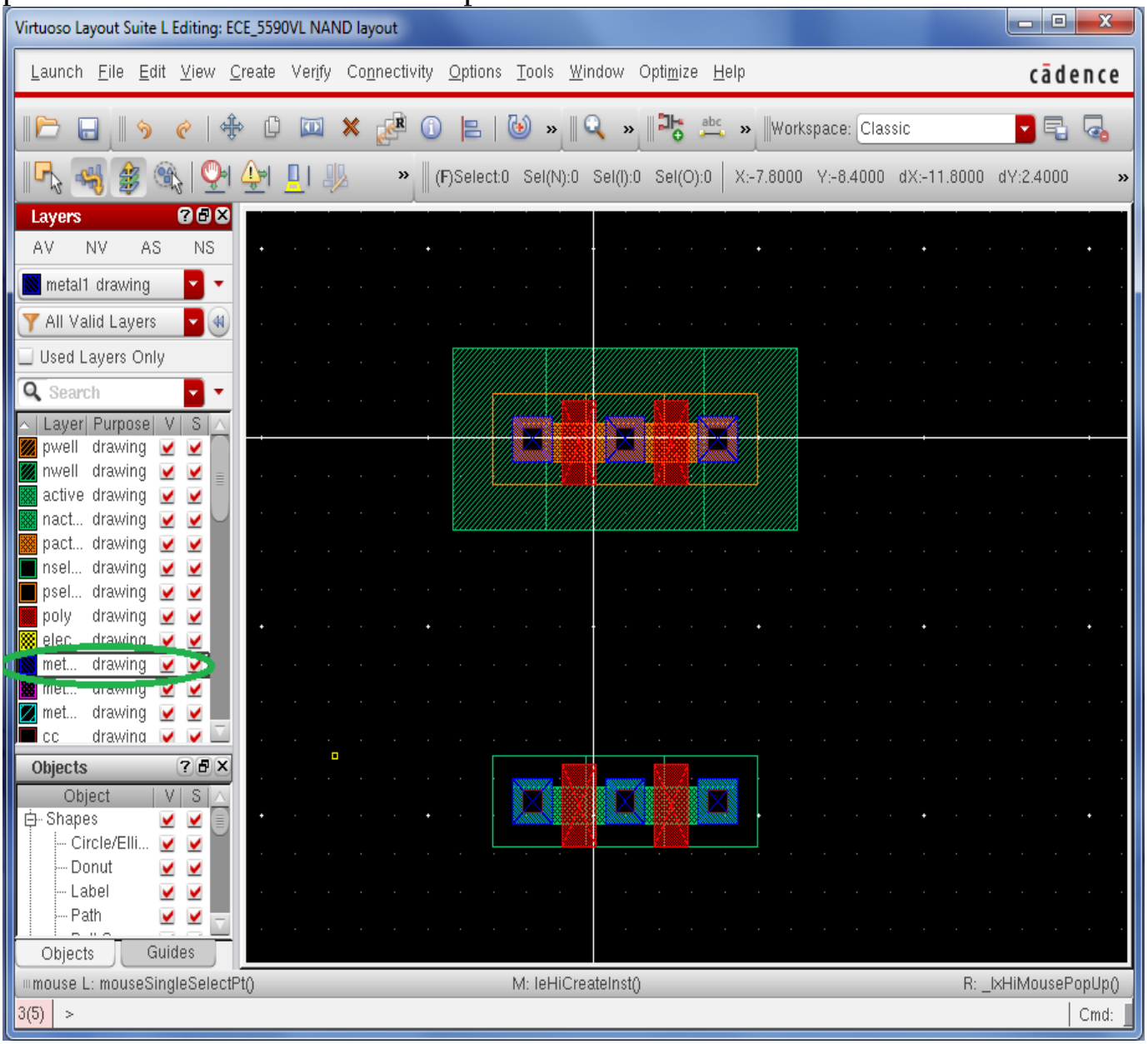


At this point, you should have a window with two PMOS and two NMOS transistors as shown above

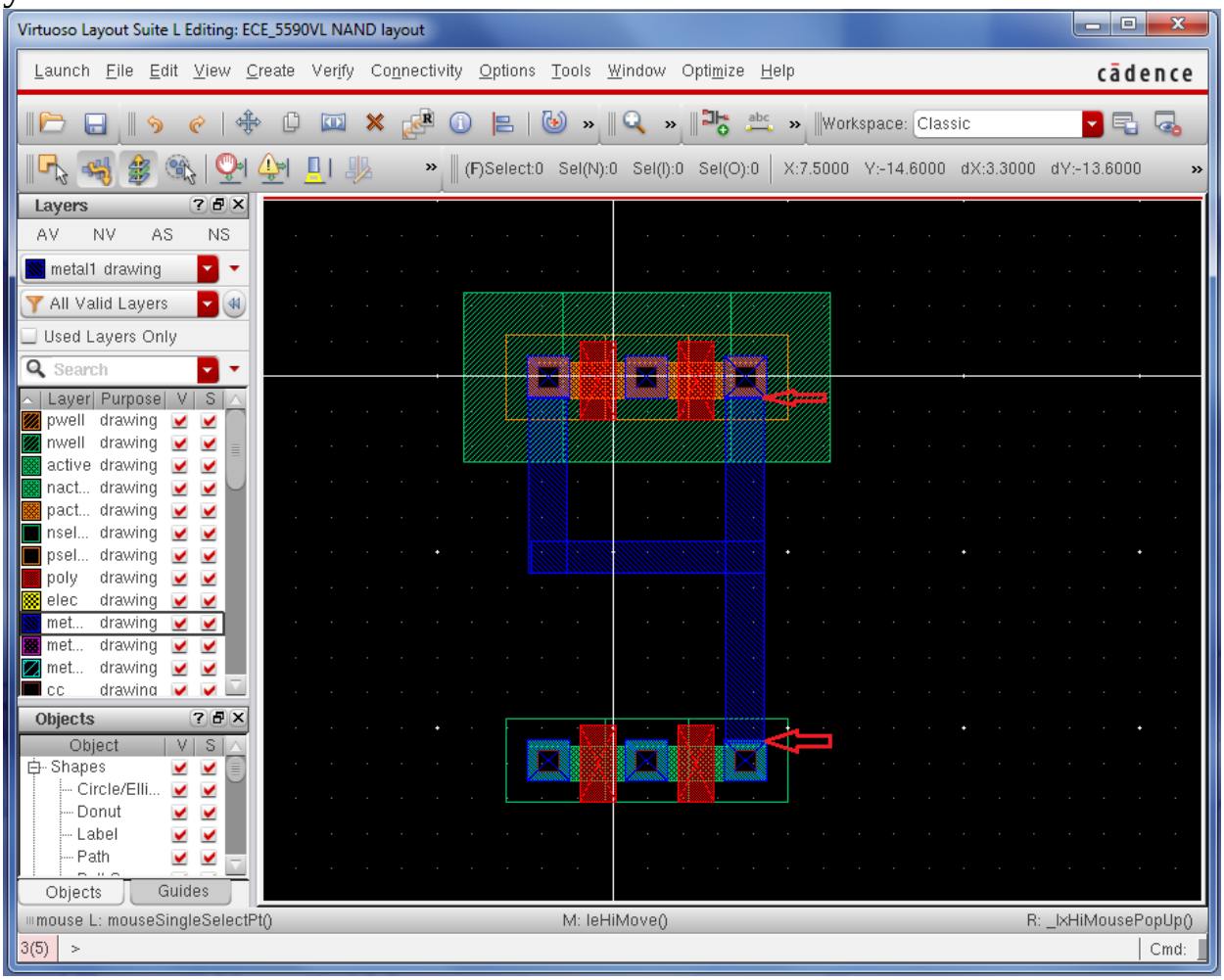
For the layout of NAND gate, a single drain diffusion region is shared between two of the pmos transistors. In addition, the nmos are sharing the source of the first transistor with the drain of the second nmos transistor. To move objects select the item and type **m**.



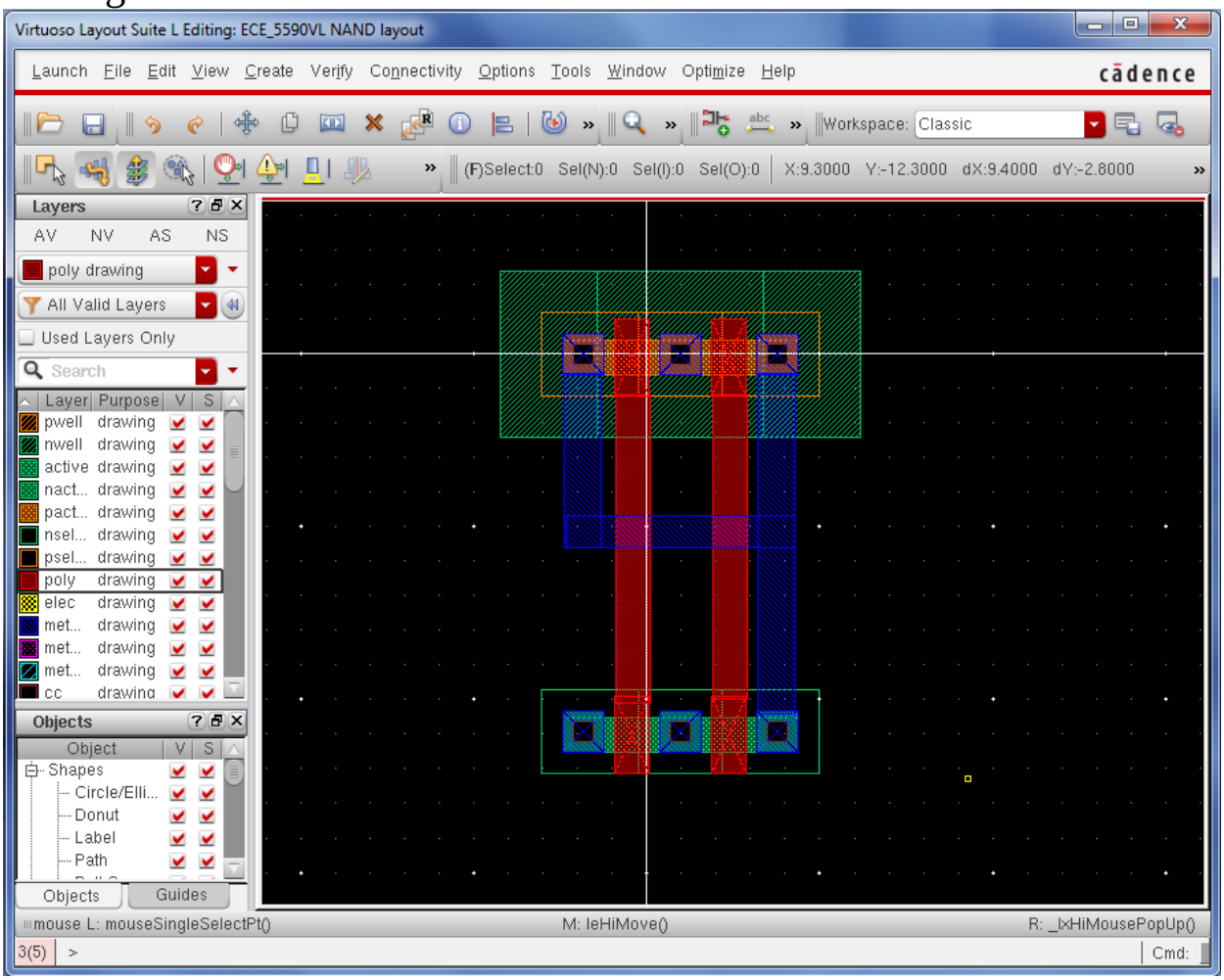
Next, we will draw the metal connection between the drain of the pmos to the drain of the nmos. In addition, we will connect both drains of the pmos transistor. Select **metal1** option from the left side of the window



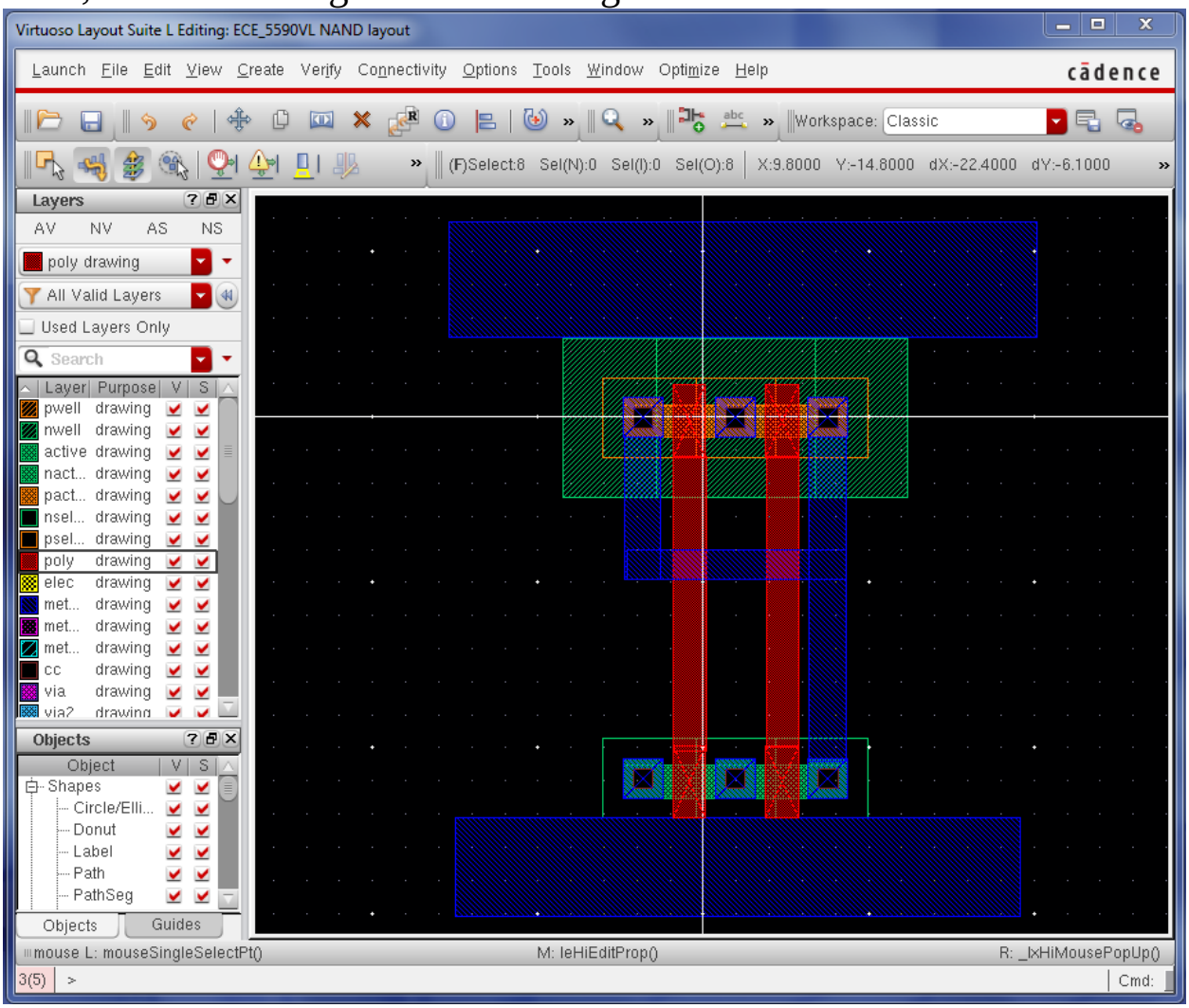
Now, type **r** to draw the rectangle. The rectangles should be drawn from tip of the one end to the other as shown. If you make a mistake while drawing the rectangle, you can use the **s** (stretch) command to correct it. To use the stretch command, type **s** on the keyboard then move the mouse over the object of interest. When yellow dashed lines appear, then you should be able to stretch the line on either direction.



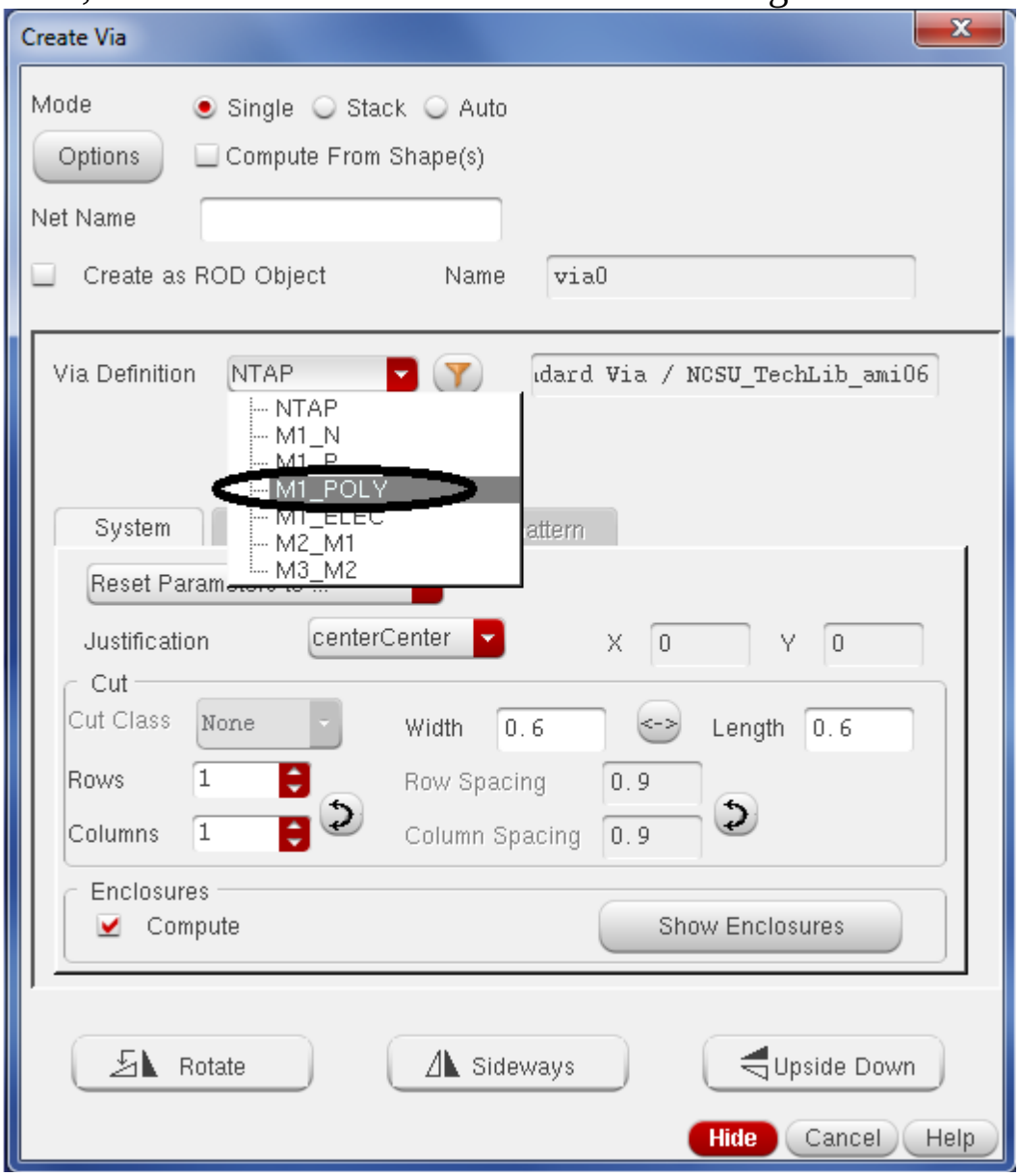
Next, select **poly** option from the left side of the window and draw the rectangles as shown.



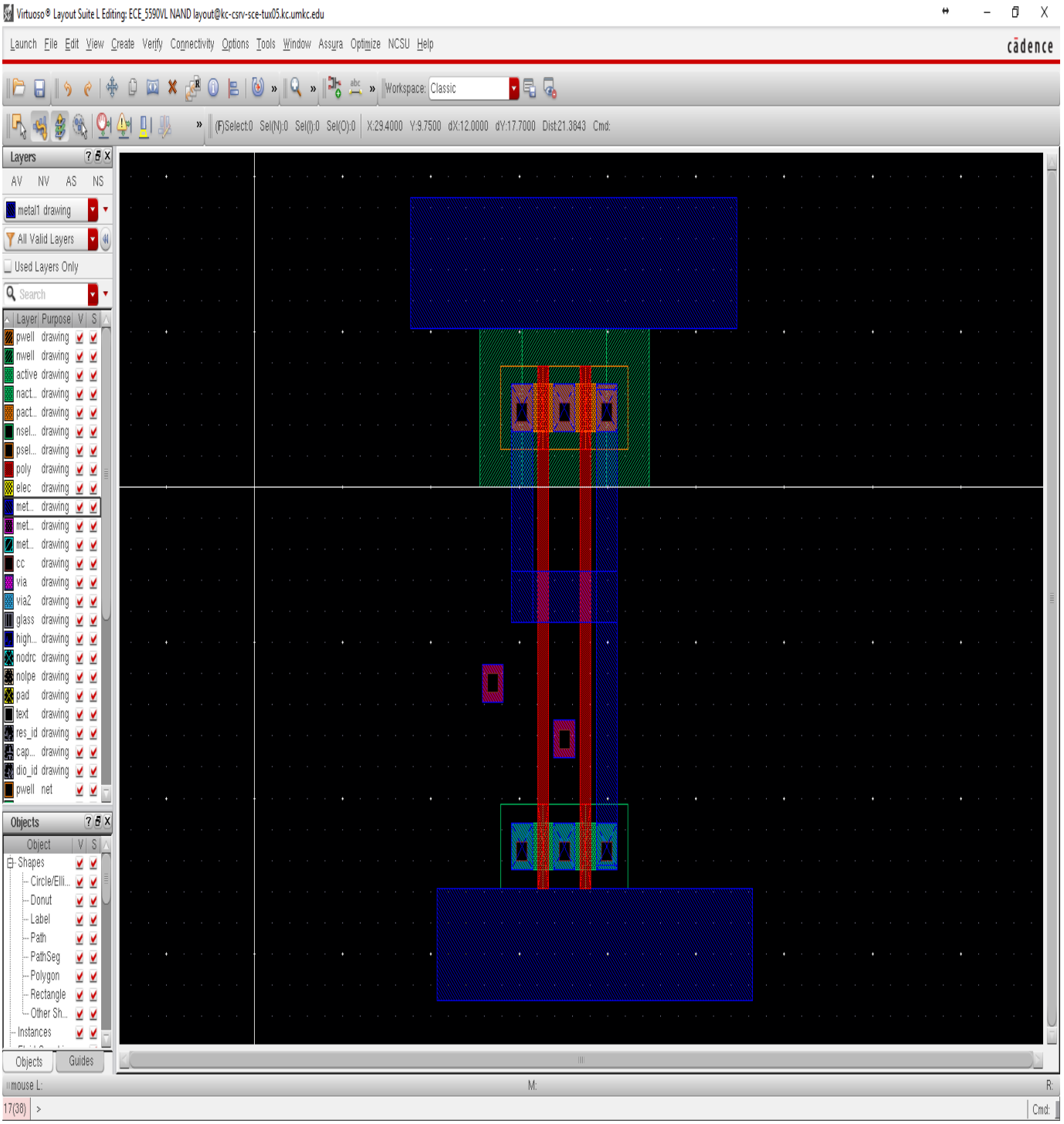
Next, add the rectangles for vdd and gnd.



Now, click on **Create → via** then the following window will appear

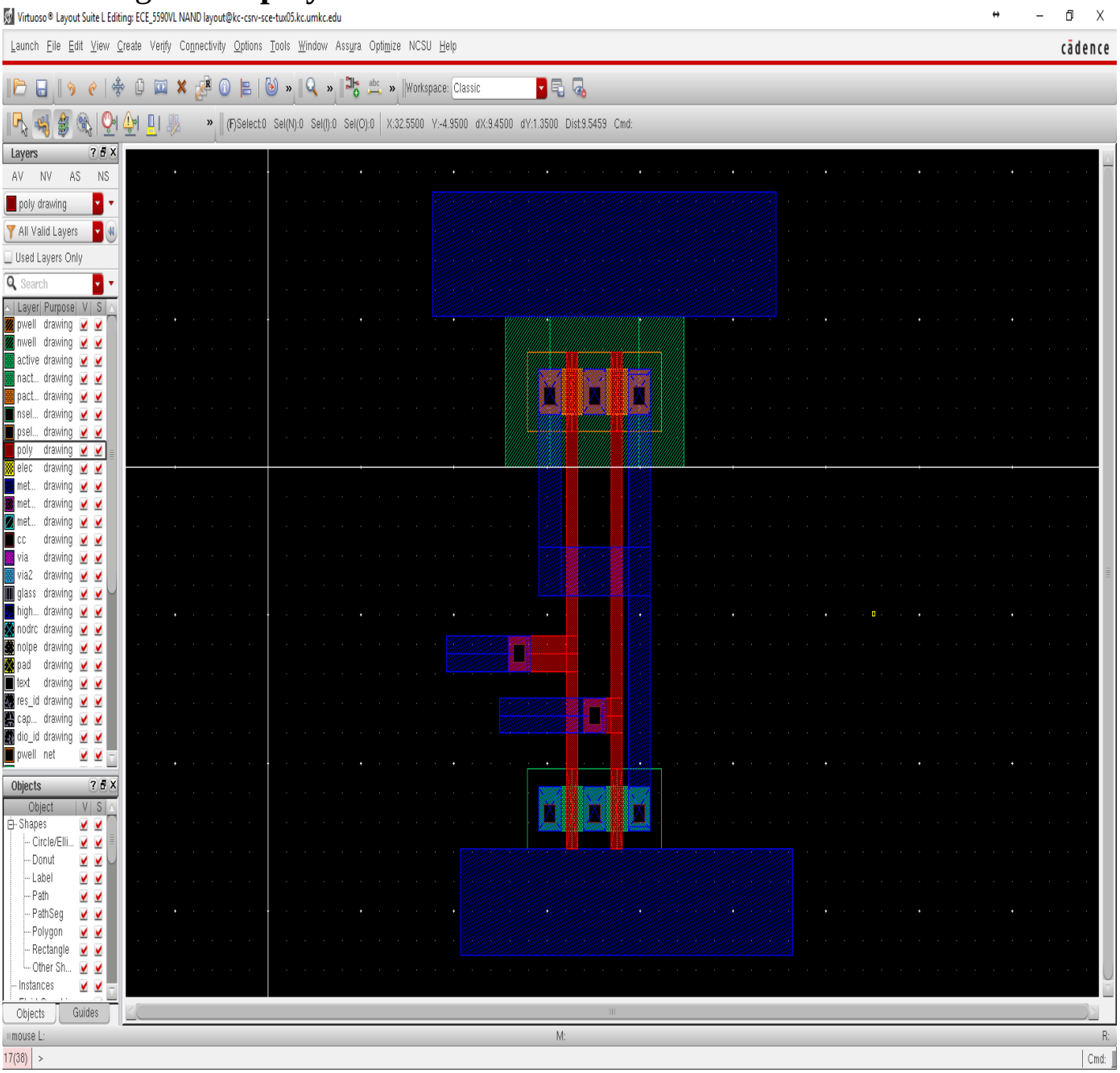


Select **M1_POLY** and place it on the virtuoso layout-editing window as shown

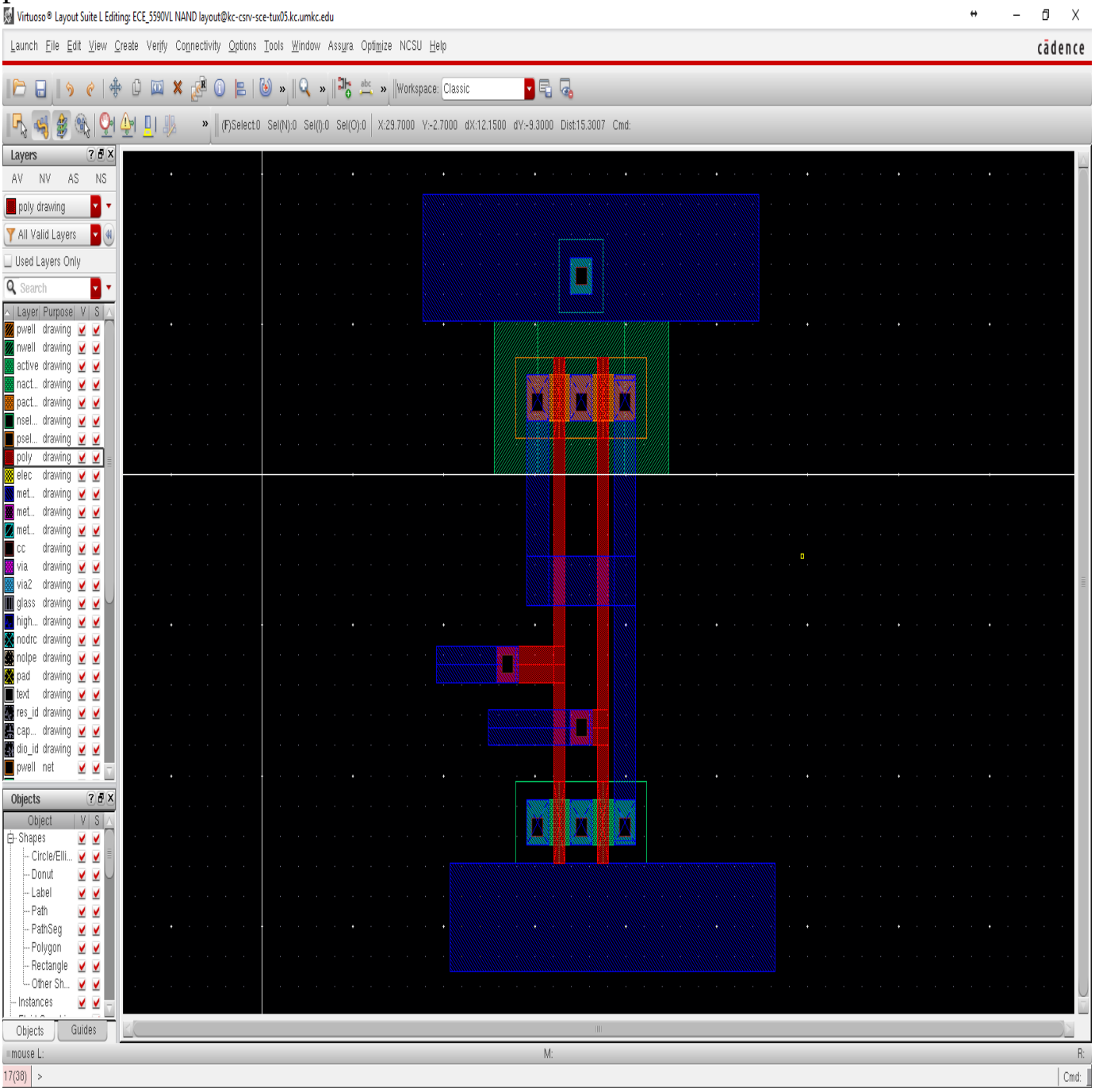


Finish the input connection by drawing the rest of the rectangles as shown.

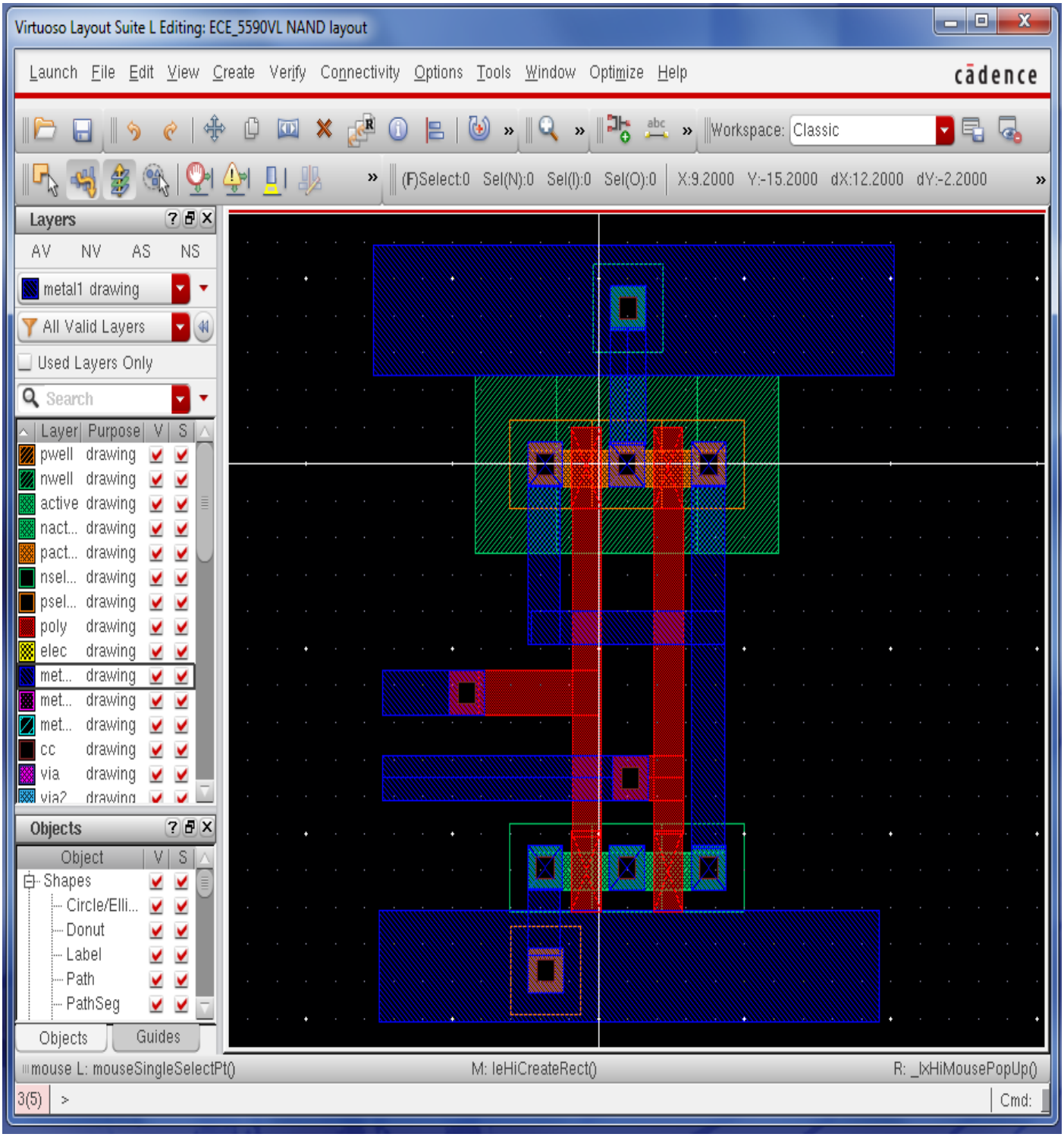
Note: you can use path '**p**' instead of **rectangle** to do the design. To change the size of **metal1**, click **p** and adjust the width to 1.2. Do the same thing for the **poly** with 0.6.



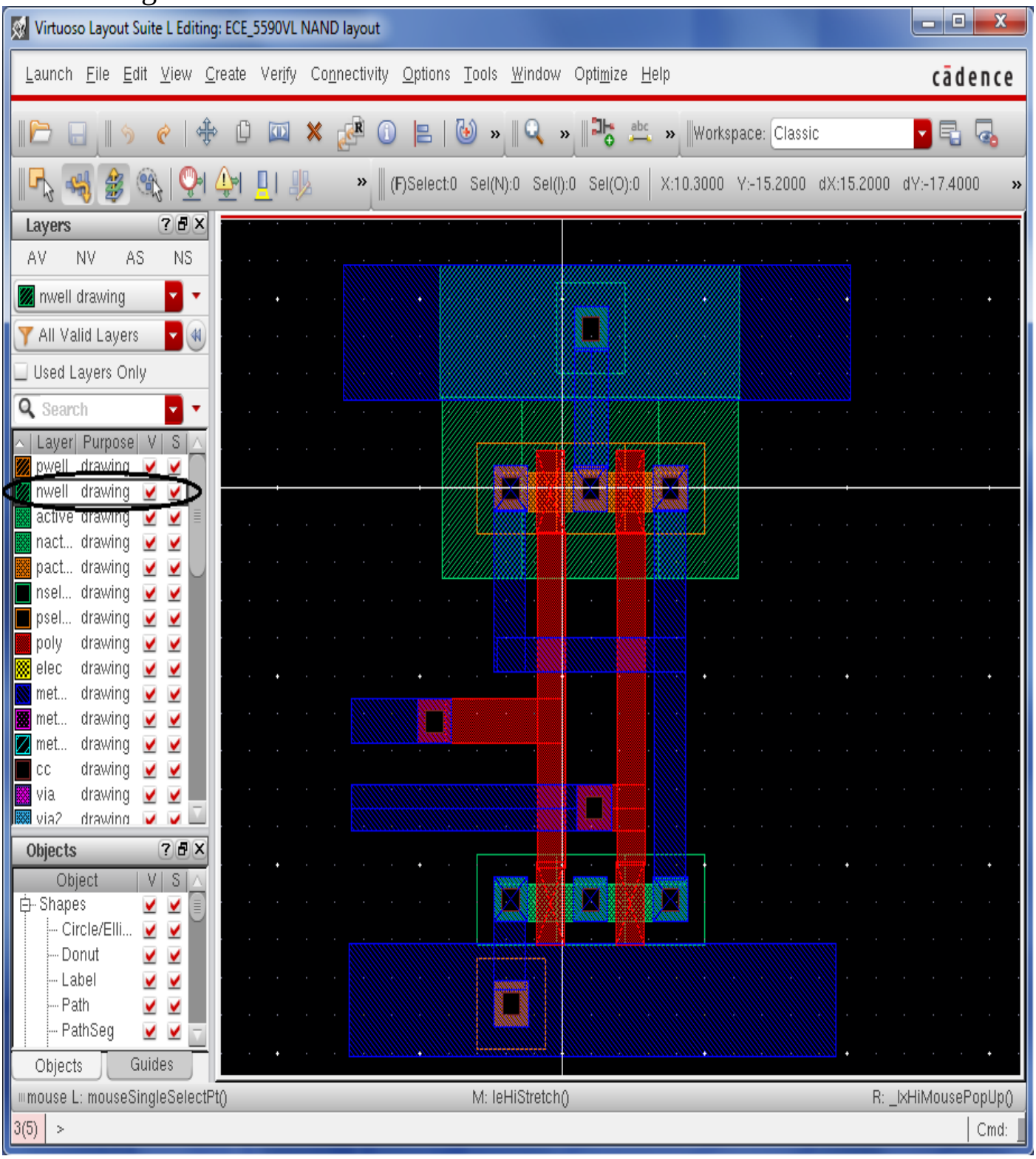
Next, click on **Create → via** then select **M1_N** from the options and place it over the **vdd** as shown.



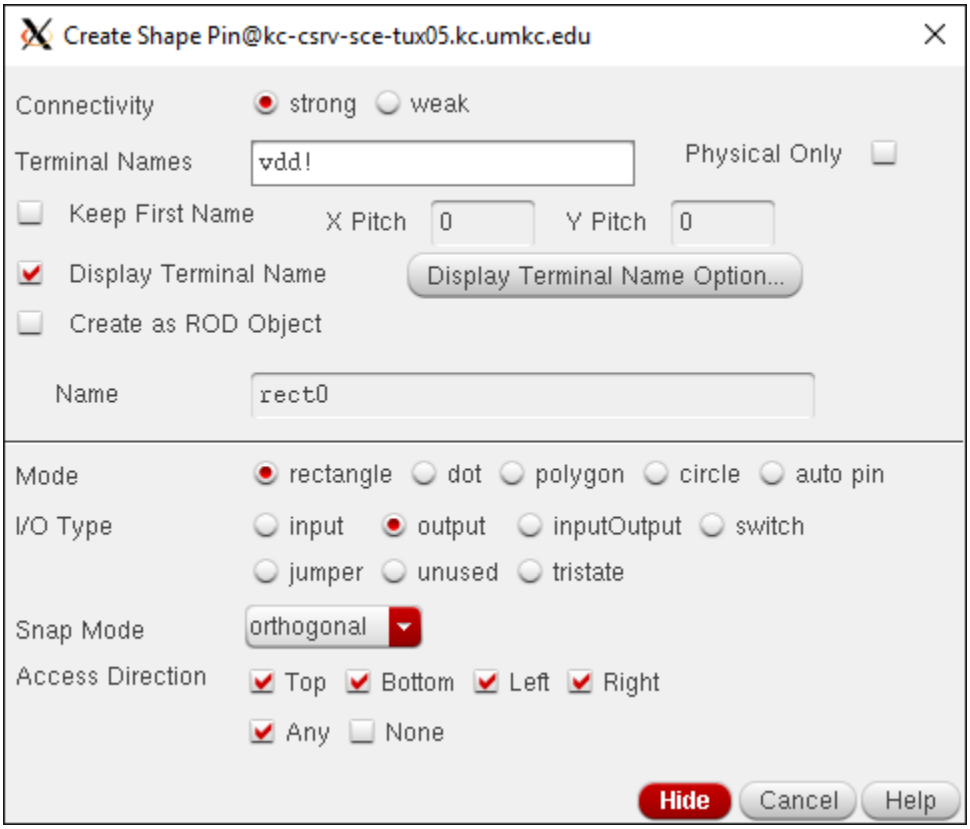
Next, click on **Create → via** then select **M1_P** from the options, place it over the gnd, and connect the source of the nmos transistor to gnd as shown.



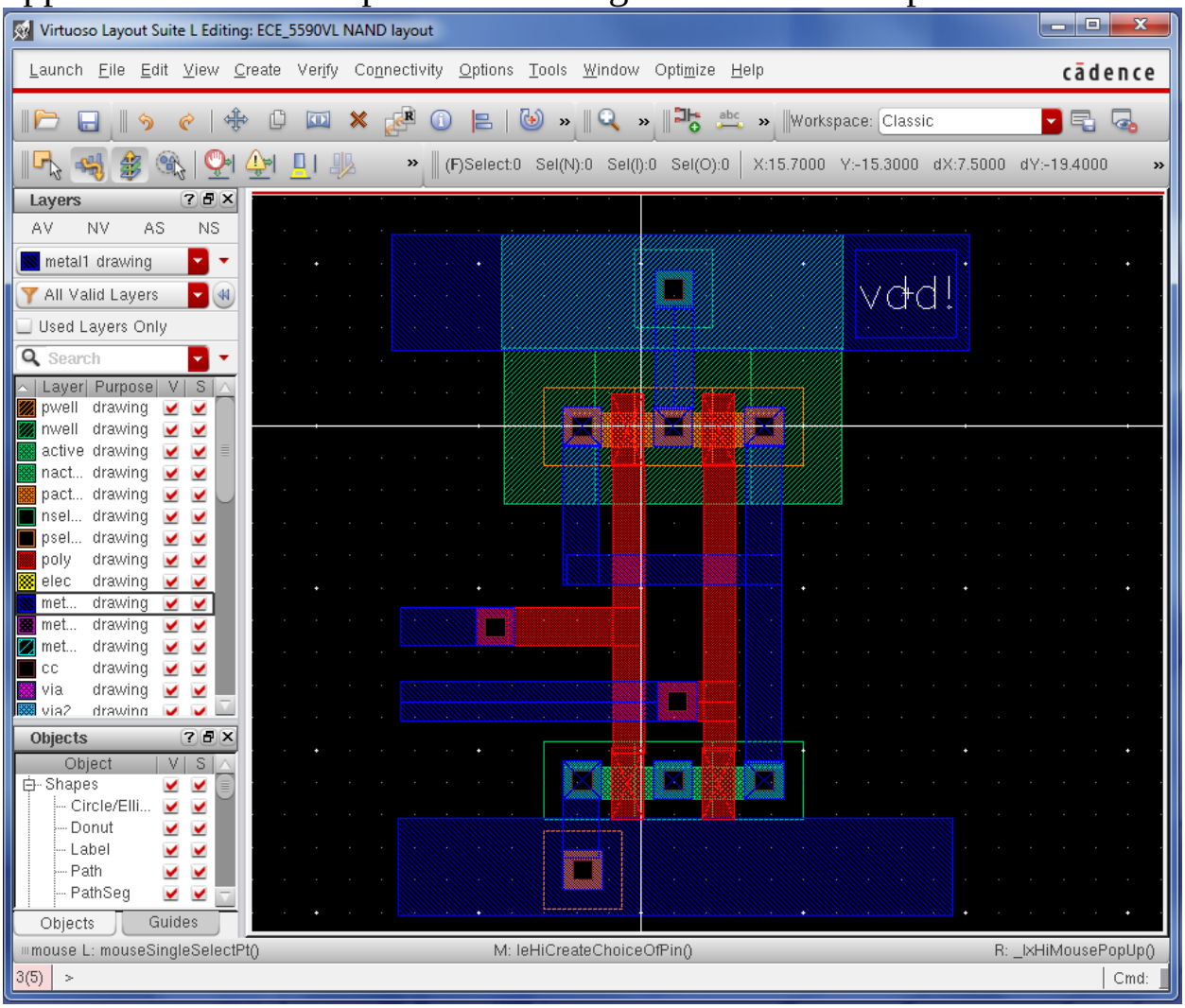
Then, extend the n-well of the pmos to cover metal1 contact by drawing **n-well** rectangle. Select **n-well** from the left side options and draw an n-well rectangle as shown.



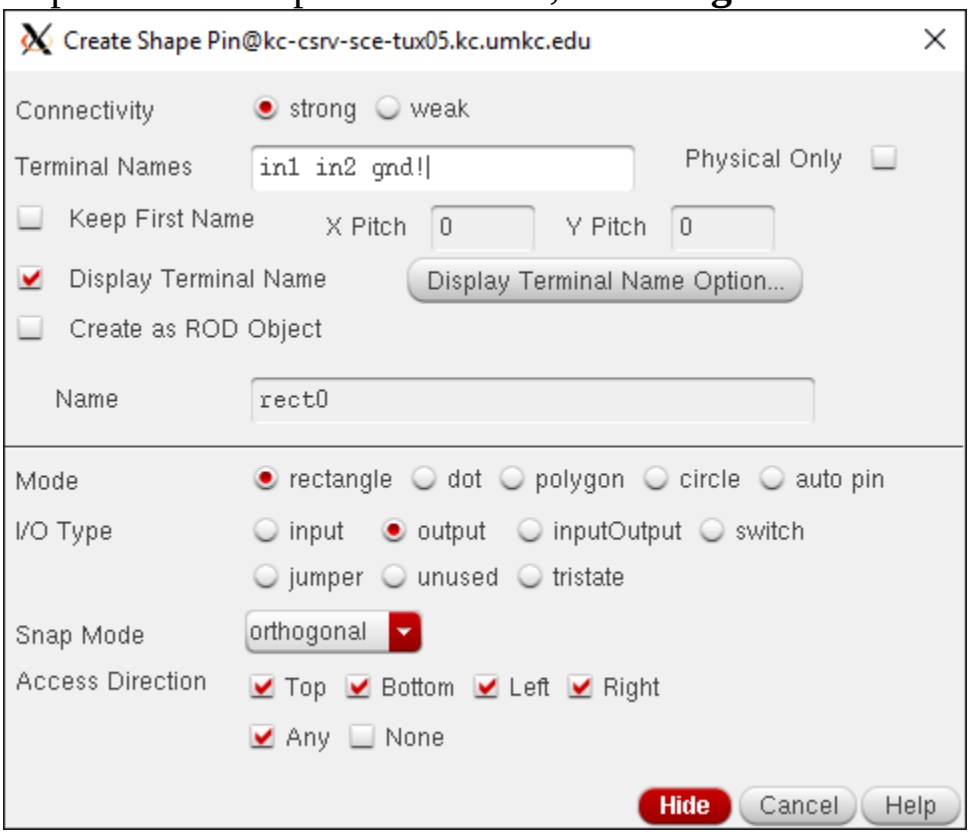
Now select **metal1** and click on **Create → Pin.** When create shape pin window appear type in vdd! and select **input** and **Display Terminal Name** as shown.



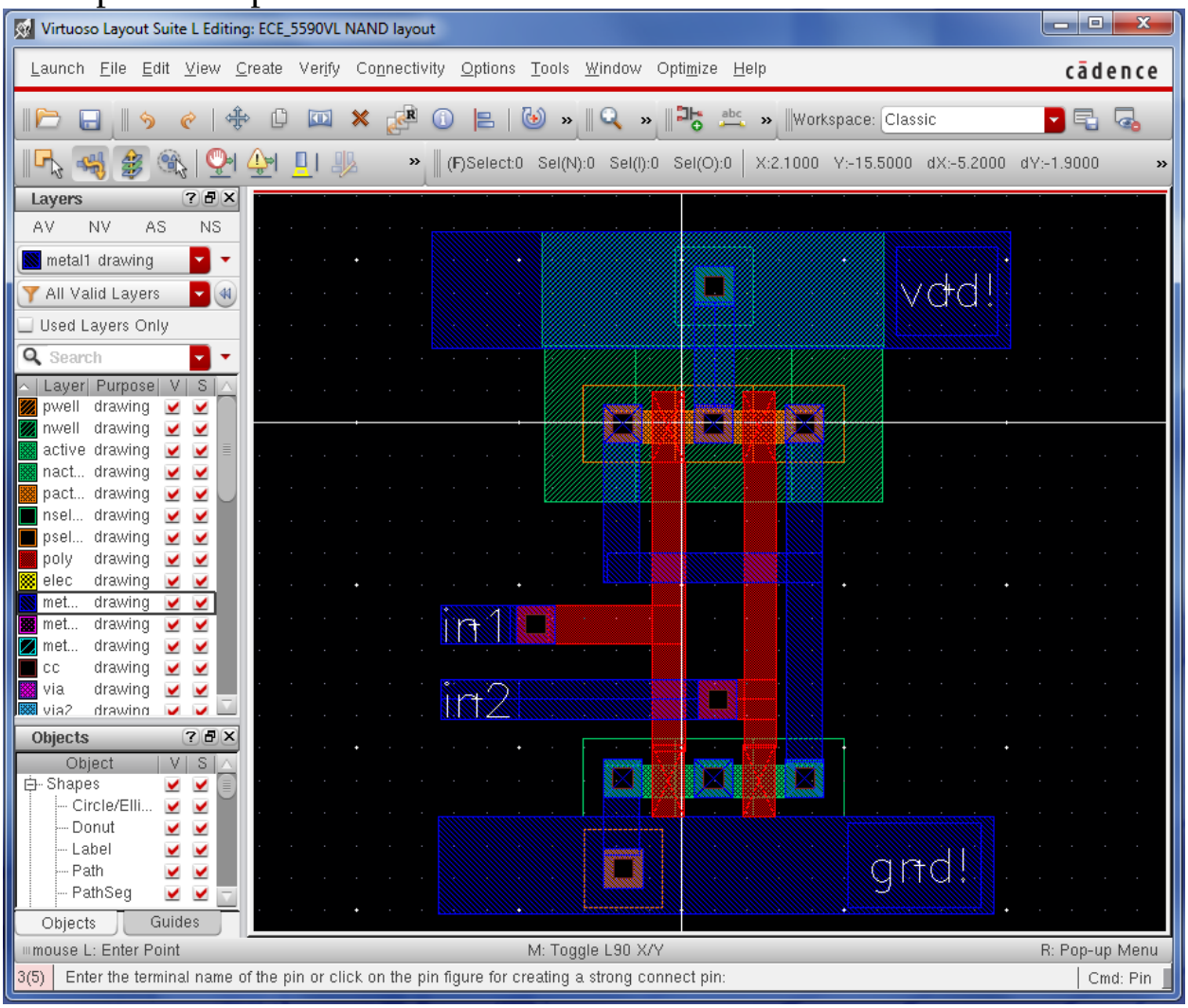
Then place the pin as shown.
Note: To place the pin select one corner of a rectangle then move to the opposite side and complete the rectangle then insert the pin.



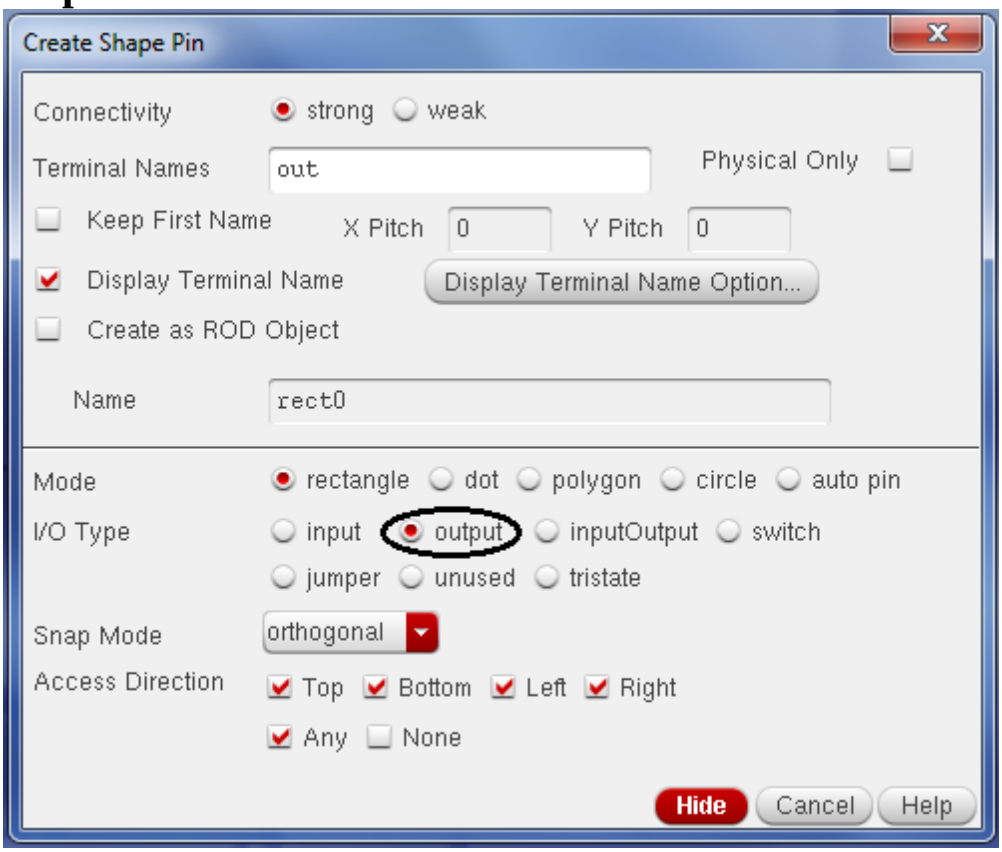
Repeat the same process for **in1**, **in2** and **gnd!**



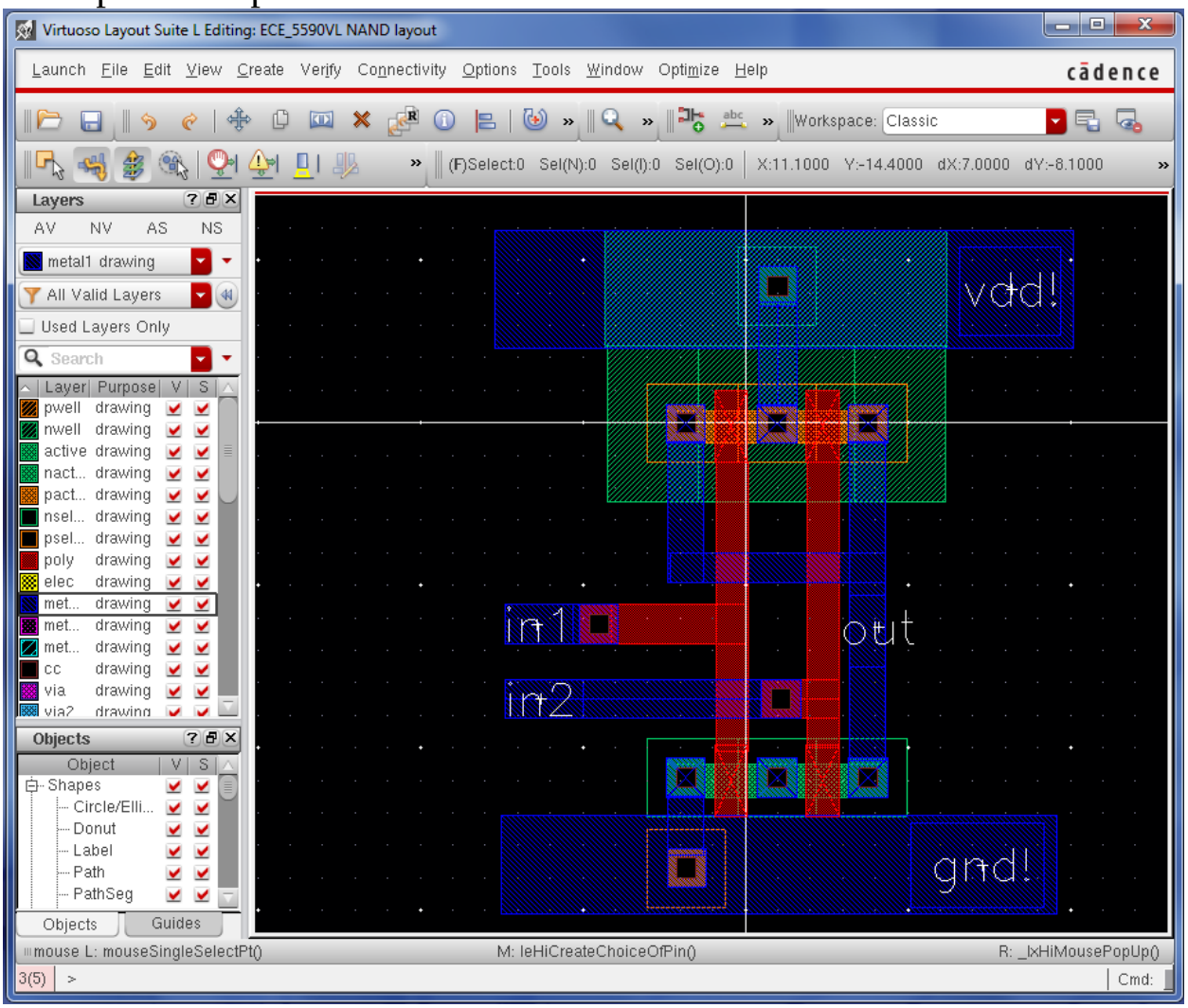
Then place the pins as shown.



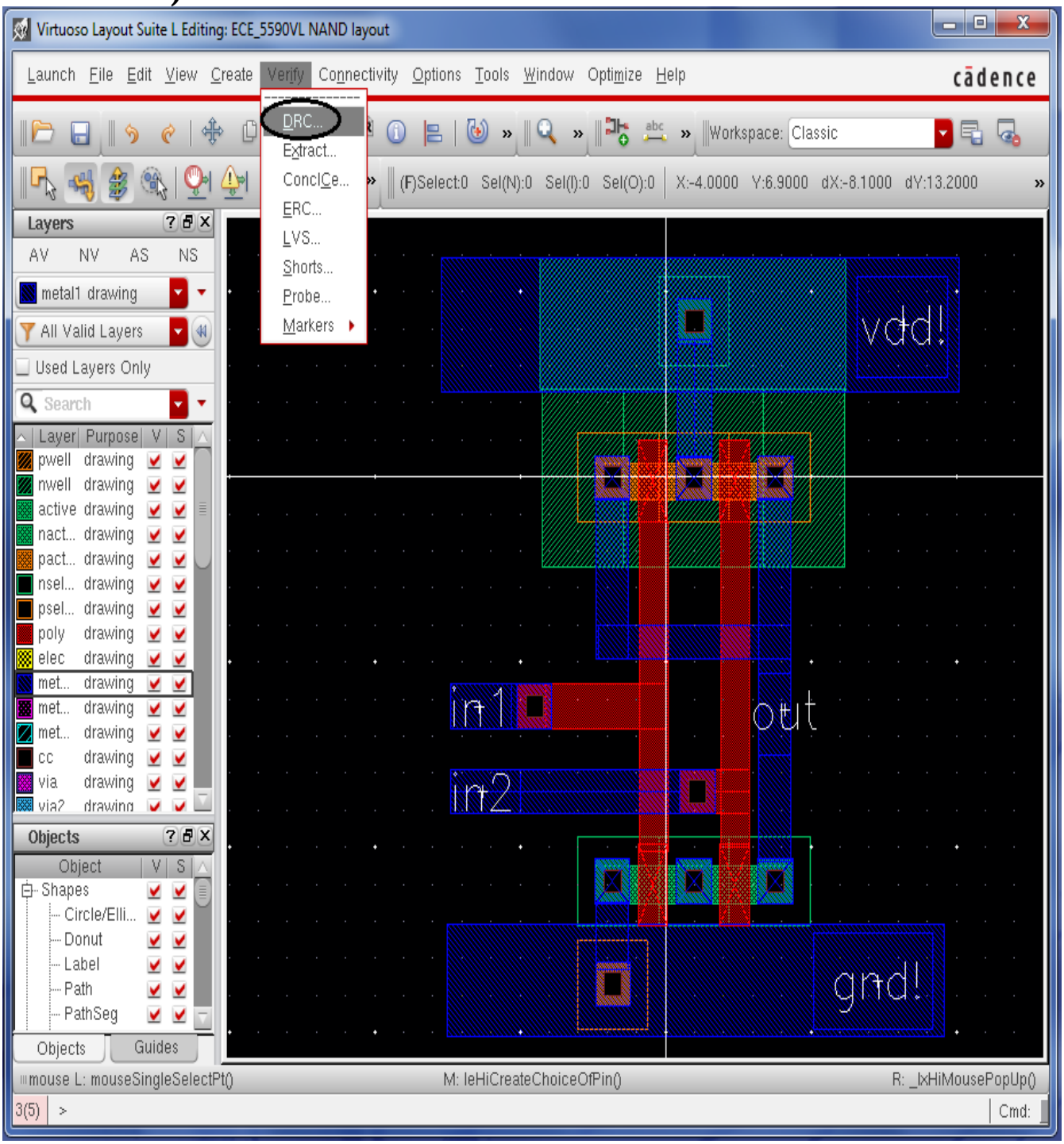
Repeat the same process for output but change the I/O selection to **output** as shown.



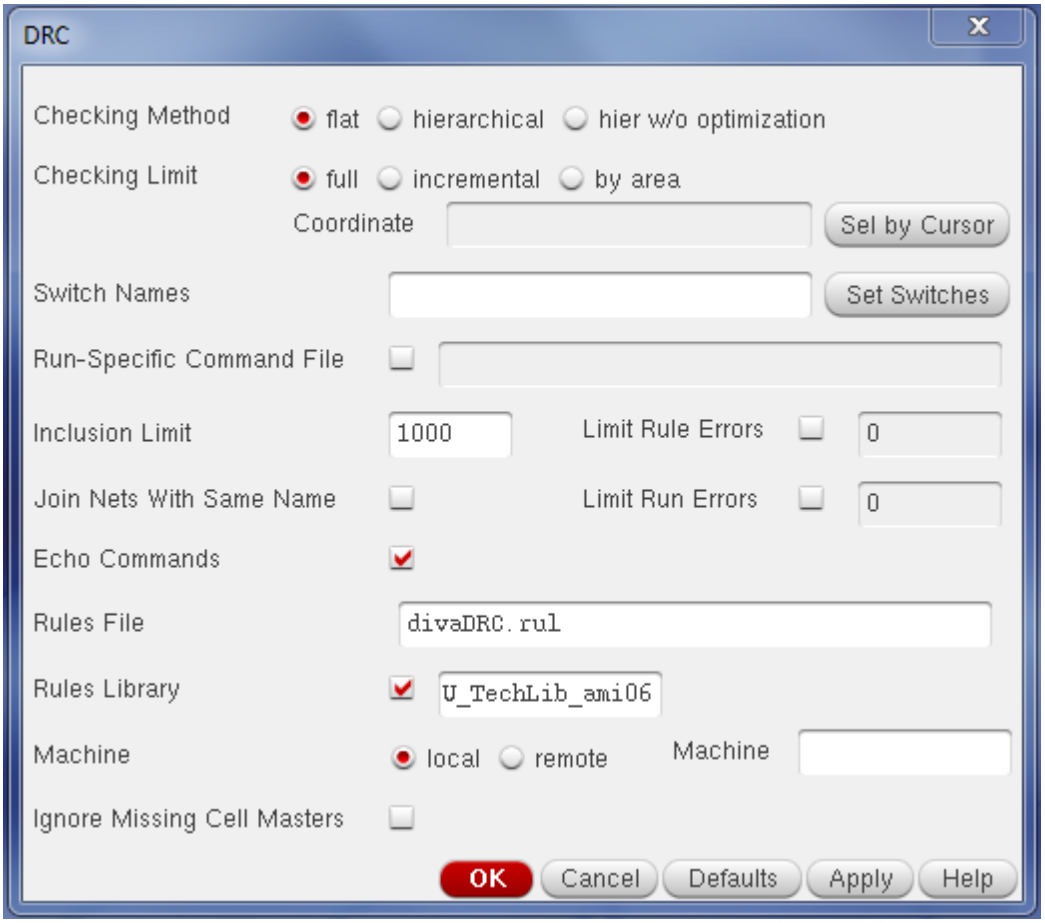
Then place the pin as shown



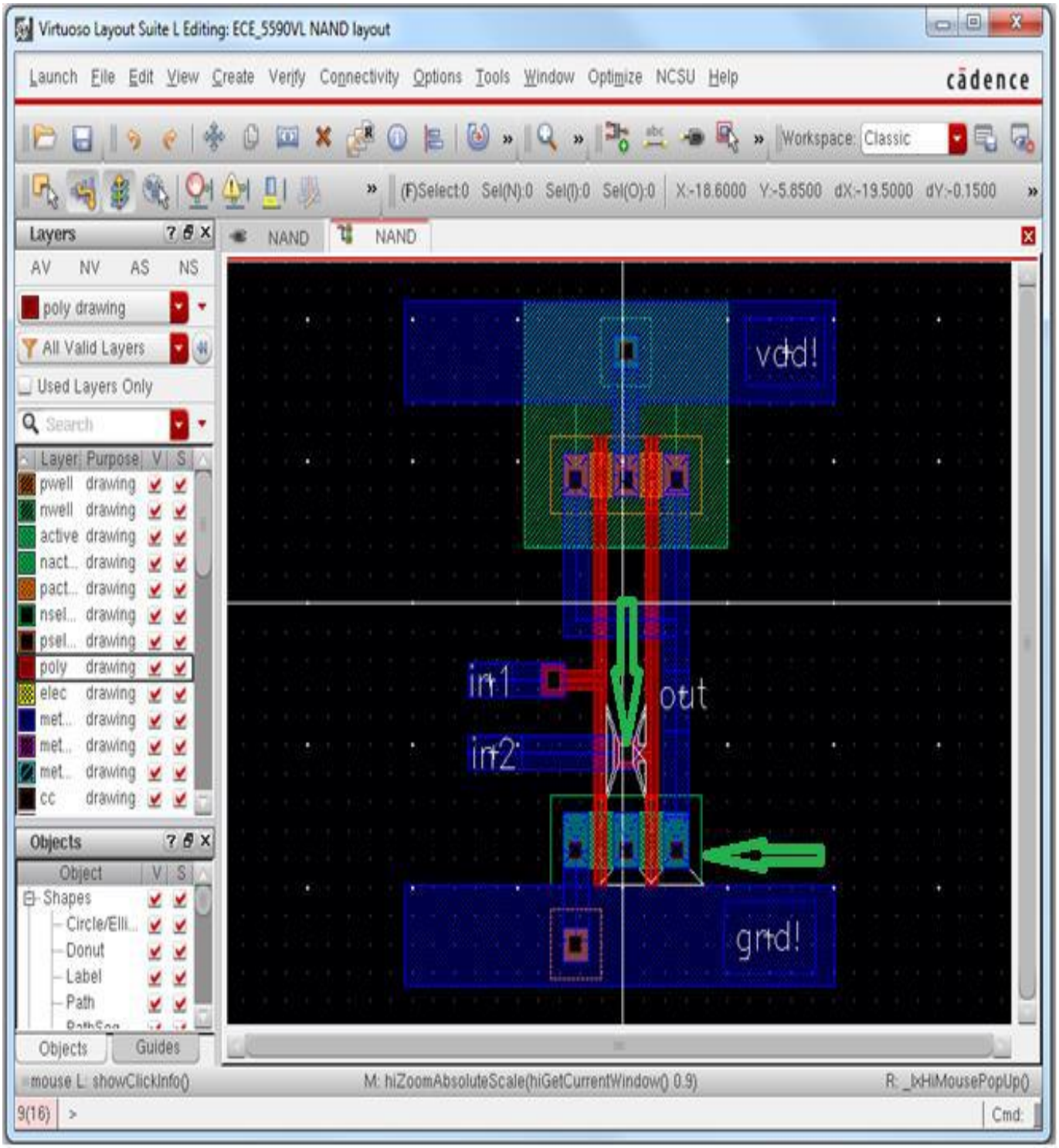
PART II: You will check the layout for errors and create extracted view
To verify the correctness of the design click on **Verify → DRC (Design Rule Check)**



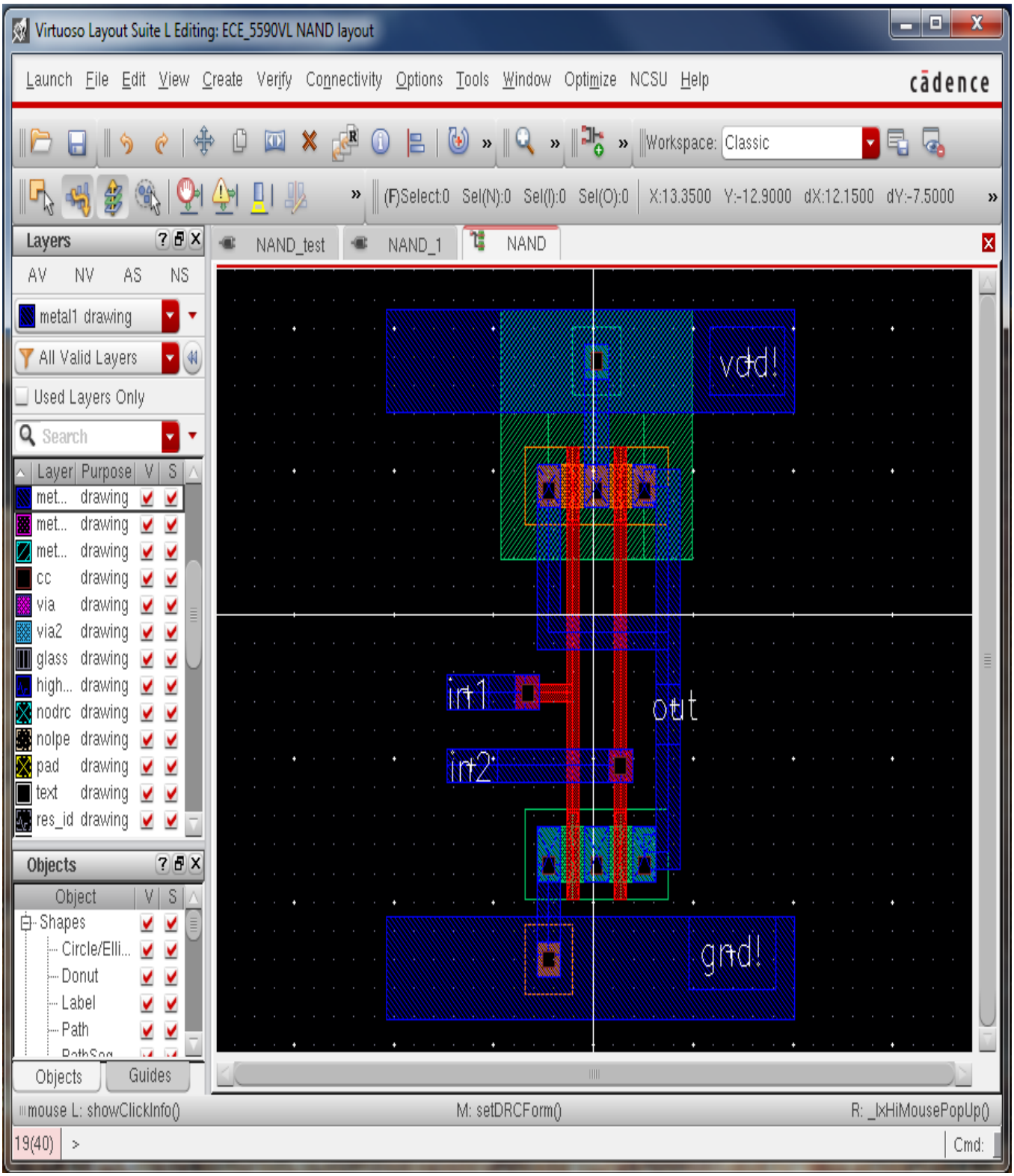
When the DRC window appears, click **ok**.
Note: The **Rules File** box should show **divaDRC.rul** and the **Rules Library** box should show **U_TechLib_ami06**.



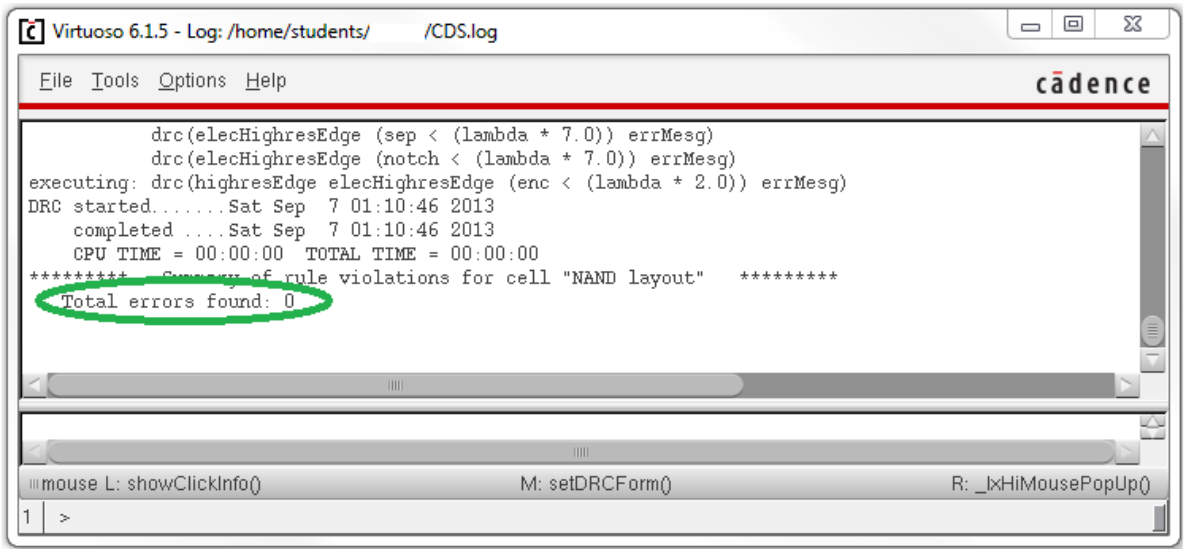
The errors on the design are shown with white lines in the following window.



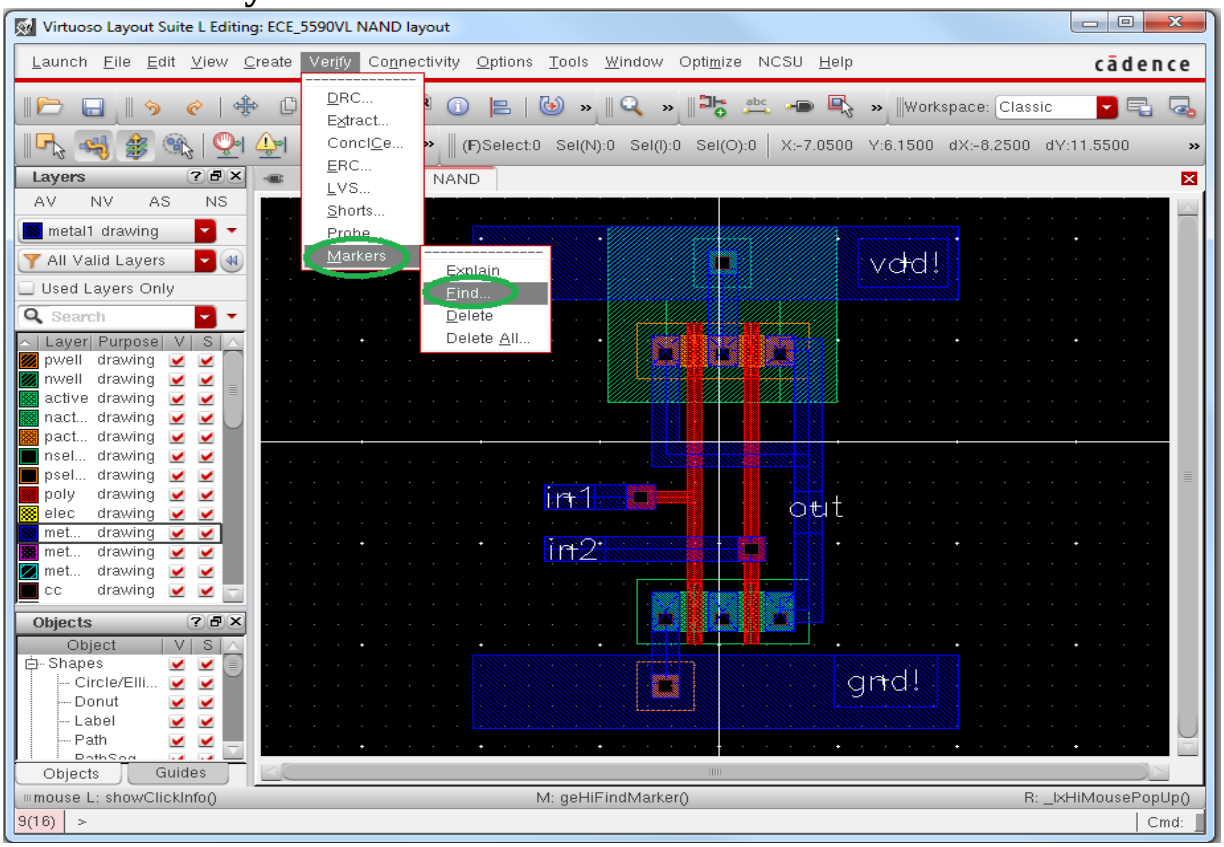
After fixing the errors the white lines disappeared as shown at the bottom



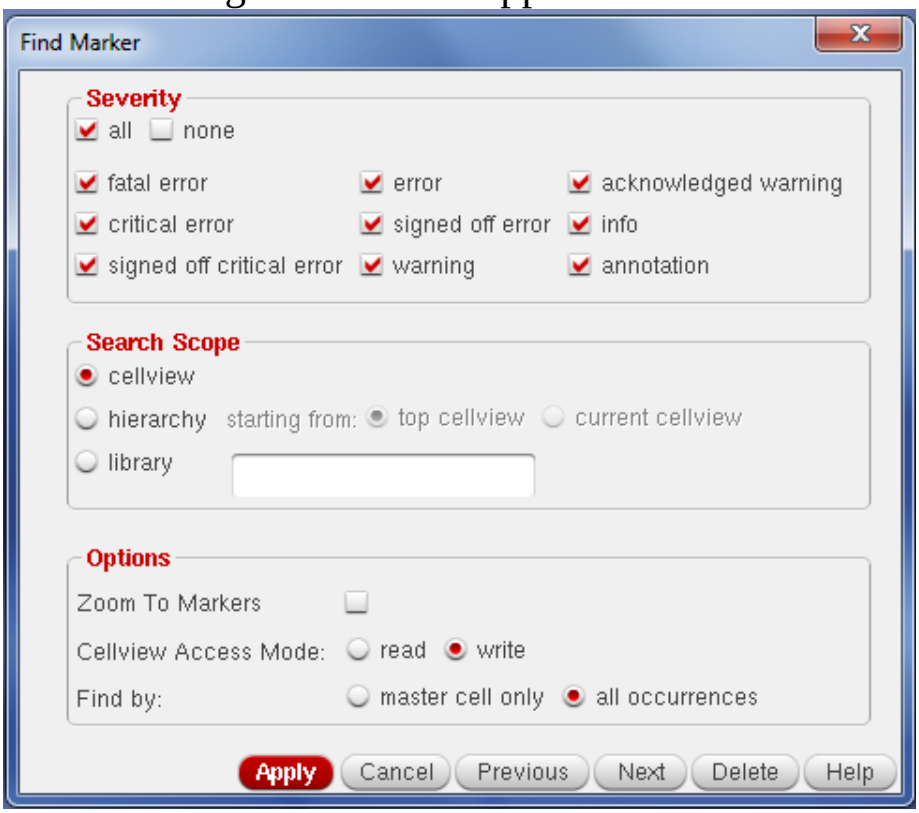
Your **CIW window** should show no error.



You can see where are the error by this option
click on **Verify → Markers → find.**

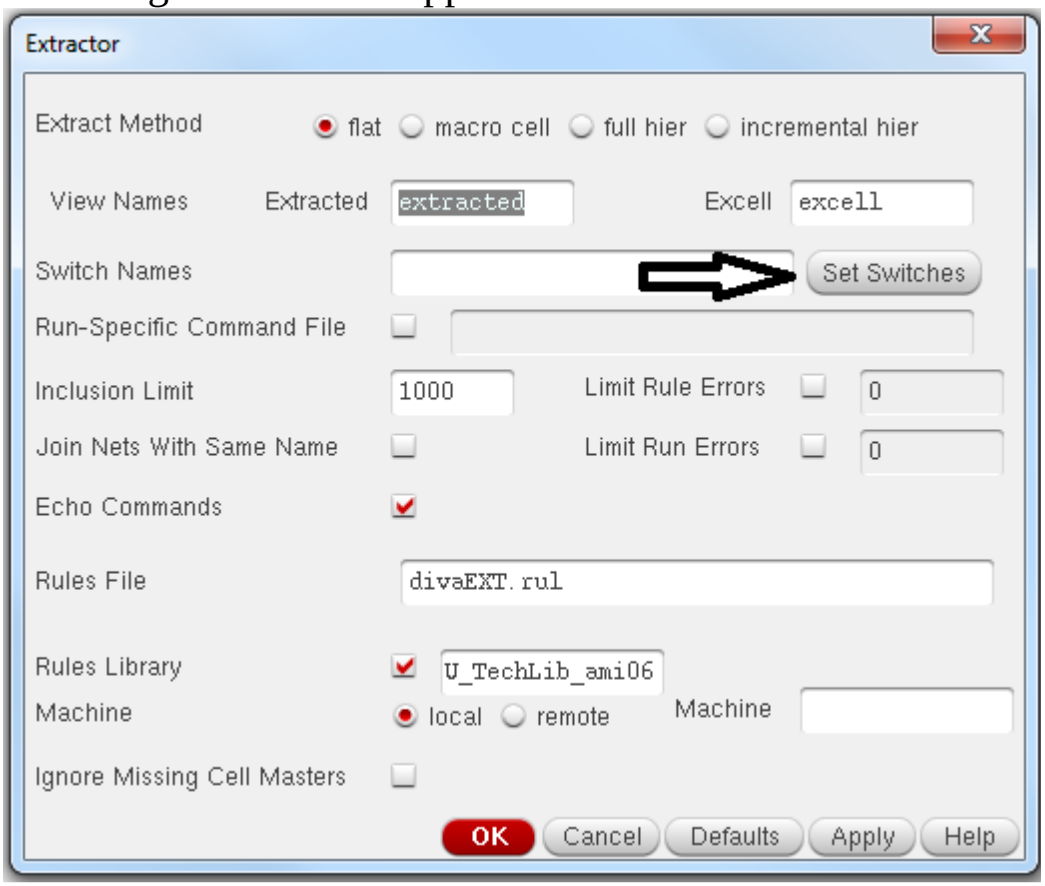


The following window will appear

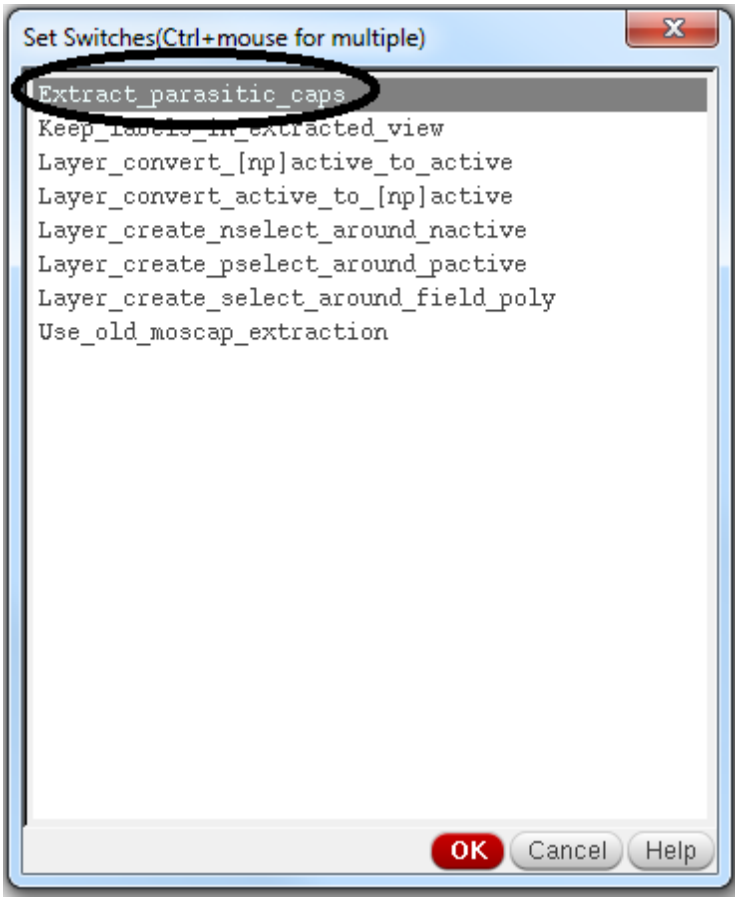


On the above window, you can check or uncheck any of the selection options you would want to find out and click on **Apply**. Then, a window will open with detail error information.

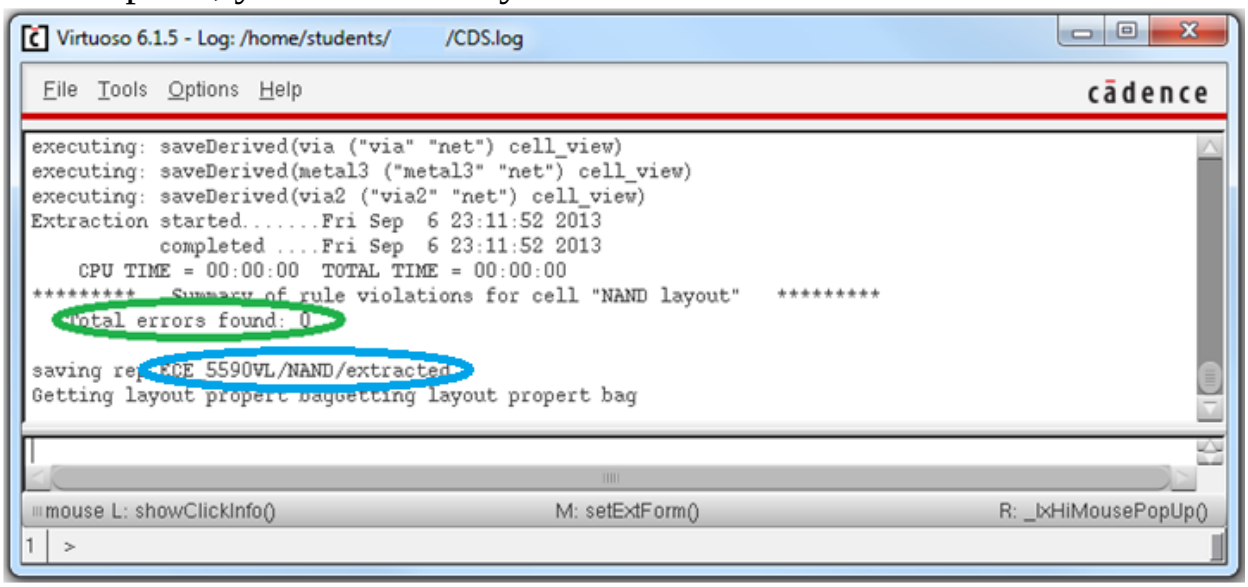
Once you are done with the layout and checked for errors, continue following the tutorial to create the extracted view.
On the Virtuoso Layout window, click on **Verify → Extract**. Then the following window will appear.



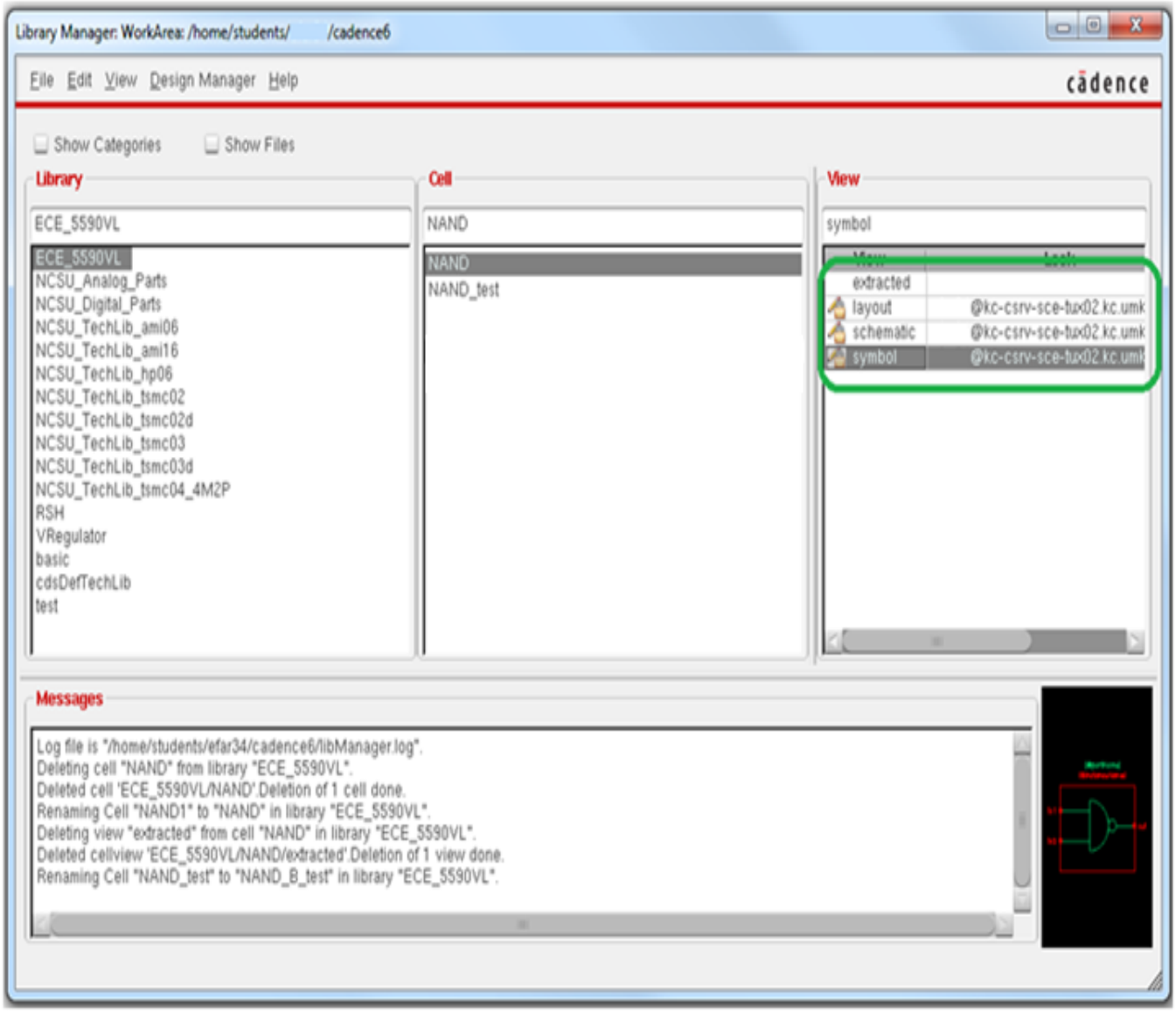
On the Extractor window, click on **Set Switches** key and select **Extracte_parasitic_caps** and click **ok**. Then click **ok** on the **Extractor** window.



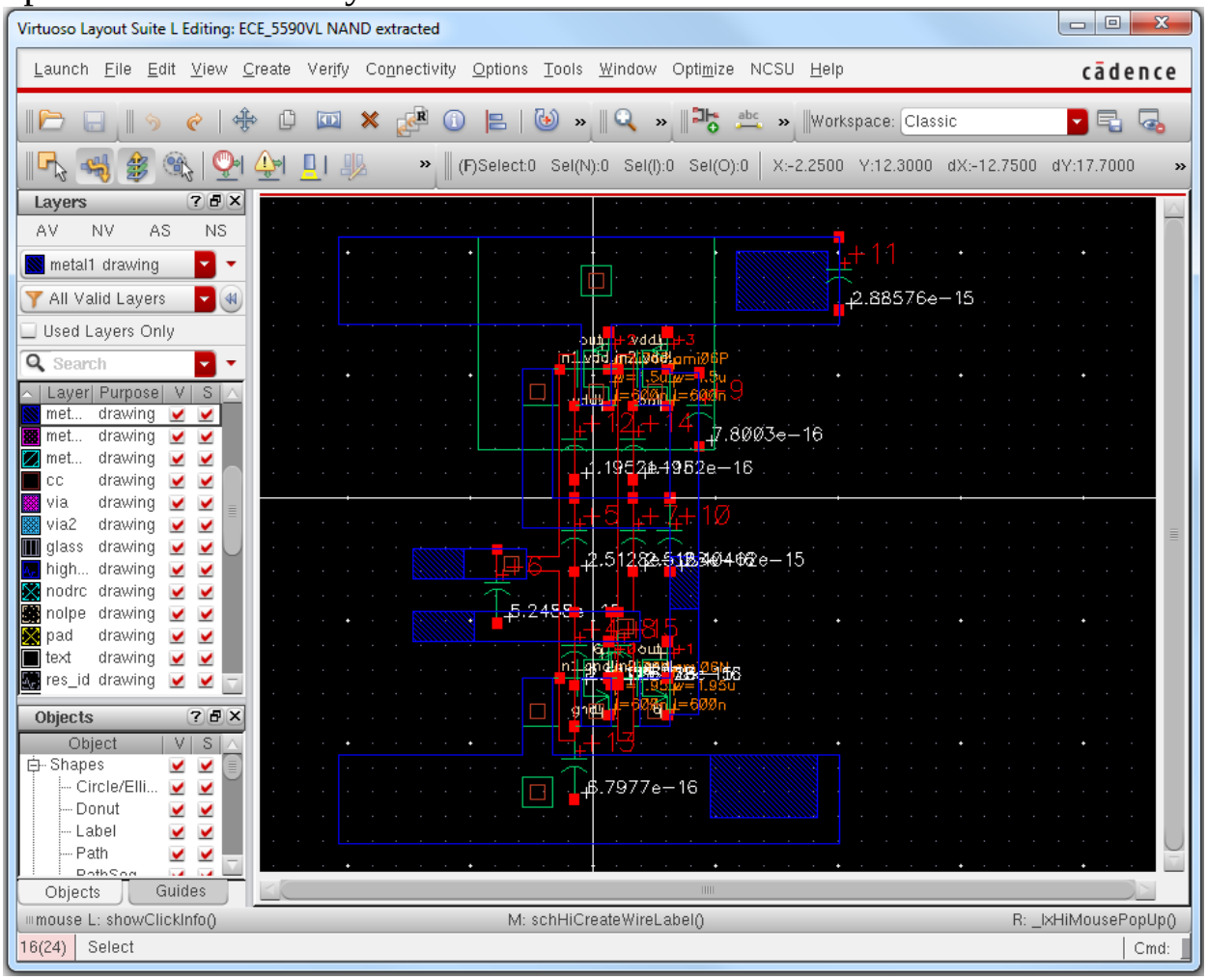
At this point, you should see your **CIW window** with no error



Save your design by clicking the save button on the Virtuoso Layout window. After that, go to your **Library Manager Window** to see your extracted cell as shown below.



By double clicking the **extracted** file under the **View** folder, you can open the extracted layout as shown below.

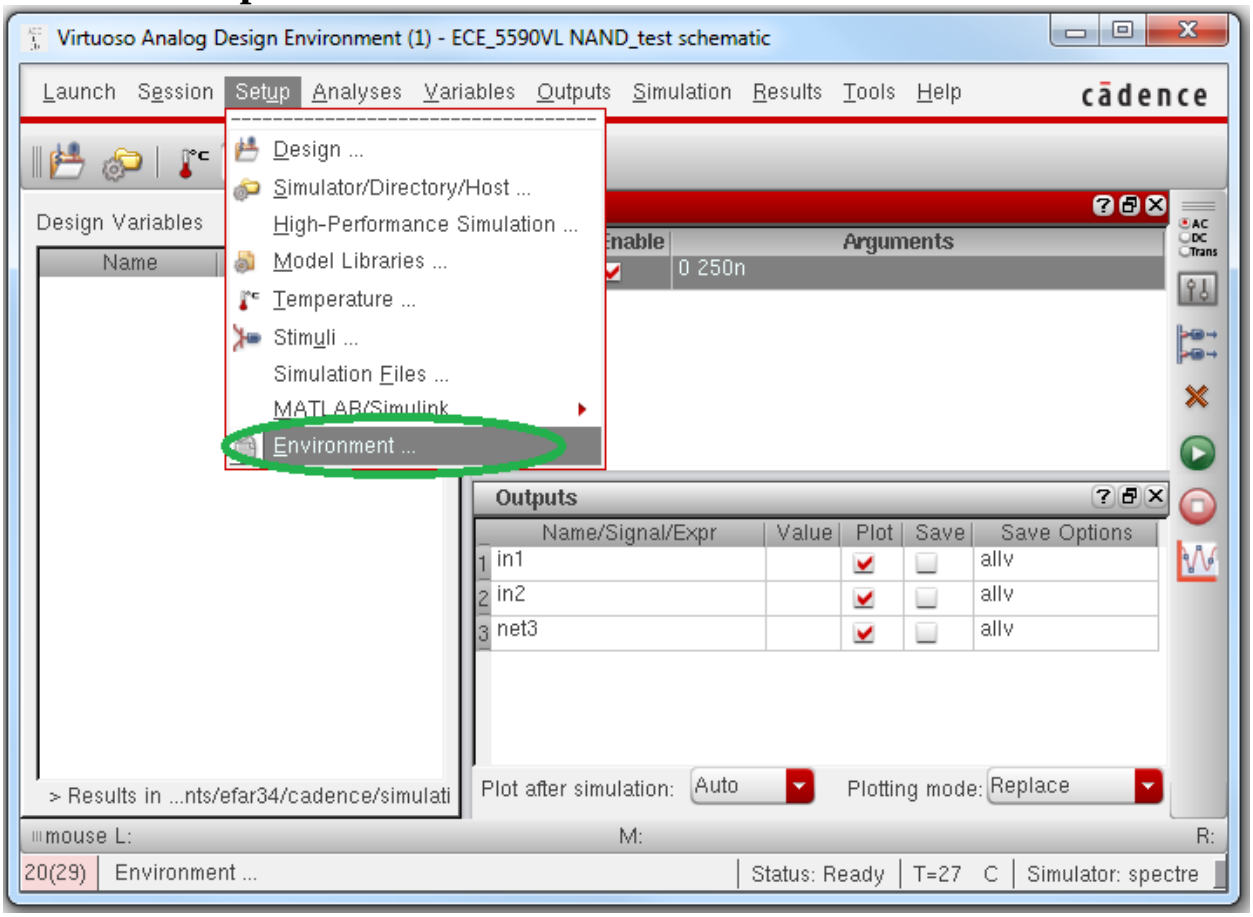


To see the name of the each component press **CNTL + f** and to go back to the default view press **Shift + f**.

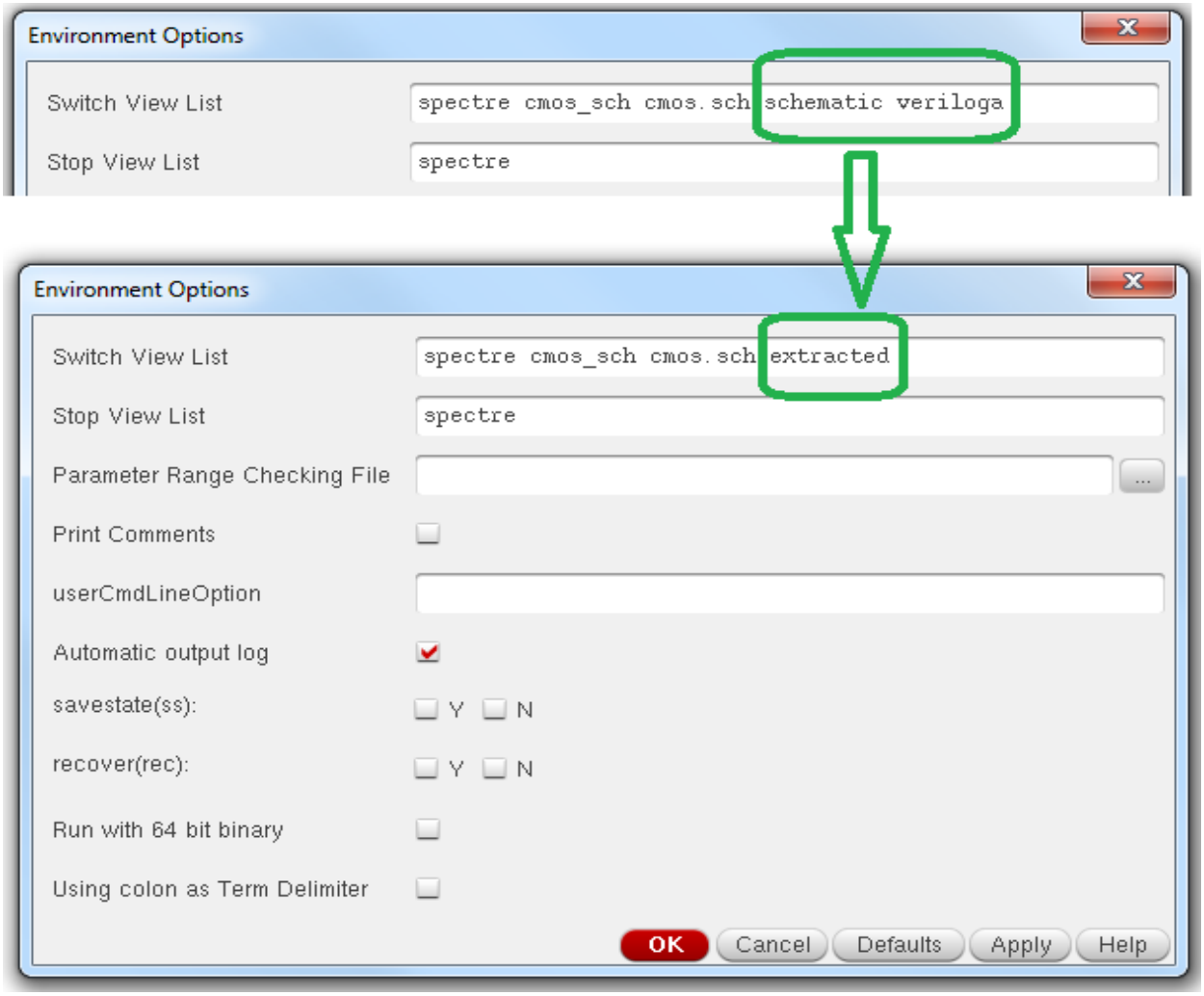
Note: The capacitors shown on the extracted window are the parasitic capacitors.

At this point, save and close all the windows except the **CIW** and **Library Manager Window**. Then open **Nand_test** schematic file. After that, follow the same simulation procedure to setup the **Virtuoso Analog Design Environment** window as previously given in tutorial 2. You only need to add the steps provided at the bottom.

Click on **Setup → Environment**

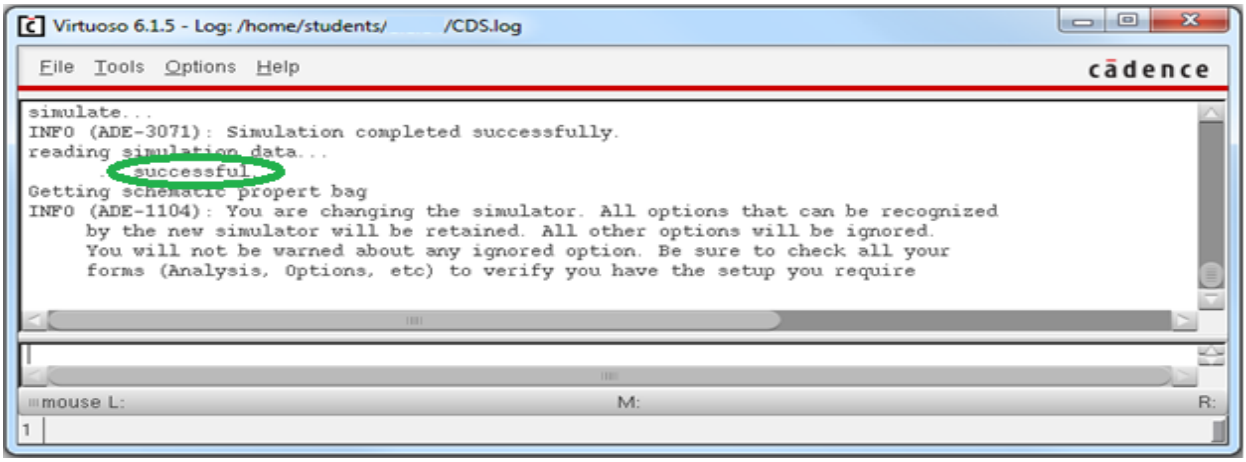


On the **Environment Options window** change the **Switch View List** as shown.



Perform the simulation as you did in the last tutorial, the output waves should show the behavior of NAND gate.

Your **CIW** window should be free of error.



This tutorial was prepared by Emeshaw Ashenafi and Dr. Masud Chowdhury.

For additional reference please find and review:

Tutorial prepared by Mohammad Benyhesan
Tutorial prepared by Dr. Daniel Leon-Salas
Also, other tutorials available on the internet.

Acknowledgment:
This tutorial was prepared with the reference previously prepared by Dr. Walter Daniel Leon-Salas and Mohammad Benyhesan.