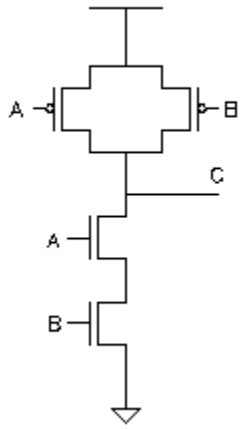
Tutorial 2: Cadence Schematic

Objective:

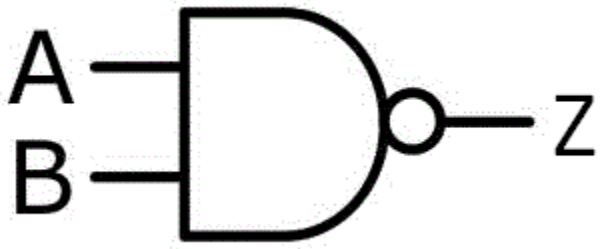
To introduce the Cadence Virtuoso Schematic and Cadence Analog Design Environment

Procedure:

1. You will draw the schematic for NAND gate in Virtuoso Schematic



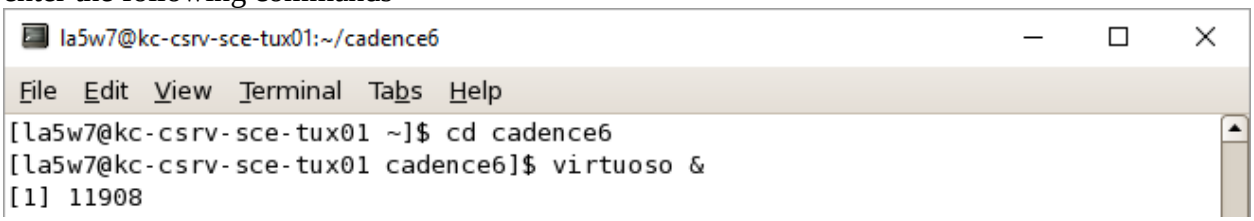
2. Test/Simulate you NAND schematic in ADLE
3. Draw a symbol for your NAND circuit



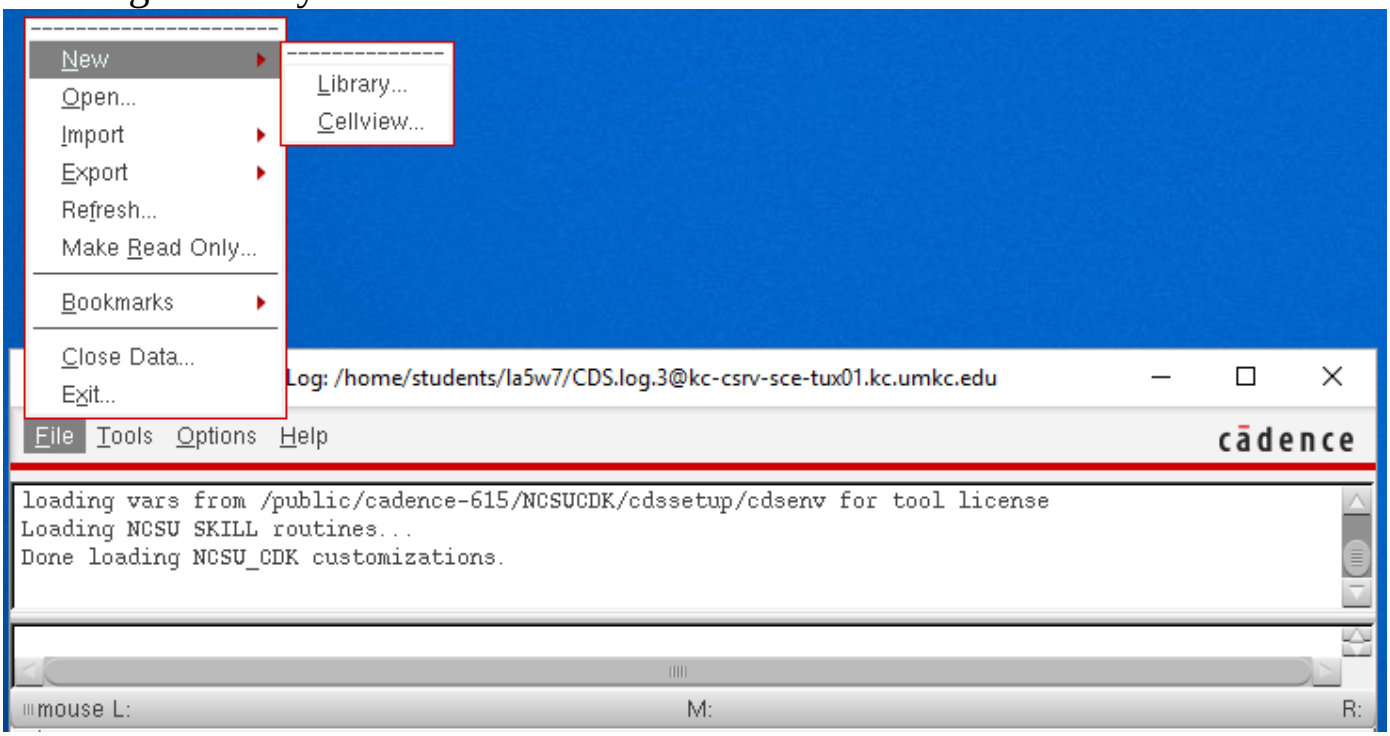
4. Test/Simulate your NAND symbol

First perform the tutorial one again. I have summarize the last tutorial here

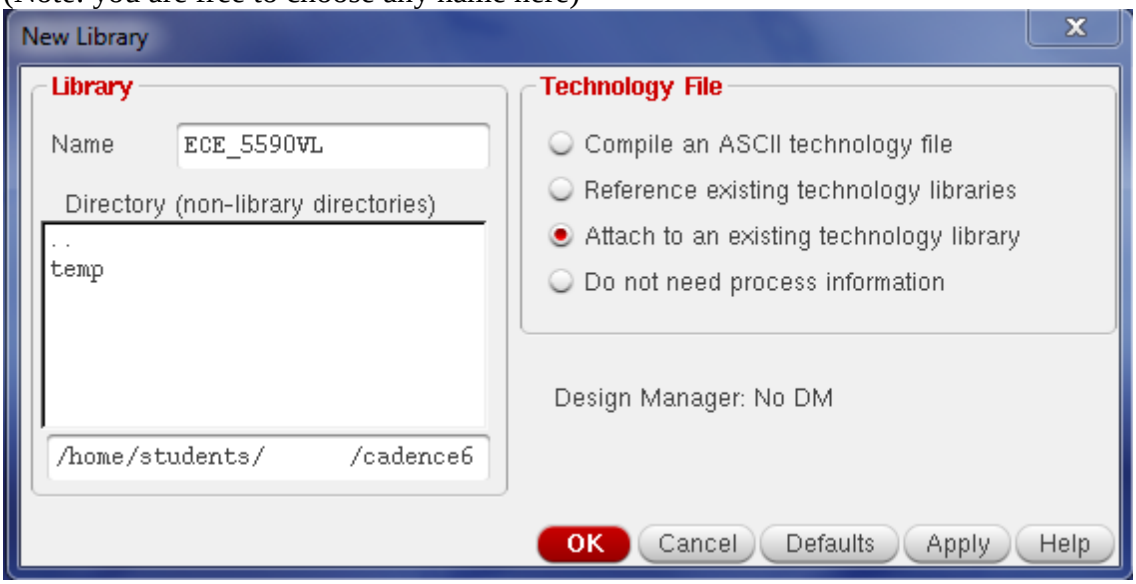
Open the cadence software → Enter your UMKC password → It will open a terminal and then enter the following commands



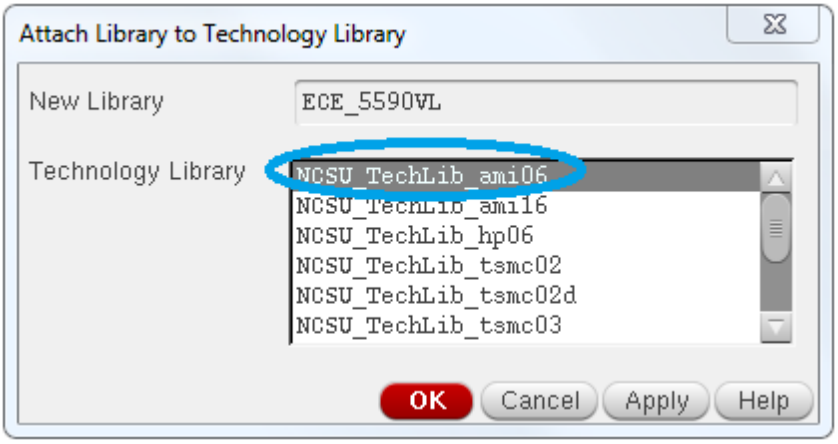
Creating a Library:



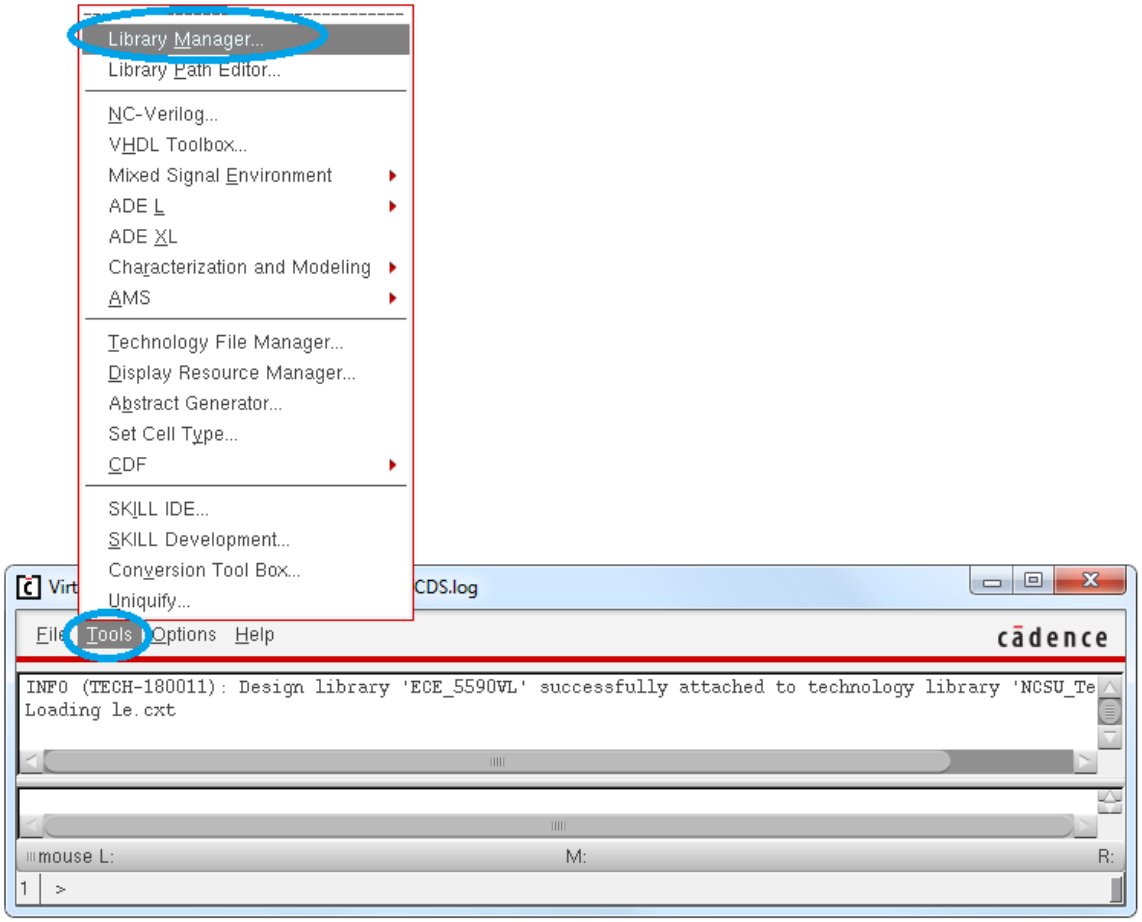
On the New Library window, put a name, click on Attach to an existing technology library button, and then click ok.
(Note: you are free to choose any name here)



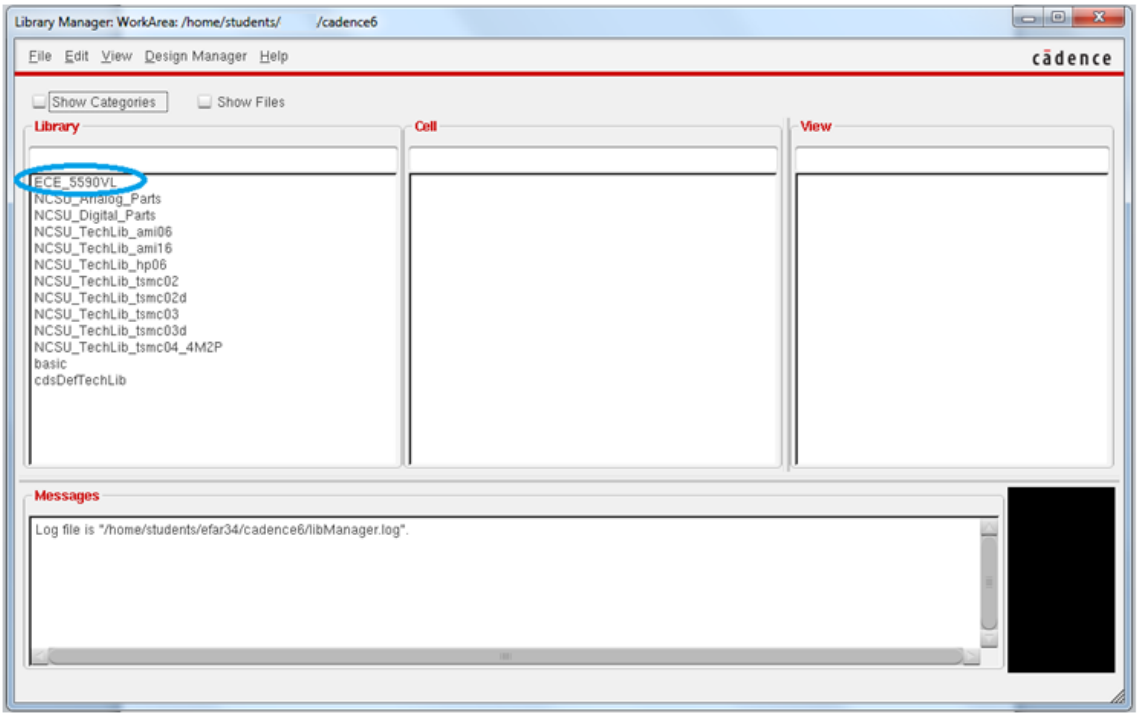
Click on NCSU_TechLib_ami06 → ok on the library window



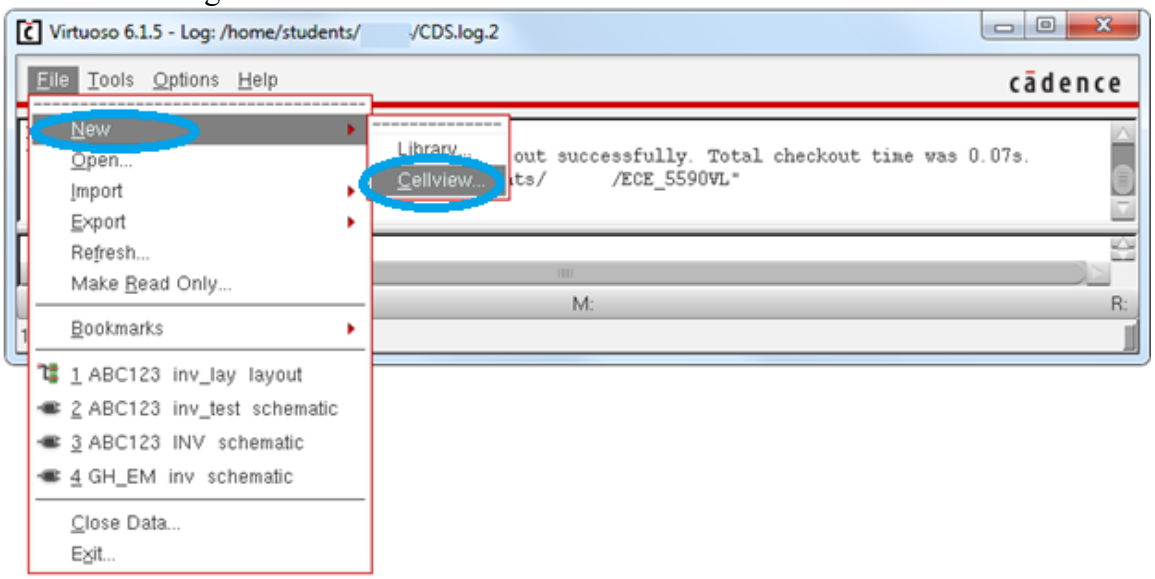
To make sure you have created the library file correctly click on Tools → Library



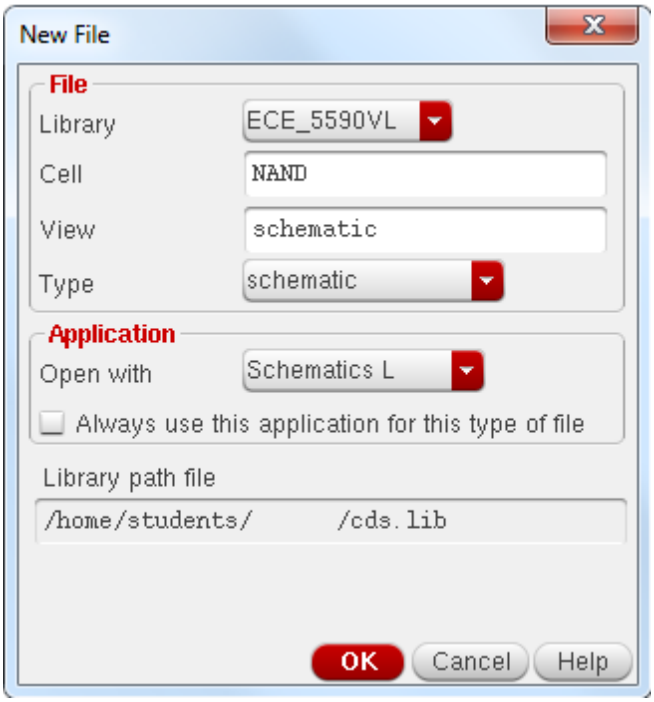
You should see your library file as shown



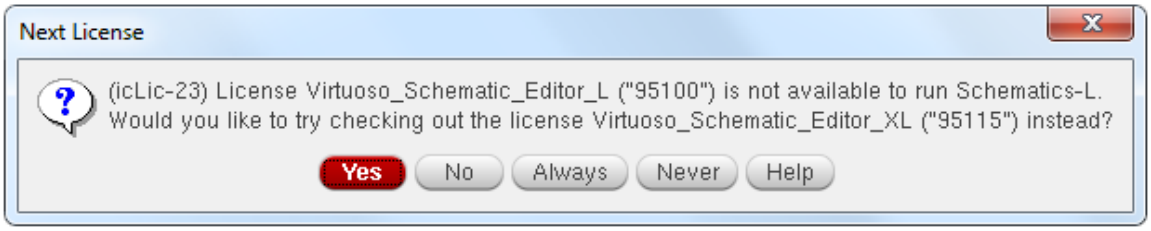
On the following window click on File → New → Cellview



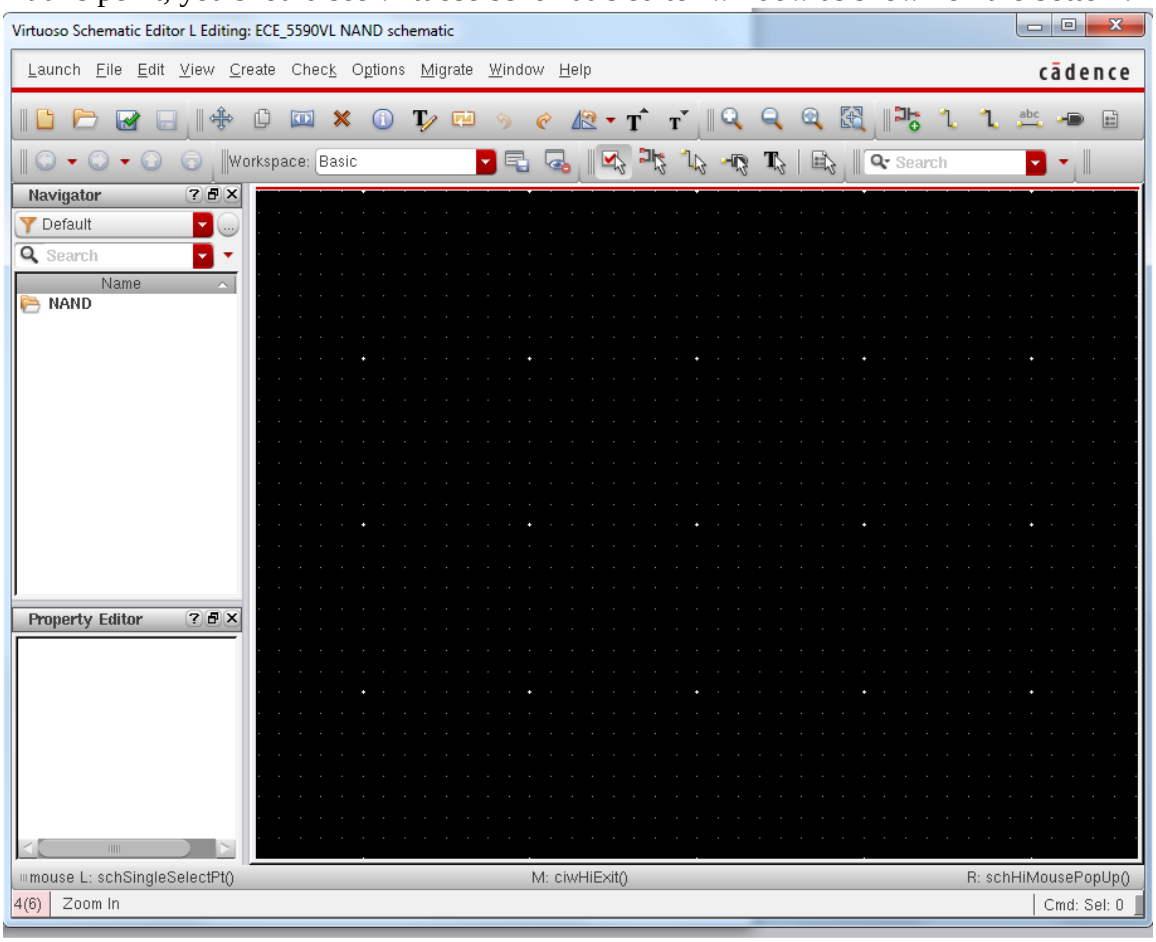
Then, on the following window type NAND for Cell file name. On the library button, scroll up and down to pick the right library name and click ok.



Then, the following window will appear. Click **Yes**.



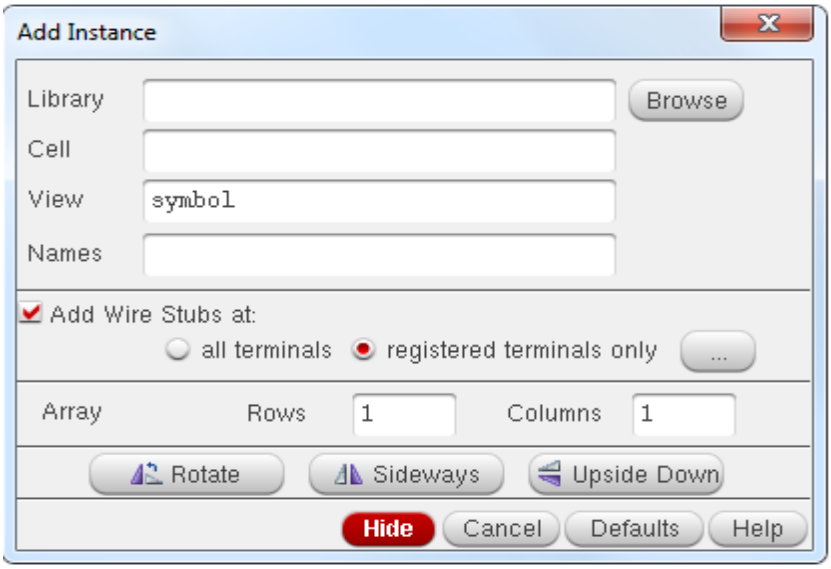
At this point, you should see virtuoso schematic editor window as shown on the bottom.



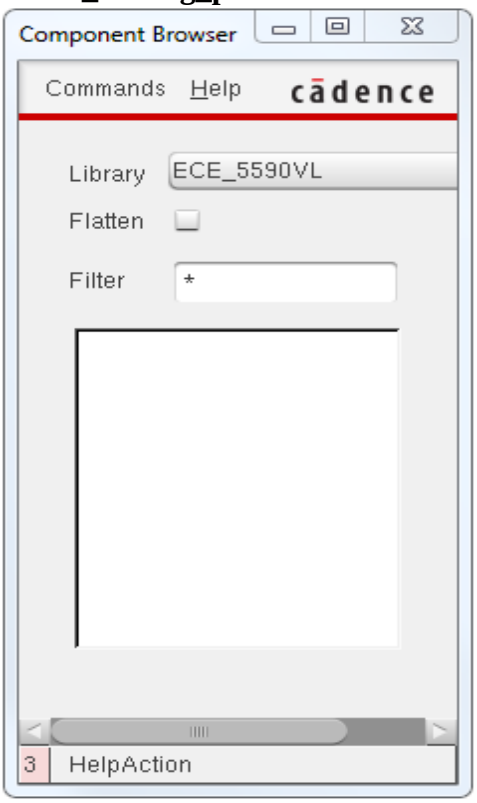
Adding NMOS and PMOS Transistors

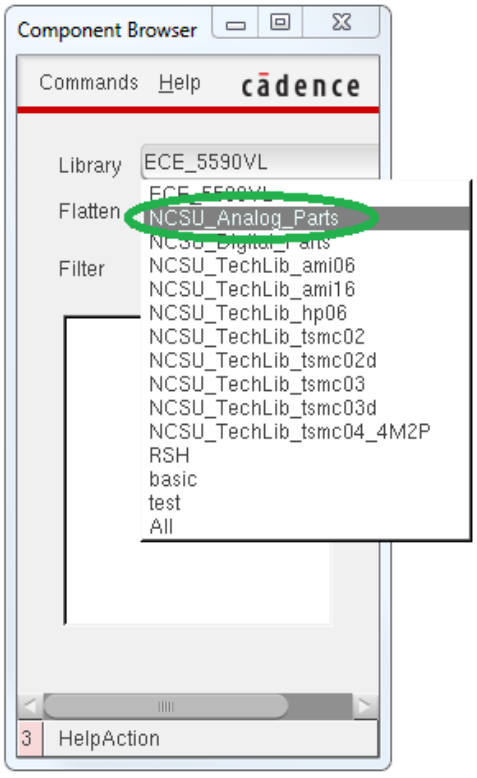
Now, we will be placing the PMOS and NMOS transistors on the schematic window editor.
To place PMOS:

Create → Instance then the following window will come.

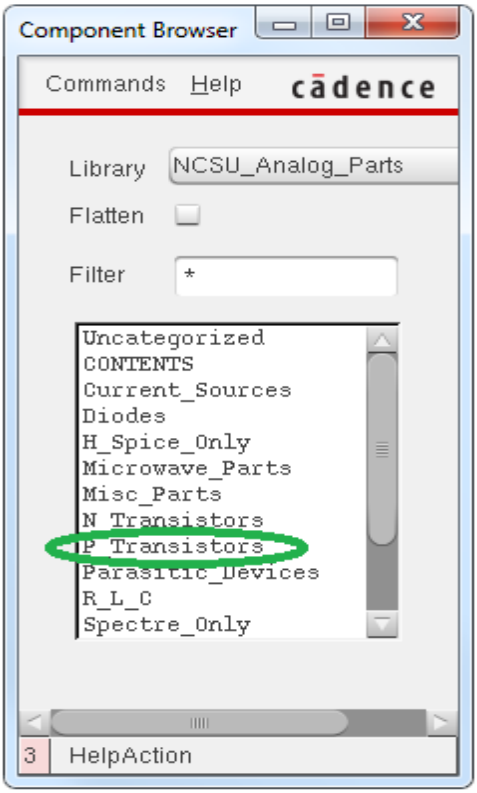


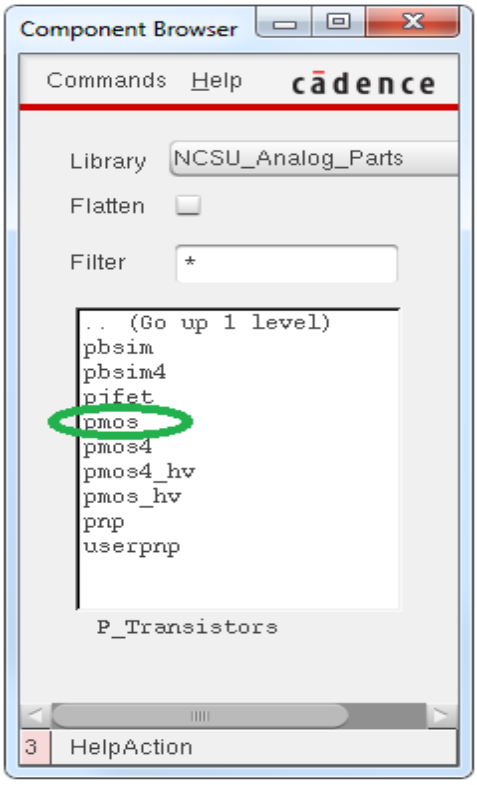
When you click on **Browse** the **Component Browser** window will be opened. Select **NCSU_Analog_parts.**



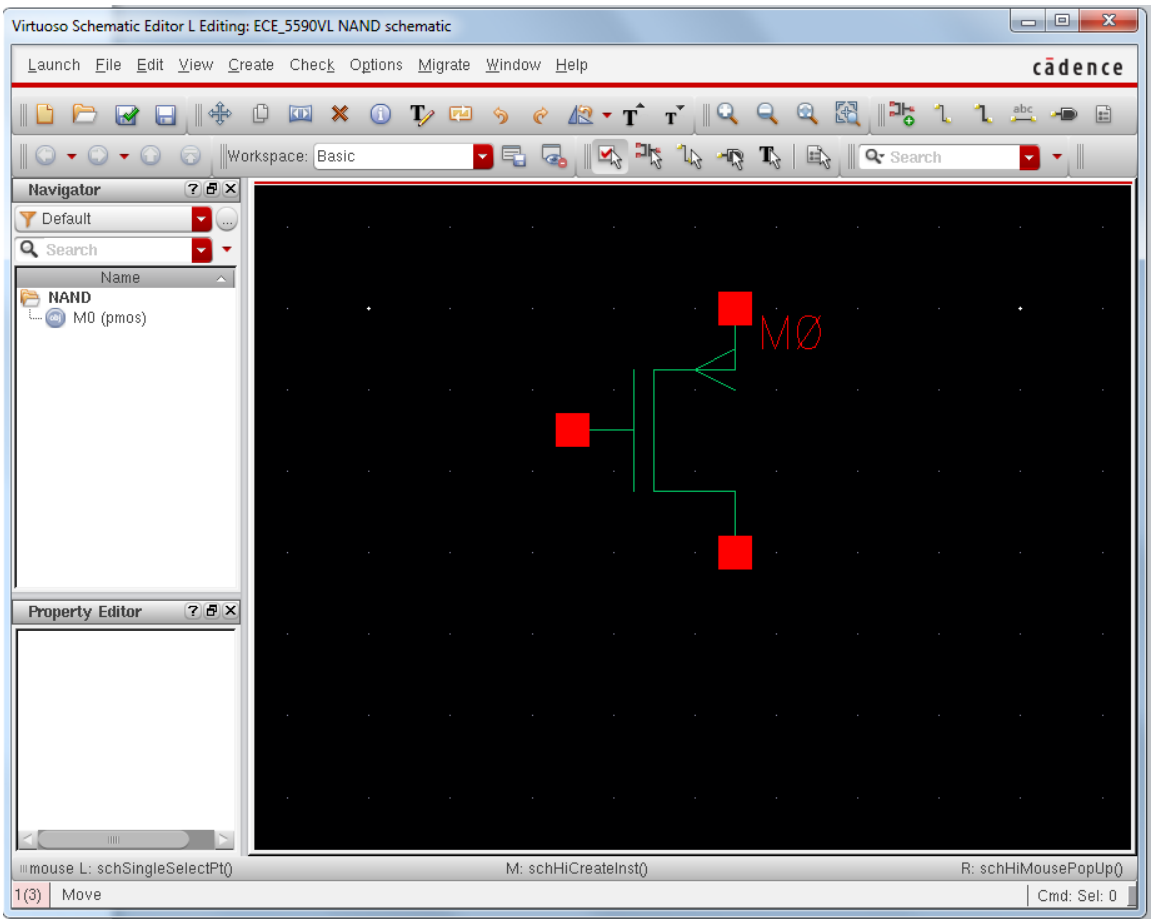


Then, click on **P_Transistors → pmos**



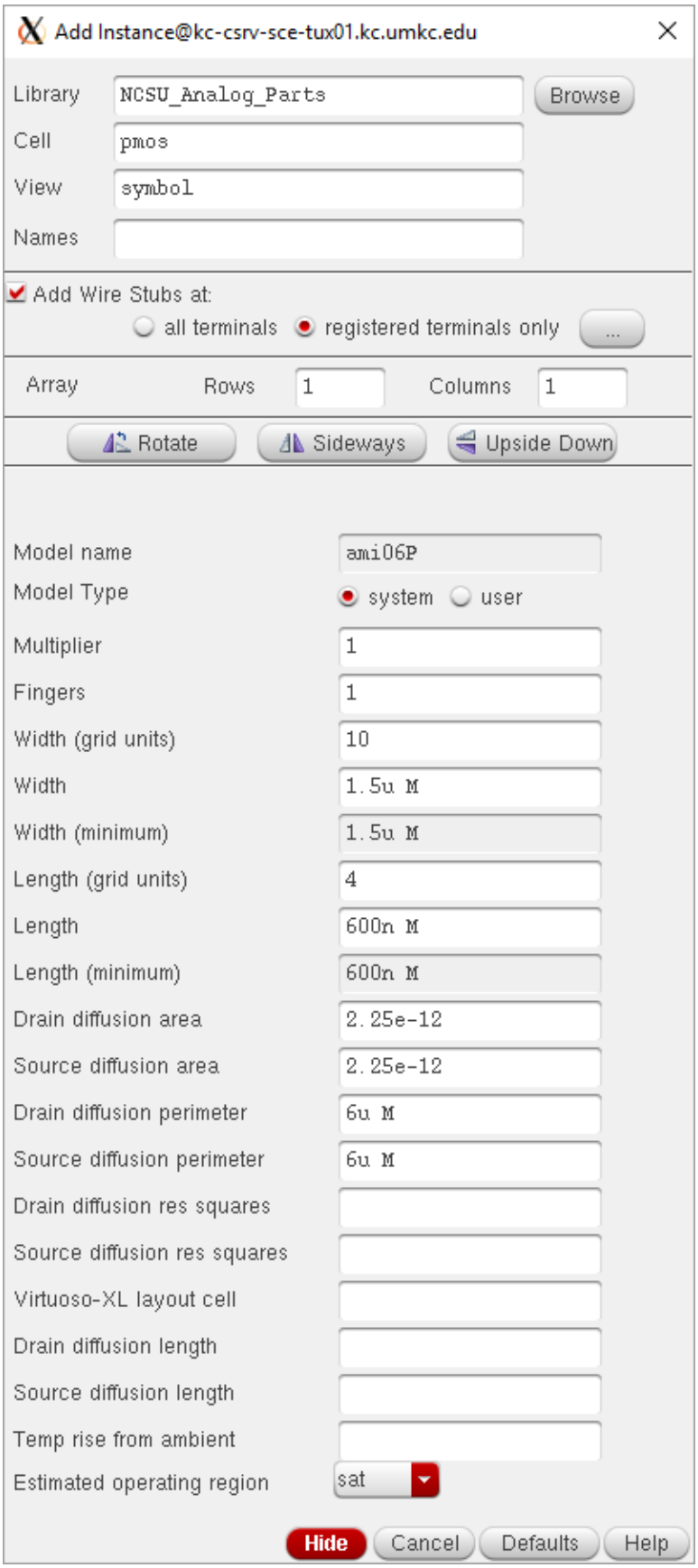


(Note: You can click on the (Go up 1 level) to go back to the previous selections)
When you click **Close**, the cursor will change to a transistor symbol. Place the **PMOS** on the virtuoso schematic editor window by left clicking on the mouse.

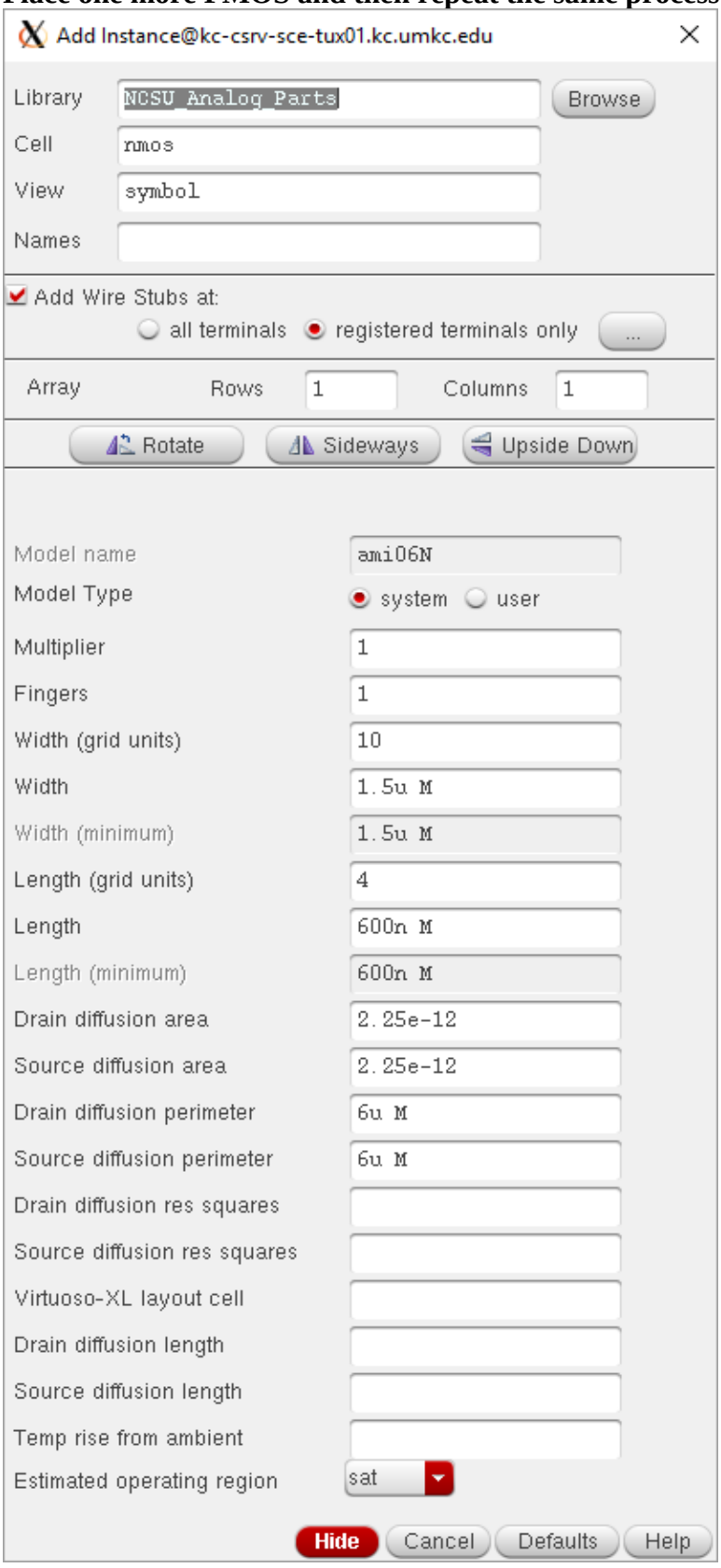


To change the characteristics of the PMOS, left click on the **PMOS** then type **q** or left click on the **PMOS** then go to **Edit → Properties → Objects**. The following window should appear

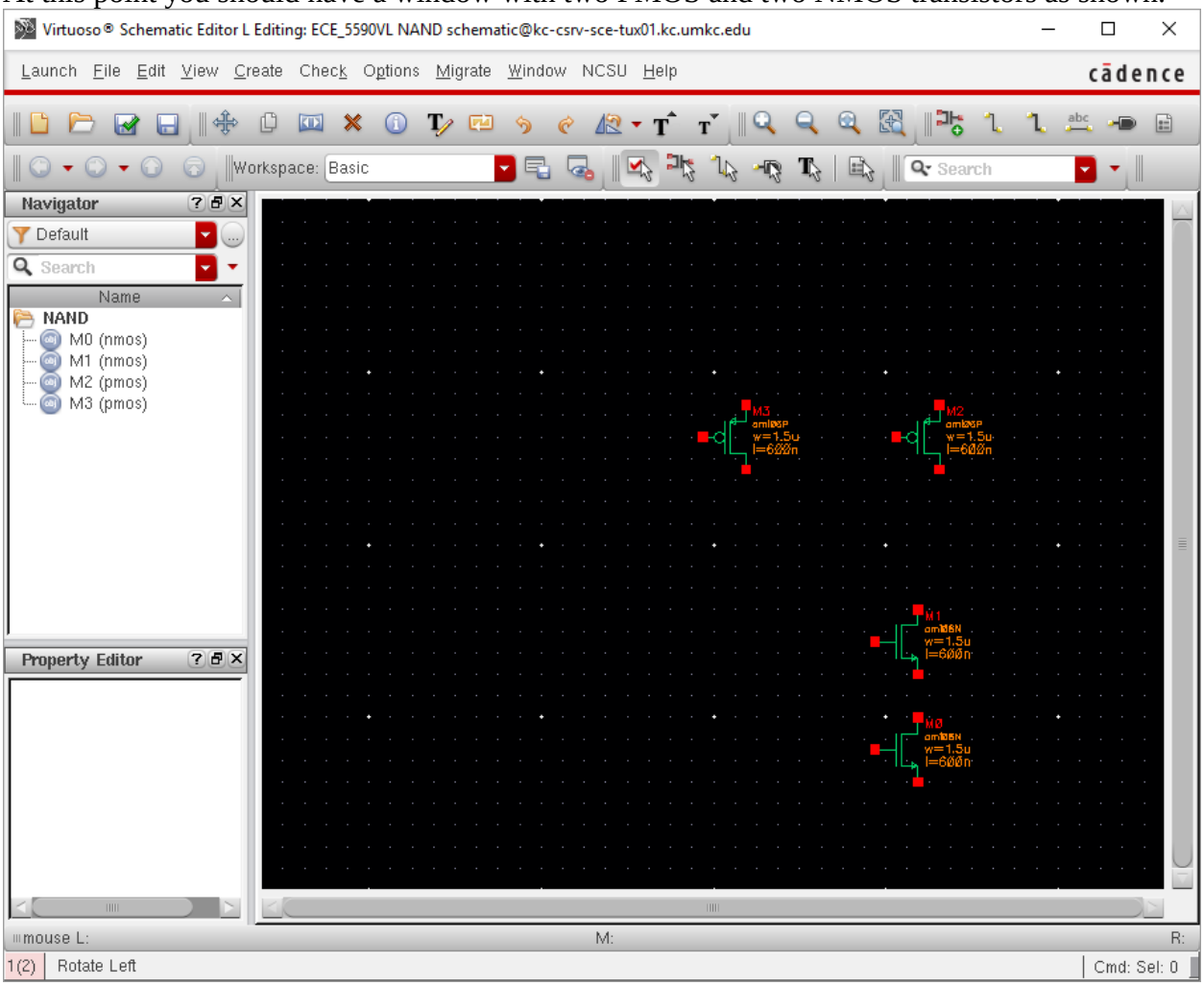
On the Edit Object Properties window enter the values for PMOS shown here and click


Add Instance@kc-csrv-sce-tux01.kc.umkc.edu
Library
NCSU_Analog_Parts
Browse
Cell
pmos
View
symbol
Names
Add Wire Stubs at:
all terminals
registered terminals only
...
Array
Rows
1
Columns
1
Rotate
Sideways
Upside Down
Model name
ami06P
Model Type
system
user
Multiplier
1
Fingers
1
Width (grid units)
10
Width
1.5u M
Width (minimum)
1.5u M
Length (grid units)
4
Length
600n M
Length (minimum)
600n M
Drain diffusion area
2.25e-12
Source diffusion area
2.25e-12
Drain diffusion perimeter
6u M
Source diffusion perimeter
6u M
Drain diffusion res squares
Source diffusion res squares
Virtuoso-XL layout cell
Drain diffusion length
Source diffusion length
Temp rise from ambient
Estimated operating region
sat
Hide
Cancel
Defaults
Help

Place one more PMOS and then repeat the same process for NMOS



At this point you should have a window with two PMOS and two NMOS transistors as shown.



Now select and place the following objects on the window:
Create → Instance → Browse
1- **NCSU_Analog_parts → Supply_Nets → vdd**

2- **NCSU_Analog_parts → Supply_Nets → gnd**

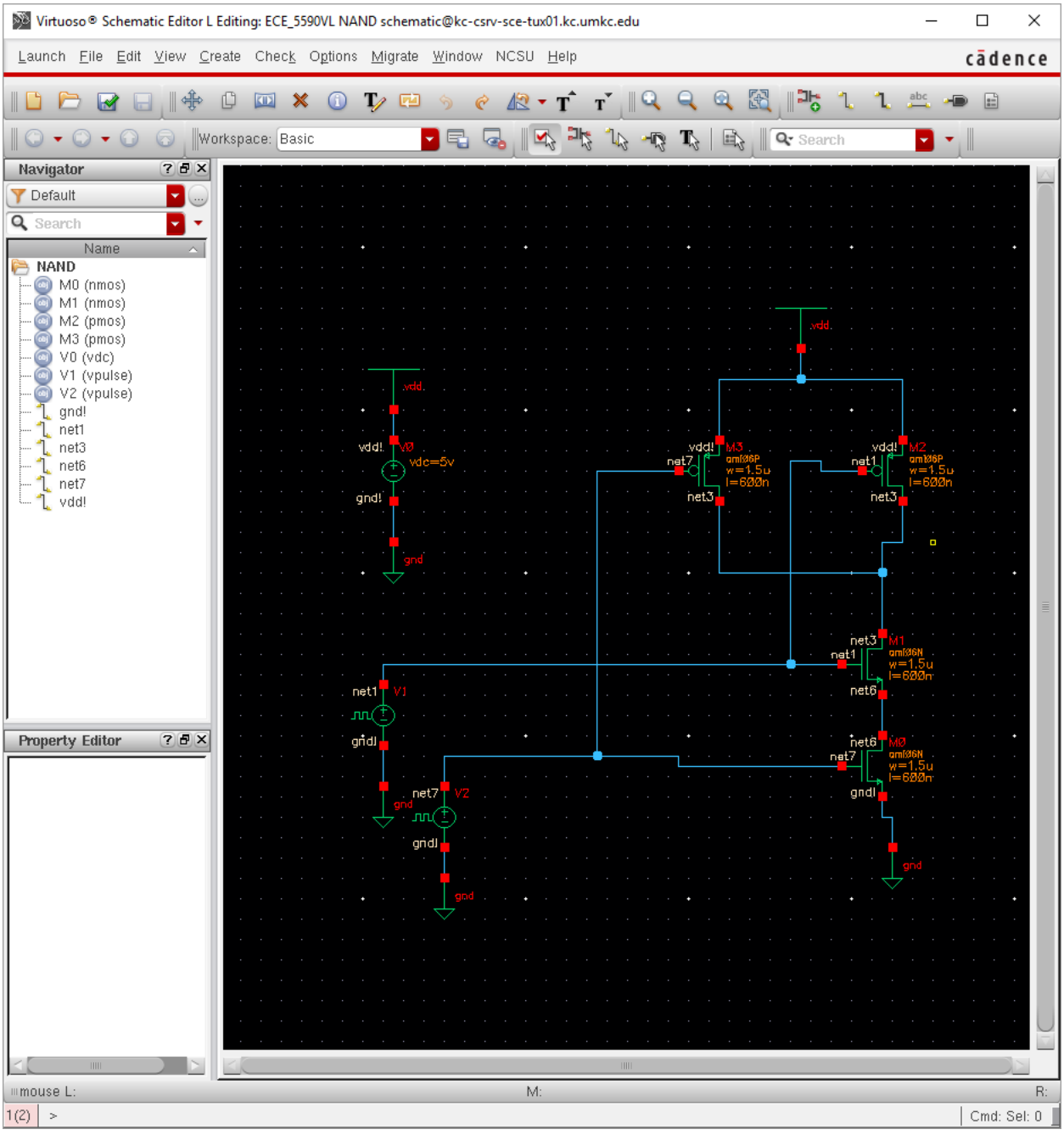
3- **NCSU_Analog_parts → Voltage_Sources → vdc**

i. left click on vdc → **q** → DC voltage **5v V**

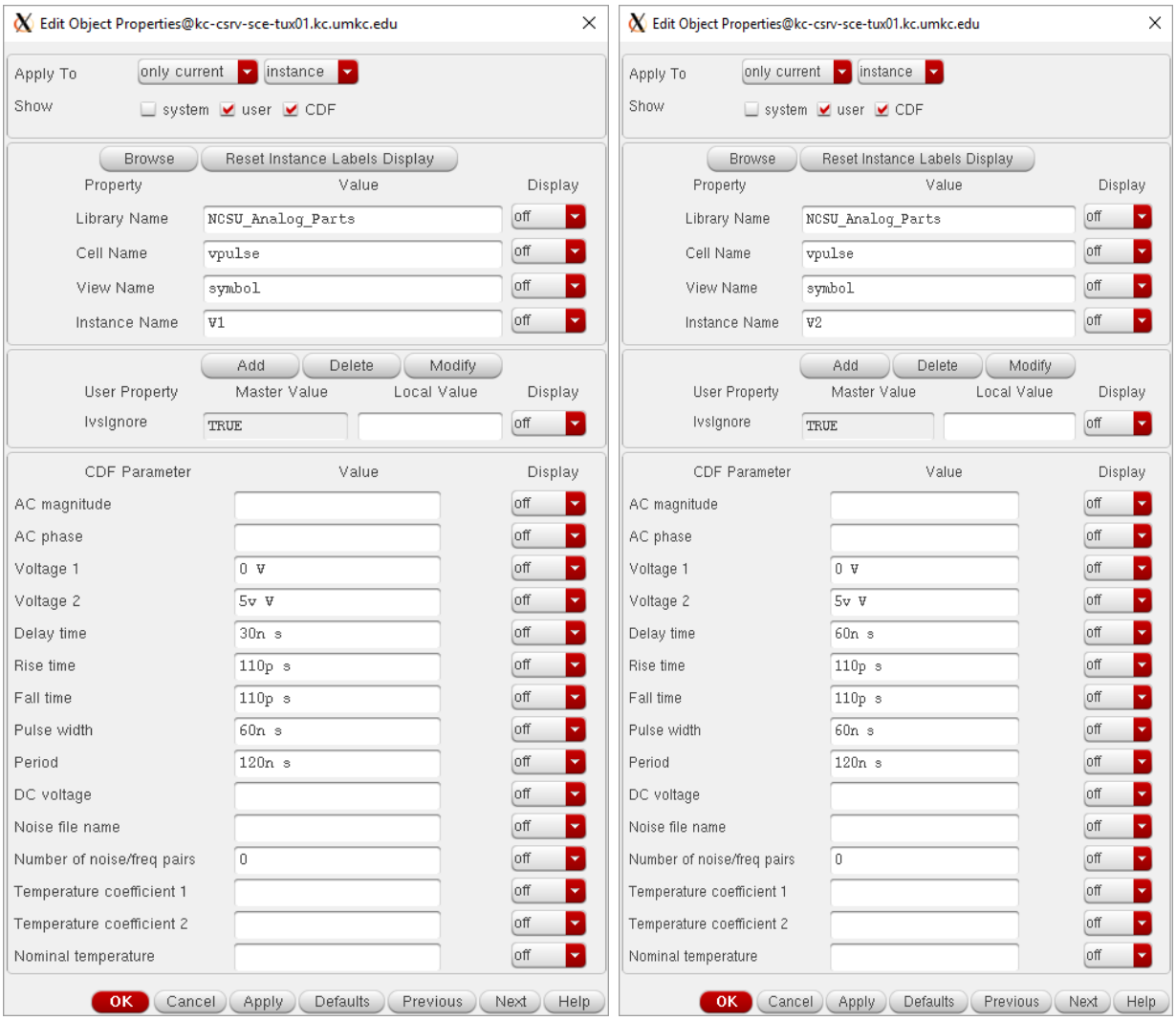
4- **NCSU_Analog_parts → Voltage_Sources → vpulse**

i. place two vpulses

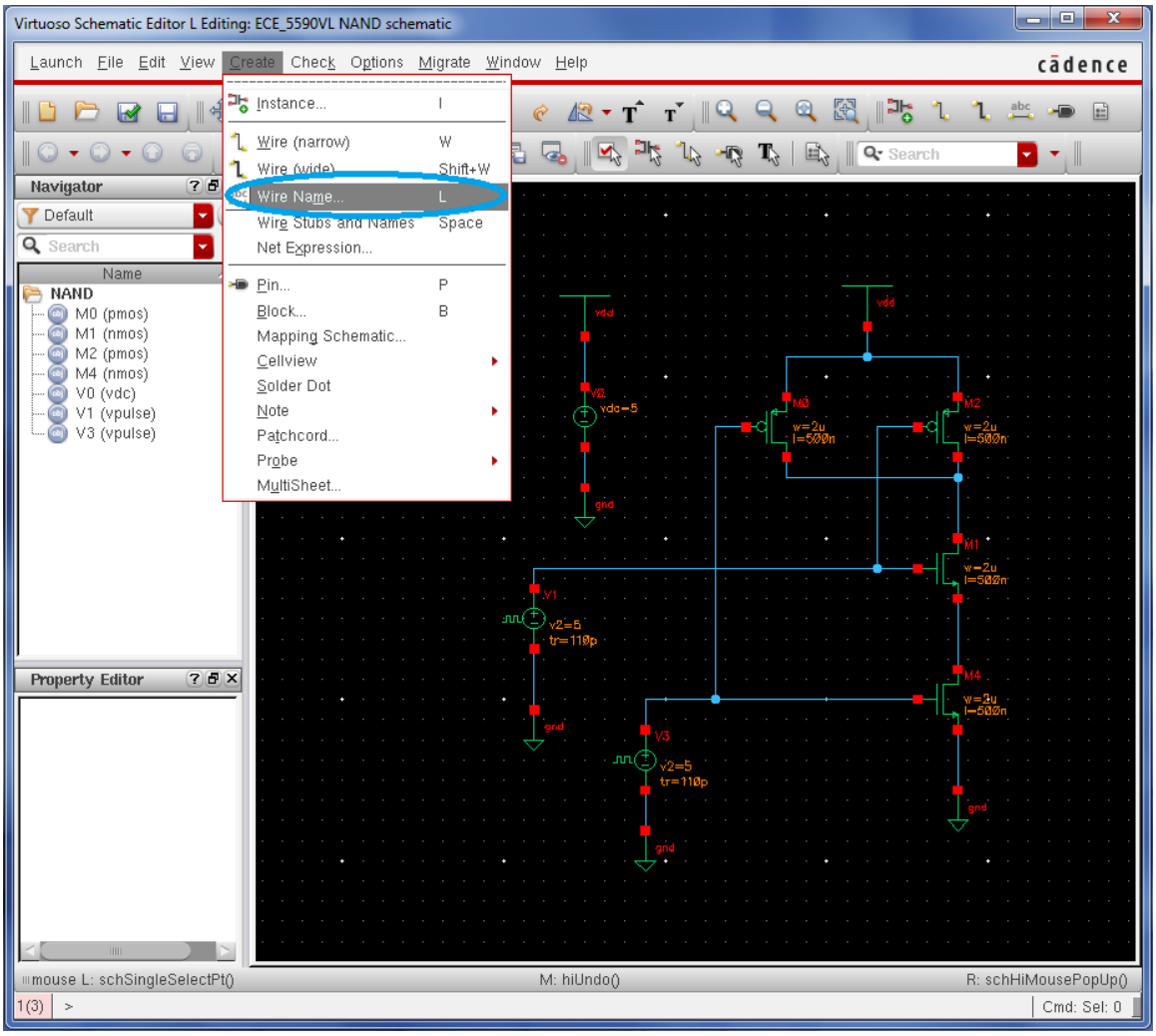
You should connect all the components by wire. To connect the one terminal of component to another click the red square box OR press "**w**" then under your mouse cursor a small wire will come and then connect the components like shown below.



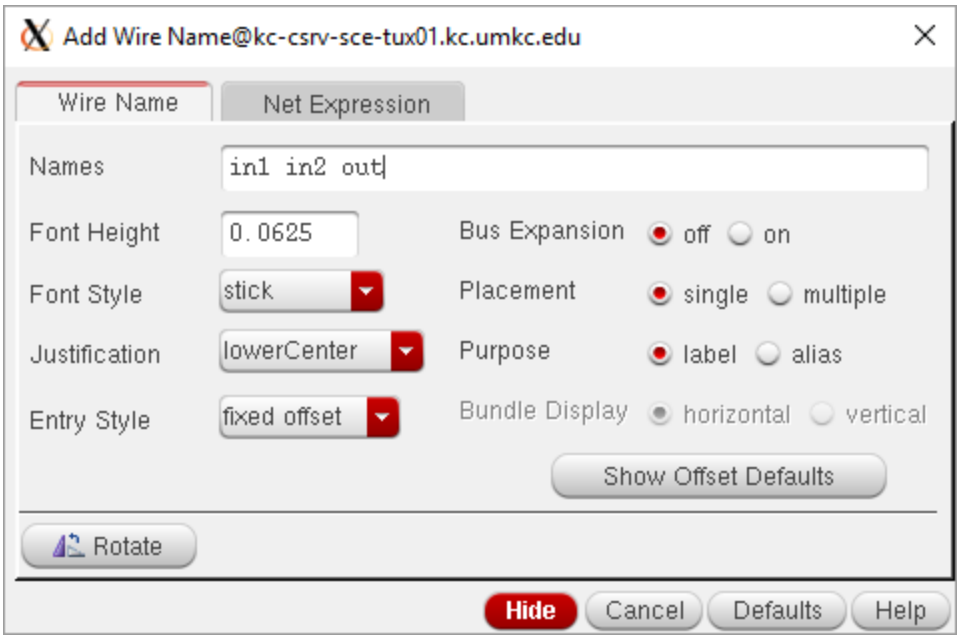
In order to observe the output we need to configure the timing of the Vpulse for each input. Click on the Vpulse and then change it properties by pressing "**q**"



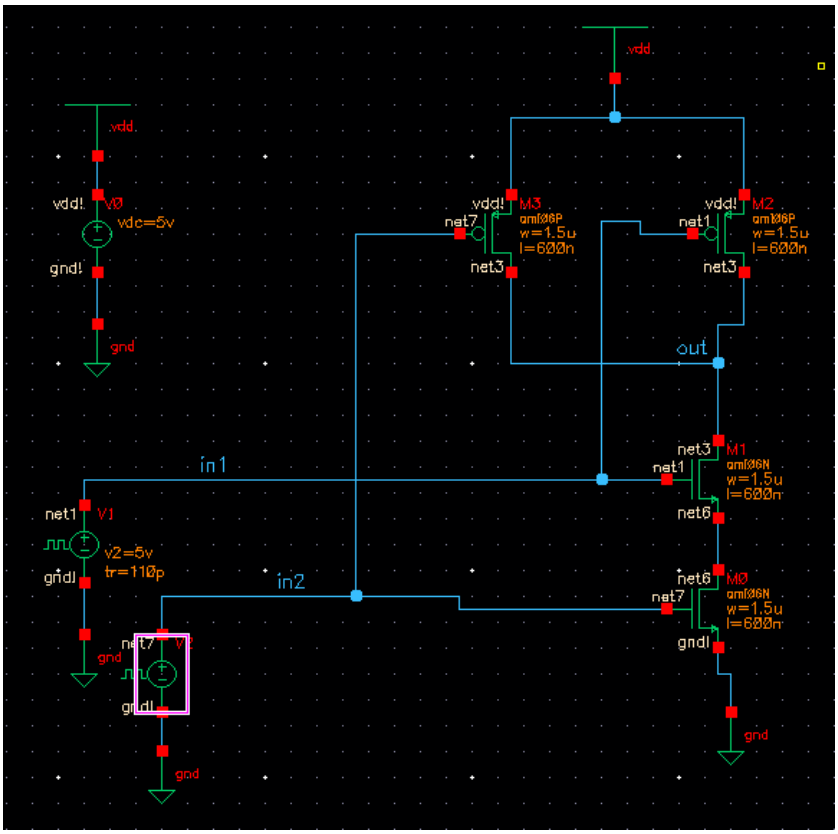
Click on **Create → Wire Name**



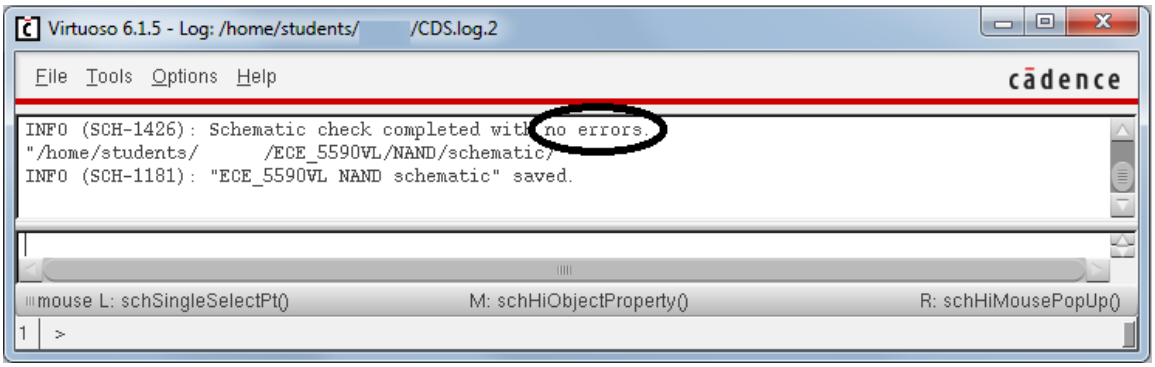
Add Wire Name window will appear



Write in1 in2 out in the names and then click on the schematic to name the wires respectively.



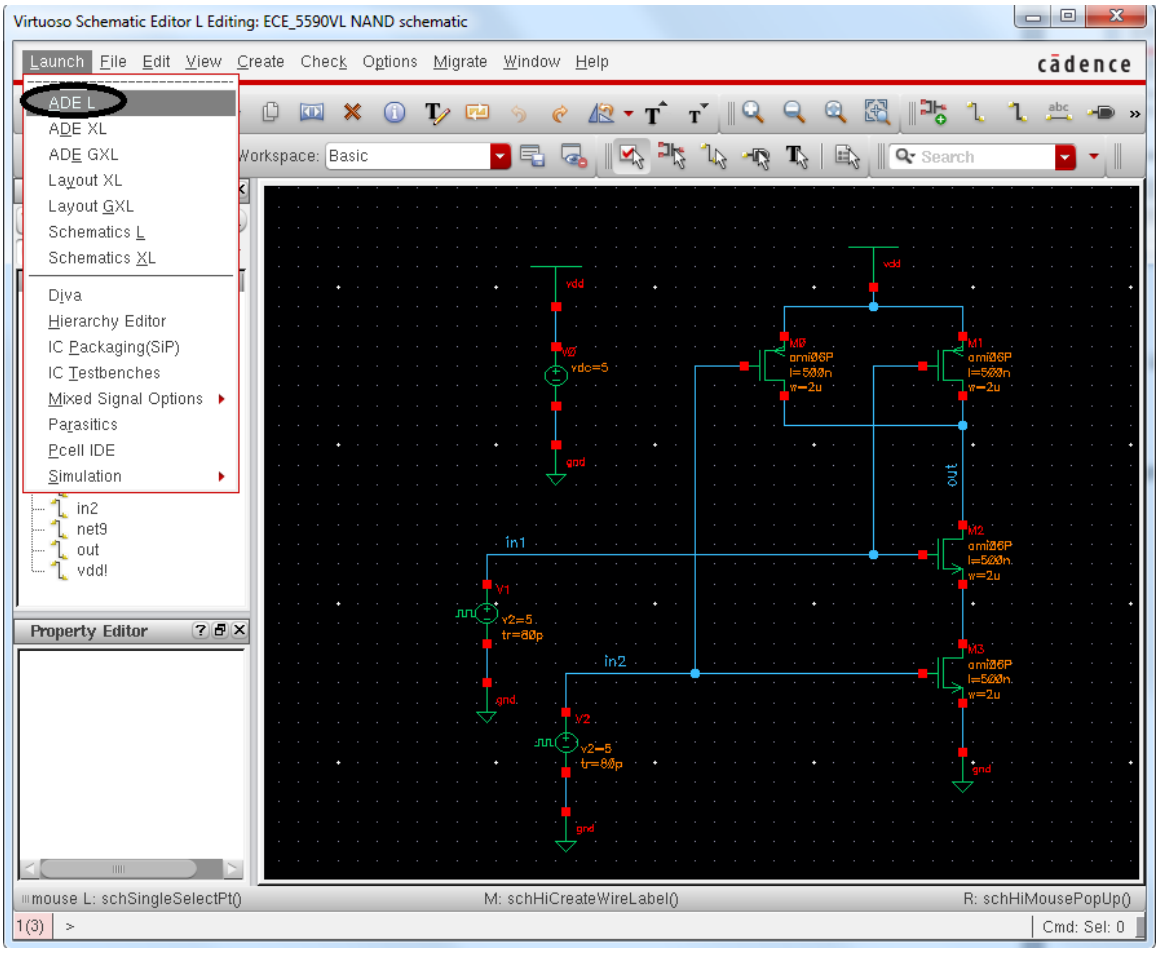
If you make a mistake you can always use **u** to undo it. Now click **Check and Save** button**.** Then you should see the virtuoso window. Make sure your design is free of error.


Virtuoso 6.1.5 - Log: /home/students/ /CDS.log.2
File Tools Options Help
cadence
INFO (SCH-1426): Schematic check completed with no errors.
"/home/students/ /ECE_5590VL/NAND/schematic"
INFO (SCH-1181): "ECE_5590VL NAND schematic" saved.
mouse L: schSingleSelectPt() M: schHiObjectProperty() R: schHiMousePopUp()
1 >

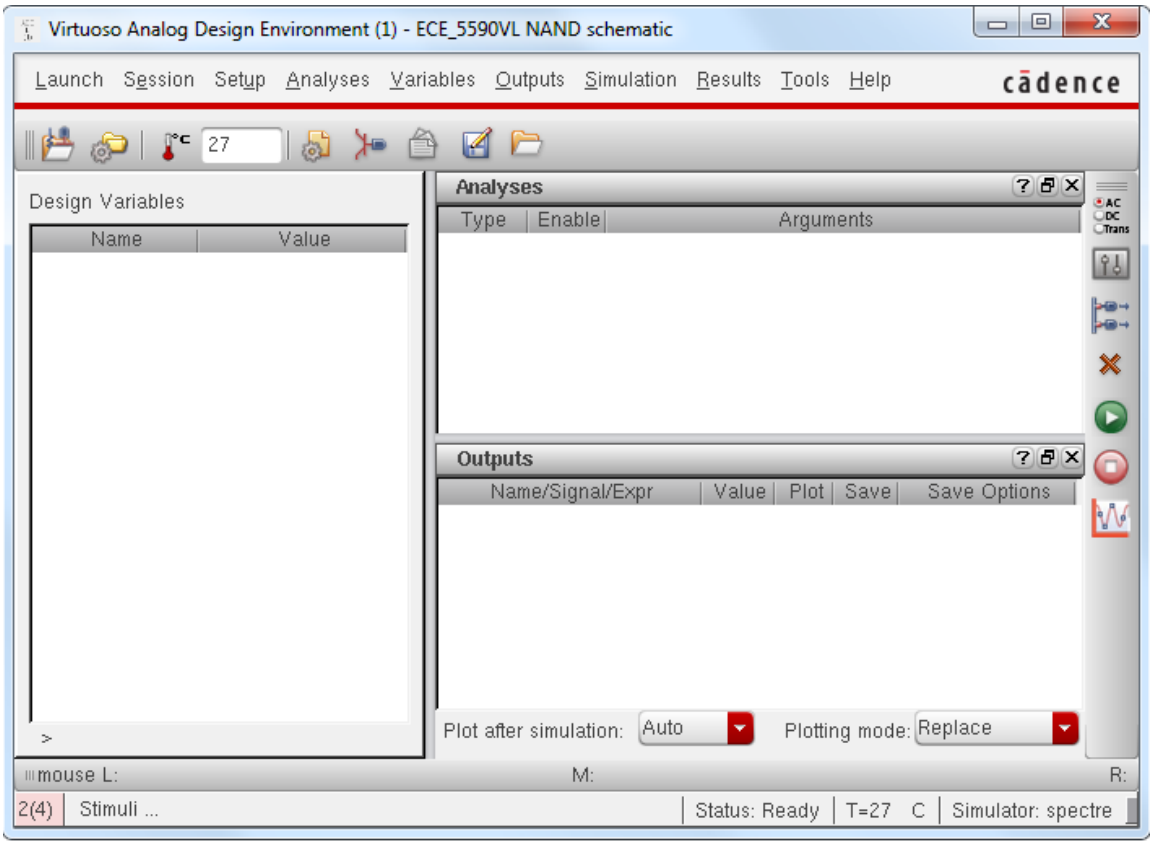
Simulation of your Circuit

We are now ready to do simulation

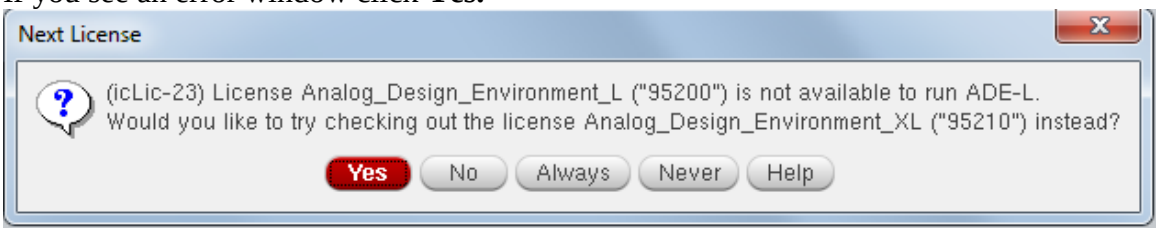
From Virtuoso Schematic Editor click on **Launch → ADE L**



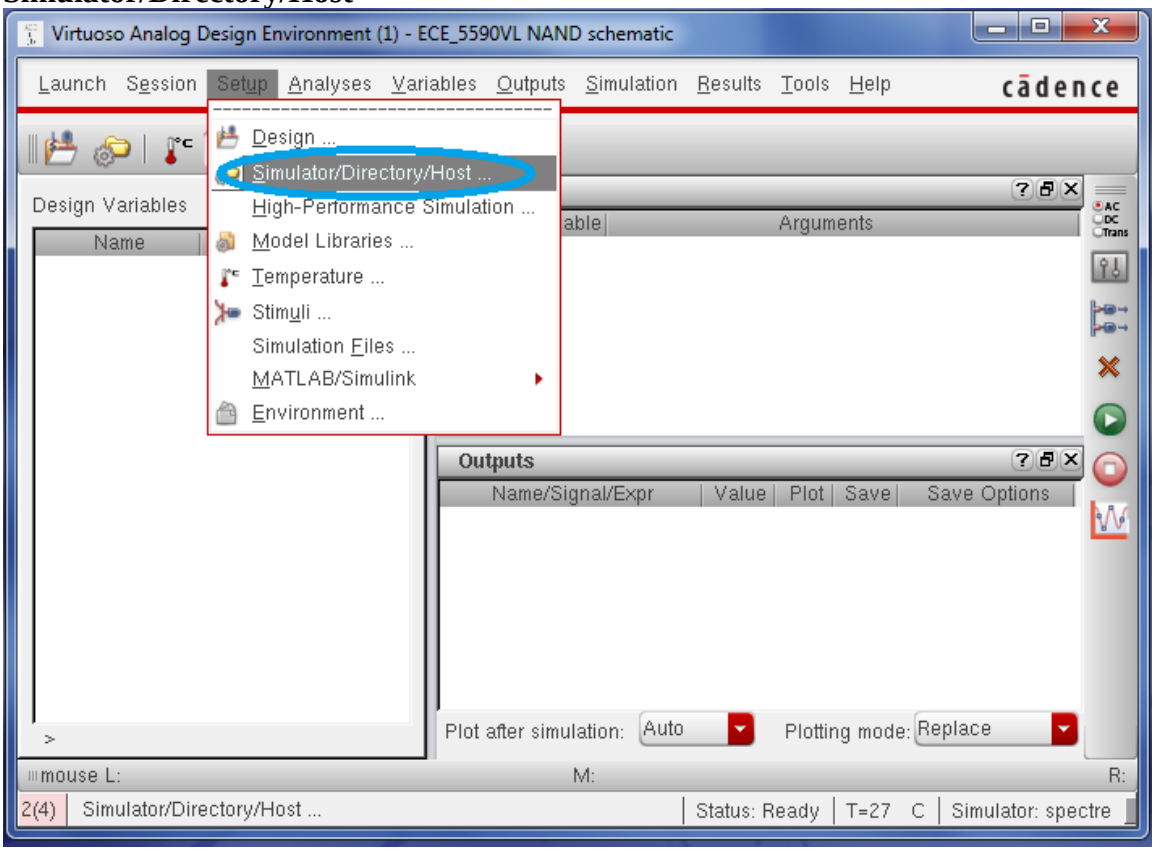
The following window should appear.



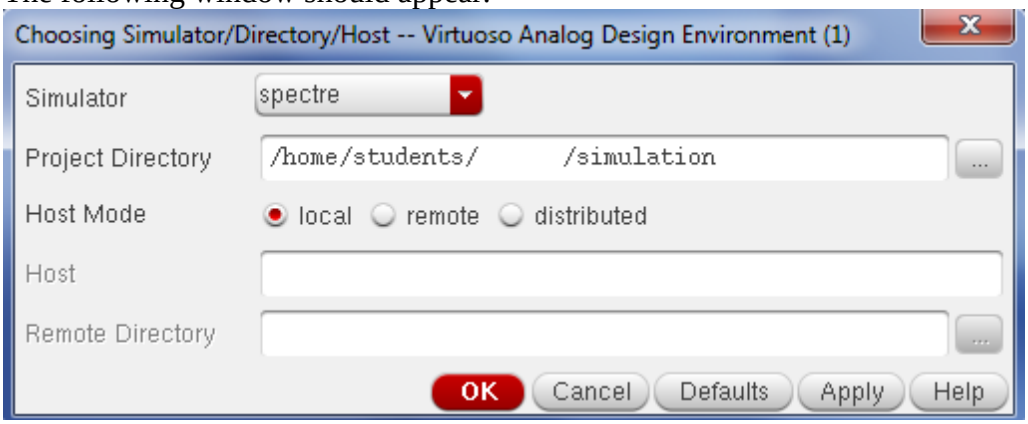
If you see an error window click **Yes.**



On the virtuoso analog design environment window click on **Setup → Simulator/Directory/Host**

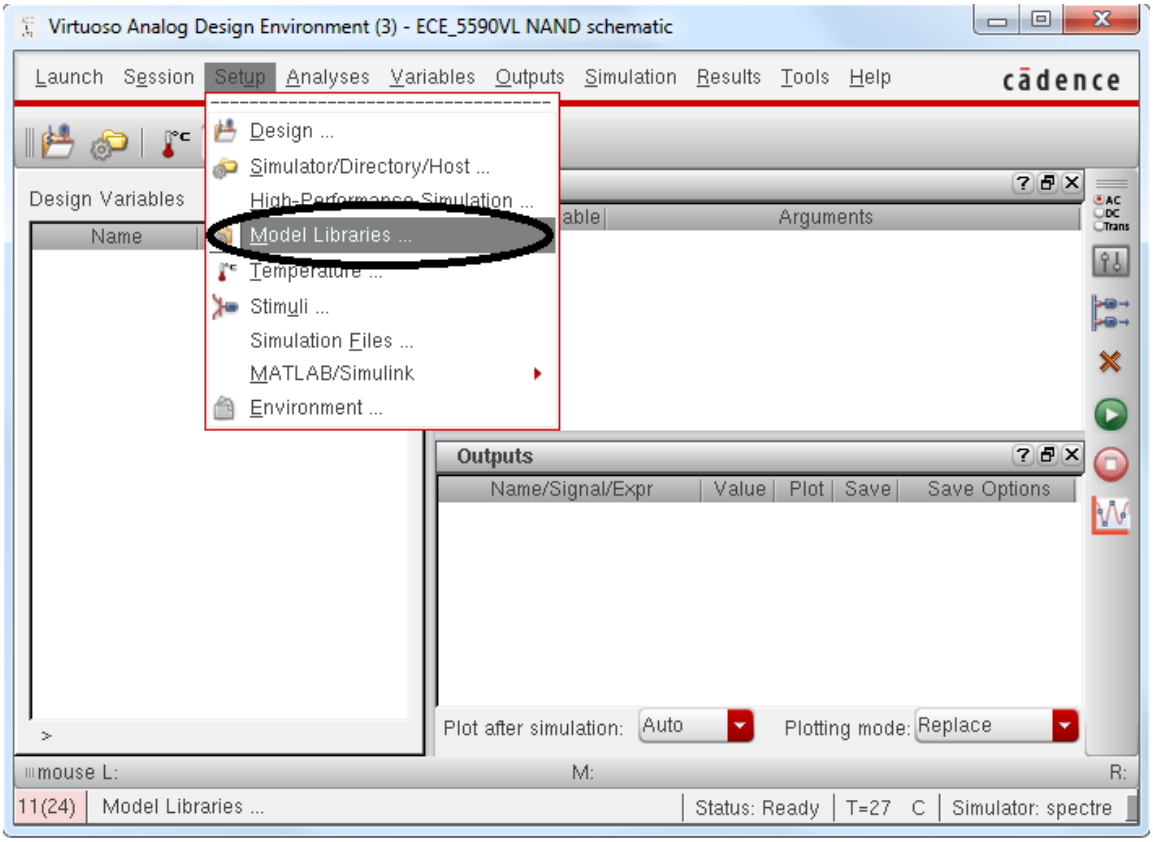


The following window should appear.

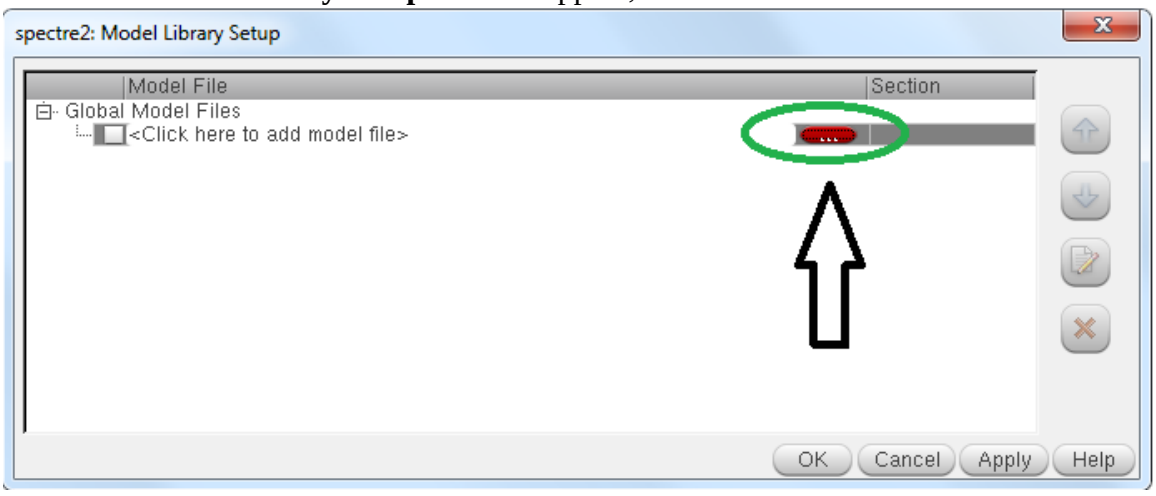


In the above window scroll up and down and select **spectre** under **Simulator** selection and click **ok**.

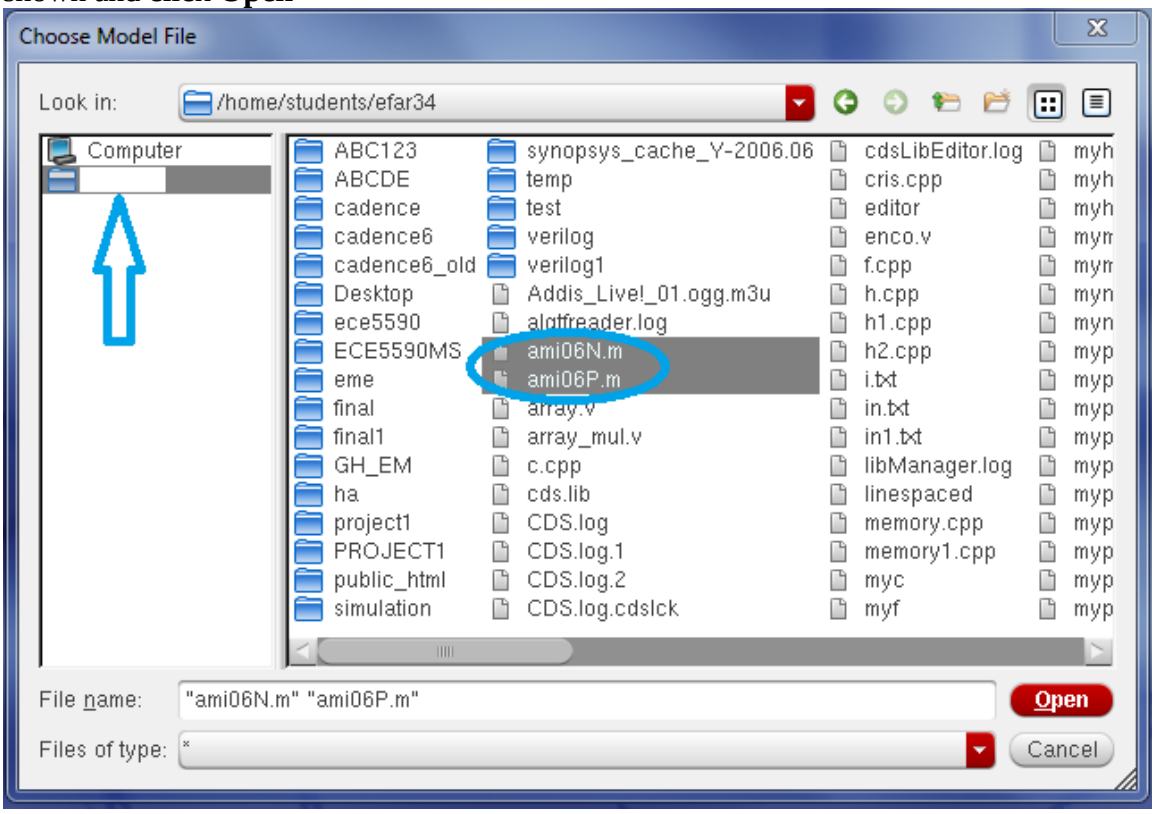
Next, on the **Virtuoso Analog Design Environment** window click on **Setup → Model Libraries**



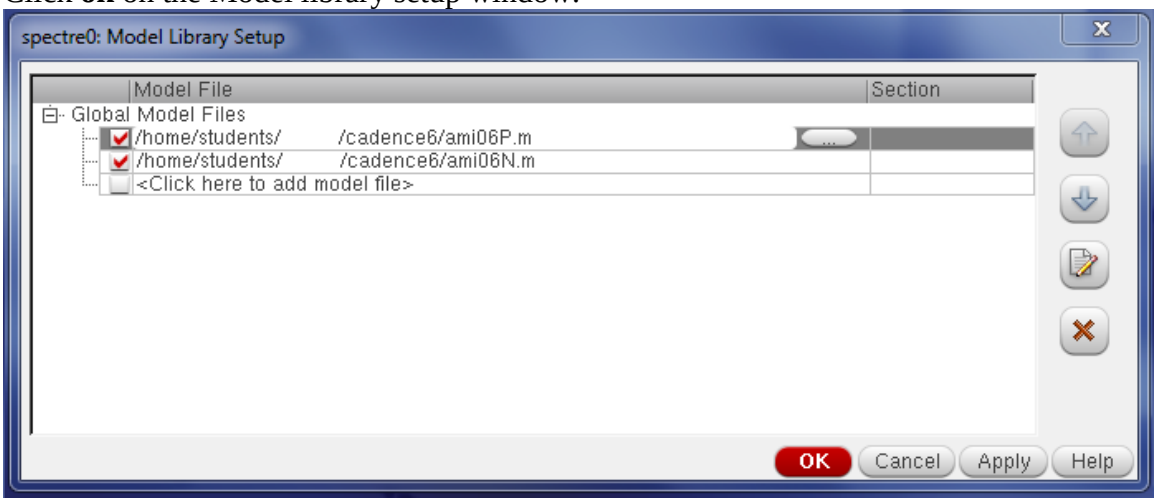
When the **Model Library Setup** window appear, click at the location shown below.



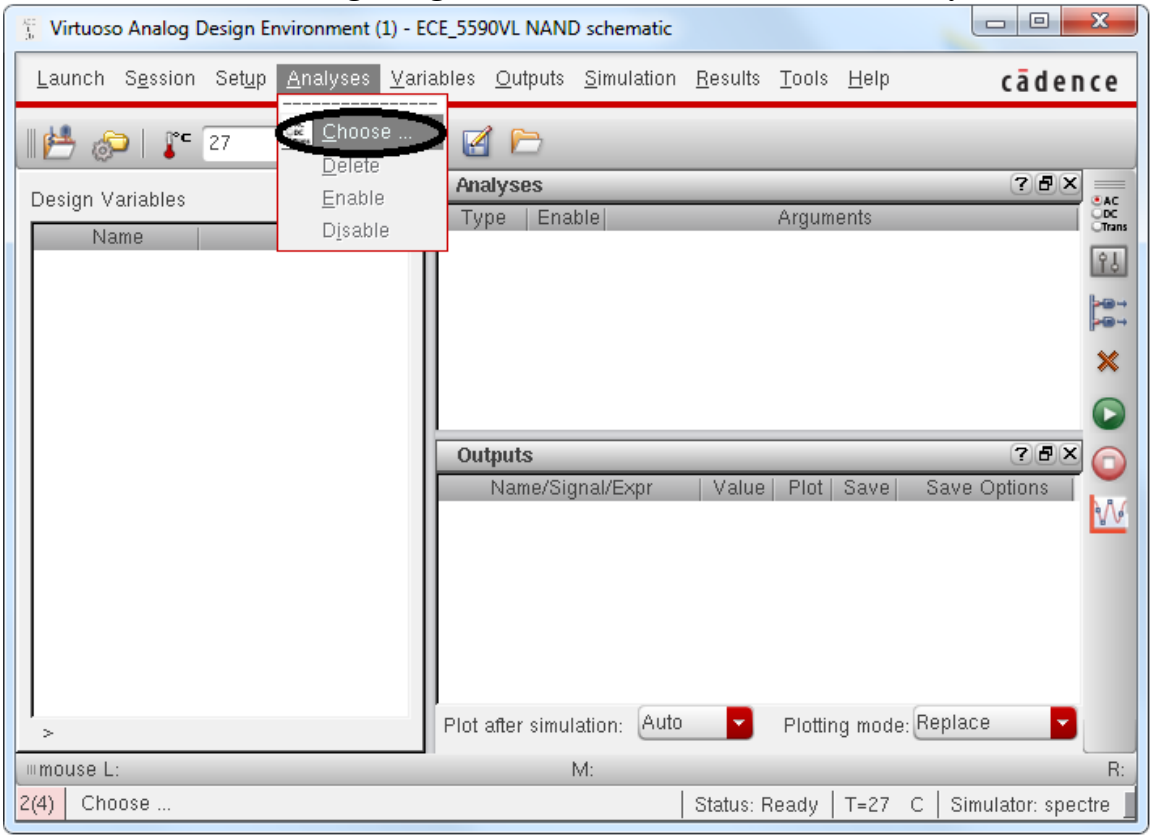
On the choose model file window, first click on your user name then, select the libraries as shown and click **Open**



Click **ok** on the Model library setup window.

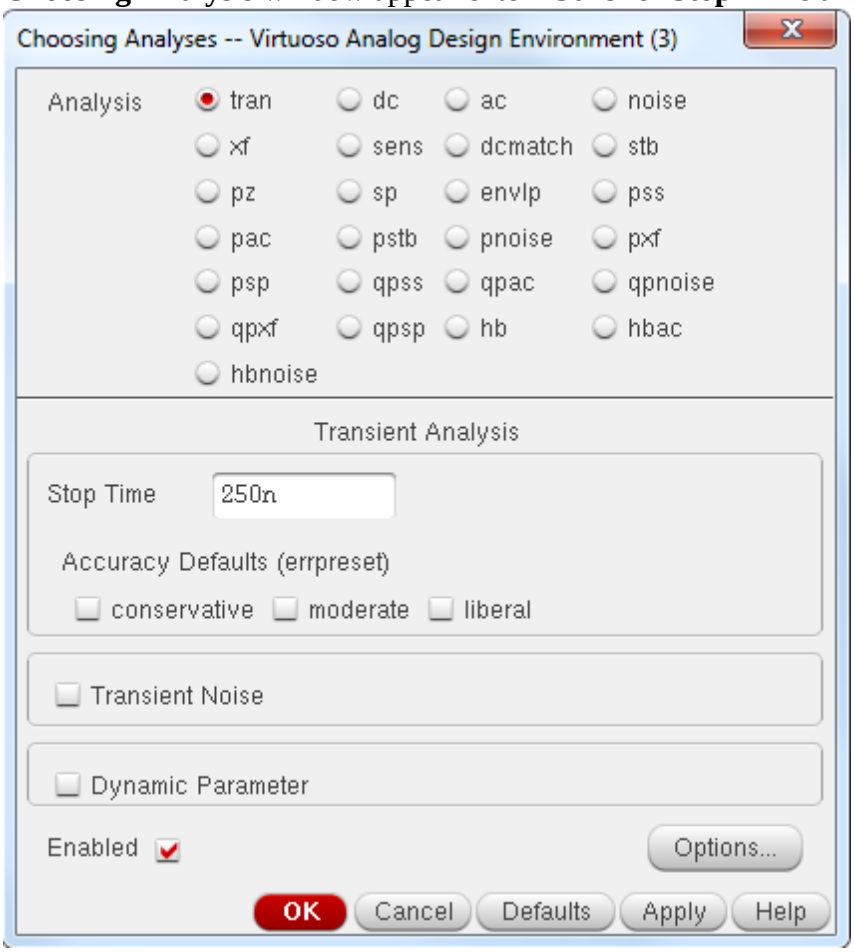


Under the **Virtuoso Analog Design Environment** window click on **Analyses → Choose**

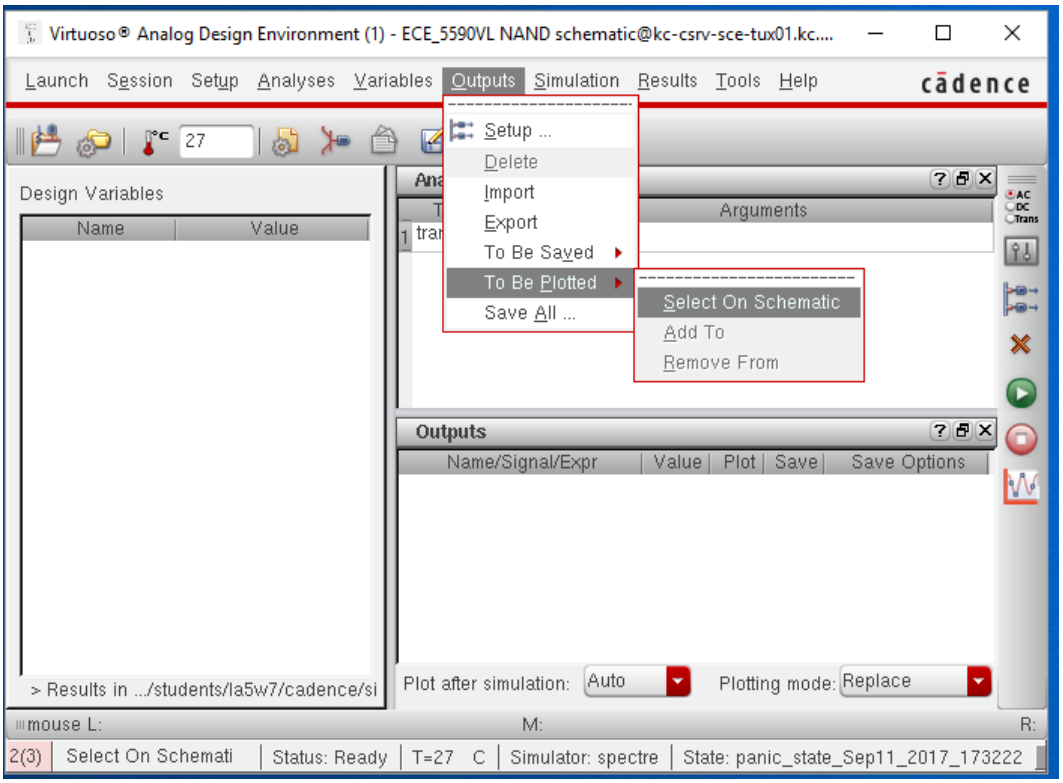


When

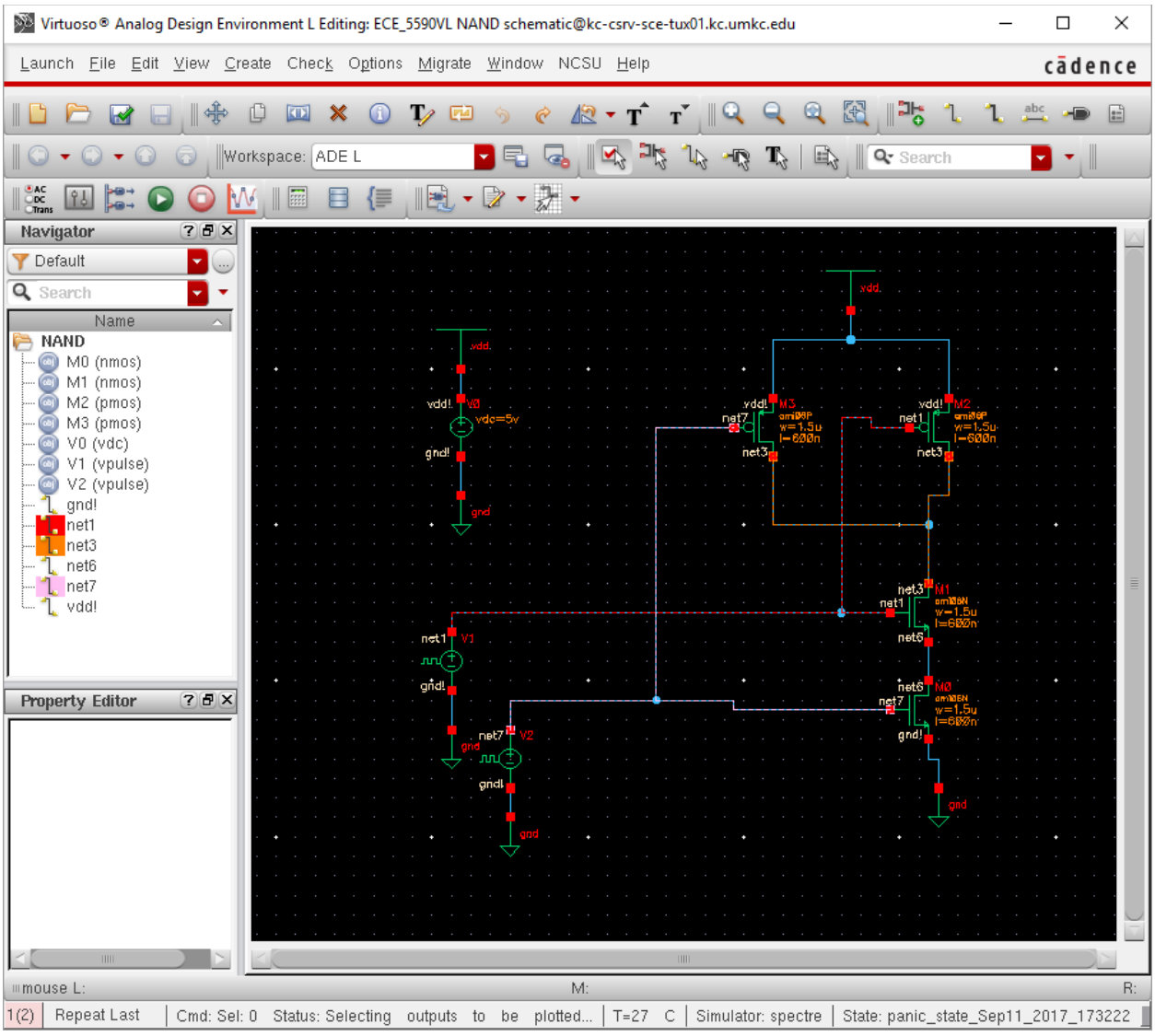
Choosing Analysis window appear enter **250ns** for **Stop Time** and click **ok**.



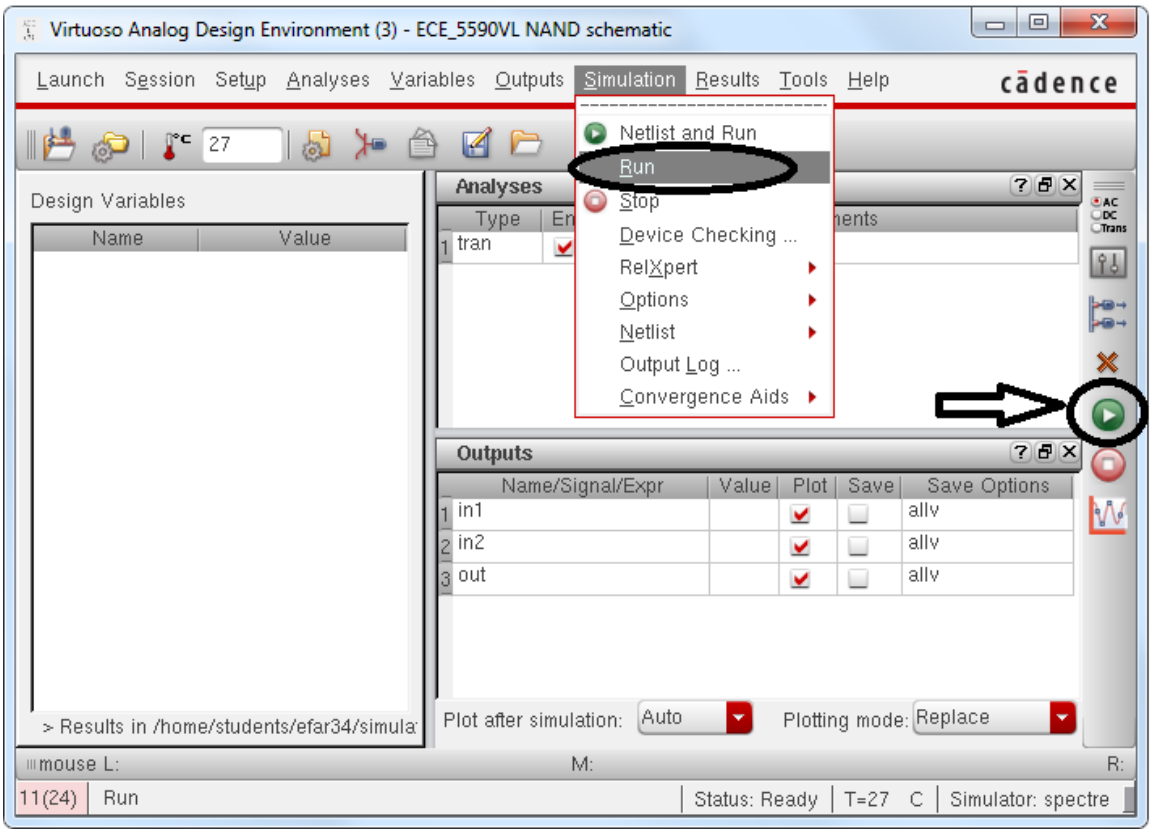
To Select the signals for input and output do the following



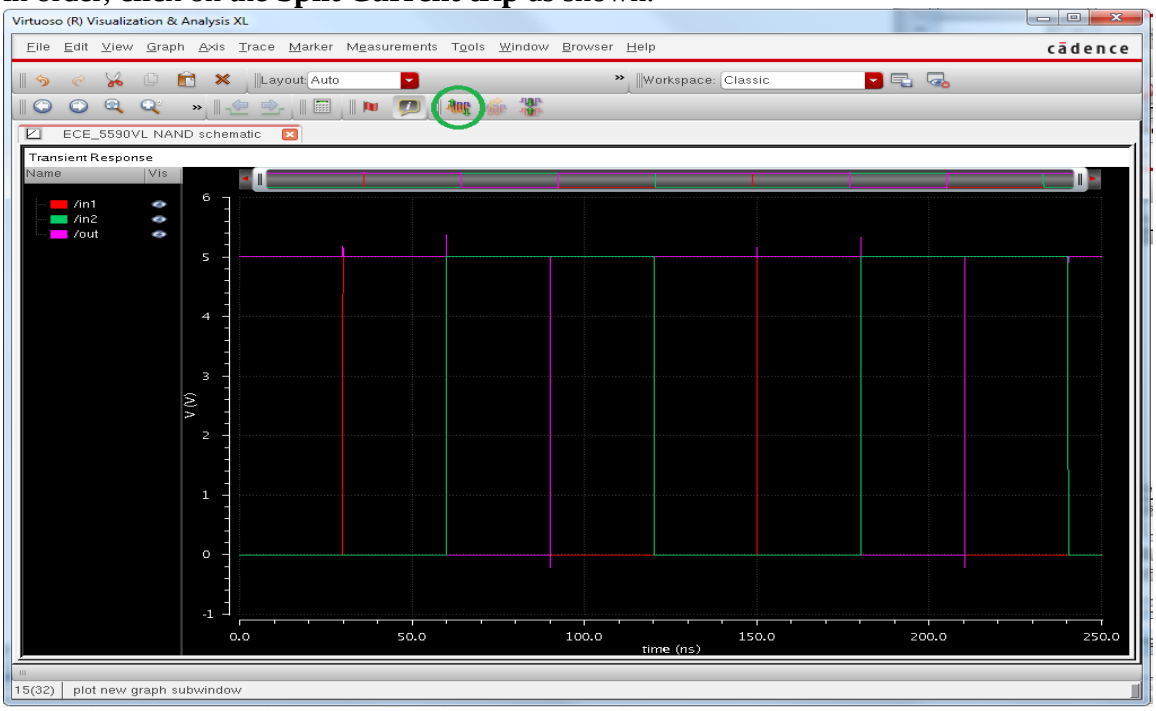
Now select the signals from the schematic



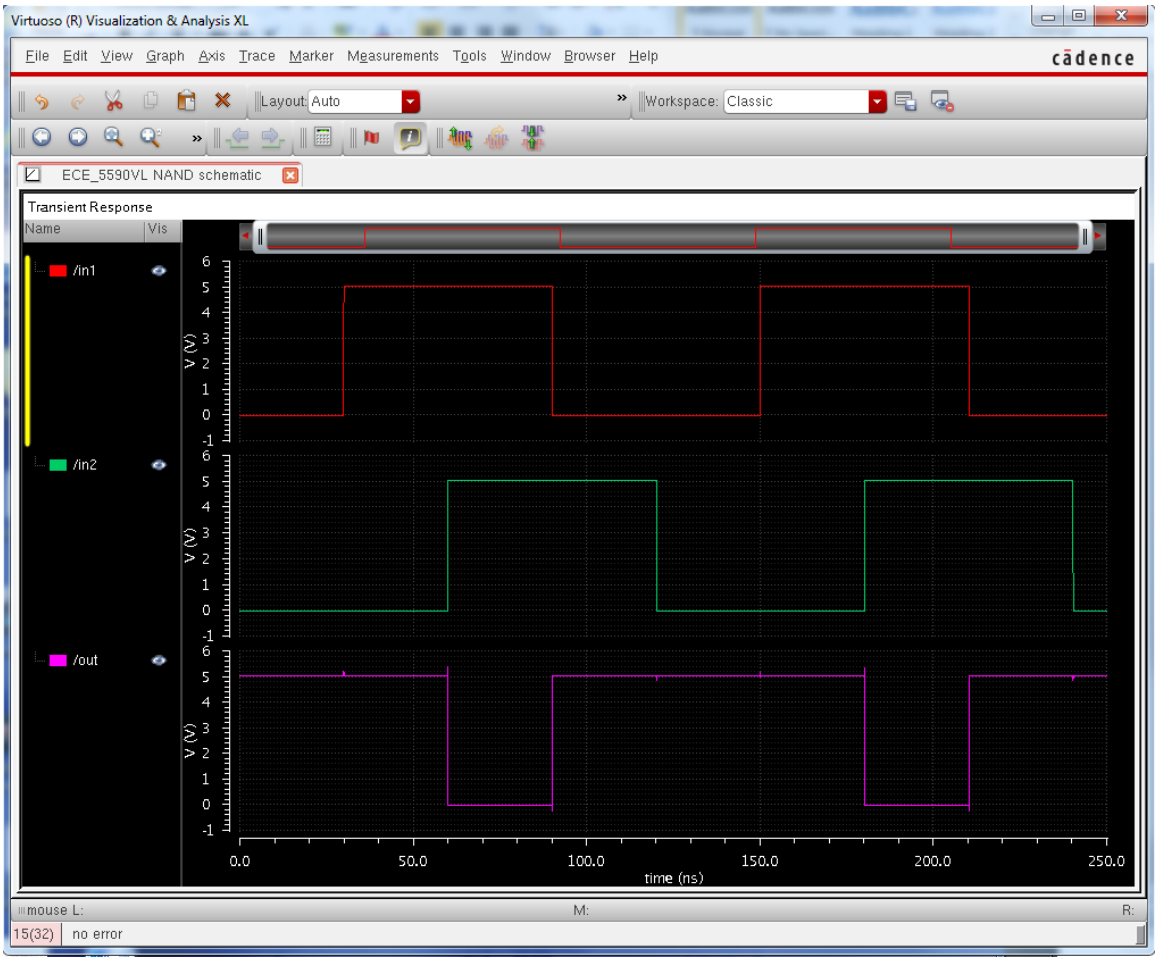
On the **Virtuoso Analog Design Environment** window **Simulation → Run**
(Note: you could also click on the green run button at the right side of the window)



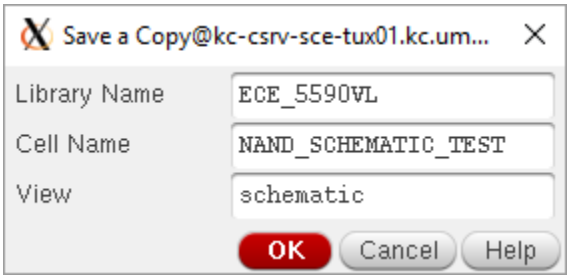
Now, you should see **Virtuoso Visualization & Analysis window.** To see the inputs and output in order, click on the **Split Current trip** as shown.



At this point the **Virtuoso Visualization & Analysis** window should look as follow.



Go to file and click on SAVE A COPY this file as “NAND_SCHEMATIC_TEST”



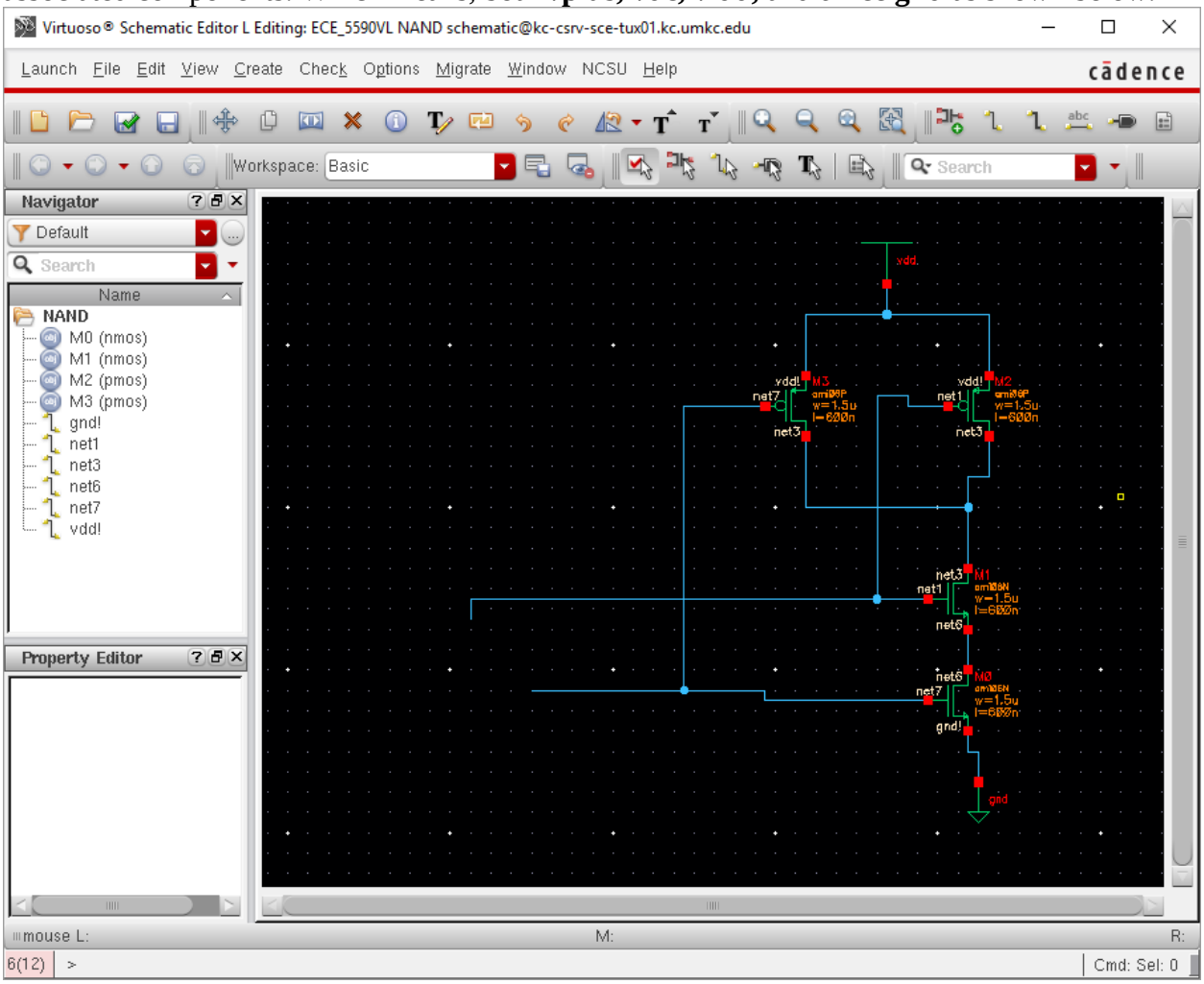
Creating the AND symbol

Close the things. Open the virtuoso again and open the file NAND.

We are now ready to create a NAND symbol

Even though our design is done, we will add few more things to it to make it better. Also, we will create a **NAND symbol**.

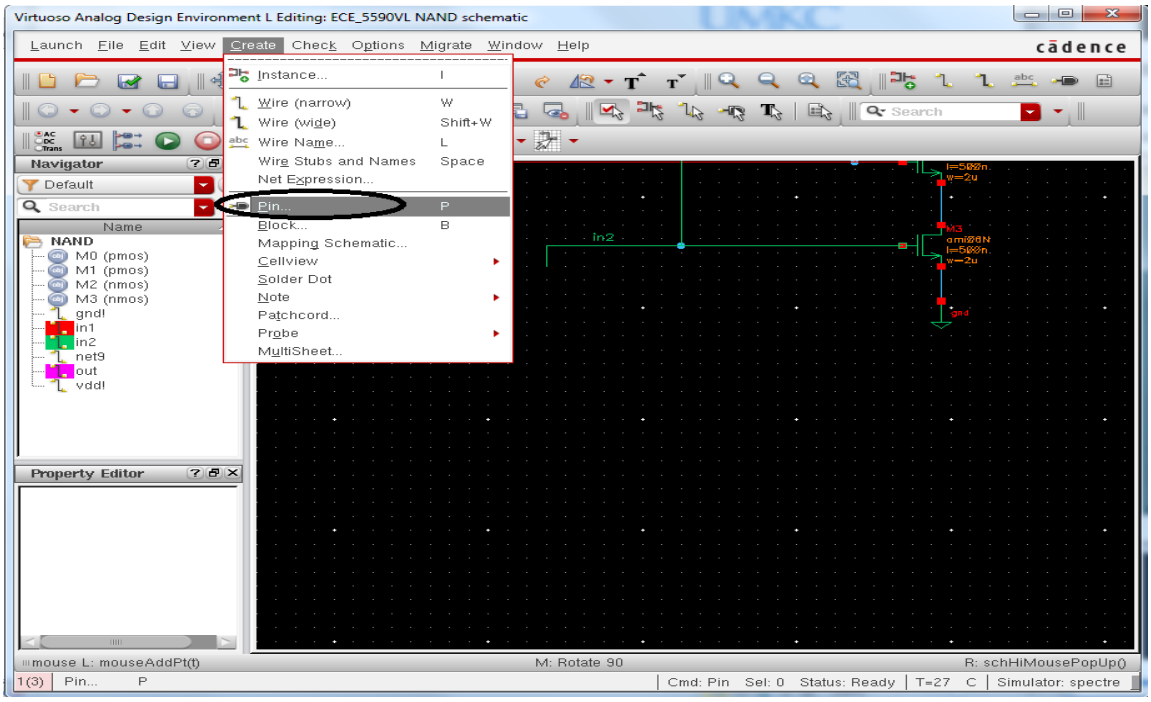
Now go back to **Virtuoso Schematic Editor** window and delete all the input voltages and associated components. Which means, both **vplus, vdc, vidd,** and **three gnd** as shown below.



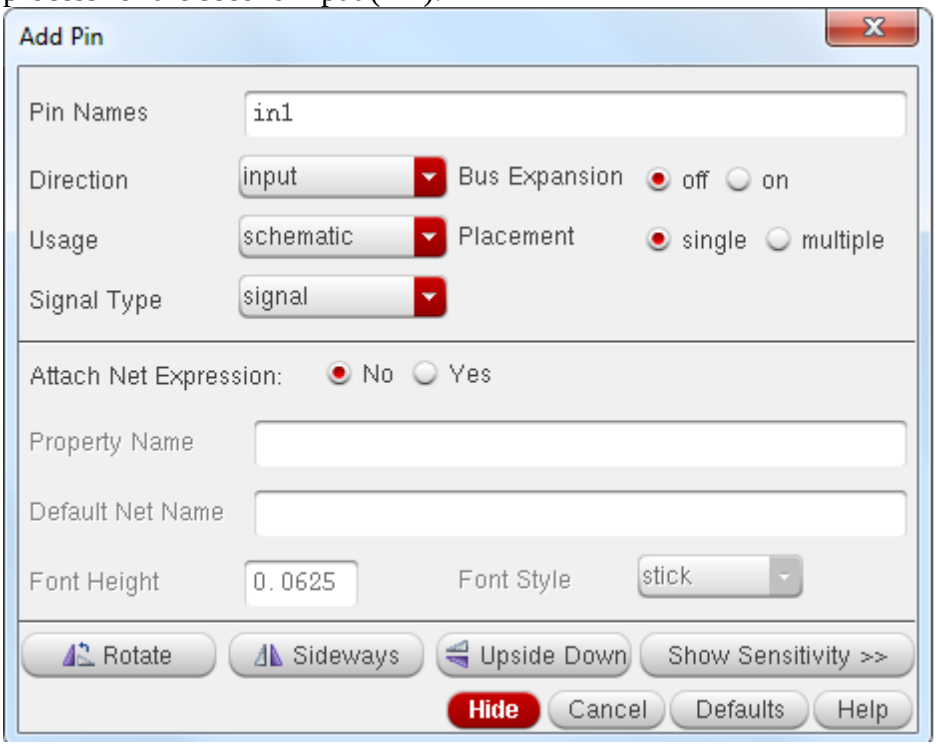
Note: to delete an object you have few options:

1. You could select on the object and tap on delete key on the keyboard
2. You could select the object and use X button from the selection options
3. You could select the object and right click on it and then click on delete

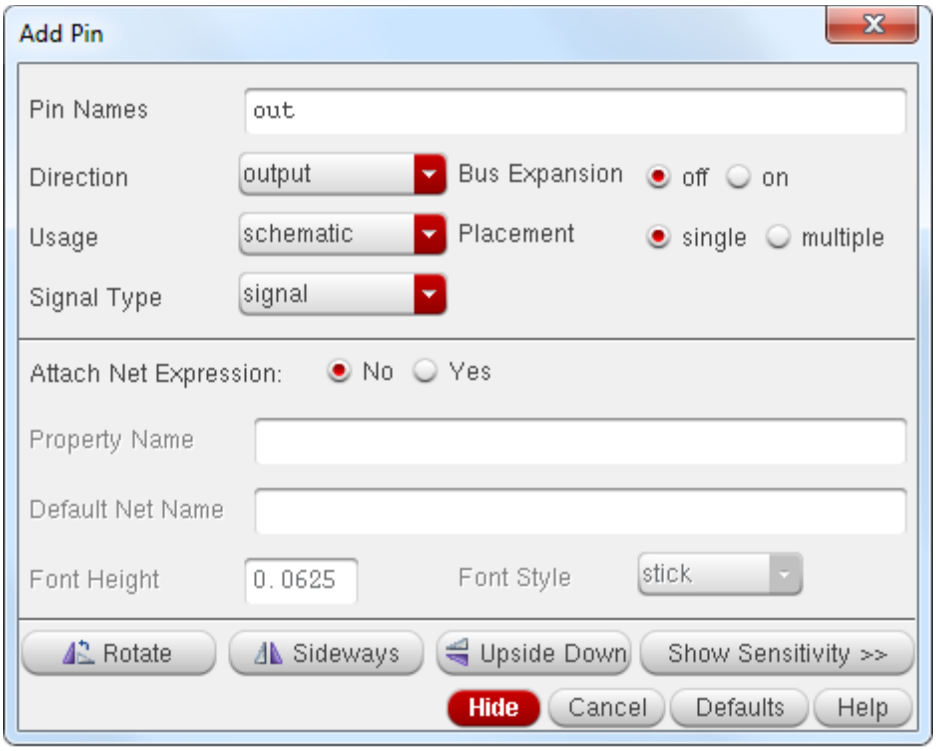
Now we will add pins to our inputs and output. Click on **create → pin**



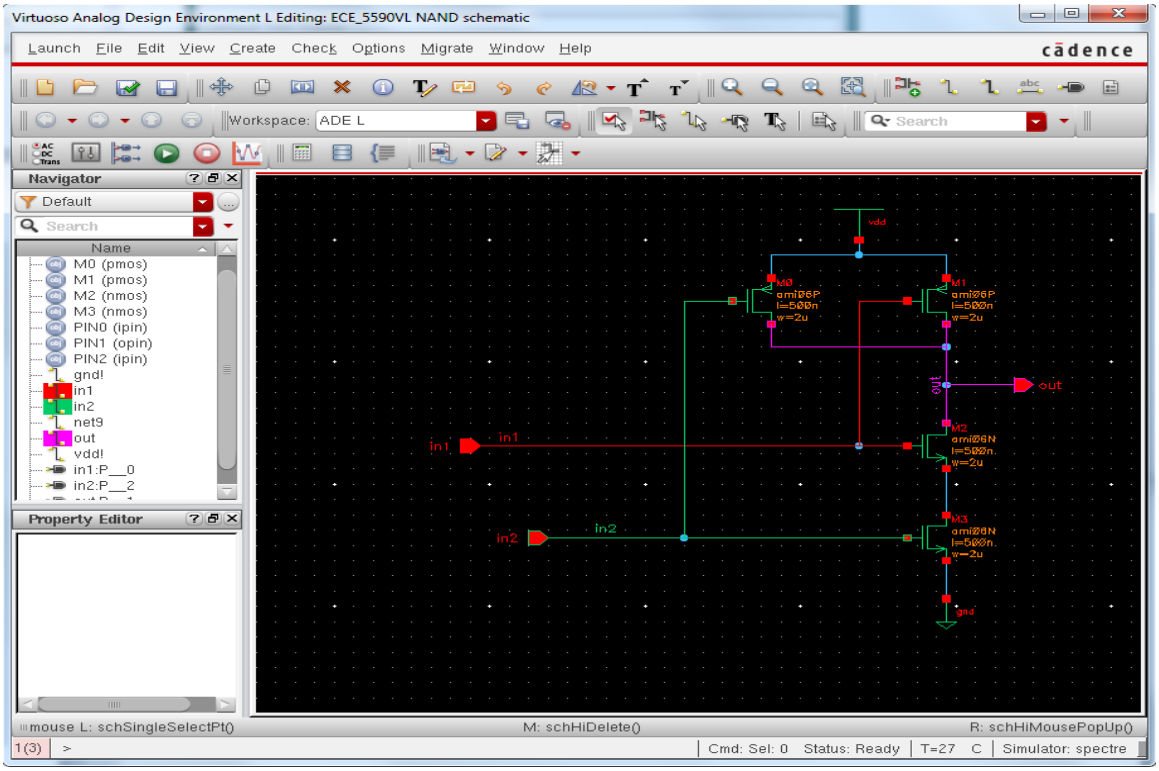
On the **Add Pin** window, under the **Pin Names** space type **in1** and chose **input** from the **Direction** selection options and click on **Hide** to place it on the window. Repeat the same process for the second input (**in2**).



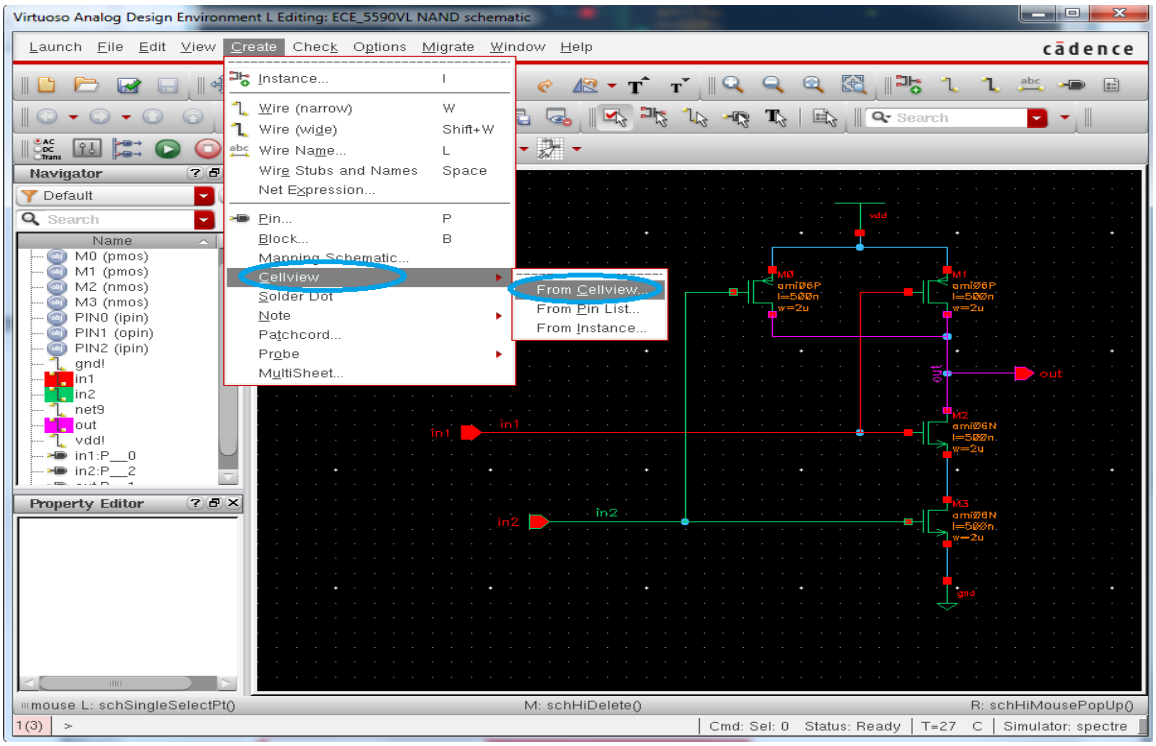
Follow the same procedure and type **out** for the output. Make sure to change the **Direction** to **output**.



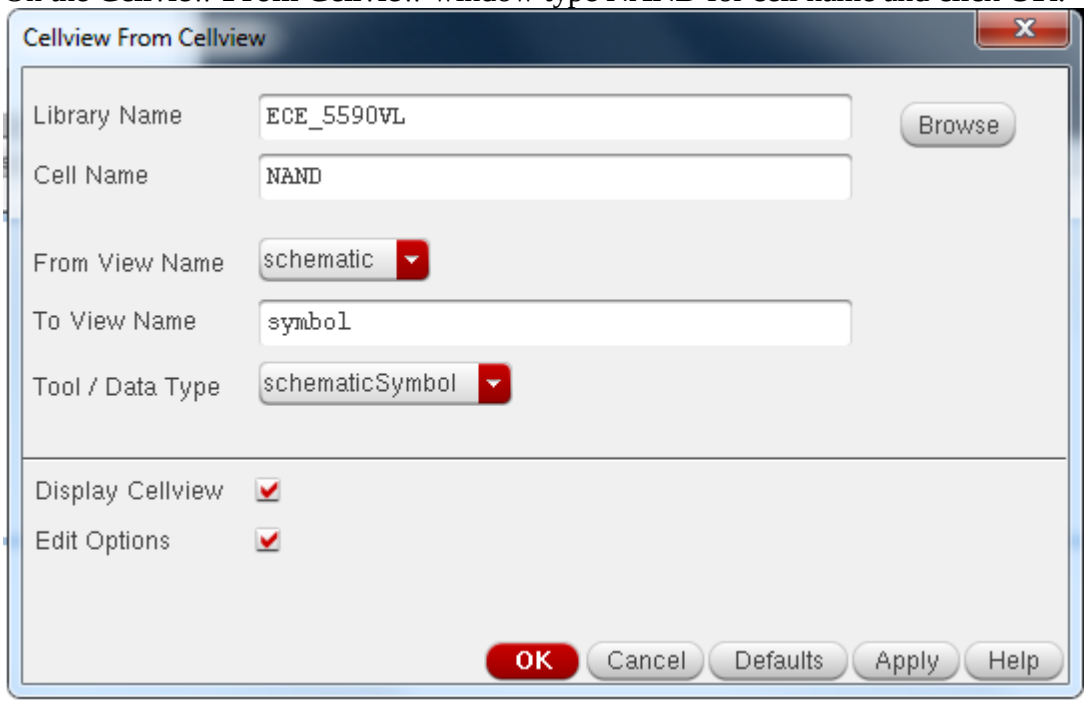
At this point, the **Virtuoso Schematic Editor** window should look as follow. Click on check and save button to verify your design. If you don't have any errors, proceed to the next steps in creating the NAND symbol.



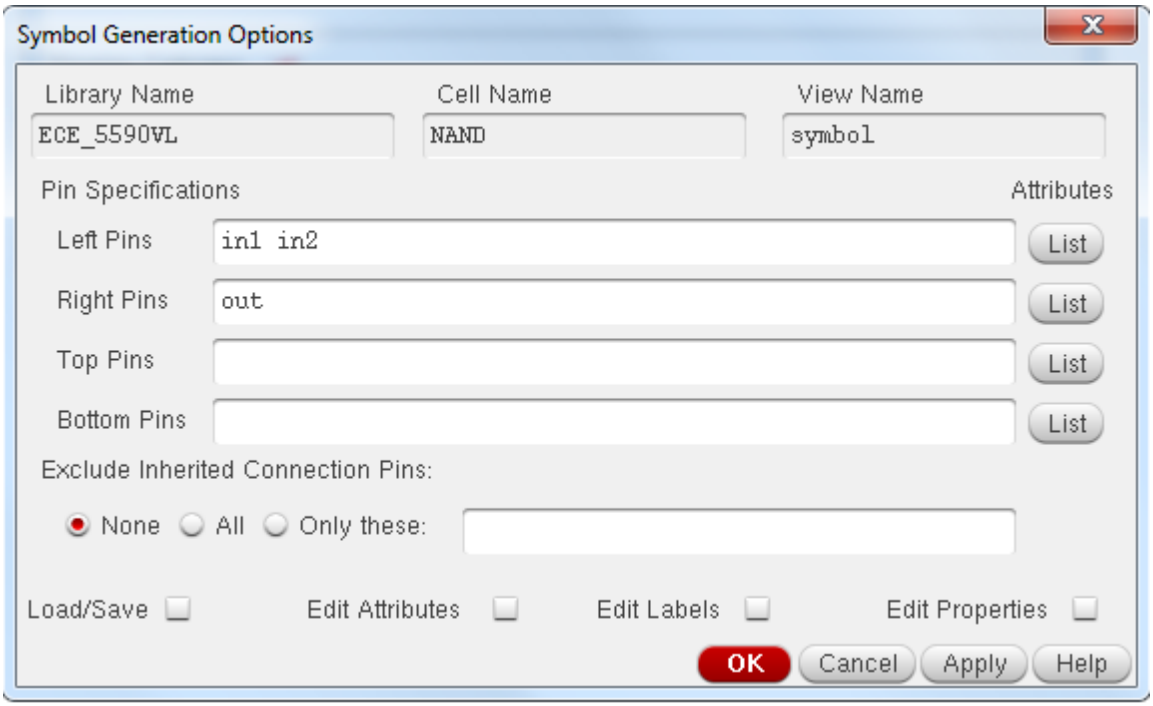
Click on **Create → Cellview → From Cellview.**



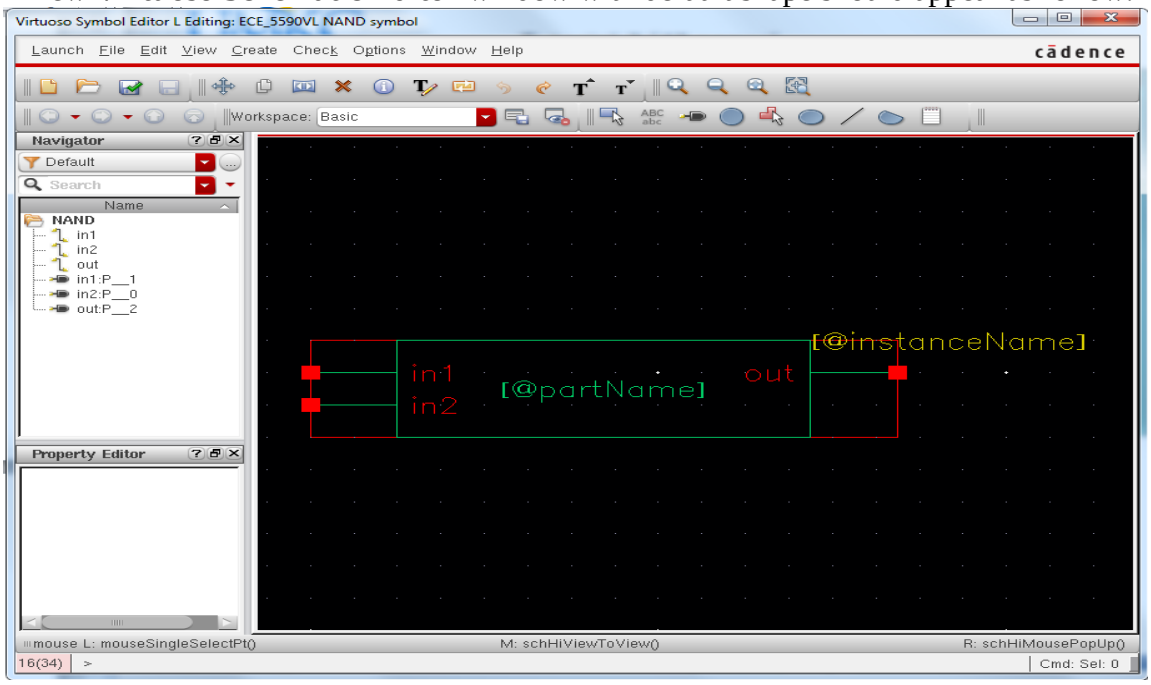
On the **Cellview From Cellview** window type **NAND** for cell name and click **OK**.



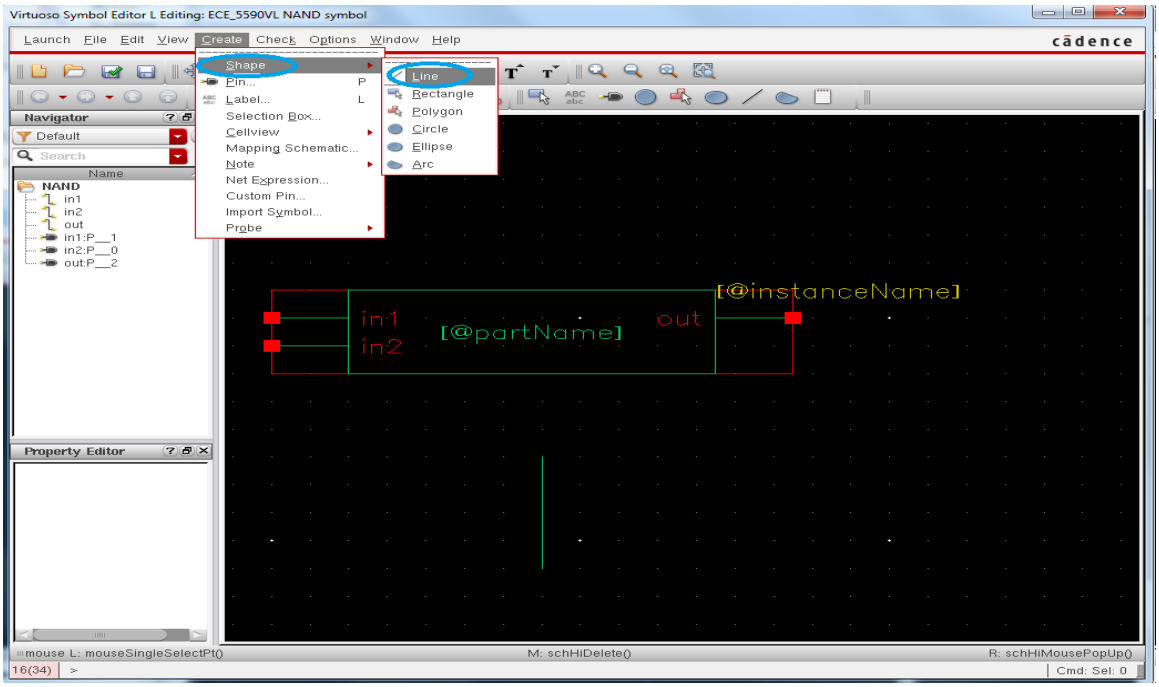
When the **Symbol Generation Options** window appear, click **OK**.


Symbol Generation Options
Library Name
Cell Name
View Name
ECE_5590VL
NAND
symbol
Pin Specifications
Attributes
Left Pins
in1 in2
List
Right Pins
out
List
Top Pins
List
Bottom Pins
List
Exclude Inherited Connection Pins:
None
All
Only these:
Load/Save
Edit Attributes
Edit Labels
Edit Properties
OK
Cancel
Apply
Help

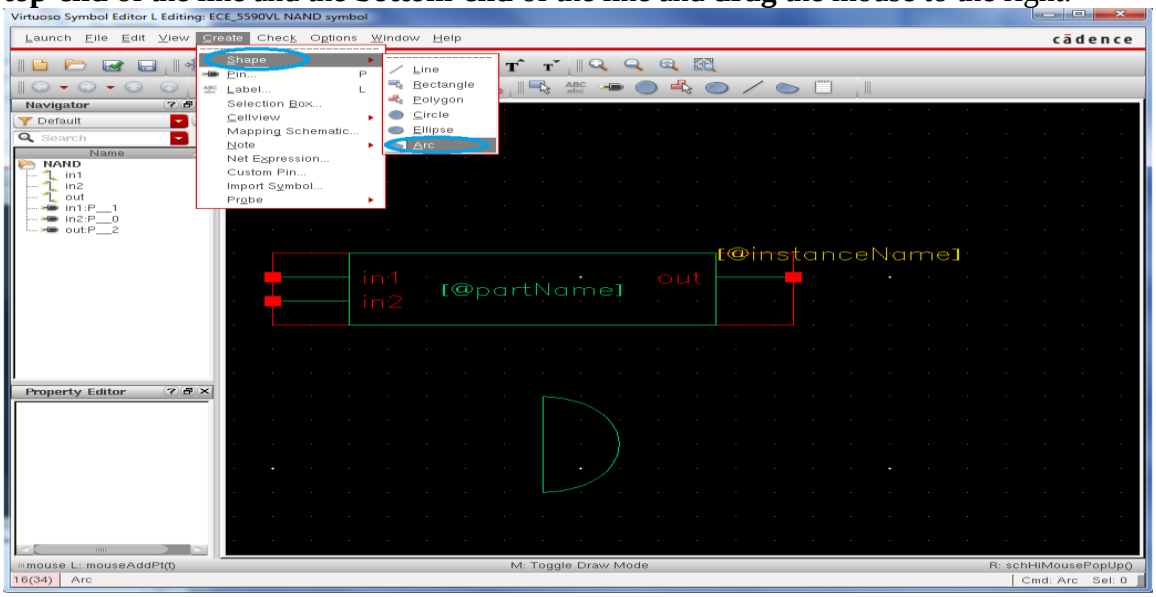
A new **Virtuoso Schematic Editor** window with default shape should appear as follow.



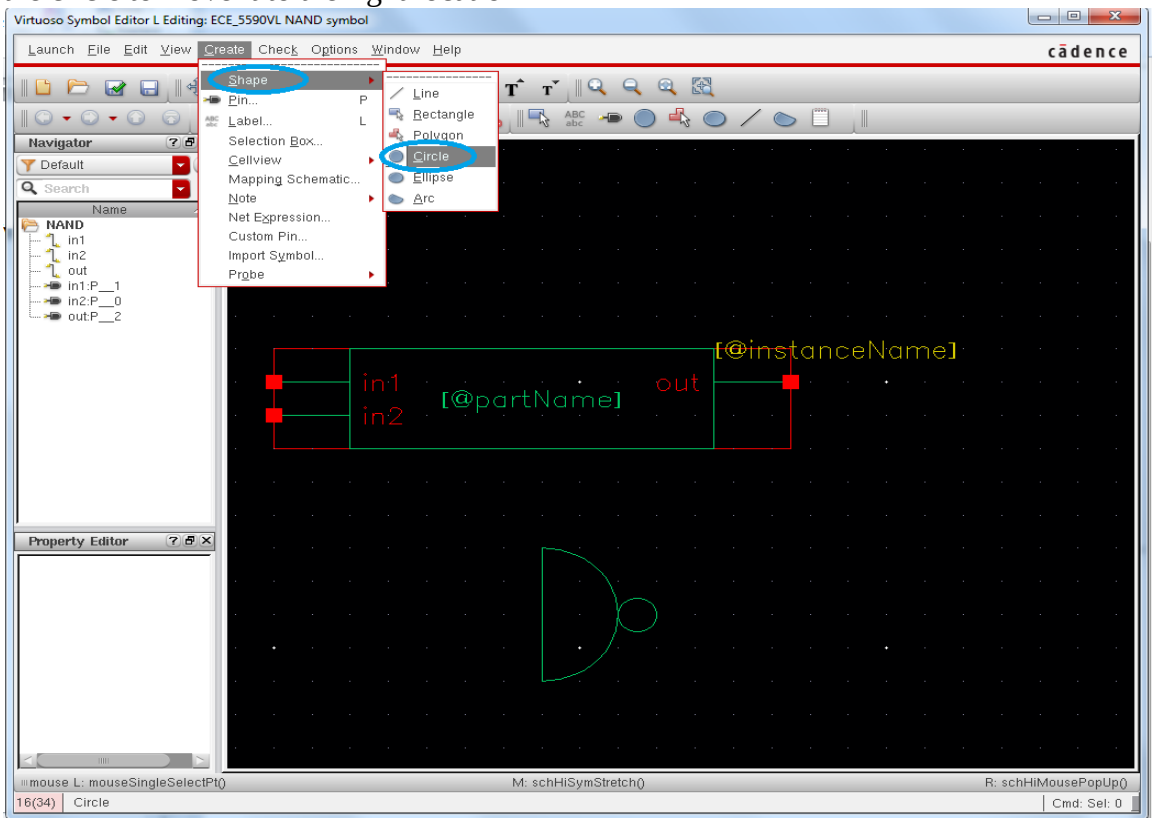
We can change the default shape in to the shape of a NAND that we are familiar with in the past. To do just that, click on **Create → Shape → Line**. Double click to place and draw the line as shown.



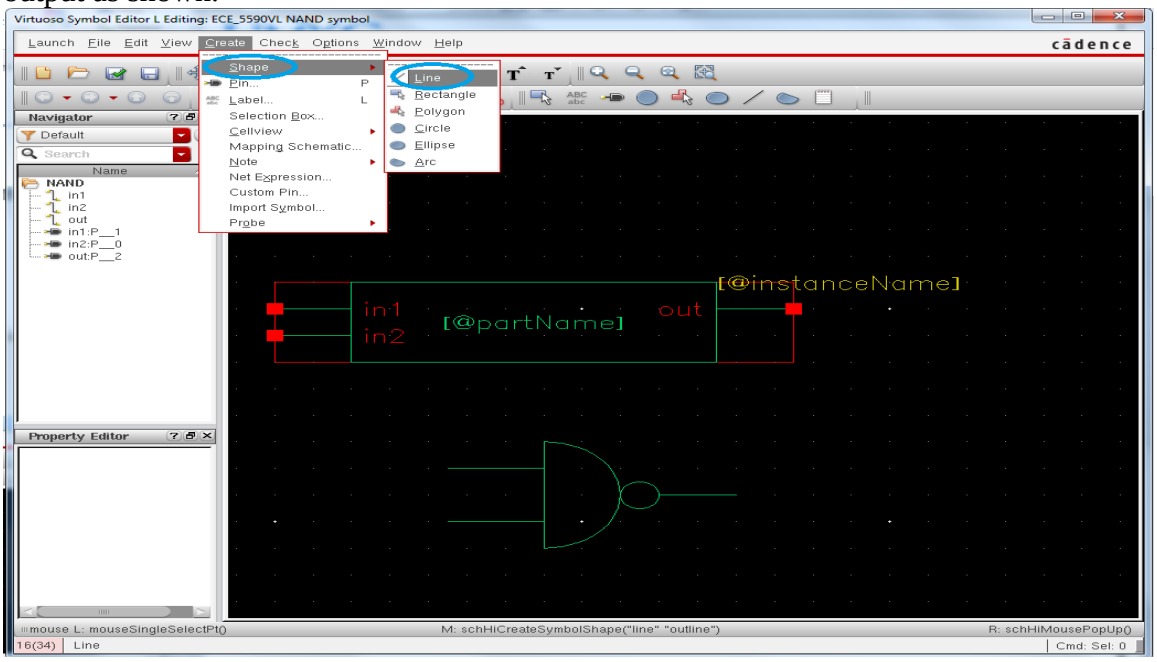
Then, click on **Create → Shape → Arc** and draw an arc as shown. To draw the **arc**, click the **top-end** of the line and the **bottom-end** of the line and **drag** the mouse to the right.



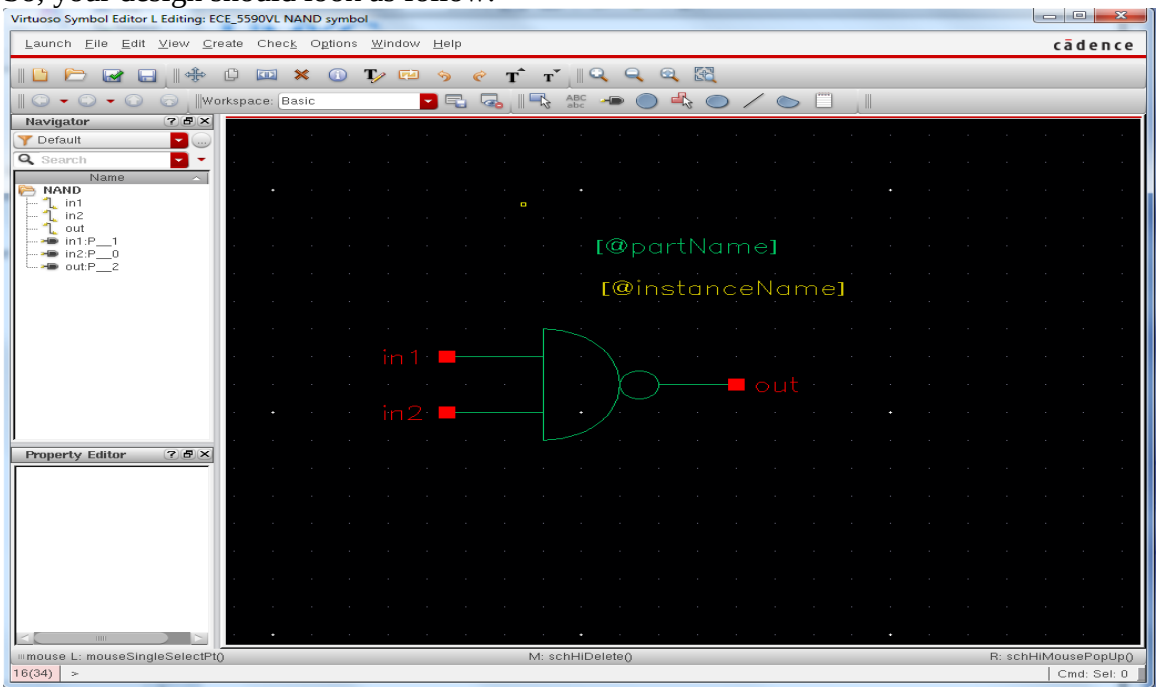
After that, click on **Create → Shape → Circle** and draw circle as shown. Type **m** and click on the circle to move it to the right location



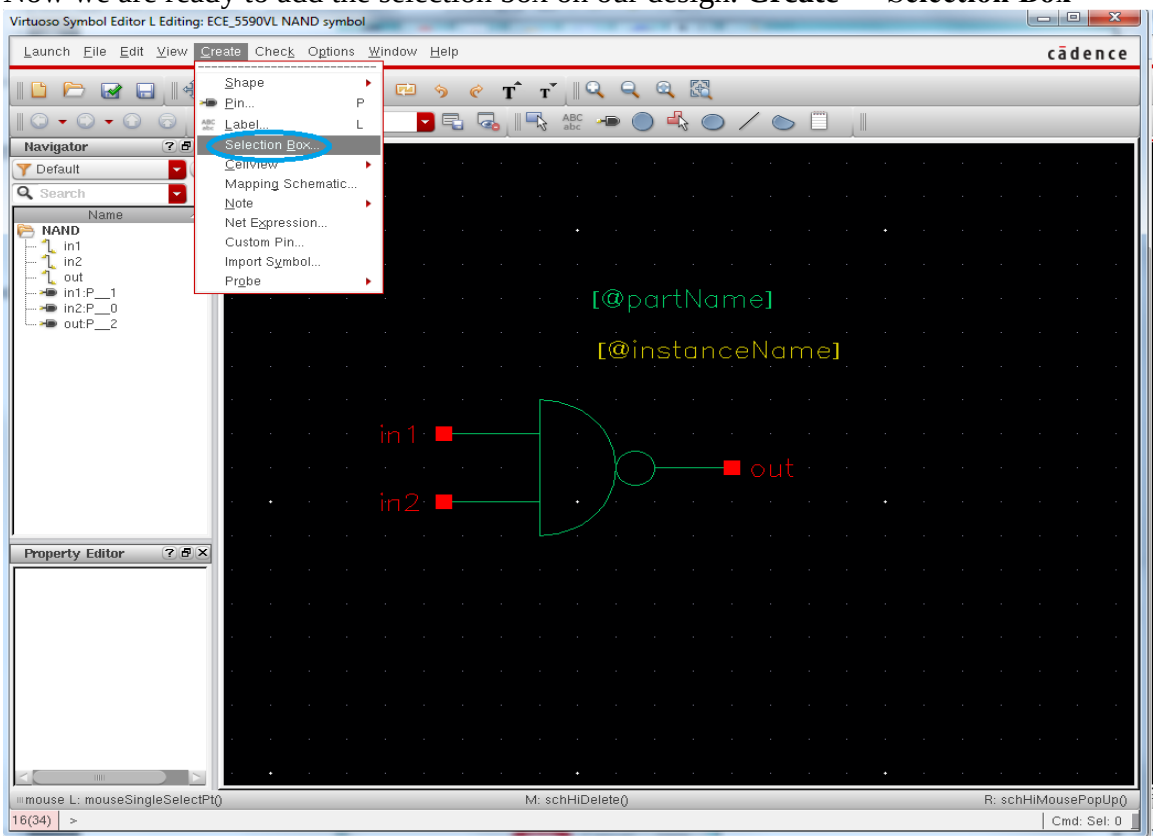
Click on **Create → Shape → Line.** Double click to place and draw the two input lines and the output as shown.



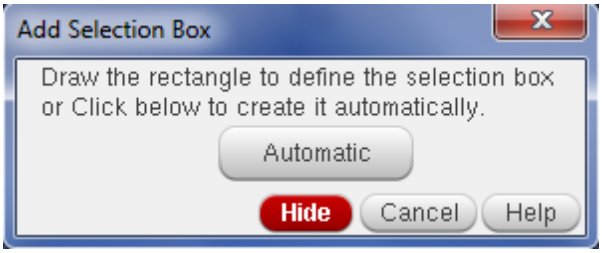
Now you can delete the default **red lines** and **green boxes** and move the **inputs** and **output** pins to the **new shape**. Also, try to rearrange the inputs and output pin names by dragging them using your mouse.
(Note: do not delete the **[@partName]**, **[@instanceNamelabels]**, and the **inputs** and **output** pins.)
So, your design should look as follow.



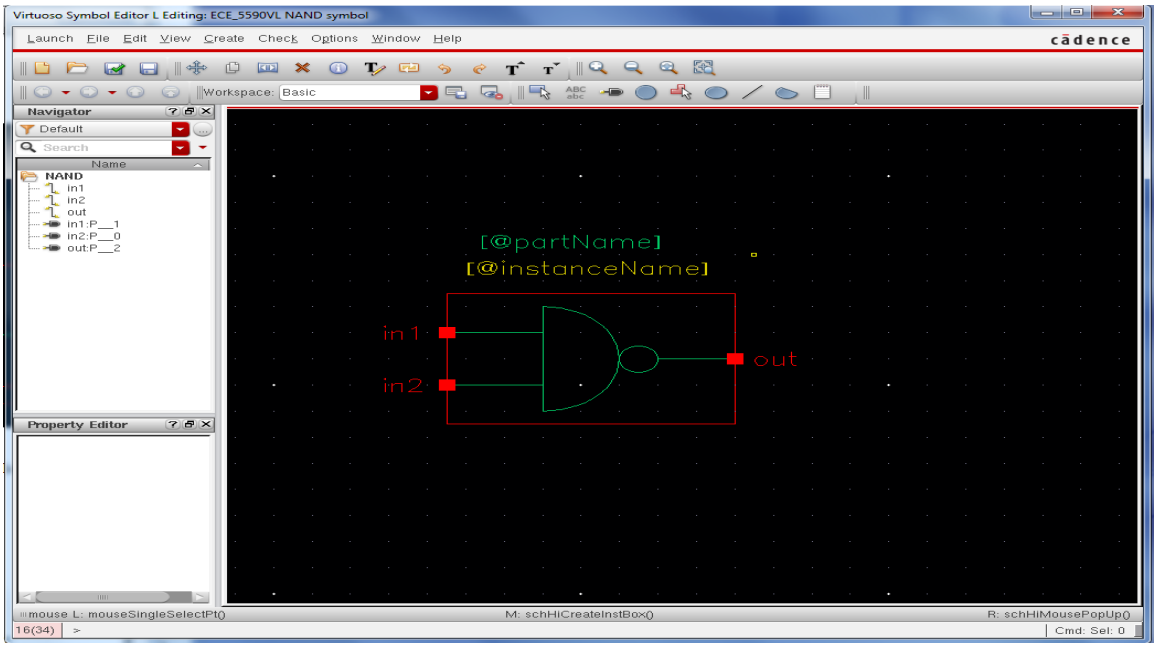
Now we are ready to add the selection box on our design. **Create → Selection Box**



Click on the Automatic

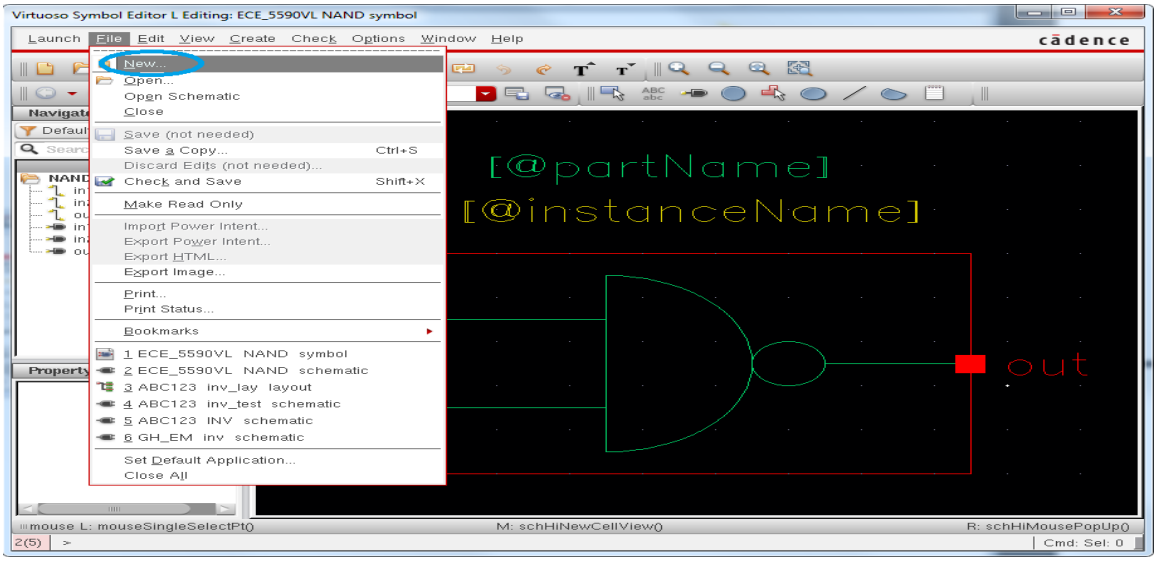


Then, by dragging any of the four sides of the rectangle and adjust your design to match the symbol shown at the bottom. After that click on **Check and Save** button to see if your design is free of error.

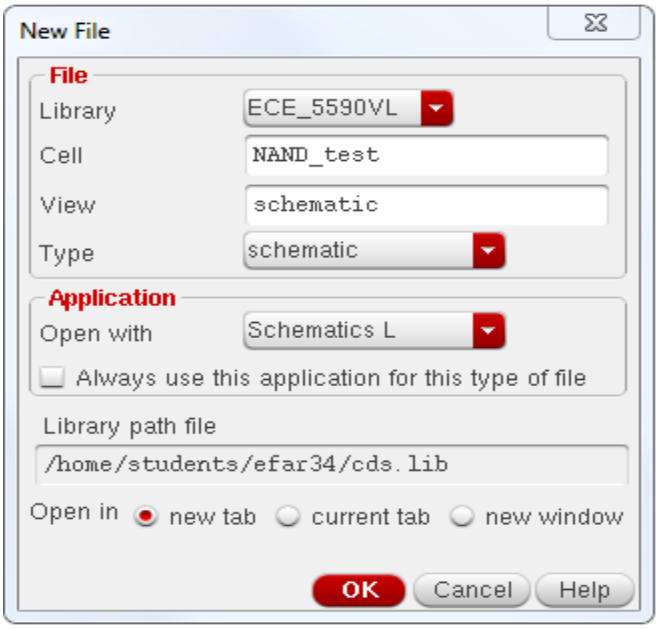

Virtuoso Symbol Editor L Editing: ECE_5590VL NAND symbol
Launch File Edit View Create Check Options Window Help
cadence
Workspace: Basic
Navigator
Default
Search
Name
NAND
in1
in2
out
in1:P__1
in2:P__0
out:P__2
Property Editor
[@partName]
[@instanceName]
in1
in2
out
mouse L: mouseSingleSelectPt()
M: schHiCreateInstBox()
R: schHiMousePopUp()
16(34)
Cmd: Sel: 0

Simulating the NAND symbol

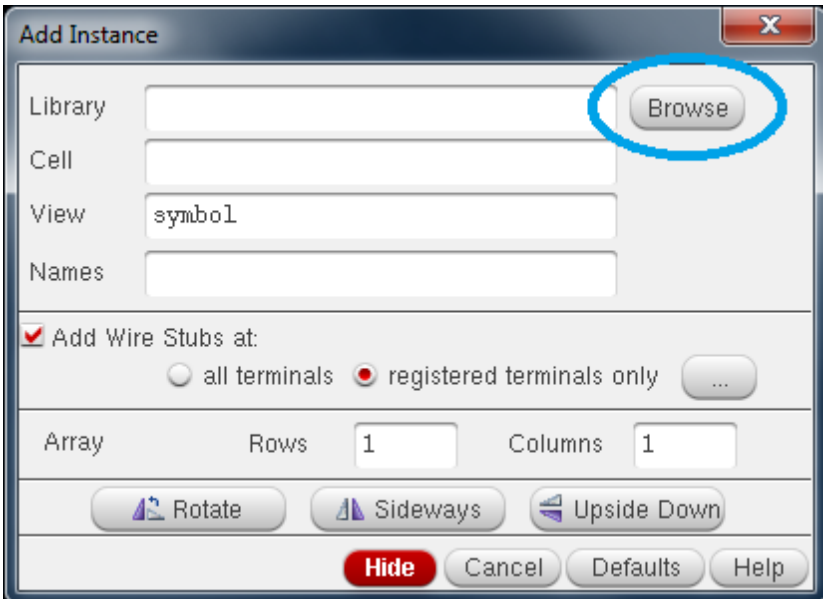
Go to file



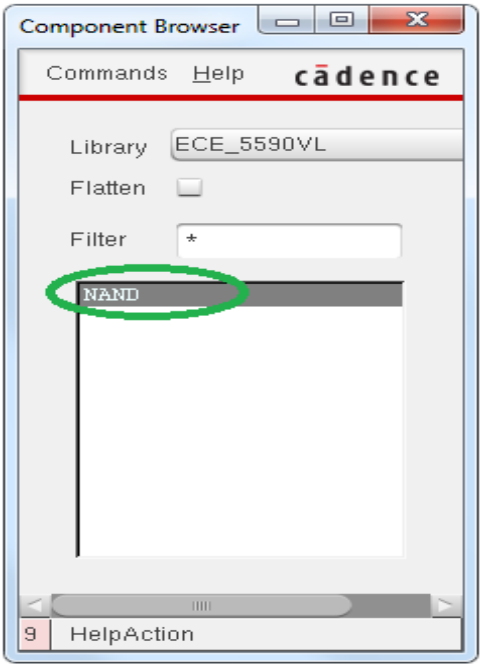
On the **New File** window select schematic from **Type** selection, and under **Cell** name wire **NAND_test** then click **OK**



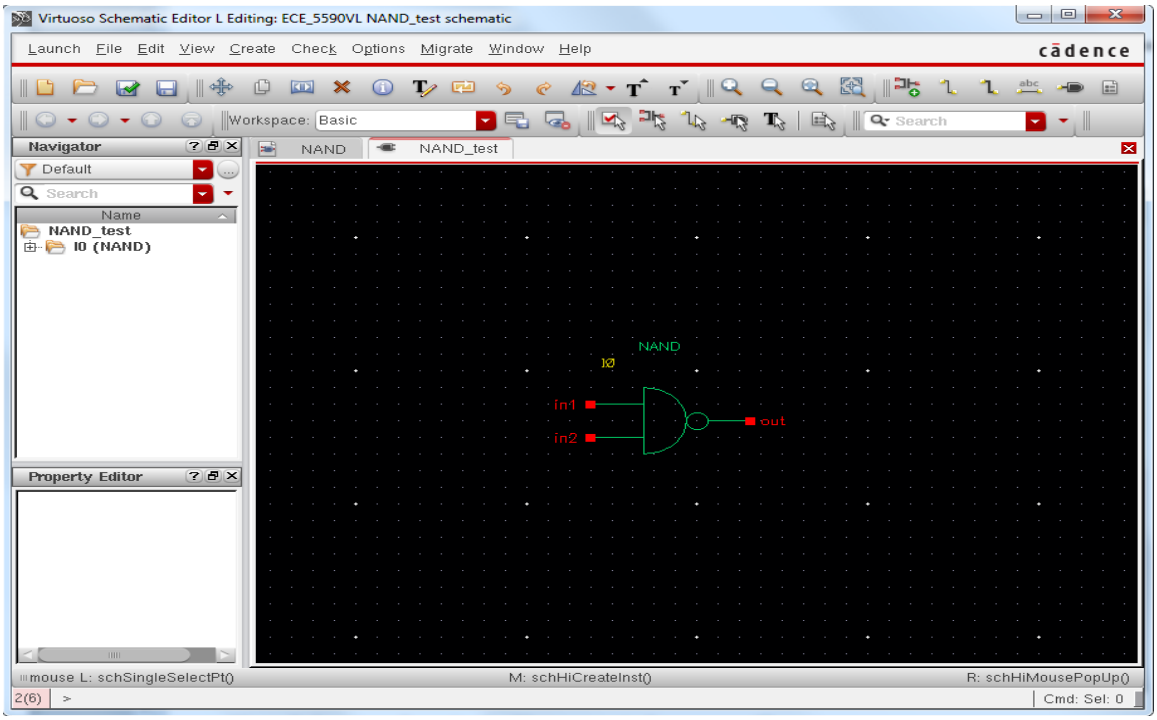
Create → Instance → Browse → Hide



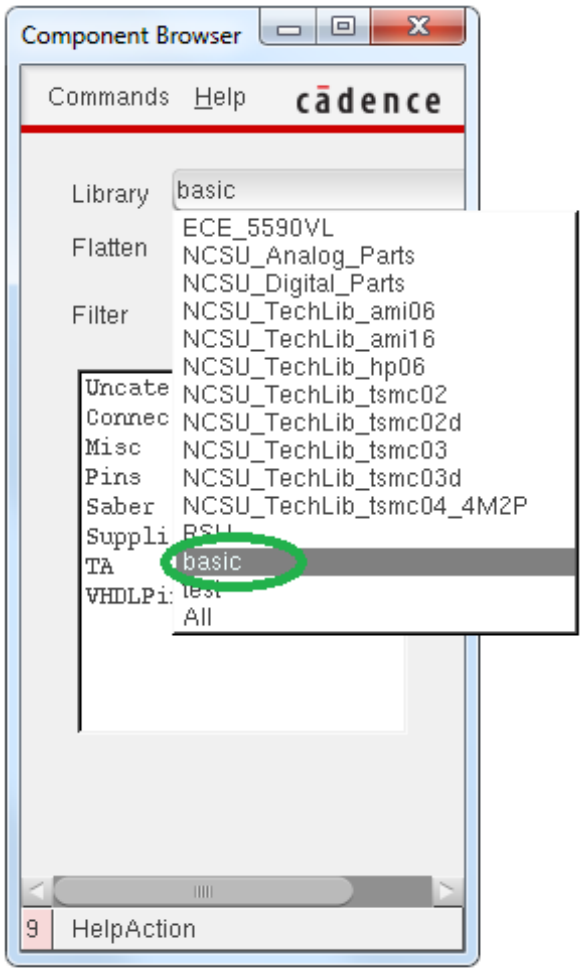
On the **Component Browser** window under the **Library** options**,** select **ECE_5590VL** (or whichever your library name). Then, click on the **NAND** symbol. After placing the symbol tap on **Esc** key on your keyboard to exit out of the command.



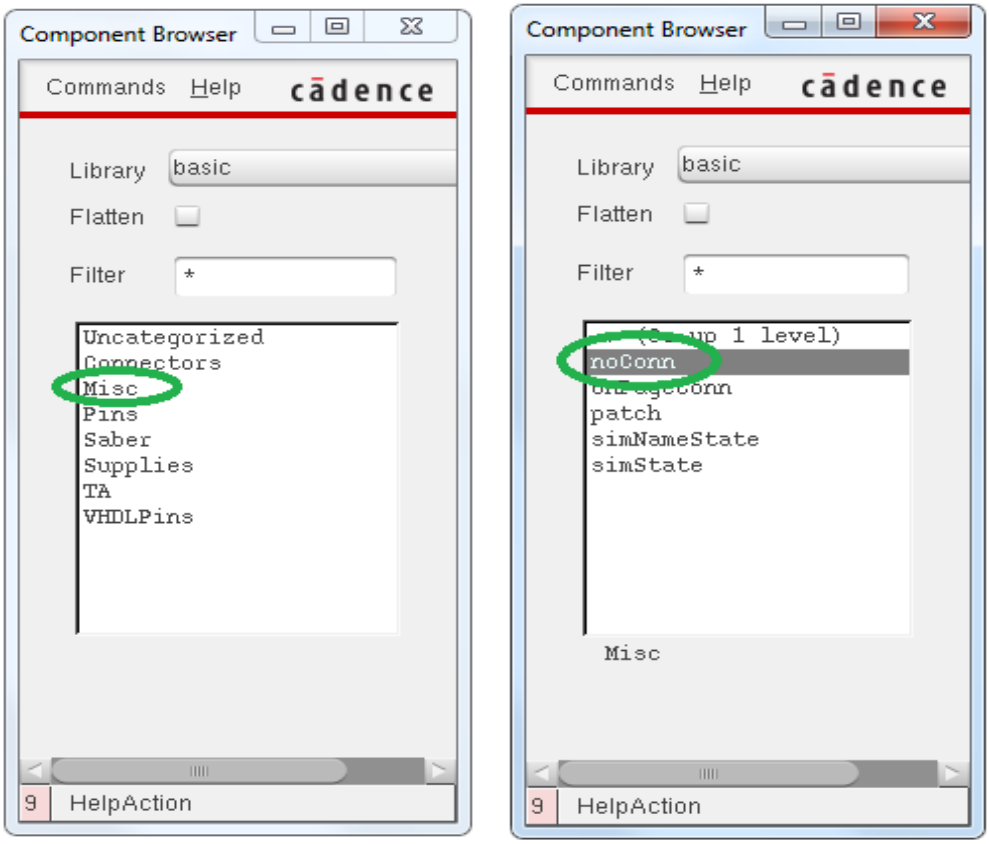
The **Virtuoso Schematic Editor** window should look as follow.


Virtuoso Schematic Editor L Editing: ECE_5590VL NAND_test schematic
Launch File Edit View Create Check Options Migrate Window Help
cadence
Workspace: Basic
Search
Navigator
Default
Search
Name
NAND_test
I0 (NAND)
Property Editor
NAND
NAND_test
NAND
I0
in1
in2
out
mouse L: schSingleSelectPt()
M: schHiCreateInst()
R: schHiMousePopUp()
2(6)
Cmd: Sel: 0

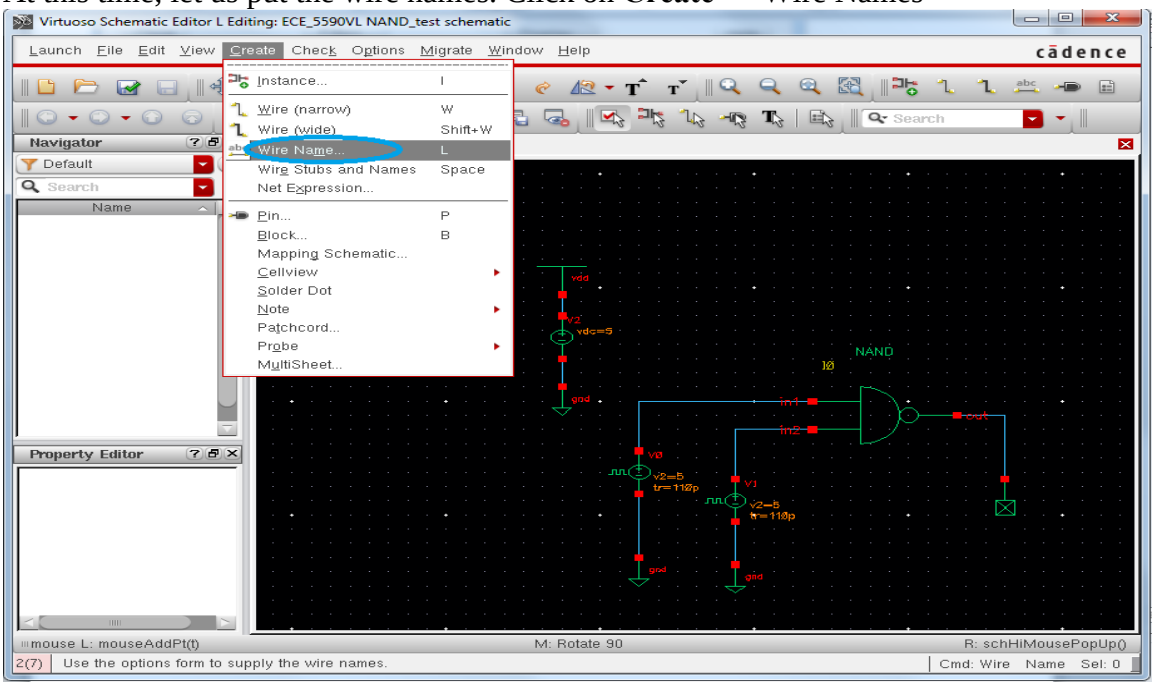
Now, we need to put back the **vdd**, **gnd**, **vdc** and both **vpulse** and enter the proper values that are given above. Also click on **Create → Instance** under the **Component Browser** select **basic**.



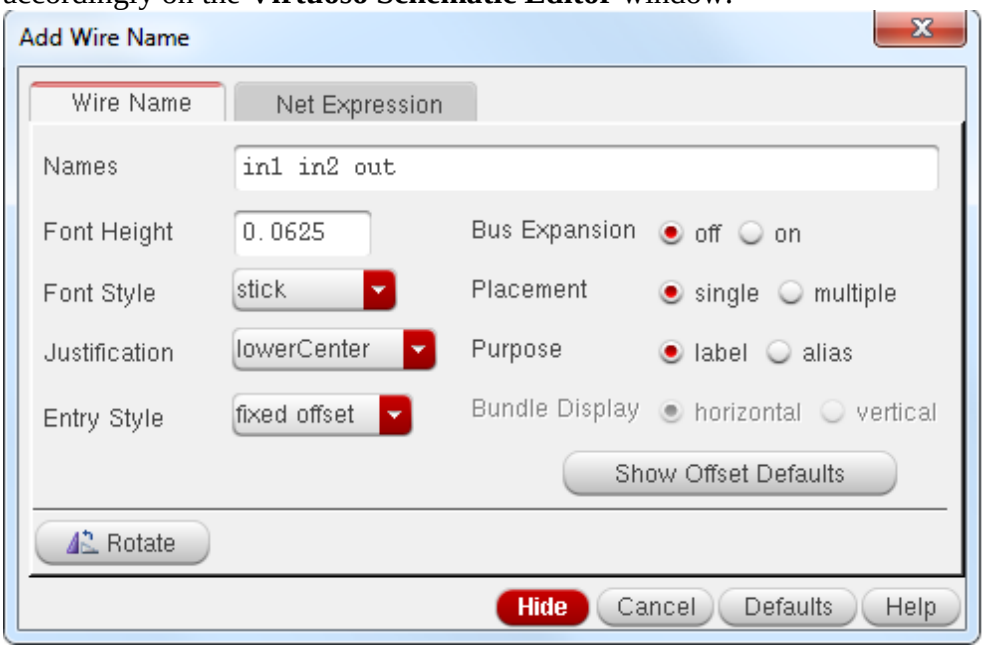
Then, click on **Misc → noConn**



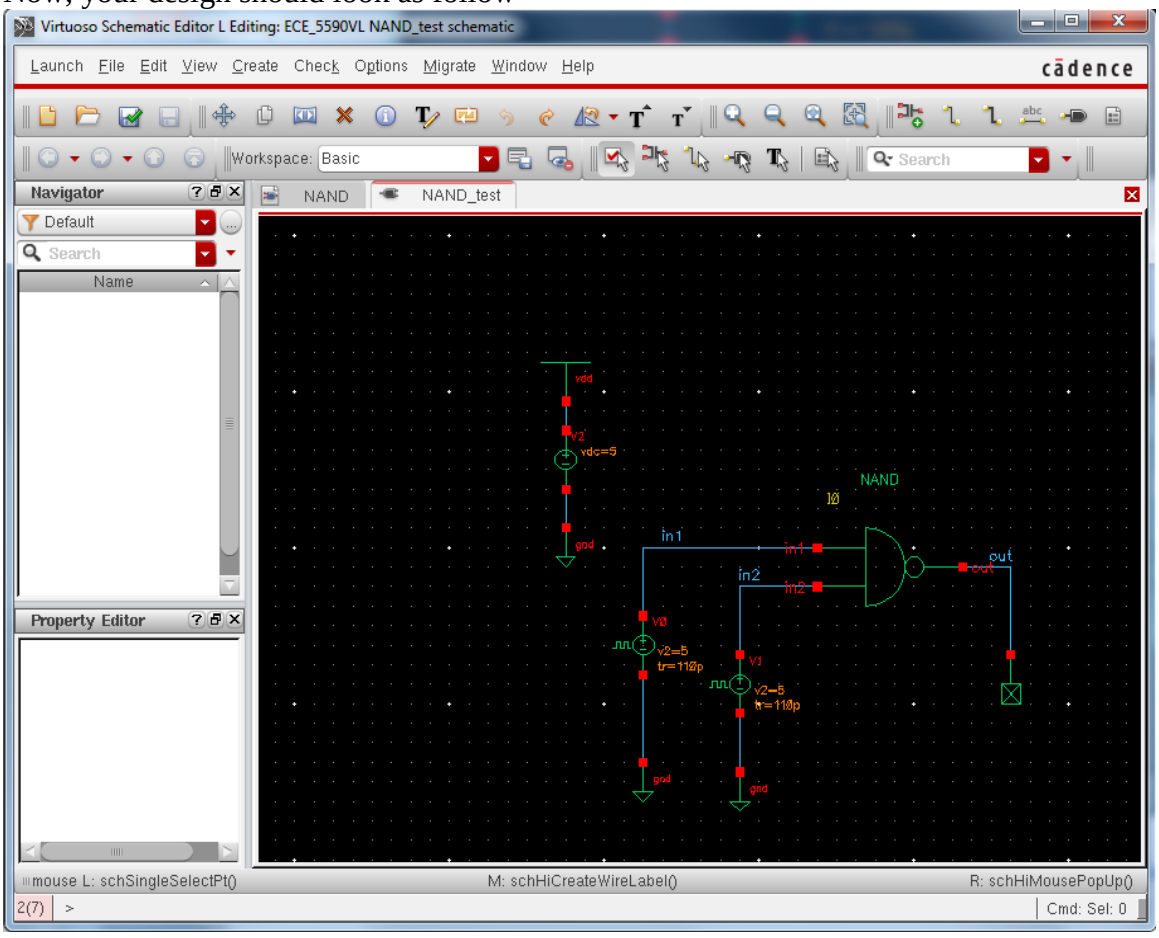
At this time, let us put the wire names. Click on **Create** → Wire Names



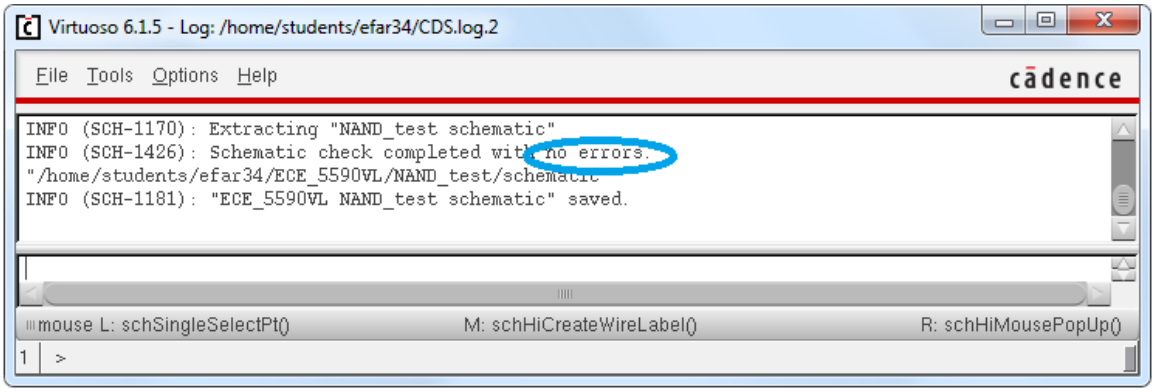
On the **Add Wire Name** window add **in1, in2** and **out** then click **Hide** and place them accordingly on the **Virtuoso Schematic Editor** window.



Now, your design should look as follow



Click on **Check and Save** button to conform if your design is free of error



Follow the simulation procedure given above and conform your result

You are done with the schematic part of the tutorial!

Acknowledgment:
This tutorial was prepared with the reference previously prepared by Dr. Daniel Leon-Salas and Mohammad Benyhesan.