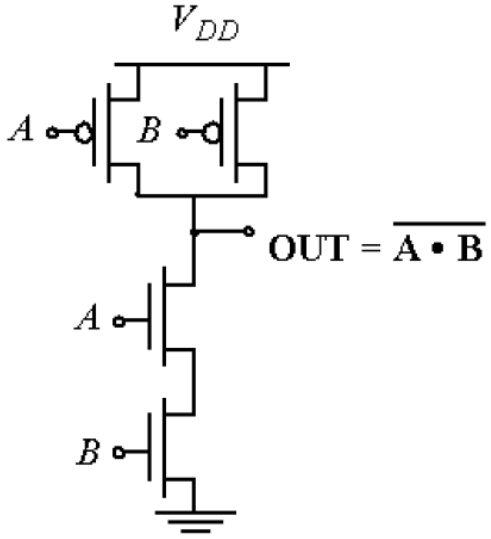
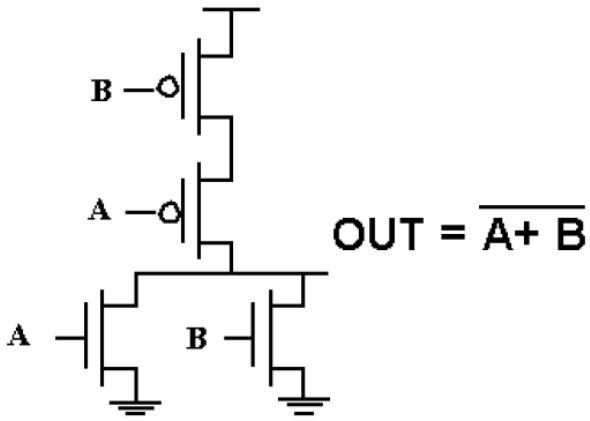
A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

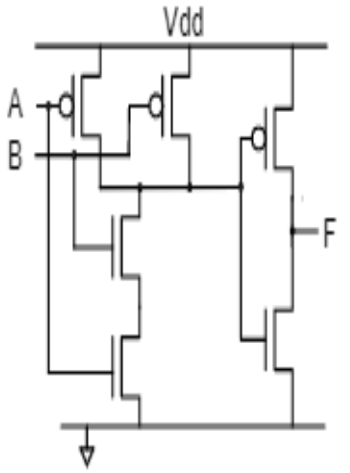
Truth Table of a 2 input NAND gate



A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

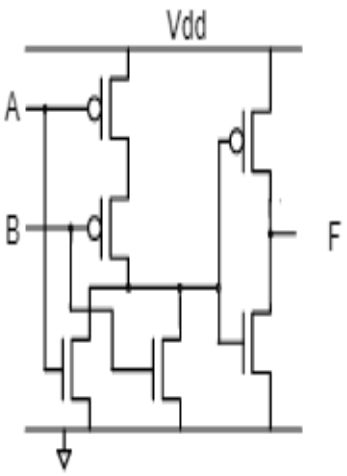
Truth Table of a 2 input NOR gate





A	B	F
L	L	L
L	H	L
H	L	L
H	H	H

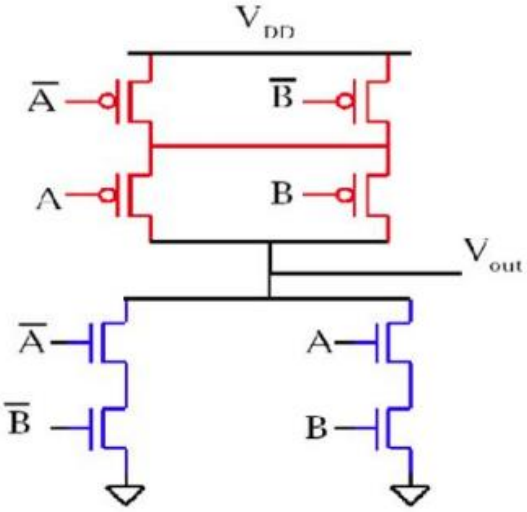
CMOS AND



A	B	F
L	L	L
L	H	H
H	L	H
H	H	H

CMOS OR

Xor gate



INPUT		OUTPUT
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0