## Answers

1 (a) Low-state DC noise margin = VIL(max) - VOL(max)

Circuit A: 0.9 – 0.4 = 0.5V

Circuit B: 0.7 – 0.3 = 0.4V

High-state dc noise margin = VOH(min) - VIH(min)

Circuit A: 2.2 – 1.6 = 0.6V

Circuit B: 2.5 – 1.8 = 0.7V

Taking the worst case (lower value) in each circuit, DC noise margin is 0.5V for circuit A and 0.4V for circuit B.

Thus circuit A has better DC noise margin.

(b) Low-state DC fan-out = IOL(max) / IIL(max)

Circuit A: 25/1 = 25

Circuit B: 30/1.5 = 20

High-state DC fan-out = IOH(max) / IIH(max)

Circuit A: 20/1 = 20

Circuit B: 27/1.5 = 18

Taking the worst case (lower value) in each circuit, DC fan-out is 20 for circuit A and 18 for circuit B.

Thus circuit A has better DC fan-out.

(c) Compare the propagation delays tPHL and tPLH.

Circuit A has much shorter delays than B.

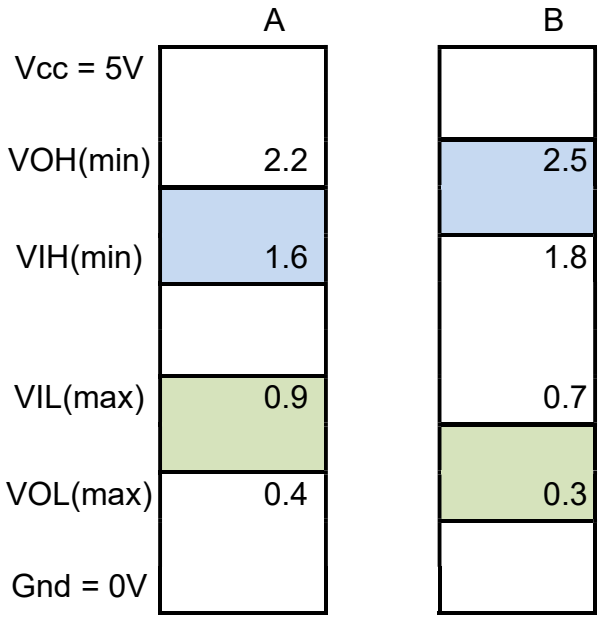
Thus circuit A can operate at a higher frequency than B.

(d) Circuit A is able to drive circuit B (meaning output of A can meet requirement of input of B) provided that ALL the following conditions are met:

VOL(max) of A must be <= VIL(max) of B
VOH(min) of A must be >= VIH(min) of B
IOL(max) of A must be >= IIL(max) of B
IOH(max) of A must be >= IIH(max) of B

Referring to the values in the table, circuit A is able to drive circuit B.

Circuit B is also able to drive circuit A.
Thus the 2 circuits are electrically compatible.
The following figure (not drawn to scale) may help to visualise it:




When A drives B, the noise margin is
Minimum (2.2 – 1.8, 0.7 – 0.4) = 0.3V

When B drives A, the noise margin is
Minimum (2.5 – 1.6, 0.9 – 0.3) = 0.6V

2. The buffer enable input has a bubble drawn. This means it is an active-Low enable input (i.e. 0: enable, 1: disable).

   When Direction=0, it enables the top buffer and disable the bottom buffer.
   Digital data can be transmitted from A to B.

   When Direction=1, it disables the top buffer and enables the bottom buffer.
   Digital data can be transmitted from B to A.

3. By now, it should be quite obvious that Q1 and Q2 form an inverter for input A.

   When A' = 1 (i.e. A=0) it turns on Q3 and turns off Q4.
   This forces Z to 0 regardless of inputs B and C.

   When A' = 0 (i.e. A=1) it turns on Q4 and turns off Q3.
   This allows Z to depend on the inputs B and C.
   When B=C=1, Q5 and Q7 turn on, Q6 and Q8 turn off and Z will be 0;
   else Z will be 1.
   Thus Z = (B C)' when A=1

   In conclusion, A serves as the active high enable input for the 2-input NAND.
   The Boolean expression of Z may be written as:
   Z = A (B C)'
   or Z = AB' + AC'  [SOP]