Answers:

(a) For Z to be 1, Q8 and Q6 and (Q4 or Q2) must turn on.
This implies that C=D=0, and (B or A = 0).

For Z to be 0, Q5 or Q7 or (both Q1 and Q3) must turn on.
This implies that C or D=1 or (A=B=1).

(b) For Z to be 1, Q6 or Q8 or (Q2 and Q4) must turn on.
This implies that C or D=0 or (A=B=0).

For Z to be 0, (both Q5 and Q7) and (Q3 or Q1) must turn on.
This implies that C=D=1, and (A or B=1)

(a)

A	B	C	D	Z
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

(b)

A	B	C	D	Z
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

When the analysis involves fewer parallel paths, there will be fewer input options, and it may make it easier to work out the required inputs.
For any correctly designed CMOS logic circuits, we may choose to analyse only for output=0 (if it involves fewer parallel paths), or analyse only for output=1 (if it involves fewer parallel paths).
It is not necessary to analyse for both other than for practice purpose.