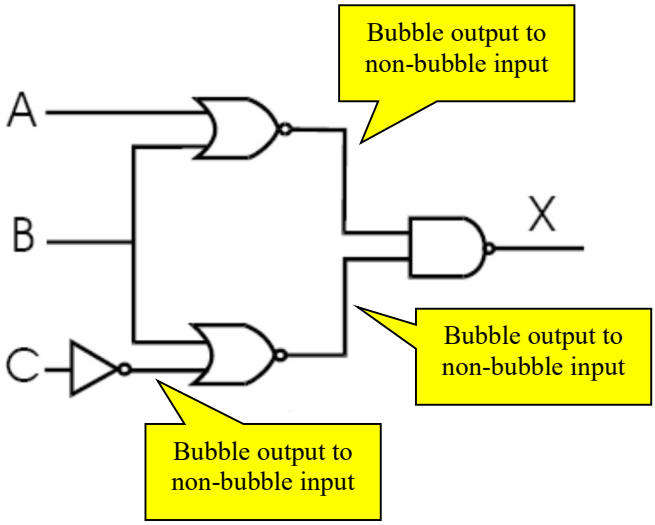
# L3 practice problems

## Answers:

1. (a) There are 3 mismatched connections:
In each case, the output has a bubble but it connects to an input that has no bubble.




*Why do we say that an unmatched bubble can be problematic for someone looking at the logic diagram?*

Let's look at the NAND. The symbol tells us X=0 if both its inputs are 1.
But the upper NOR symbol on top tells us that when A=1 or B=1 it produces 0.
This value of 0, when supplied to the input of the NAND, does not help to produce X=0.
We face a situation where a part of the diagram shows the logic value being produced at an output, but it does not match nicely to the desired input value of the next stage, and thus it does not help us to see readily the value of X.

We can certainly reason it out ourselves: When A=1 or B=1 the NOR gate produces 0. Since X=0 only when both inputs are 1, then this input value of 0 will not make X=0, meaning that X will be 1.

We prefer to avoid having to perform this extra layer of reasoning by drawing diagrams with logic symbols whose output/input is matched, i.e. either both with bubbles, or both without bubbles. This benefit is more obvious when a circuit has multiple stages.

(b)

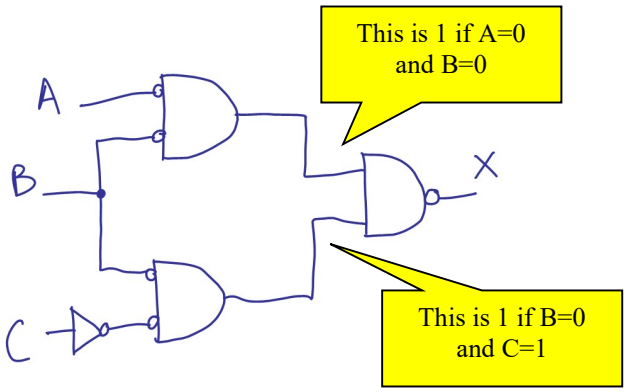



Diagram (b) clearly expresses this dependency of output X on inputs A, B, C:

X=0 if
(top path) A=0 and B=0
and at the same time
(bottom path) B=0 and C=1

Or simply X=0 if A=0, and B=0, and C=1
i.e X = (A' B' C)'

(c)

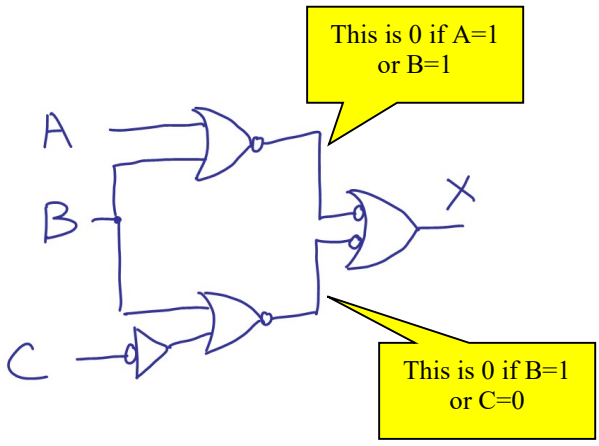



Diagram (c) expresses this relation:

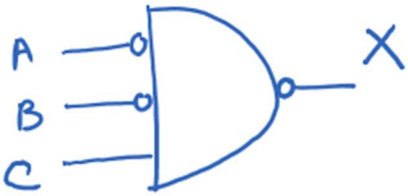
X=1 if
(top path) A=1 or B=1
or
(bottom path) B=1 or C=0

i.e. X = A + B + C'

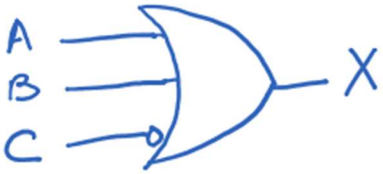
Check against the truth table obtained for the circuit in L1 Practice to verify that both diagrams (b) and (c) are logically correct.

Note that the above diagrams can be made simpler to express the same logic behaviour:

(b)




(c)




Diagrams (b) and (c) are equivalent based on DeMorgan's theorem:

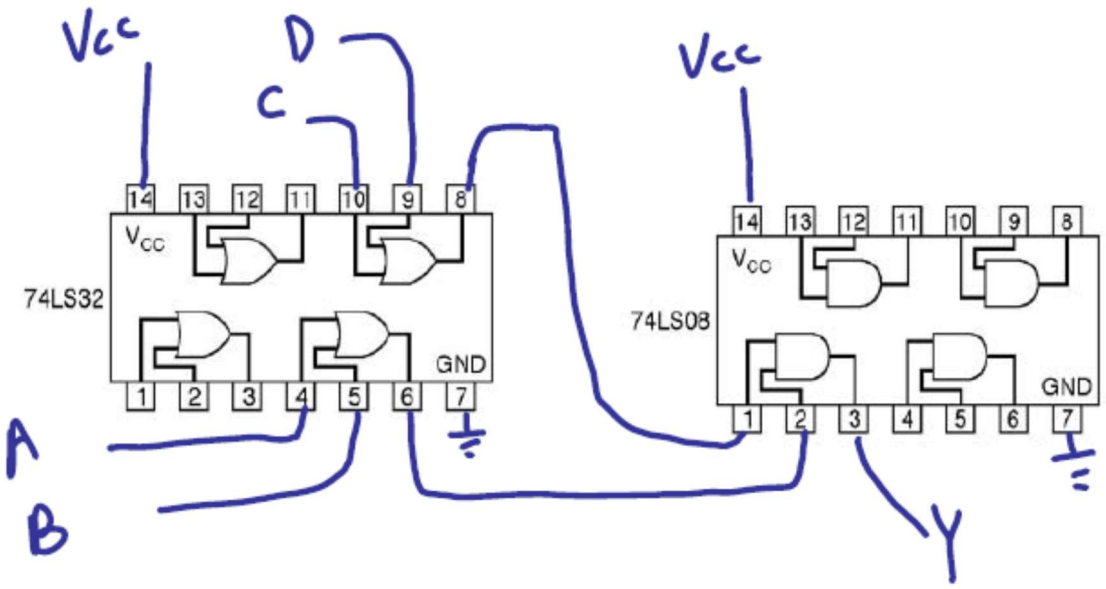
X = (A' B' C)' = A'' + B'' + C' = A + B + C'

Which is effectively the same method for drawing alternate symbols:

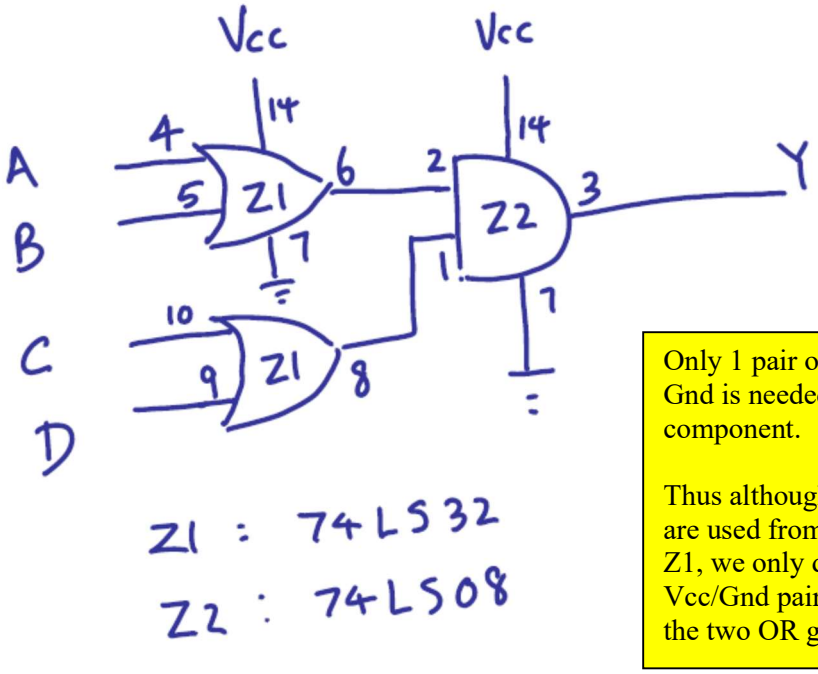
- Interchange OR-shape with AND-shape
- Interchange presence/absence of bubble at inputs as well as output

2. Y = (A + B)(C + D)

Suggested physical connection (any gates on the ICs can be used):




Corresponding circuit connection diagram:




Only 1 pair of Vcc and Gnd is needed for each component.

Thus although 2xOR gates are used from component Z1, we only draw the Vcc/Gnd pair on one of the two OR gates.

This type of circuit connection diagram is useful for lab experiment 1.