SC1005 Digital Logic
Tutorial 8

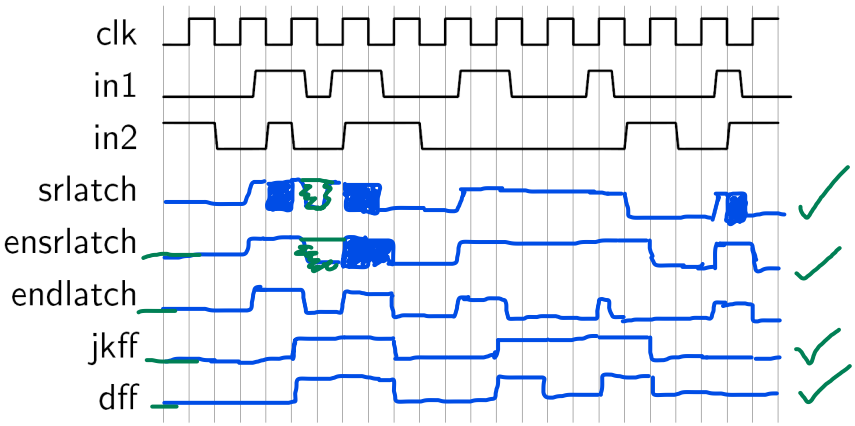
Q1. Using a behavioural description, write a Verilog module that has three 8-bit inputs, a, b, and c, and outputs the largest (max) and smallest (min) of them. Add a third output (diff) that outputs the difference between the two. You should use if statement(s). You can ignore equal inputs.

Q2. The *clk* input in the timing diagram is connected to the control/enable/clk input of the following circuits:

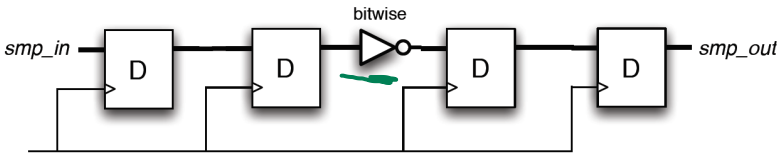
- SR-latch (no enable/control)
- Enabled SR-latch
- Enabled D-type latch
- JK flip-flop
- D flip-flop

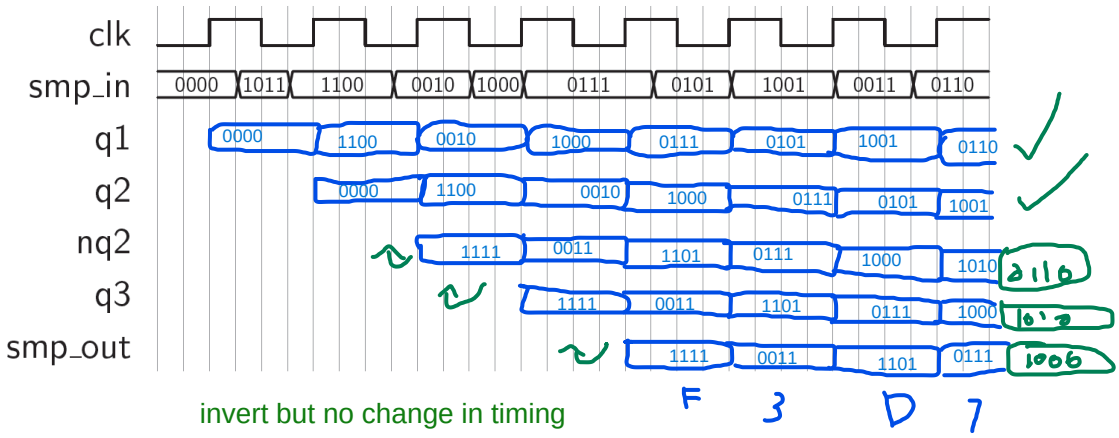
For the D-type latch and D flip-flop, the *in1* input is connected to the D input, and *in2* is left disconnected. For the SR-latches, *in1* is connected to the S input and *in2* is connected to the R input. For the JK flip-flop, *in1* is connected to the J input and *in2* is connected to the K input.

Complete the timing diagram showing the outputs of the four sequential circuits. Indicate any undefined output by shading the relevant area.



Q3. A bank of 4-bit registers is arranged as per the diagram below, to form a FIFO, with a bitwise inversion in the middle. The input shown in the diagram is applied to the leftmost register. All registers share the same clock. Show a timing diagram for the output at the rightmost register. A bitwise inversion simply inverts each bit of the signal individually. Write down the resulting hexadecimal number sequence at the output.





invert but no change in timing