5.1 Input/Output (I/O) Interface

1) With reference to the computer system diagram (Figure 1) in the case study notes,

(a) What are the type (input, output or bi-directional) of processor pins you would connect each of the module's data signal to?

Table 1a

No.	Module	Type (Input, Output or Bidirectional)
i.	Buttons	input
ii.	Wifi	input bi-directional
iii.	Touch Screen Controller	input/bi directional
iv.	System Memory	bi directional
v.	Display	output

(b) Given the following interface requirement, select the appropriate module from the device information list in the case study notes to connect to the processor.

Table 1b

No.	Module	Interface Type
i.	Wifi	SPI
ii.	Touch Screen Controller	UART
iii.	System Memory	Parallel Bus

WIFI0010AC,serial, synchronous

TS002UART,serial, Asynchronous

SRAM0002-2M16, parallel,both synchronous and ~~asynchronous~~

can also be DRAM002-16M16,NOR0001-1M

(c) For each of the interface shown in **Table 1b**, is the data transfer serial or parallel?

(d) Describe the difference between synchronous and asynchronous interface. Are the interfaces shown in **Table 1b** asynchronous or synchronous? Explain.

Strobe signal used to tell receiver when to latch in the data on the data bus

(e) With reference to the SPI wifi module chosen in 1(b) above, what is the maximum speed that data can be transferred between the wifi module and the processor?

e)~~100~~Mbps
-Max SPI clock on Wifi = 50MHz
-Max processor SPI clock = 50MHz
50Mbps

(f) With reference to the device information of the system memory you have chosen in 1(b) above, what is the maximum data transfer rate achievable between the system memory and the processor? Assuming that data on the parallel bus gets transferred on each rising edge of the data strobe.

d)Synchronous have a common clock signal to synchronize data transfer while Asynchronous do not have a common clock signal and devices have to agree on a pre-fixed clock frequency to use for data transfer.

~~381.47Mb/s~~

f) Max data transfer rate = slowest device x bits on interface
Max data strobe rate supported by SRAM = 200MHz, Max processor parallel bus strobe rate = 200MHz =>Max supported data strobe rate on this link = 200MHz

16 bit interface => 16 bits data transferred with each strobe => 200M x 16 = 3200MBps

5.2 Data Transfer

2) **Fig. 2** shows the logical waveform of an asynchronous data frame.

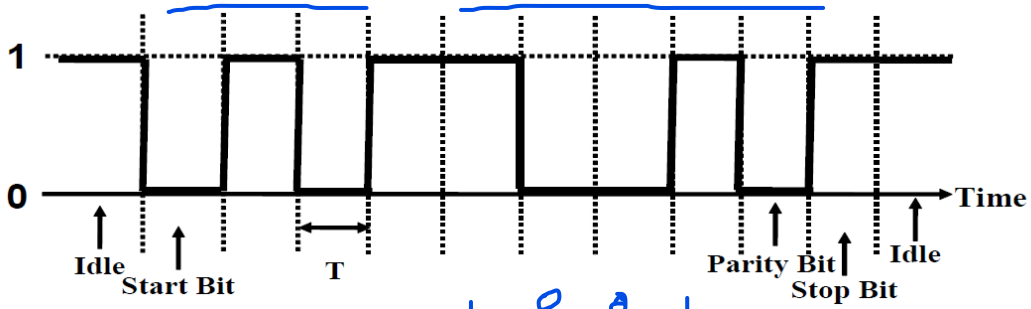

Fig. 2

Answer the following question with reference to **Fig. 2**:

(a) Specify the 7-bit ASCII character that is transmitted (LSB is transmitted first).

(b) Assume there are no errors in the transmitted waveform, state whether even or odd parity is being used.

(c) Assume two of the bits received in the character are erroneous; can the receiver detect the error? Can you extend the example to determine the limitations of parity checking?

(d) If 7-bit ASCII characters are transmitted continuously in the format shown (with no idle periods between the frames) at a baud rate of 9600, calculate the following:

i. The value of **T** in **Fig 2**.

ii. The data transfer rate of this serial interface in characters per second (cps).

(e) Re-compute the data transfer rate (cps) if the transmission does not use any parity bit. Compare the results with those obtained in Q3d(ii), and state your observation(s).

(f) Assume the baud rate of the transmitter is 4800, but the baud rate of the receiver is configured as 9600. Based on **Fig. 2**, determine, if any, the ASCII character(s) that will be received.

Integrity of data packet cannot be determined and which signal option to choose depends on signal line condition between transmitter and receiver

c) no the receiver cannot detect the error. If two '1' bits are wrong, two '0' bits or one '1' and one '0' bit are wrong, then the number of '1' bits is still even. Parity checking only works when only one bit is wrong.

start bit is also duplicated

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(Not necessary to be covered during tutorial)

3) There has been a trend of 'serialization' of interface bus standard. E.g. USB replacing Parallel Port Interface, SATA replacing IDE in HDD.
   (a) What are the advantages that Serial Bus has over Parallel Bus interface that enticed industry player to move in this direction?
   (b) What are the scenarios in which Parallel bus will still be preferred over Serial bus? What are the design considerations that need to be put in place in such cases?

4) In Q3(f) above, a wrong sampling result is observed when a wrong baud rate is used. This can actually be used to implement auto baud rate detection. Briefly describe how this can be done.

3a) Serial bus has less data lines than parallel bus
-less issue with signal skew and less chance of being influenced by crosstalk
-less bulky so easier to route PCB trace and cabling
-good design and testing conditions allow serial data transfer to reach high speeds

3b) Parallel bus is still used when sustained high speed is needed. Designing high speeds parallel buses require deep knowledge of electrical circuit behaviour to reduce signal skew and crosstalk. Length of parallel bus is very short while considering shielding and grounding.

A carriage return has the ASCII value of 0x0D and would be sampled as different value with different baud rate assumption. If the recieving device knows that the transmitting device sends 0x0D then it will be able to derive the baud rate based on the value sampled.