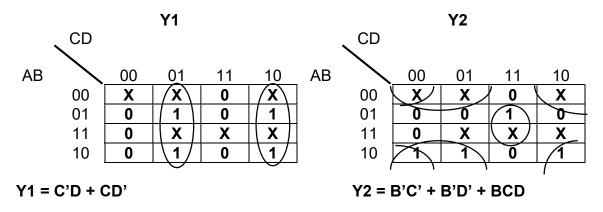
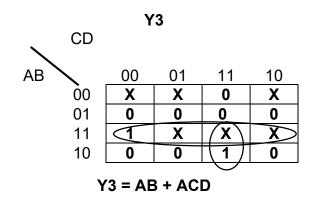
L8 Practice answers:

1. Excess-3 to BCD converter

	Excess-3 input				BCD output			
Decimal	Α	В	С	D	Y3	Y2	Y1	Y0
invalid	0	0	0	0	X	X	X	X
invalid	0	0	0	1	Х	Х	Х	X
invalid	0	0	1	0	X	Х	X	X
0	0	0	1	1	0	0	0	0
1	0	1	0	0	0	0	0	1
2	0	1	0	1	0	0	1	0
3	0	1	1	0	0	0	1	1
4	0	1	1	1	0	1	0	0
5	1	0	0	0	0	1	0	1
6	1	0	0	1	0	1	1	0
7	1	0	1	0	0	1	1	1
8	1	0	1	1	1	0	0	0
9	1	1	0	0	1	0	0	1
invalid	1	1	0	1	Х	Х	Х	Х
invalid	1	1	1	0	X	X	X	X
invalid	1	1	1	1	X	X	X	Х

By observation, **Y0 = D'**

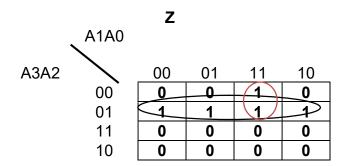




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2.

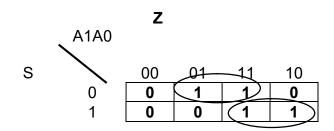
Z	A0	A 1	A2	A3
0	0	0	0	0
0	1	0	0	0
0	0	1	0	0
1	1	1	0	0
1	0	0	1	0
1	1	0	1	0
1	0	1	1	0
1	1	1	1	0
0	0	0	0	1
0	1	0	0	1
0	0	1	0	1
0	1	1	0	1
0	0	0	1	1
0	1	0	1	1
0	0	1	1	1
0	1	1	1	1



Z = A3' A2 + A3' A1 A0

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3.



$$Z = S' \bullet A0 + S \bullet A1$$

4. From Q3,

$$Z = S' \bullet A0 + S \bullet A1$$

An enable input EN can be added to the circuit using an AND gate:

Modified_Z =
$$EN \bullet (S' \bullet A0 + S \bullet A1)$$

$$if (EN = 0)$$
 $Modified_Z = 0$

else

 $Modified_Z$ behaves the same as $Original_Z$ in Q3

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