RTL8197F

Integrated 802.11bgn 2.4GHz Router WiSoC

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document provides detailed user guidelines to achieve the best performance when implementing the Realtek 11ac AP/Routers.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	20150814	Initial draft
0.2	20150820	Add I2C part for DR-QFN128 type 1 (5 port Ethernet)
0.3	20150831	1.) Pin: RSET rename to Pin: VDD_REF_EPHY 2.) rename SPS related pin name
0.4	20150909	1.) Add TF-BGA268 2.) bug fixed
0.5	20151113	Bug fixed for FS/FN pin22/23 inverse Correct: PIN 22: AVDD1P05_RTX_S0 PIN 23: AVDD1P05_RTX_S1
0.6	20151126	1.) Remove all mark: "Type1" and "Type2" 2.) Add 8197FB Mechanical Dimension
0.7	20151127	1.) Modify SPI description (separate SPI-Nor and General SPI) 2.) Modify SPI-Nor flash support MAX size 3.) Modify figure 1 8197F block diagram (including SPI/ SPI-Nor/ Switch)
0.8	20151210	1.) Bug fixed for 8197F mechanical Dimension (DR-QFN128)

Revision	Release Date	Summary
0.9	20151228	1.) Add New Chapter: MISC Control - GPIO part - Interrupt part 2.) Remove the min/max value in “Power Supply DC Characteristics”
1.0	20160105	1.) Add Switch Chapter 2.) Add Comparison between packages 3.) Add Register & DRAM Address Summary 4.) Bug fixed for AVDD1P05_DDRPLL pin attribute (add NC mode)
1.1	20160201	1.) Add Timer & Watchdog chapter 2.) Add APB Timer & PWM & Event chapter 3.) Delete Marked description 4.) Add Pin-Mux Register Control Chapter
1.2	20160321	1.) Bug fixed for DRAM Map Graph 2.) Add description for DRAM Max Size Support
1.3	20160427	1.) Add I2S chapter 2.) Add PCM chapter
1.4	20160511	1.) Add Thermal Chapter 2.) Add Crystal Clock Timing
1.5	20160517	1.) Add SPI interface Pin-Mux 2.) Add SPI-Nand Flash Pin-mux 3.) Add Table: Difference between Packages 4.) Add Figure: WiFi Function Difference between Packages
1.6	20160621	1.) To Complete the data in Chapter: Power Supply DC Characteristics
1.7	20160623	1.) Remove Chapter: Power State and Power Consumptions (Provided by another doc) 2.) Correct 97FB DDR IO number from 53 to 49 3.) Correct 97FB 10/100 Ethernet IO number from 16 to 20 4.) Add new feature: 8197FN package support RGMII (Use GPIO pin to simulate MDC/MDIO dedicated pin) 5.) RF 4 Power pin for 1.05V: separate two mode, dedicated LDO or not 6.) Add Chapter: Electrical Specifications - DDR
1.8	20160627	1.) To complete Chapter: Electrical Specifications – Digital IO Pin 2.) Add Chapter: Digital IO Pin Attribute (Not Share Pin)
1.9	20160628	1.) Add Chapter: Electrical Specification – RGMII 2.) Add part number in Chapter: Ordering information
2.0	20160701	1.) Add GPIO support direction @ - Chapter: Shared I/O Pin Mapping - Chapter: GPIO Pin During Boot State
2.1	20160712	1.) Update Chapter: DRAM Max Size Support 2.) Add PCM interface into Pin-Mux
2.2	20160805	1.) Add description for Pin: ENSWR 2.) Rename Symbol “Input leakage Current” from IIL to II 3.) Add Chapter 4.4: Scenario Suggestion for different Part Number

Revision	Release Date	Summary
2.3	20160908	1.) Chapter 16: Ordering Information -Add New Part Number – 8197FH 2.) Add 8197FH information into datasheet 3.) Update Chapter13.1.1: Crystal Clock Timing 4.) Update WiFi STA Proxy count from 38 to 39 5.) Update 8197FB new pin assignment & corresponding pin number (Ground & RF power location) 6.) Revise figure: Pin Support between Part Number - SPI_Nand from 5 to (4 + 1*GPIO)
2.4	20161021	1.) Chapter 5.1 (8197FN) / 5.2 (8197FH) / 5.3 (8197FS) - IC Mark rotation to match ASIC
2.5	20161102	Add new chapter: Security Engine
2.6	20161107	Add new Part Number and modify corresponding chapter: 1.) RTL8197FNT-VEx-CG 2.) RTL8197FS-VSx-CG
2.7	20161109	1.) Revise chapter: Power Supply DC Characteristics -Add description for AVDD1P05_DDRPLL 2.) Add booting mode -SD booting -Switch booting (Image to DRAM) -Switch booting (Image to SPI-Nor Flash)
2.8	20161116	1.) Revise Chapter: Temperature Limit Ratings -Max Ambient Temperature from 55 to 70
2.9	20161205	1.) Bug fixed for 8197F mechanical Dimension (DR-QFN128) (D2/E2, eR) 2.) Revise chapter: Scenario – RTL8197FS-VEx-CG -Add VOIP Scenario
3.0	20161209	1.) Bug fixed: 8197FNT DMIPS from 1600 to 960 (600MHz) 2.) Add more description for Mechanism dimension (DR-QFN128 part) - REF / BSC TOLERANCE
3.1	20161219	1.) Add Parallel-Nand Flash Pin-mux (97FS/97FB)
3.2	20170106	Update the latest thermal data

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1. General Description

The RTL8197F is ultra-high competitive product with high performance, low power and many connectivity interfaces. Integrated with RTK famous 2x2 11bgn WiFi IP and 5 port 10/100 Switch. It also includes popular MIPS 24Kc CPU Core and clock can reach to 1GHz. And a variety of interfaces support can satisfy your product requirement.

2. Features

- Package
  - DR-QFN128 (MCM, DDR2 memory) 10x10mm^2
    - RTL8197FNT-VEx-CG : 5 port switch with 5 FE PHY (No PCIe)
    - RTL8197FN-VEx-CG : 5 port switch with 5 FE PHY
    - RTL8197FH-VEx-CG : 5 port switch with 5 FE PHY or (1 RGMII + 4 FE PHY)
    - RTL8197FS-VEx-CG : 2 port switch with 1 FE PHY and 1 RGMII
    - RTL8197FS-VSx-CG : 2 port switch with 1 FE PHY and 1 RGMII (supporting Security booting)
  - TF-BGA268 12x12mm^2
    - RTL8197FB-CG : 5 port switch with 5 FE PHY or (1 RGMII + 4 FE PHY)
- CPU
  - 24Kc
  - Up to 1000MHz
  - I-Cache 64KB / D-Cache 32KB
- Memory
  - 96KB ROM and 16KB SRAM (Secure ROM supported by RTL8197FS-VSx-CG)
  - Up to 16 bit DDR1-500 128MB / DDR2-1066 512MB
  - SPI Nor Flash, up to 128MB (64MB x 2)
  - Support SPI-Nand (4Gbit)
  - Support Parallel-Nand (8GB)
- WIFI
  - 2.4G 2x2 b/g/n Solution
  - TxBF/STBC/LDPC-Tx/MRC support
- Engine

- Security Engine
- GDMA 4 Channel

- Peripheral
  - 2 USB Interface
    - One EHCI
    - OTG (support device or host)
  - 1 PCIe Interface
    - One Host RC Gen1
  - 1 R/G/MII Interface
  - 1 SDXC/eMMC Interface
    - SDXC 3.0, eMMC 4.5
  - 2 SPI Interface
    - Two(SPI0/SPI1) for Master/Slave mode with DMA Engine (SPI0 supporting one of Master and Slave modes, and SPI1 supporting Master mode only)
  - 3 UART Interface
    - One Console UART
    - Two HS-UART with DMA Engine
  - 2 I2C Interface
    - two with DMA Engine + Master/Slave Mode
      - 100Kbps / 400Kbps / 3.4Mbps
  - 1 I2S Interface
    - Support Master Mode
    - Support 16/24/32 bit
      - Support 8/16/32/48/64/96/192/384KHz, 44.1/88.2/176.4 KHz
  - 1 PCM Interface
    - Support Master Mode
    - Support 8KHz, 16 bit
  - Gtimer/PWM IP
    - 8 generic timers

- **4 PWMs**
- **4 Timer Events**

3. System Applications

- N300 - 802.11b/g/n AP Router
- AC750/AC1200FE - Dual-band Concurrent AP Router
- IoT Gateway
- Wireless Repeater
- IPCam
- NAS - Network-Attached Storage
- VOIP

■

3.1. N300 - 802.11b/g/n AP Router

3.2. AC750/AC1200FE - Dual-band Concurrent AP Router

3.3. IOT Gateway

3.4. Wireless Repeater

3.5. IPCAM

3.6. NAS - Network-Attached Storage

3.7. VOIP

4. Block Diagram

The system control of the RTL8197F can be divided into four main parts:

1.) CPU / Bus Platform / Memory Controller
2.) packet forwarding Switch Core
3.) 2x2 11bgn embedded WiFi
4.) other peripheral interfaces

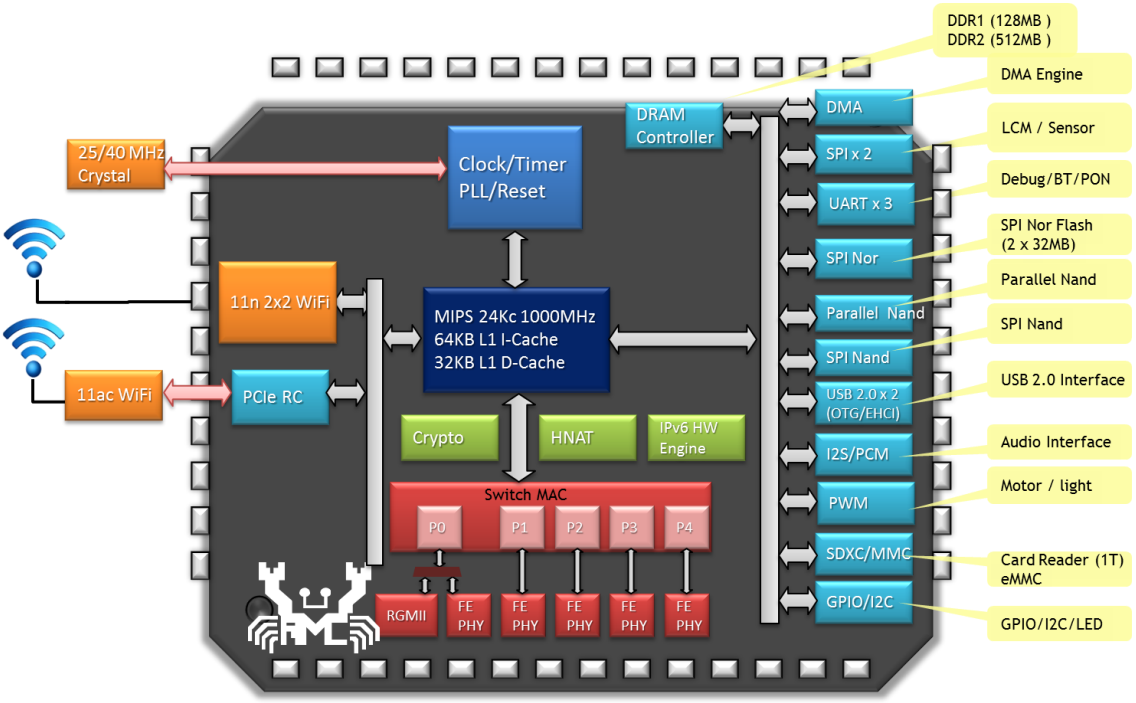


Figure 1. RTL8197F Block Diagram

4.1. RTL8197FNT-VEx-CG

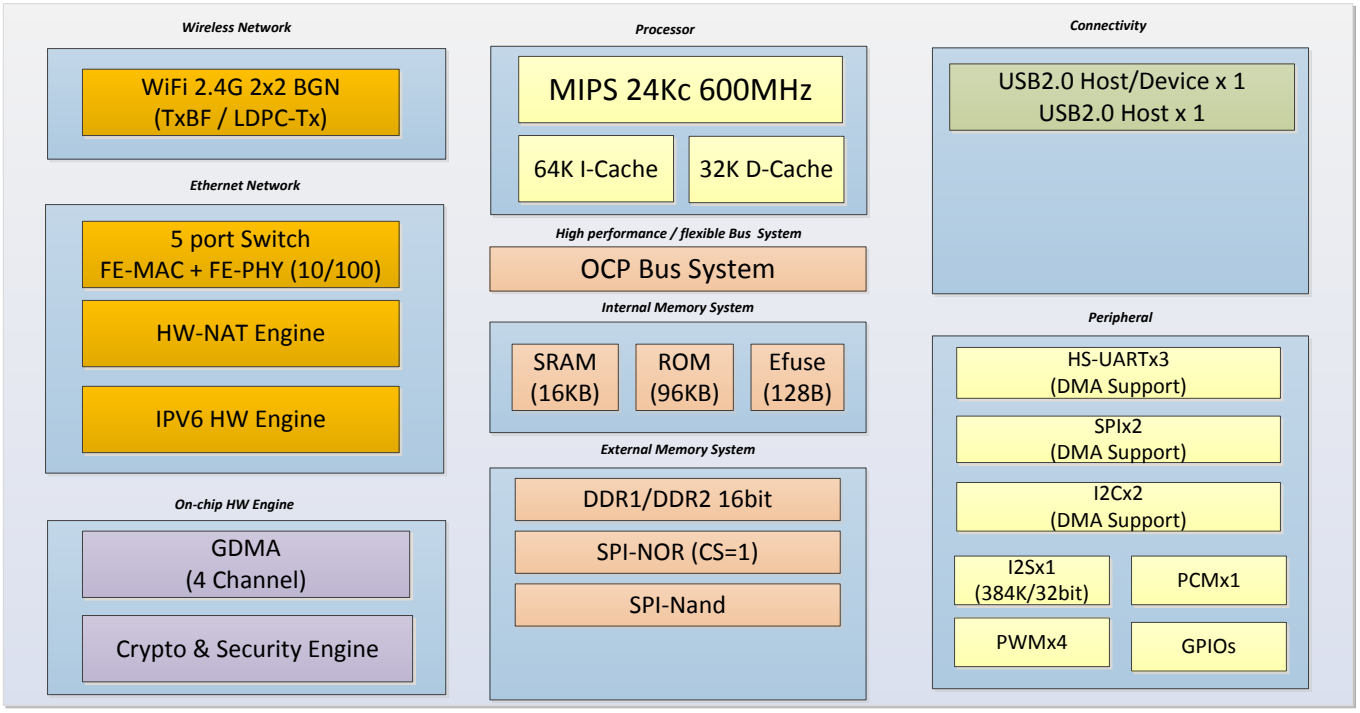


Figure 2. RTL8197FNT-VEx-CG Block Diagram

4.2. RTL8197FN-VEx-CG

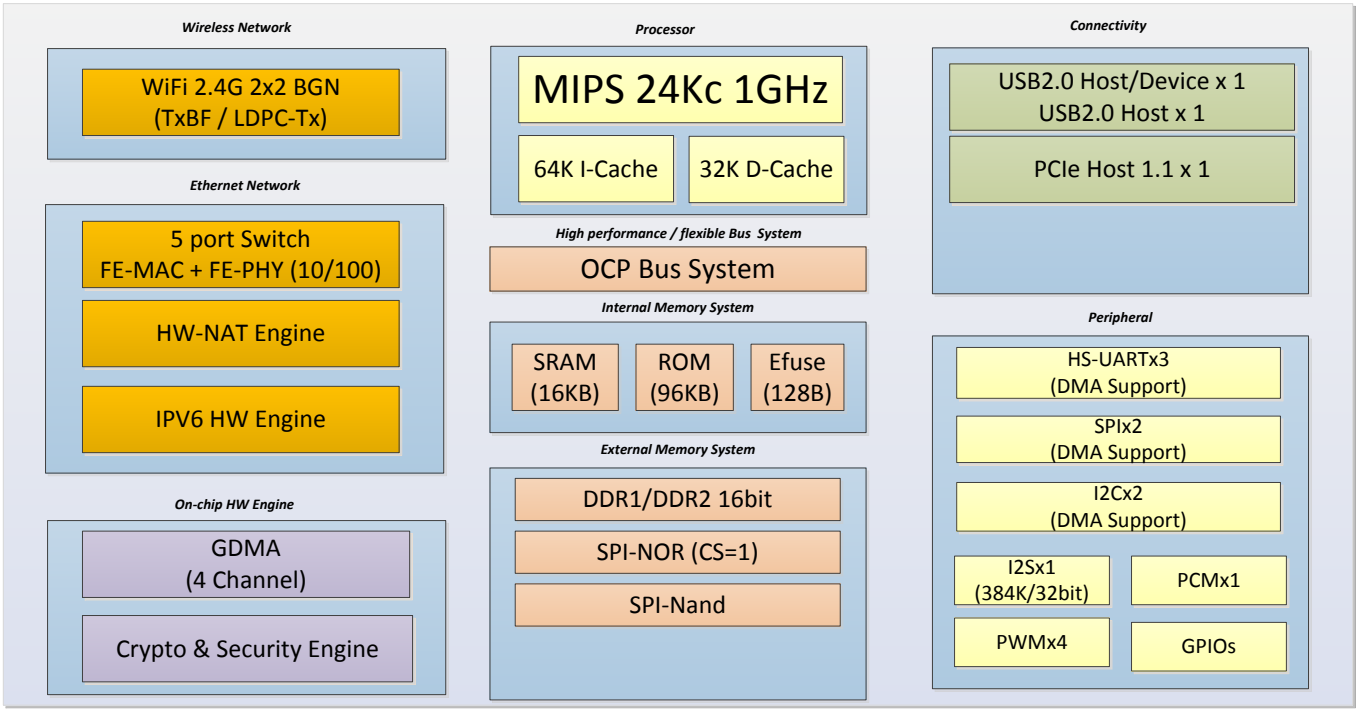


Figure 3. RTL8197FN-VEx-CG Block Diagram

4.3. RTL8197FH-VEx-CG

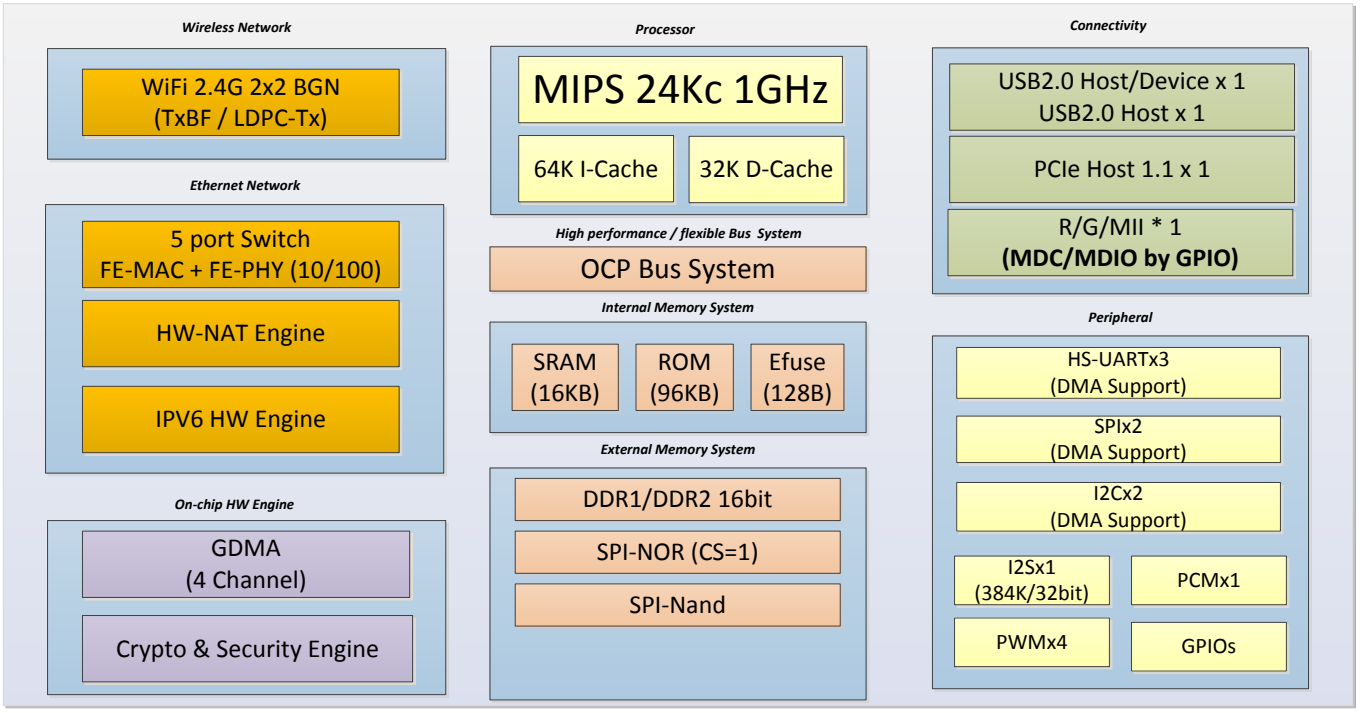


Figure 4. RTL8197FH-VEx-CG Block Diagram

4.4. RTL8197FS-VEx-CG

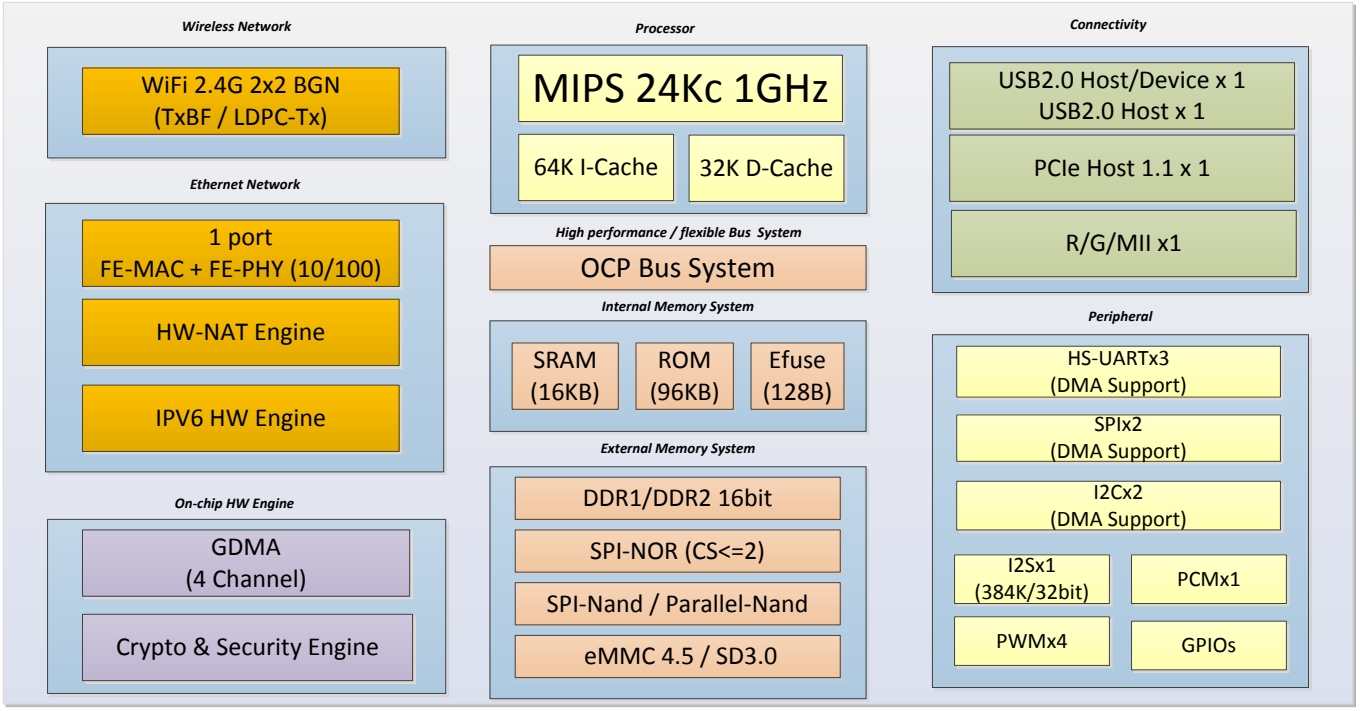


Figure 5. RTL8197FS-VEx-CG Block Diagram

4.5. RTL8197FS-VSx-CG

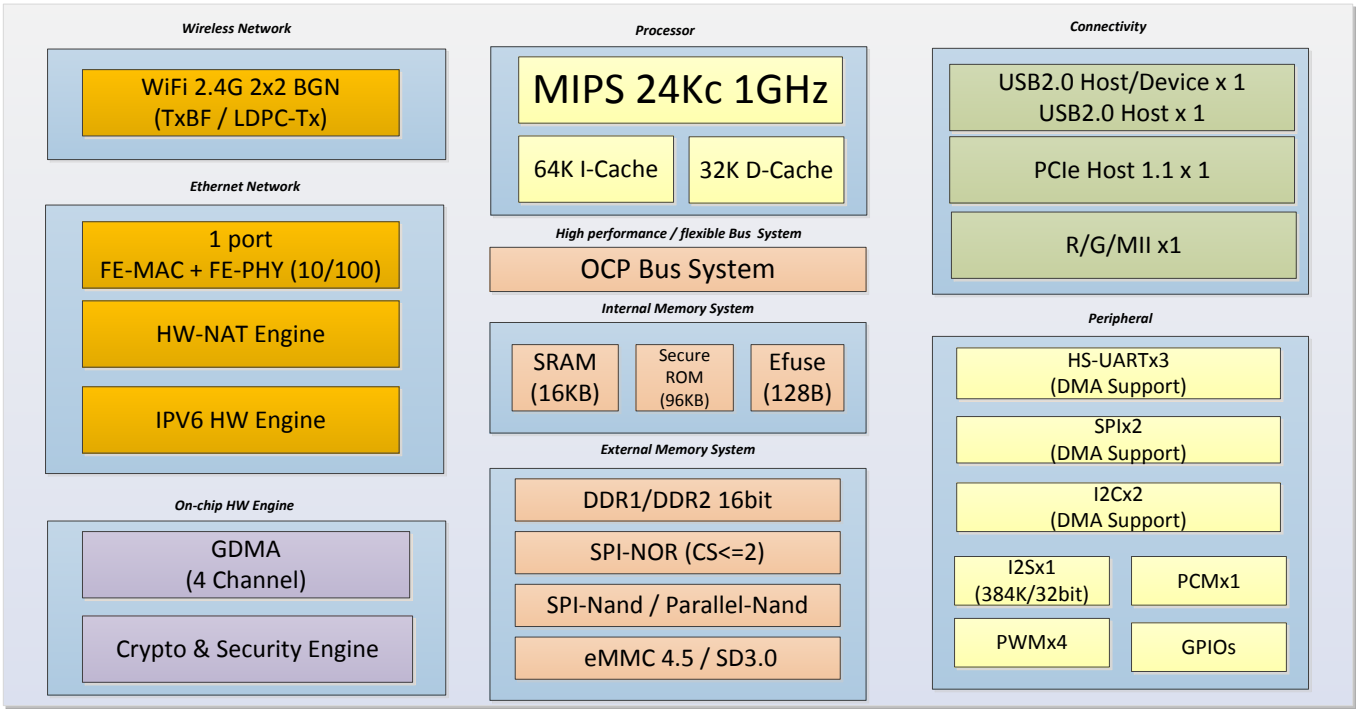


Figure 6. RTL8197FS-VSx-CG Block Diagram

4.6. RTL8197FB-CG

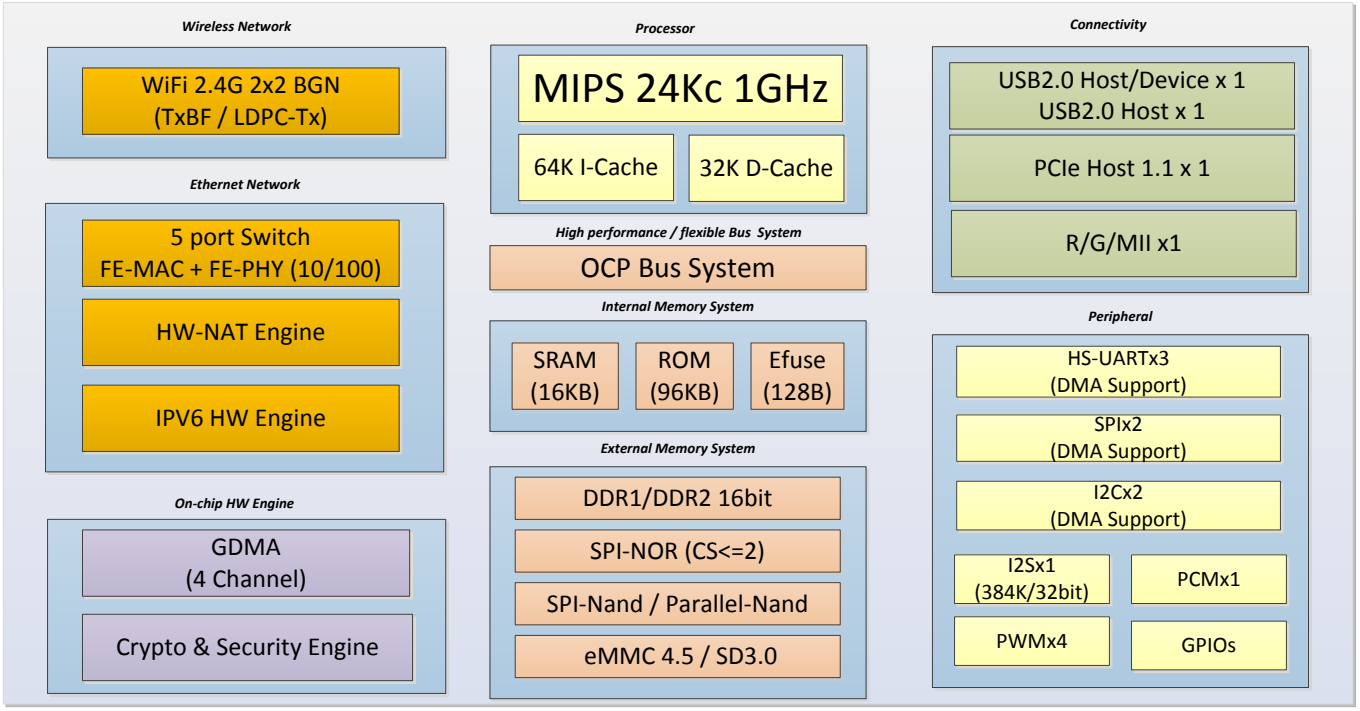


Figure 7. RTL8197FB-CG Block Diagram

4.7. Scenario Suggestion for different Part Number

4.7.1. Scenario – RTL8197FNT-VEx-CG

Table 1. Scenario – RTL8197FNT-VEx-CG

		Realtek	Realtek
		Internal Function	8197FNT-VEx-CG
SoC	IC	RTL8197F	RTL8197FNT-VEx-CG (Router Mode)
	Scenario	-	N300-FE
	Package	-	DR-QFN128 (10x10)
	Host CPU	MIPS 24Kc	MIPS 24Kc
	Clock	1000MHz	600MHz
	I/D Cache	64KB / 32KB	64KB / 32KB
	IMEM, DMEM	-	-
	L2 Cache	-	-
	RAM i/f	DDR1: 500/128MB DDR2: 1066/512MB	DDR2 Embedded (Size TBD)
	NAND Flash	SPI (4Gbit) /Parallel	SPI (share w/ SPI-Nor)
	eMMC	4/8 bits	-
	SD Card	SDXC	-
	WiFi TRX	2x2 11bgn	2x2 11bgn
	WiFi STA Proxy	39	39
	WiFi K-free	Yes	Yes

	WiFi FEM integration	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)
	ePA / eLNA	Yes	Yes
	DPD	Yes	Yes
	Internal Balun	External	External
	PCI-e	Host (gen1.0*1)	**No**
	USB	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)
	Switch	5 Port (10/100)	5 Port (10/100)
	Ethernet i/f	RGMII x 1	-
	HNAT	Yes	Yes
	SPI-Nor	2 x 64MB	1 x 64MB (share with SPI NAND)
	SPI	1 x Master/Slave + 1 x Master	1 x Master (share w/ I2S)
	I2C	2	1
	UART(Lite)	1	1
	UART(Full)	2	-
	PCM / SLIC	1	-
	I2S	384K, 32b	384K, 32b (share with SPI)
	PWM	4	-
	GPIO	Depend on Package	6 / 5
	Crypto Engine	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT
	iNIC	Yes	Yes
	Xtal input	25/40 MHz	25/40 MHz
	Xtal output	12 MHz	12 MHz
Digital Pin (excluding DRAM)		Depend on Package	**33**
OS		eCos / Linux / OpenWRT	eCos / Linux / OpenWRT
DMIPS		1600	960

Digital Pin List (excluding DRAM)		WiFi: 7 PCIe: 0 SPI-Nor: 5 SPI Master: 4 I2C: 2 Uart-Lite: 2 Uart-Full: 0 I2S: 0 Switch_LED: 5 GPIO: 7 XTAL out: 1
WiFi		7
PCIe		0
SPI-Nor		5
SPI-Master		4
I2C		2
Uart-Lite		2
Uart-Full		
I2S		
Switch_LED		5
GPIO		7
XTAL_out		1
PCM		
PWM		
SDXC		
Parallel Nand		
RGMII		
eMMC		
SPI Slave		
Digital Pin SUM (excluding DRAM)		33

4.7.2. Scenario – RTL8197FN-VEx-CG

Table 2. Scenario – RTL8197FN-VEx-CG

		Realtek	Realtek
		Internal Function	8197FN-VEx-CG
SoC	IC	RTL8197F	RTL8197FN-VEx-CG (Router Mode)
	Scenario	-	N300-FE / AC750-FE / AC1200-FE
	Package	-	DR-QFN128 (10x10)
	Host CPU	MIPS 24Kc	MIPS 24Kc
	Clock	1000MHz	1000MHz
	I/D Cache	64KB / 32KB	64KB / 32KB
	IMEM, DMEM	-	-
	L2 Cache	-	-
	RAM i/f	DDR1: 500/128MB DDR2: 1066/512MB	DDR2 embedded (Size TBD)
	NAND Flash	SPI (4Gbit) /Parallel	SPI (share w/ SPI-Nor)
	eMMC	4/8 bits	-
	SD Card	SDXC	-
	WiFi TRX	2x2 11bgn	2x2 11bgn
	WiFi STA Proxy	39	39
	WiFi K-free	Yes	Yes
	WiFi FEM integration	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)
	ePA / eLNA	Yes	Yes
	DPD	Yes	Yes

	Internal Balun	External	External
	PCI-e	Host (gen1.0*1)	Host (gen1.0*1)
	USB	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)
	Switch	5 Port (10/100)	5 Port (10/100)
	Ethernet i/f	RGMII x 1	-
	HNAT	Yes	Yes
	SPI-Nor	2 x 64MB	1 x 64MB (share with SPI NAND)
	SPI	1 x Master/Slave + 1 x Master	1 x Master (share w/ I2S)
	I2C	2	1
	UART(Lite)	1	1
	UART(Full)	2	-
	PCM / SLIC	1	-
	I2S	384K, 32b	384K, 32b (Share with SPI)
	PWM	4	-
	GPIO	Depend on Package	6 / 5
	Crypto Engine	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT
	iNIC	Yes	Yes
	Xtal input	25/40 MHz	25/40 MHz
	Xtal output	12 MHz	12 MHz
Digital Pin (excluding DRAM)		Depend on Package	**33**
OS		eCos / Linux / OpenWRT	eCos / Linux / OpenWRT
DMIPS		1600	1600

Digital Pin List (excluding DRAM)		WiFi: 7 PCIe: 1 SPI-Nor: 5 SPI Master: 4 I2C: 2 Uart-Lite: 2 Uart-Full: 0 I2S: 0 Switch_LED: 5 GPIO: 6 XTAL out: 1
WiFi		7
PCIe		1
SPI-Nor		5
SPI-Master		4
I2C		2
Uart-Lite		2
Uart-Full		
I2S		
Switch_LED		5
GPIO		6
XTAL_out		1
PCM		
PWM		
SDXC		
Parallel Nand		
RGMII		
eMMC		
SPI Slave		
Digital Pin SUM (excluding DRAM)		33

4.7.3. Scenario – RTL8197FH-VEx-CG

Table 3. Scenario – RTL8197FH-VEx-CG

		Realtek	Realtek
		Internal Function	8197FH-VEx-CG
SoC	IC	RTL8197F	RTL8197FH-VEx-CG (Router Mode)
	Scenario	-	AC750-GE / AC1200-GE (1 Giga WAN + 4 10/100 LAN)
	Package	-	DR-QFN128 (10x10)
	Host CPU	MIPS 24Kc	MIPS 24Kc
	Clock	1000MHz	1000MHz
	I/D Cache	64KB / 32KB	64KB / 32KB
	IMEM, DMEM	-	-
	L2 Cache	-	-
	RAM i/f	DDR1: 500/128MB DDR2: 1066/512MB	DDR2 embedded (Size TBD)
	NAND Flash	SPI (4Gbit) /Parallel	SPI (share w/ SPI-Nor)
	eMMC	4/8 bits	-
	SD Card	SDXC	-
	WiFi TRX	2x2 11bgn	2x2 11bgn
	WiFi STA Proxy	39	39
	WiFi K-free	Yes	Yes
	WiFi FEM integration	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)
	ePA / eLNA	Yes	**No**
	DPD	Yes	Yes
	Internal Balun	External	External

	PCI-e	Host (gen1.0*1)	Host (gen1.0*1)
	USB	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)
	Switch	5 Port (10/100)	4 Port (10/100)
	Ethernet i/f	RGMII x 1	RGMII (1) (MDC/MDIO by GPIO)
	HNAT	Yes	Yes
	SPI-Nor	2 x 64MB	1 x 64MB (share with SPI NAND)
	SPI	1 x Master/Slave + 1 x Master	-
	I2C	2	-
	UART(Lite)	1	1
	UART(Full)	2	-
	PCM / SLIC	1	-
	I2S	384K, 32b	-
	PWM	4	-
	GPIO	Depend on Package	0
	Crypto Engine	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT
	iNIC	Yes	Yes
	Xtal input	25/40 MHz	25/40 MHz
	Xtal output	12 MHz	-
Digital Pin (excluding DRAM)		Depend on Package	**33**
OS		eCos / Linux / OpenWRT	eCos / Linux / OpenWRT
DMIPS		1600	1600

Digital Pin List (excluding DRAM)		WiFi: 1 PCIe: 1 SPI-Nor: 5 SPI Master: 0 I2C: 0 Uart-Lite: 2 Uart-Full: 0 I2S: 0 Switch_LED: 4 GPIO: 6 XTAL out: 0 PCM: 0 PWM: 0 SDXC: 0 RGMII: 14
WiFi		1
PCIe		1
SPI-Nor		5
SPI-Master		0
I2C		0
Uart-Lite		2
Uart-Full		
I2S		
Switch_LED		4
GPIO		6
XTAL_out		0
PCM		
PWM		
SDXC		
Parallel Nand		
RGMII		14
eMMC		
SPI Slave		
Digital Pin SUM (excluding DRAM)		33

4.7.4. Scenario – RTL8197FS-VEx-CG

Table 4. Scenario – RTL8197FS-VEx-CG

		Realtek	Realtek	Realtek	Realtek
		Internal Function	97FS-1	97FS-2	97FS-3
SoC	IC	RTL8197F	RTL8197FS-VEx-CG (Router Mode)	RTL8197FS-VEx-CG (Router Mode w/ SD)	RTL8197FS-VEx-CG (IoT/Repeater Mode)
	Scenario	-	AC750-GE / AC1200-GE (5 Port Giga)	AC750-GE / AC1200-GE / VOIP (5 Port Giga)	Repeater / IoT
	Package	-	DR-QFN128 (10x10)	DR-QFN128 (10x10)	DR-QFN128 (10x10)
	Host CPU	MIPS 24Kc	MIPS 24Kc	MIPS 24Kc	MIPS 24Kc
	Clock	1000MHz	1000MHz	1000MHz	1000MHz
	I/D Cache	64KB / 32KB	64KB / 32KB	64KB / 32KB	64KB / 32KB
	IMEM, DMEM	-	-	-	-
	L2 Cache	-	-	-	-
	RAM i/f	DDR1: 500/128MB DDR2: 1066/512MB	DDR2 embedded (Size TBD)	DDR2 embedded (Size TBD)	DDR2 embedded (Size TBD)
	NAND Flash	SPI (4Gbit) /Parallel	SPI (share w/ SPI-Nor)	SPI (share w/ SPI-Nor)	SPI (share w/ SPI-Nor)
	eMMC	4/8 bits	-	4 bit (share w/ SDXC)	4 bit (share w/ SDXC)
	SD Card	SDXC	-	SDXC (share with eMMC)	SDXC (share with eMMC)
	WiFi TRX	2x2 n	2x2 11bgn	2x2 11bgn	2x2 11bgn
	WiFi STA Proxy	39	39	39	39
	WiFi K-free	Yes	Yes	Yes	Yes
	WiFi FEM integration	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)

	ePA / eLNA	Yes	Yes	Yes	Yes
	DPD	Yes	Yes	Yes	Yes
	Internal Balun	External	External	External	External
	PCI-e	Host (gen1.0*1)	Host (gen1.0*1)	Host (gen1.0*1)	Host (gen1.0*1)
	USB	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)
	Switch	5 Port (10/100)	1 Port (10/100)	1 Port (10/100)	1 Port (10/100)
	Ethernet i/f	RGMII x 1	RGMII	RGMII	-
	HNAT	Yes	Yes	Yes	Yes
	SPI-Nor	2 x 64MB	2 x 64MB (share with SPI-NAND)	2 x 64MB (share with SPI-NAND)	2 x 64MB (share with SPI-NAND)
	SPI	1 x Master/Slave + 1 x Master	1 x Master	-	1 x Master/Slave
	I2C	2	1	-	1
	UART(Lite)	1	1	1	1
	UART(Full)	2	-	-	1
	PCM / SLIC	1	-	1	-
	I2S	384K, 32b	384K, 32b	-	384K, 32b
	PWM	4	-	-	2
	GPIO	Depend on Package	5	3	3
	Crypto Engine	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT
	iNIC	Yes	Yes	Yes	Yes
	Xtal input	25/40 MHz	25/40 MHz	25/40 MHz	25/40 MHz
	Xtal output	12 MHz	-	-	12 MHz
Digital Pin (excluding DRAM)		-	**47**	**47**	**47**
OS		eCos / Linux / OpenWRT	eCos / Linux / OpenWRT	eCos / Linux / OpenWRT	eCos / Linux / OpenWRT
DMIPS		1600	1600	1600	1600

		WiFi: 7 PCIe: 1 SPI-Nor: 6 SPI Master: 4 I2C: 2 Uart-Lite: 2 Uart-Full: 0 I2S: 5 Switch_LED: 1 GPIO: 5 XTAL out: 0 PCM: 0 PWM: 0 SDXC: 0 RGMII: 14	WiFi: 7 PCIe: 1 SPI-Nor: 6 SPI Master: 0 I2C: 0 Uart-Lite: 2 Uart-Full: 0 I2S: 0 Switch_LED: 1 GPIO: 3 XTAL out: 0 PCM: 4 PWM: 0 SDXC: 9 RGMII: 14	WiFi: 7 PCIe: 1 SPI-Nor: 6 SPI Master: 4 I2C: 2 Uart-Lite: 2 Uart-Full: 4 I2S: 5 Switch_LED: 1 GPIO: 3 XTAL out: 1 PCM: 0 PWM: 2 SDXC: 9
Digital Pin List (excluding DRAM)				
WiFi		7	7	7
PCIe		1	1	1
SPI-Nor		6	6	6
SPI-Master		4	0	4
I2C		2	0	2
Uart-Lite		2	2	2
Uart-Full		0	0	4
I2S		5	0	5
Switch_LED		1	1	1
GPIO		5	3	3
XTAL_out		0	0	1
PCM			4	
PWM			0	2
SDXC			9	9
Parallel Nand				
RGMII		14	14	
eMMC				
SPI Slave				
Digital Pin SUM (excluding		47	47	47

DRAM)				

4.7.5. Scenario – RTL8197FS-VSx-CG

Table 5. Scenario – RTL8197FS-VSx-CG

		Realtek	Realtek
		Internal Function	97FS-VSx-CG
SoC	IC	RTL8197F	RTL8197FS-VSx-CG (Secure Boot / IoT Mode)
	Scenario	-	Secure Boot / IoT
	Package	-	DR-QFN128 (10x10)
	Host CPU	MIPS 24Kc	MIPS 24Kc
	Clock	1000MHz	1000MHz
	I/D Cache	64KB / 32KB	64KB / 32KB
	IMEM, DMEM	-	-
	L2 Cache	-	-
	RAM i/f	DDR1: 500/128MB DDR2: 1066/512MB	DDR2 embedded (Size TBD)
	NAND Flash	SPI (4Gbit) /Parallel	SPI (share w/ SPI-Nor)
	eMMC	4/8 bits	4 bit (share w/ SDXC)
	SD Card	SDXC	SDXC (share with eMMC)
	WiFi TRX	2x2 11bgn	2x2 11bgn
	WiFi STA Proxy	39	39
	WiFi K-free	Yes	Yes
	WiFi FEM integration	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)
	ePA / eLNA	Yes	Yes
	DPD	Yes	Yes

	Internal Balun	External	External
	PCI-e	Host (gen1.0*1)	Host (gen1.0*1)
	USB	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)
	Switch	5 Port (10/100)	1 Port (10/100)
	Ethernet i/f	RGMII x 1	-
	HNAT	Yes	Yes
	SPI-Nor	2 x 64MB	2 x 64MB (share with SPI NAND)
	SPI	1 x Master/Slave + 1 Master	1 x Master/Slave
	I2C	2	1
	UART(Lite)	1	1
	UART(Full)	2	1
	PCM / SLIC	1	-
	I2S	384K, 32b	384K, 32b
	PWM	4	2
	GPIO	Depend on Package	3
	Crypto Engine	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT
	iNIC	Yes	Yes
	Xtal input	25/40 MHz	25/40 MHz
	Xtal output	12 MHz	12 MHz
Digital Pin (excluding DRAM)		-	**47**
OS		eCos / Linux / OpenWRT	eCos / Linux / OpenWRT
DMIPS		1600	1600

WiFi: 7
PCIe: 1
SPI-Nor: 6
SPI Master: 4
I2C: 2
Uart-Lite: 2
Uart-Full: 4
I2S: 5
Switch_LED: 1
GPIO: 3
XTAL out: 1
PCM: 0
PWM: 2
SDXC: 9

Digital Pin List
(excluding DRAM)

WiFi		7
PCIe		1
SPI-Nor		6
SPI-Master		4
I2C		2
Uart-Lite		2
Uart-Full		4
I2S		5
Switch_LED		1
GPIO		3
XTAL_out		1
PCM		
PWM		2
SDXC		9
Parallel Nand		
RGMII		
eMMC		
SPI Slave		
Digital Pin SUM (excluding DRAM)		47

4.7.6. Scenario – RTL8197FB-CG

Table 6. Scenario – RTL8197FB-CG

		Realtek	Realtek	Realtek	Realtek	Realtek	Realtek
			97FB-1	97FB-2	97FB-3	97FB-4	97FB-5
SoC	IC	RTL8197F	RTL8197FB-CG (Router Mode)	RTL8197FB-CG (Router Mode)	RTL8197FB-CG (Router Mode)	RTL8197FB-CG (IPCAM Mode)	RTL8197FB-CG (Smart Router Mode)
	Scenario	-	N300-FE / AC750-FE / AC1200-FE (SPI-Nor)	N300-FE / AC750-FE / AC1200-FE (Parallel-Nand)	AC750-GE / AC1200-GE	IPCAM	Smart Router (AC1200-FE) (touch Panel, BT, NFC)
	Package	-	TF-BGA268 (12x12)	TF-BGA268 (12x12)	TF-BGA268 (12x12)	TF-BGA268 (12x12)	TF-BGA268 (12x12)
	Host CPU	MIPS 24Kc	MIPS 24Kc	MIPS 24Kc	MIPS 24Kc	MIPS 24Kc	MIPS 24Kc
	Clock	1000MHz	1000MHz	1000MHz	1000MHz	1000MHz	1000MHz
	I/D Cache	64KB / 32KB	64KB / 32KB	64KB / 32KB	64KB / 32KB	64KB / 32KB	64KB / 32KB
	IMEM, DMEM	-	-	-	-	-	-
	L2 Cache	-	-	-	-	-	-
	RAM i/f	DDR1: 500/128MB DDR2: 1066/512MB	DDR1: 500/128MB DDR2: 1066/512MB	DDR1: 500/128MB DDR2: 1066/512MB	DDR1: 500/128MB DDR2: 1066/512MB	DDR1: 500/128MB DDR2: 1066/512MB	DDR1: 500/128MB DDR2: 1066/512MB
	NAND Flash	SPI (4Gbit) /Parallel	SPI (share w/ SPI-Nor)	Parallel Nand (share with eMMC)	SPI (share w/ SPI-Nor)	SPI (share w/ SPI-Nor)	SPI (share w/ SPI-Nor)
	eMMC	4/8 bits	-	8 bits (share with Parallel Nand)	-	4 bit (share with SDXC) / 8 bit (share with SDXC + SPI-Nor)	-
	SD Card	SDXC	SDXC x (1 / 0)	-	SDXC	SDXC x (1 / 0)	-
	WiFi TRX	2x2 11bgn	2x2 11bgn	2x2 11bgn	2x2 11bgn	2x2 11bgn	2x2 11bgn
	WiFi STA Proxy	39	39	39	39	39	39
	WiFi K-free	Yes	Yes	Yes	Yes	Yes	Yes

	WiFi FEM integration	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)	PA/LNA/TR SW (2.4GHz)
	ePA / eLNA	Yes	Yes	Yes	Yes	Yes	Yes
	DPD	Yes	Yes	Yes	Yes	Yes	Yes
	Internal Balun	External	External	External	External	External	External
	PCI-e	Host (gen1.0*1)	Host (gen1.0*1)	Host (gen1.0*1)	Host (gen1.0*1)	Host (gen1.0*1)	Host (gen1.0*1)
	USB	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)	U2 Host (1) + U2 Host/Device (1)
	Switch	5 Port (10/100)	5 Port (10/100)	5 Port (10/100)	5 Port (10/100)	5 Port (10/100)	5 Port (10/100)
	Ethernet i/f	RGMII x 1	-	-	RGMII (1)	-	-
	HNAT	Yes	Yes	Yes	Yes	Yes	Yes
	SPI-Nor	2 x 64MB	2 x 64MB (share with SPI NAND)	-	2 x 64MB (share with SPI NAND)	2 x 64MB (share with SPI NAND)	2 x 64MB (share with SPI NAND)
	SPI	1 x Master/Slave + 1 x Master	1 x Master/Slave + 1 x Master (share w/ SDXC)	1 x Master	1 x Master	-	1 x Master
	I2C	2	1	1	1	1	2
	UART(Lite)	1	1	1	1	1	1
	UART(Full)	2	1 + 1 (share w/ SDXC)	1 (share /w Parallel Nand)	1	1	1
	PCM / SLIC	1	1	1	-	-	1
	I2S	384K, 32b	384K, 32b	384K, 32b	-	384K, 32b	384K, 32b
	PWM	4	2	4	-	4	-
	GPIO	Depend on Package	7	7	7	18	8
	Crypto Engine	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT	AES128/192/256-ECB/CBC/CNT
	iNIC	Yes	Yes	Yes	Yes	Yes	Yes
	Xtal input	25/40 MHz	25/40 MHz	25/40 MHz	25/40 MHz	25/40 MHz	25/40 MHz
	Xtal output	12 MHz	12 MHz	12 MHz	12MHz	-	12 MHz
Digital Pin (excluding DRAM)		-	**62**	**62**	**62**	**62**	**62**
OS		eCos / Linux / OpenWRT	eCos / Linux / OpenWRT	eCos / Linux / OpenWRT	eCos / Linux / OpenWRT	eCos / Linux / OpenWRT	eCos / Linux / OpenWRT

DMIPS	1600	1600	1600	1600	1600	1600
		WiFi: 11 PCIe: 1 SPI-Nor: 6 SPI Master: 4 I2C: 2 Uart-Lite: 2 Uart-Full: 4 I2S: 5 Switch_LED: 5 GPIO: 6 XTAL out: 1 PCM: 4 PWM: 2 SDXC: 9	WiFi: 11 PCIe: 1 SPI-Nor: 0 SPI Master: 4 I2C: 2 Uart-Lite: 2 Uart-Full: 0 I2S: 5 Switch_LED: 5 GPIO: 7 XTAL out: 1 PCM: 4 PWM: 4 SDXC: 0 Parallel-Nand: 16	WiFi: 11 PCIe: 1 SPI-Nor: 6 SPI Master: 4 I2C: 2 Uart-Lite: 2 Uart-Full: 4 I2S: 0 Switch_LED: 1 GPIO: 7 XTAL out: 1 PCM: 0 PWM: 0 SDXC: 9 RGMII: 14	WiFi: 11 PCIe: 1 SPI-Nor: 5 SPI Master: 0 I2C: 2 Uart-Lite: 2 Uart-Full: 4 I2S: 5 Switch_LED: 1 GPIO: 18 XTAL out: 0 SDXC: 9 PWM: 4	WiFi: 18 PCIe: 1 SPI-Nor: 6 SPI Master: 4 I2C: 4 Uart-Lite: 2 Uart-Full: 4 I2S: 5 Switch_LED: 5 GPIO: 8 XTAL out: 1 PCM: 4 PWM: 0 SDXC: 0

Digital Pin List (excluding DRAM)

WiFi		11	11	11	11	18
PCIe		1	1	1	1	1
SPI-Nor		6		6	5	6
SPI-Master		4	4	4		4
I2C		2	2	2	2	4
Uart-Lite		2	2	2	2	2
Uart-Full		4		4	4	4
I2S		5	5		5	5
Switch_LED		5	5	1	1	5
GPIO		6	7	7	18	8
XTAL_out		1	1	1		1
PCM		4	4			4
PWM		2	4		4	
SDXC		9		9	9	
Parallel Nand			16			
RGMII				14		
eMMC						
SPI Slave						

Digital Pin SUM (excluding DRAM)		62	62	62	62	62

4.8. Comparison between Part Number

	RTL8197FB-CG	RTL8197FS-VSx-CG	RTL8197FS-VEx-CG	RTL8197FH-VEx-CG	RTL8197FN-VEx-CG	RTL8197FNT-VEx-CG
Scenario	1.) AC750-GE W/ SD 2.) AC1200-GE W/ SD 3.) IPCAM 4.) Smart Router	1.) Secure Boot 2.) IoT	1.) AC750-GE W/ SD 2.) AC1200-GE W/ SD 3.) IoT / Repeater PS: 5 Port Giga	1.) AC750-GE 2.) AC1200-GE PS: (1 Giga WAN + 4 10/100 LAN)	1.) N300-FE 2.) AC750-FE 3.) AC1200-FE	1.) N300-FE
CPU Clock	1GHz	1GHz	1GHz	1GHz	1GHz	600MHz
Secure Boot	No	Yes	No	No	No	No
Boot mode	1.) SPI-Nor 2.) SPI-Nand 3.) Switch booting 4.) eMMC 1.8V 5.) eMMC 3.3V 6.) SD booting 7.) P-Nand	1.) SPI-Nor 2.) SPI-Nand 3.) Switch booting 4.) eMMC 1.8V 5.) eMMC 3.3V 6.) SD booting	1.) SPI-Nor 2.) SPI-Nand 3.) Switch booting 4.) eMMC 1.8V 5.) eMMC 3.3V 6.) SD booting 7.) P-Nand	1.) SPI-Nor 2.) SPI-Nand 3.) Switch booting	1.) SPI-Nor 2.) SPI-Nand 3.) Switch booting	1.) SPI-Nor 2.) SPI-Nand 3.) Switch booting
PCIe Support	Yes	Yes	Yes	Yes	Yes	No
Package	TF-BGA268	DR-QFN128	DR-QFN128	DR-QFN128	DR-QFN128	DR-QFN128
DRAM	External DRAM	In Package	In Package	In Package	In Package	In Package
MAX DRAM Size (Data bit width:16 bit)	256MB	128MB	128MB	TBD	128MB	TBD
MAX DRAM Size (Data bit width:8 bit)	512MB (256MB/8bit * 2 DRAM)	-	-	-	-	-
Ethernet-PHY port count (10/100)	5 port	1 port	1 port	5 port	5 port	5 port
SPI-Nor Flash Chip Select	2	2	2	1	1	1
SPI-Nand I/O Support	Quad IO	Quad IO	Quad IO	Dual IO	Dual IO	Dual IO
Parallel-Nand Support	Yes	Yes	Yes	No	No	No
RGMII Support	Yes (3.3V/2.5V)	Yes (3.3V/2.5V)	Yes (3.3V/2.5V)	Yes (3.3V only, use GPIO to simulate MDC/MDIO)	No	No
Switch LED Pin Count	5	4	4	5	5	5

SD Host Support	Yes	Yes	Yes	No	No	No
eMMC Host Support	Yes	Yes	Yes	No	No	No
WiFi digital Pin Count	18	7	7	7	7	7
WiFi ePA/eLNA	Yes	Yes	Yes	No	Yes	Yes
WiFi Antenna Diversity W/ iPA	Yes	Yes	Yes	Yes	Yes	Yes
WiFi Antenna Diversity W/ ePA	Yes	No	No	No	No	No
JTAG Pin Count	5	0 (but jtag function could be shared from RGMII)	0 (but jtag function could be shared from RGMII)	0 (but jtag function could be shared from RGMII)	0 (but jtag function could be shared from RGMII)	0 (but jtag function could be shared from RGMII)

Table 7. Difference between Part Number

		D0 (0)	I1 (1)	I5 (2)	IB8 (3)		E9 (4)	E11 (5)	EB18 (6)	IL4 (7)
Pin Usecase / WLAN GPIO	Pin Name	Package Support	Power-up default	iPA/iLNA (1-pin)	iPA/iLNA (5-pin)	iPA/iLNA/BT (8-pin)	ePA/eLNA_with_inv (7-pin)	ePA/eLNA_with_inv (9-pin)	ePA/eLNA (11-pin)	ePA/eLNA/BT (18-pin)
Package			8197FN 8197FH 8197FS 8197FB	8197FN 8197FH 8197FS 8197FB	8197FN 8197FH 8197FS 8197FB	8197FN 8197FH 8197FS 8197FB	8197FN 8197FH 8197FS 8197FB	8197FB	8197FB	8197FB
wlan_gpio[0]	WBB0	FH/FN/FS/FB	-	TRX_LED	TRX_LED	TRX_LED	TRX_LED	TRX_LED	TRX_LED	TRX_LED
wlan_gpio[1]	WBB1	FH/FN/FS/FB	-	-	ANTSEL_0	BTCOEX_BT_PRI	PAPE0	ANTSEL_0	ANTSEL_0	ANTSEL_0
wlan_gpio[2]	WBB2	FH/FN/FS/FB	-	-	ANTSEL_1	BTCOEX_BT_STA	PAPE1	ANTSEL_1	ANTSEL_1	ANTSEL_1
wlan_gpio[3]	WBB3	FH/FN/FS/FB	-	-	ANTSEL_2	BTCOEX_BT_CK	TRSW_P0	PAPE0	ANTSEL_2	ANTSEL_2
wlan_gpio[4]	WBB4	FH/FN/FS/FB	-	-	ANTSEL_3	BTCOEX_WL_ACT	TRSW_N0	PAPE1	ANTSEL_3	ANTSEL_3
wlan_gpio[5]	WBB5	FB	-	-	-	-	-	TRSW_P0	PAPE0	PAPE0
wlan_gpio[6]	WBB6	FB	-	-	-	-	-	TRSW_N0	PAPE1	PAPE1
wlan_gpio[7]	WBB7	FH/FN/FS/FB	-	-	-	-	TRSW_P1	TRSW_P1	TRSW_P0	TRSW_P0
wlan_gpio[8]	WBB8	FH/FN/FS/FB	-	-	-	-	TRSW_N1	TRSW_N1	TRSW_N0	TRSW_N0
wlan_gpio[9]	WBB9	FB	-	-	-	-	-	-	TRSW_P1	TRSW_P1
wlan_gpio[10]	WBB10	FB	-	-	-	-	-	-	TRSW_N1	TRSW_N1
wlan_gpio[11]	WBB11	FB	-	-	-	-	-	-	-	BTCOEX_BT_PRI
wlan_gpio[12]	WBB12	FB	-	-	-	-	-	-	-	BTCOEX_BT_STA
wlan_gpio[13]	JTAG_TRSTN	FB	-	-	-	-	-	-	-	BTCOEX_BT_CK
wlan_gpio[14]	JTAG_CLK	FB	-	-	-	-	-	-	-	BTCOEX_WL_ACT
wlan_gpio[15]	JTAG_TMS	FB	-	-	-	-	-	-	-	-
wlan_gpio[16]	JTAG_TDI	FB	-	-	-	-	-	-	-	-
wlan_gpio[17]	JTAG_TDO	FB	-	-	-	-	-	-	-	-

Figure 8. WiFi Function Difference between Part Number

Part No.			RTL8197FB	RTL8197FS	RTL8197FH	RTL8197FN
Package Type			TFBGA-268	MCM-DR-QFN128	MCM-DR-QFN128	MCM-DR-QFN128
CPU		MIPS24Kc	Y	Y	Y	Y
SDRAM		SDR168	N	N	N	N
		DDR1-500	Y	Y, But no bonding diagram	Y, But no bonding diagram	Y, But no bonding diagram
		DDR2-1066	Y	Y *MCM-64MB	Y *MCM-64MB	Y *MCM-64MB
EtherPHY		10/100	Y *(UTP=5)	Y *(UTP=1)	Y *(UTP=5)	Y *(UTP=5)
PCIE1.1		HOST*1	Y	Y	Y	Y
USB2.0		HOST*1	Y	Y	Y	Y
		OTG *1	Y	Y	Y	Y
		OTG-detect	N	N	N	N
SPI-Flash share function - total 6*pins		SPI-NOR	Y *6 (dual+2*cs_n+rst)	Y *6 (dual+2*cs_n+rst)	Y *5 (dual+1*cs_n+rst)	Y *5 (dual+1*cs_n+rst)
		SPI-NAND	Y *6 (qual+1*cs_n)	Y *6 (qual+1*cs_n)	Y *4 + GPIO*1 (dual+1*cs_n)	Y *4 + GPIO*1 (dual+1*cs_n)
		I2S 5.1ch out	Y *6	Y *6	N	N
		I2S stereo out	Y *4 +GPIO*2	Y *4 +GPIO*2	Y *4 +GPIO*1	Y *4 +GPIO*1
		I2S mono in+out	Y *5 +GPIO*1	Y *5 +GPIO*1	Y*5	Y*5
	Subgroup -1 *4	UART-1	Y *4	Y *4	Y *4	Y *4
		SPI-1	Y*4	Y*4	Y*4	Y*4
		I2C0+I2C1	Y*4	Y*4	Y*4	Y*4
	Subgroup -2 *2	I2C-1	Y *2	Y *2	N	N
		CK12M	Y *1 +GPIO*1	Y *1 +GPIO*1	Y *1	Y *1
		GPIO	Y *6	Y *6	Y *5	Y *5
R/G/MII-P0 share function - total 14*pins		GMII	N	N	N	N
		RGMII/MII	Y *14	Y *14	Y * 13 (use other GPIO to replace MDIO)	N
		Parallel NAND *12/16	Y *12 +subgroup-4	Y *12 +subgroup-4	N	N
		JTAG	Y *5 + GPIO*9	Y *5 + GPIO*9	Y *5 + GPIO*8	Y *5 + GPIO*8
	Subgroup -1 *4	SPI-0 host	Y*4	Y*4	Y*4	Y*4
		I2C-1	Y*2 +GPIO*2	Y*2 +GPIO*2	Y*2 +GPIO*2	Y*2 +GPIO*2
		I2S stereo out	Y *4	Y *4	Y *4	Y *4
		I2S 5.1ch out	Y *2 sd2+sd3	Y *2 sd2+sd3	Y *2 sd2+sd3	Y *2 sd2+sd3
		CK12M	Y *2 +GPIO*2	Y *2 +GPIO*2	Y *2 +GPIO*2	Y *2 +GPIO*2
		PWM 0~3	Y *4	Y *4	Y *4	Y *4
	Subgroup	SPI-0 slave	Y *4	Y *4	Y *4	Y *4

	-2 *4	I2S stereo out	Y *4	Y *4	Y *4	Y *4
		PCM	Y *4	Y *4	Y *4	Y *4
		UART-2	Y *4	Y *4	Y *4	Y *4
		Event Timer 0~3	Y *4	Y *4	Y *4	Y *4
	Subgroup -3 *4	SPI-1 host	Y *4	Y *4	Y *4	Y *4
		UART-1	Y *4	Y *4	Y *4	Y *4
		I2C0+I2C1	Y*4	Y*4	Y*4	Y*4
		CK12M	Y *2 +GPIO*2	Y *2 +GPIO*2	Y *2 +GPIO*2	Y *2 +GPIO*2
		PWM 0~3	Y *4	Y *4	Y *4	Y *4
	Subgroup -4 *2	I2C-0	Y *2	Y *2	N	N
		I2C-1	Y *2	Y *2	N	N
		GPIO	Y *14	Y *14	Y *13	Y *13
LED share function - total 5*pins		LED	Y *5	Y *4	Y *5	Y *5
		PWM 0~3	Y *4 +LED*1	Y *3 +LED*1	Y *4 +LED*1	Y *4 +LED*1
		or GPIO	Y *5	Y *4	Y *5	Y *5
UART0		UART0-half	Y *2	Y *2	Y *2	Y *2
eMMC share function - total 13*pins		EMMC	Y *11 + GPIO*2	Y *11 + GPIO*2	N	N
		SDXC	Y*9 +GPIO*4	Y*9 +GPIO*4	N	N
		I2S stereo out	Y *4 +GPIO*9	Y *4 +GPIO*9	N	N
		I2S 5.1ch out	Y *6 +GPIO*7	Y *6 +GPIO*7	N	N
	Subgroup -1 *9	SPI-1 host	Y *4 +GPIO*5	Y *4 +GPIO*5	N	N
		UART-1	Y *4 +GPIO*5	Y *4 +GPIO*5	N	N
		UART-2	Y *4 +GPIO*5	Y *4 +GPIO*5	N	N
		Parallel NAND *4/16	Y *4 +GPIO*5	Y *4 +GPIO*5	N	N
	Subgroup -2 *4	SPI-1 host	Y*4	Y*4	N	N
		UART-1	Y*4	Y*4	N	N
		PCM	Y*4	Y*4	N	N
		PWM 0~3	Y *4	Y *4	N	N
		I2C-0	Y *2 +GPIO*2	Y *2 +GPIO*2	N	N
		GPIO	Y *13	Y *13	N	N
WBB share function - total 13*pins		WBB_0~12	Y*13	Y*7	Y*7	Y*7
	Subgroup -1 *9	Xout	Y*1 +GPIO*8	Y*1 +GPIO*6	Y*1 +GPIO*6	Y*1 +GPIO*6
	Subgroup -2 *4	SPI-0 host	Y*4	N	N	N
		I2S stereo out	Y*4	N	N	N
		I2C-1	Y *2 +GPIO*2	N	N	N

		Event Timer 0~3	Y *4	N	N	N
		Xout	Y*1 +GPIO*3	N	N	N
		GPIO	Y *13	Y*7	Y*7	Y*7
		WBB13~17	Y *5	N	N	N
		JTAG	Y *5	N	N	N
		UART-1	Y*4 + GPIO*1	N	N	N
		PCM	Y *4 + GPIO*1	N	N	N
		PWM	Y *4 + GPIO*1	N	N	N
		I2C-0	Y *2 +GPIO*3	N	N	N
JTAG share function - total 5*pins		**CK12M**	Y *2 +GPIO*3	N	N	N
		or GPIO	Y *5	N	N	N
IPSec			Y	Y	Y	Y
RF		**RF**	Y *2X2N	Y *2X2N	Y *2X2N	Y *2X2N
		3.3-to-1.8/2.5 SWR	Y *option with LDO	Y *option with LDO	Y *option with LDO	Y *option with LDO
		3.3-to-1.8/2.5 LDO	Y *option with SWR	Y *option with SWR	Y *option with SWR	Y *option with SWR
DDR-SWR/LDO		**configurable**	Y	Y	Y	Y
SWR 1.2A		**3.3-to-1.05**	Y	Y	Y	Y
		40M OSC	Y	Y	Y	Y
Clock Source		**25M Crystal**	Y	Y	Y	Y

Figure 9. Pin Support between Part Number

5. Pin Assignments

5.1. RTL8197FNT DR-QFN128

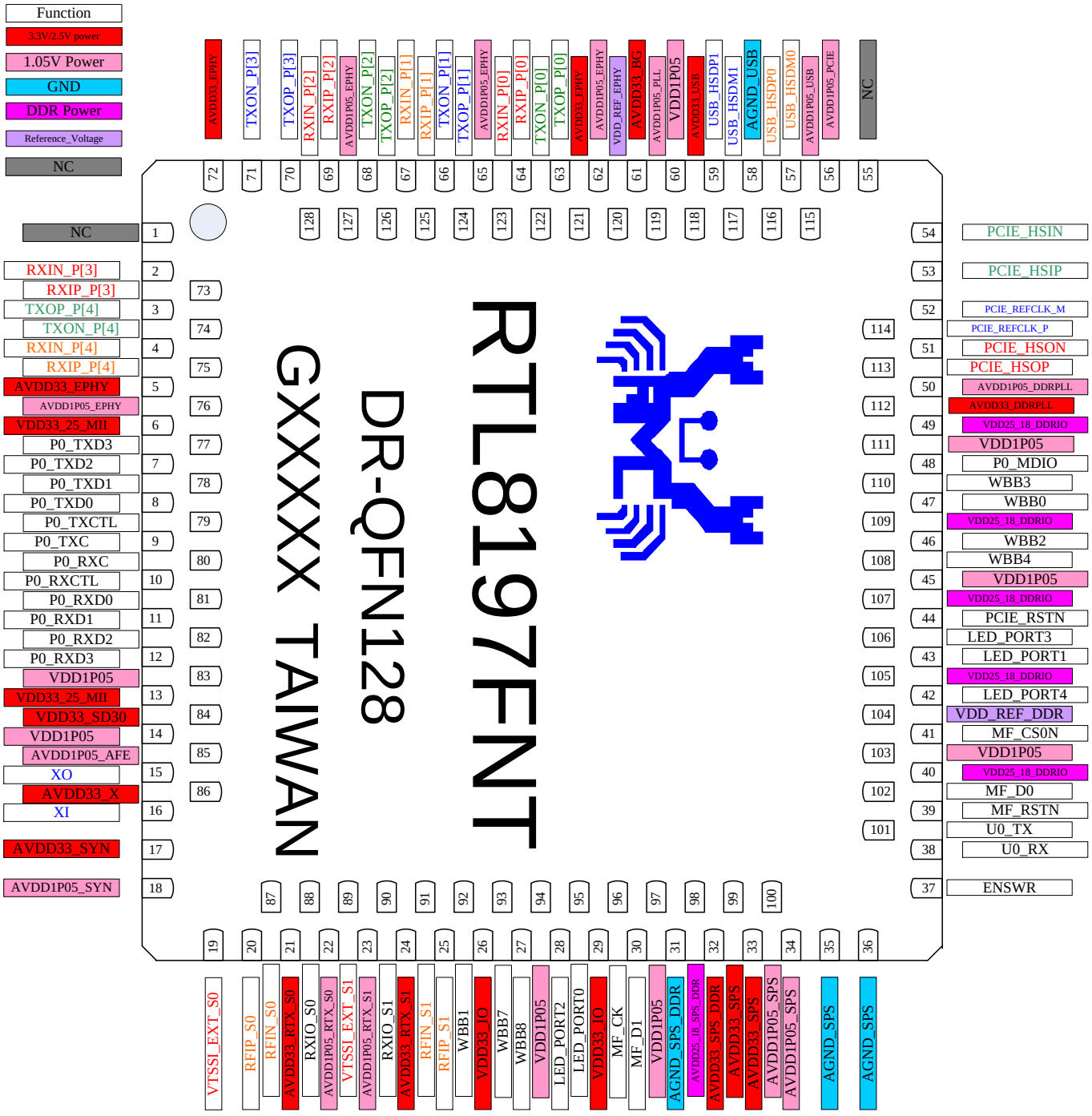


Figure 10. RTL8197FNT DR-QFN128 Pin Assignments

5.2. RTL8197FN DR-QFN128

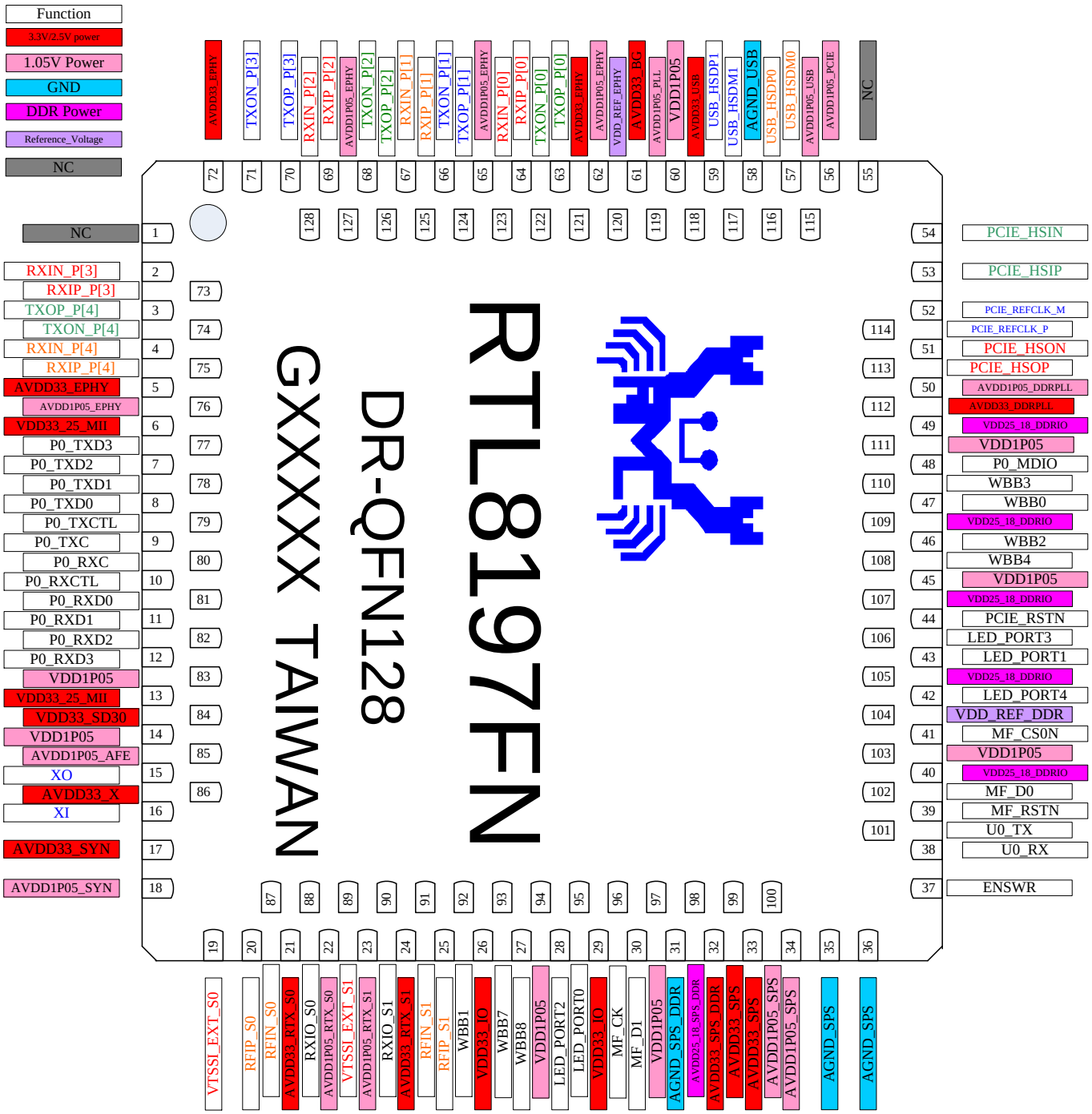


Figure 11. RTL8197FN DR-QFN128 Pin Assignments

5.3. RTL8197FH DR-QFN128

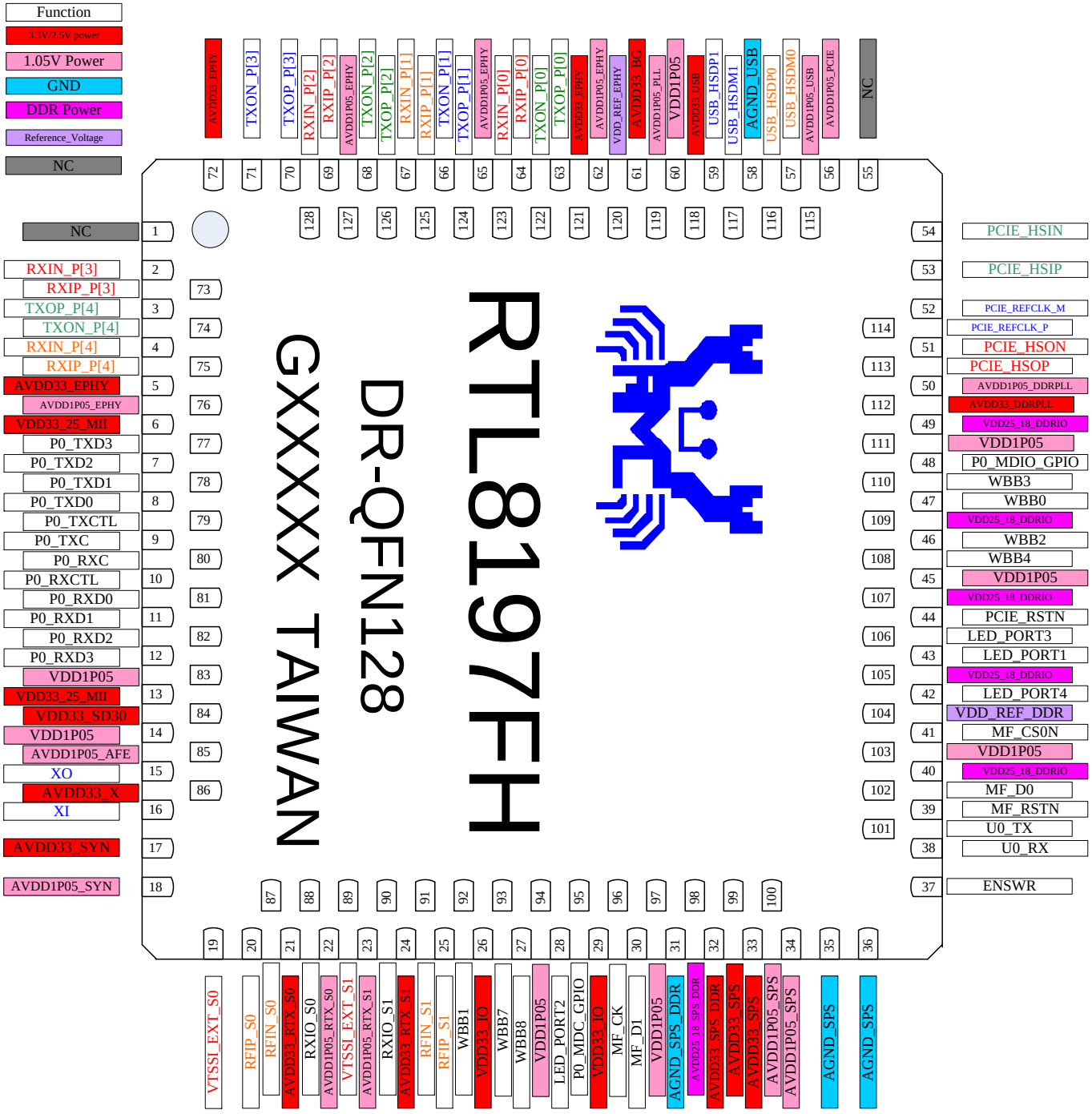


Figure 12. RTL8197FH DR-QFN128 Pin Assignments

5.4. RTL8197FS DR-QFN128

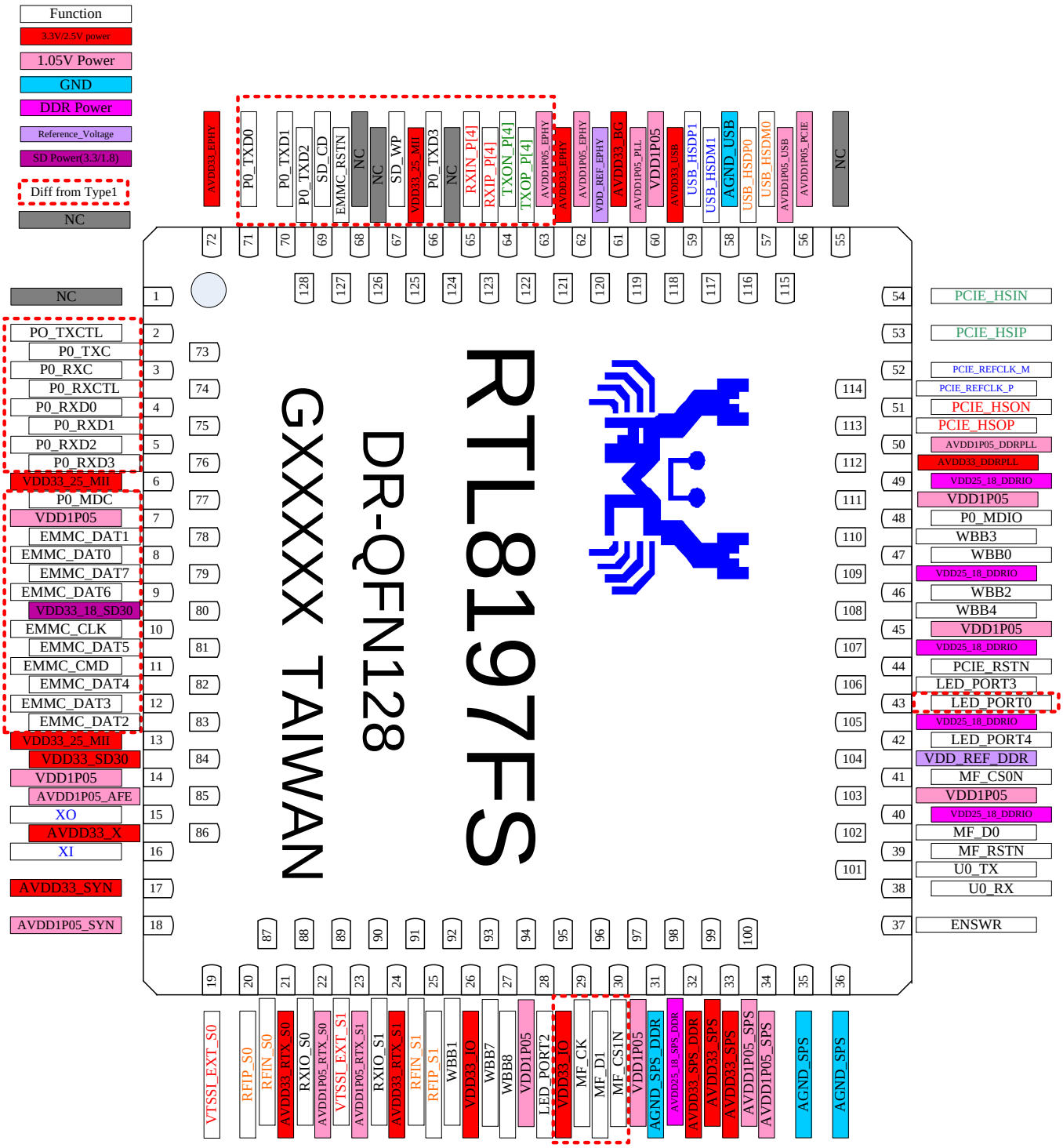


Figure 13. RTL8197FS DR-QFN128 Pin Assignments

5.5. RTL8197FB TF-BGA268

RTL8197F(RL6387) Ball Assignment
(268-TFBGA 12x12mm)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DDR_A3	DDR_A12	DDR_A14	DDR_BS0	DDR_WE#	DDR_A15	DDR_A13	DDR_A6	DDR_A0	DDR_RAS#	CKE	DCLK	DDR_DQ2	DDR_DQ7	DDR_DQ10	DDR_DQ15	DDR_UDQS#	DDR_UDQS	A
B	DDR_A5	DDR_A7	DDR_A9	DDR_A1	DDR_BS1	DDR_A2	DDR_A11	DDR_A8	DDR_A4	DDR_CAS#	DDR_ODT	DDR_DCLK#	DDR_DQ5	DDR_DQ0	DDR_DQ13	DDR_DQ8	DDR_DQ3	DDR_DQ4	B
C	DDR_A10	DDR_BS2	AVDD33_DDRPLL	AVDD1P05_DDRPLL	VDD1P05	VDD25¬_18_DDRIO	VDD25¬_18_DDRIO	VDD1P05	VDD25¬_18_DDRIO	VDD25¬_18_DDRIO	DDR_CS#	VDD1P05	VDD25¬_18_DDRIO	VDD25¬_18_DDRIO	VDD_REF_DDR	MF_CS1N	DDR_DQ1	DDR_UDQM	C
D	PCIE_HSON	PCIE_HSOP	GND	AVDD33_USB	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD1P05	VDD33_IO	MF_RSTN	DDR_DQ14	DDR_DQ9	D
E	PCIE_REFCLK_M	PCIE_REFCLK_P	AVDD1P05_PCIE	AVDD1P05_USB					GND	GND					VDD1P05	MF_D1	DDR_DQ11	DDR_DQ12	E
F	PCIE_HSIN	PCIE_HSIP	GND	AGND_USB											VDD33_IO	MF_D0	DDR_DQ6	DDR_LDQM	F
G	USB_HSDM0	USB_HSDP0	GND	AVDD1P05_PLL			GND	GND	GND	GND	GND	GND			LED_PORT4	MF_CK	DDR_LDQS#	DDR_LDQS	G
H	USB_HSDM1	USB_HSDP1	AVDD1P05_EPHY	RTT			GND	GND	GND	GND	GND	GND			LED_PORT0	MF_CS0N	AVDD25_18_SPS_DDR	AVDD25_18_SPS_DDR	H
J	TXOP_P0	TXON_P0	AVDD33_EPHY	AVDD33_EPHY	VDD_REF_EPHY		GND	GND	GND	GND	GND	GND		U0_RX	LED_PORT1	AVDD33_SPS_DDR	AGND_SPS_DDR	AGND_SPS_DDR	J
K	RXIP_P0	RXIN_P0	AVDD1P05_EPHY	RTT1	AVDD33_BG		GND	GND	GND	GND	NC_GND	NC_GND		U0_TX	LED_PORT2	AVDD33_SPS	AVDD1P05_SPS	AVDD1P05_SPS	K
L	TXOP_P1	TXON_P1	AVDD1P05_EPHY	AVDD33_EPHY			GND	GND	GND	GND	NC_GND	GND			LED_PORT3	AVDD33_SPS	AGND_SPS	AGND_SPS	L
M	RXIP_P1	RXIN_P1	GND	GND			GND	GND	GND	AVDD1P05_AFE	GND	GND			JTAG_TMS	JTAG_TDO	PCIE_RSTN	ENSWR	M
N	TXOP_P2	TXON_P2	AVDD1P05_EPHY	AVDD33_EPHY											JTAG_TDI	JTAG_CLK	WBB8	WBB5	N
P	RXIP_P2	RXIN_P2	AVDD1P05_EPHY	AVDD33_EPHY					GND	VDD1P05					JTAG_TRSTN	WBB4	WBB6	RFIP_S1	P
R	TXOP_P3	TXON_P3	EMMC_RSTN	SD_CD	GPIO_1	P0_MDC	VDD33_25_MII	VDD33_25_MII	GND	VDD33_18_SD30	VDD33_SD30	AVDD33_X	AVDD1P05_SYN	AVDD33_RTX_S0	AVDD33_RTX_S1	WBB7	GND	RFIN_S1	R
T	RXIP_P3	RXIN_P3	SD_WP	GPIO_0	GPIO_2	P0_MDIO	EMMC_DAT1	EMMC_DAT0	EMMC_DAT7	EMMC_DAT5	EMMC_DAT4	EMMC_DAT2	AVDD33_SYN	AVDD1P05_RTX_S0	AVDD1P05_RTX_S1	WBB9	VTSSI_EXT_S1	RXIO_S1	T
U	TXOP_P4	TXON_P4	P0_TXD2	P0_TXD0	P0_TXCTL	P0_RXCTL	P0_RXD1	P0_RXD3	EMMC_DAT6	EMMC_CMD	EMMC_DAT3	VTSSI_EXT_S0	WBB0	GND	WBB1	WBB2	WBB10	WBB12	U
V	RXIP_P4	RXIN_P4	P0_TXD3	P0_TXD1	P0_TXC	P0_RXC	P0_RXD0	P0_RXD2	EMMC_CLK	XO	XI	GND	AGPIO	RFIP_S0	RFIN_S0	RXIO_S0	WBB11	WBB3	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

DRAM	PCIE	USB	SWITCH	RGMII	MMC	RF	RF control& JTAG	SWR	FLASH	digital	POWER	GND

Figure 14. RTL8197FB TF-BGA268 Pin Assignments

5.6. Package Identification

Green package is indicated by the 'G' in GXXXX

6. Pin Descriptions

In this section the following abbreviations are used:

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input

O: Output

I/O: Bi-Directional Input/Output

P: Digital Power

G: Digital Ground

I_{PD}: Input Pin With Pull-Down Resistor

AI: Analog Input

AO: Analog Output

AI/O: Analog Bi-Directional Input/Output

AP: Analog Power

AG: Analog Ground

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

6.1. Pin Descriptions (RTL8197FNT)

Table 8. Pin Descriptions – RTL8197FNT DRQFN-128

Pin Name	Pin No.	Type	Description
Clock & Reset			
XI	16	I	25/40MHz External Clock Input.
XO	15	O	25/40MHz Crystal Clock Output.
10/100M Ethernet Physical Layer			
TXOP_P[4:0] TXON_P[4:0]	TXOP_P0: 63 TXON_P0: 122 TXOP_P1: 124 TXON_P1: 66 TXOP_P2: 126 TXON_P2: 68 TXOP_P3: 70 TXON_P3: 71 TXOP_P4: 3 TXON_P4: 74	AO	10/100M Ethernet Physical Layer Transmit Pair. For differential data transmission.
RXIP_P[4:0] RXIN_P[4:0]	RXIP_P0: 64 RXIN_P0: 123 RXIP_P1: 125 RXIN_P1: 67 RXIP_P2: 69 RXIN_P2: 128 RXIP_P3: 73 RXIN_P3: 2 RXIP_P4: 75 RXIN_P4: 4	AI	10/100M Ethernet Physical Layer Receive Pair. For differential data reception.
Ethernet MAC RGMII/MII Interface			
~~P0_MDC~~		~~O~~	~~Management Data Clock.~~
P0_MDIO	48	I_{PU}/O	Management Data I/O.
P0_TXC	9	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.

Pin Name	Pin No.	Type	Description
P0_TXCTL	79	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_TXD[3:0]	P0_TXD0: 8 P0_TXD1: 78 P0_TXD2: 7 P0_TXD3: 77	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXC	80	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXCTL	10	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
P0_RXD[3:0]	P0_RXD0: 81 P0_RXD1: 11 P0_RXD2: 82 P0_RXD3: 12	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
Serial SPI-Nor Flash Control			
MF_CS0N	41	O	SPI Serial Flash Chip Select 0.
MF_RSTN	39	O	SPI Serial Flash Reset
MF_D[1:0]	MF_D0: 102 MF_D1: 30	I/O	SPI Serial Flash Serial Data Input/Output.
MF_CK	96	O	SPI Serial Flash Serial Clock Output.
Serial SPI-Nand Flash Control (Share Pin)			
SPI_NAND_CK	MF_CK	O	SPI Nand Flash Clock Output
SPI_NAND_D[2:0]	SPI_NAND_D0: MF_D0 SPI_NAND_D1: MF_D1 SPI_NAND_D2: MF_RSTN	I/O	SPI Nand Flash Data Input/Output
SPI_NAND_CS0N	MF_CS0N	O	SPI Nand Flash Chip Select 0
~~SPI_NAND_D[3]~~		~~I/O~~	~~SPI Nand Flash Data Input/Output~~
UART			
U0_TX	101	O	Data Transmit Serial Output of UART0.
U0_RX	38	I_{PU}	Data Receive Serial Input of UART0.
UART (Full) (Share Pin)			
U1_TX	P0_TXCTL	O	Data Transmit Serial Output of UART1.
U1_RX	P0_TXC	I_{PU}	Data Receive Serial Input of UART1.
U1_RTS	P0_TXD0	O	Request To Send of UART1.
U1_CTS	P0_RXCTL	I	Clear To Send of UART1.
U2_TX	P0_RXD2	O	Data Transmit Serial Output of UART2.
U2_RX	P0_RXD1	I_{PU}	Data Receive Serial Input of UART2.
U2_RTS	P0_RXD3	O	Request To Send of UART2.
U2_CTS	P0_RXD0	I	Clear To Send of UART2.

Pin Name	Pin No.	Type	Description
SPI (4-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3	O	SPI0 Clock output
SPI0_TXD	MF_D0, P0_TXD1	O	SPI0 Data Transmit
SPI0_RXD	MF_D1, P0_RXC	I	SPI0 Data Receive
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO	O	SPI0 Chip Select 0
SPI1_CLK	P0_TXD0	O	SPI1 Clock output
SPI1_TXD	P0_TXCTL	O	SPI1 Data Transmit
SPI1_RXD	P0_RXCTL	I	SPI1 Data Receive
SPI1_CS0N	P0_TXC, P0_MDIO	O	SPI1 Chip Select 0
SPI (3-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3	O	SPI0 Clock output
SPI0_TRXD	MF_D1, P0_RXC	I/O	SPI0 Data Transmit/Receive
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO	O	SPI0 Chip Select 0
SPI1_CLK	P0_TXD0	O	SPI1 Clock output
SPI1_TRXD	P0_RXCTL	I/O	SPI1 Data Transmit/Receive
SPI1_CS0N	P0_TXC, P0_MDIO	O	SPI1 Chip Select 0
SPI (4-Wire Slave mode) (Share Pin)			
SPI0_CLK_SLV	P0_RXD1	I	SPI0 Slave Mode Clock Input
SPI0_TXD_SLV	P0_RXD3	O	SPI0 Slave Mode Data Transmit
SPI0_RXD_SLV	P0_RXD2	I	SPI0 Slave Mode Data Receive
SPI0_CS0N_SLV	P0_RXD0	I	SPI0 Slave Mode Chip Select 0 Input
PCM (Master Mode) (Share Pin)			
PCM_CLK	P0_RXD3	O	PCM Master Mode Clock Output
PCM_FS	P0_RXD2	O	PCM Master Mode Frame Sync
PCM_TXD	P0_RXD1	O	PCM Master Mode Data Transmit
PCM_RXD	P0_RXD0	I	PCM Master Mode Data Receive
JTAG (Share Pin)			
JTAG_TCK	P0_RXC	I_{PU}	JTAG Test Clock.
JTAG_TMS	P0_RXD2	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	P0_TXD0	O	JTAG Test Data Output.
JTAG_TDI	P0_RXD1	I_{PU}	JTAG Test Data In.
JTAG_TRSTN	P0_RXD3	I_{PU}	JTAG Test Reset.
I2C (Share Pin)			
I2C0_SCL	MF_CK, P0_TXCTL	B	I2C0 Serial Clock Line

Pin Name	Pin No.	Type	Description
I2C0_SDA	MF_D0, P0_RXCTL	B	I2C0 Serial Data Line
I2C1_SCL	MF_D1, MF_CS0N, P0_TXD1, P0_TXD0	B	I2C1 Serial Clock Line
I2C1_SDA	MF_RSTN, P0_RXC, P0_TXC	B	I2C1 Serial Data Line
I2C0_SCL_SLV	P0_TXC	B	I2C0 Slave Serial Clock Line
I2C0_SDA_SLV	P0_RXCTL	B	I2C0 Slave Serial Data Line
I2C1_SCL_SLV	MF_D1	B	I2C1 Slave Serial Clock Line
I2C1_SDA_SLV	MF_RSTN	B	I2C1 Slave Serial Data Line
LED			
LED_PORT[4:0]	LED_PORT[0]: 95 LED_PORT[1]: 43 LED_PORT[2]: 28 LED_PORT[3]: 106 LED_PORT[4]: 42	O	Link or Link/Speed Status (Low Active).
WiFi Digital			
WBB0	47	O	LED for Wlan TRX
WBB[4:1]	WBB1: 92 WBB2: 46 WBB3: 110 WBB4: 108	I/O	Reserved for external RF component control or Wireless Coexistence interface
WBB[8:7]	WBB7: 93 WBB8: 27	I/O	Reserved for external RF component control or Wireless Coexistence interface
GPIO			
-	-	I/O	-
USB Host 2.0 / OTG			
USB_HSDP0	116	AI/O	USB Port0 Host Device Data Plus Pin.
USB_HSDM0	57	AI/O	USB Port0 Host Device Data Minus Pin.
USB_HSDP1	59	AI/O	USB Port1 Host Device Data Plus Pin.
USB_HSDM1	117	AI/O	USB Port1 Host Device Data Minus Pin.
~~**PCI Express Interface**~~			
~~PCIE_HSON PCIE_HSOP~~	~~51, 113~~	~~AO~~	~~Transmitter Differential Pair.~~
~~PCIE_HSIN PCIE_HSIP~~	~~54, 53~~	~~AI~~	~~Receiver Differential Pair.~~
~~PCIE_REFCLK_M PCIE_REFCLK_P~~	~~52, 114~~	~~AO~~	~~Reference Clock Differential Pair.~~
~~PCIE_RSTN~~	~~44~~	~~O~~	~~PCI Express Reset.~~
Reference Voltage			
VDD_REF_DDR	104	AI	Voltage Reference 1.25V for DDR1. Voltage Reference 0.9V for DDR2.
VDD_REF_EPHY	120	AO	Voltage Reference 0.6V for Ethernet PHY. 2.5K ohm 1% resister pull down

Pin Name	Pin No.	Type	Description
Power & GND			
VDD33_IO	26, 29	P	Digital I/O Power Supply 3.3V.
VDD25_18_DDRIO	40, 105, 107, 109, 49	P	Memory I/O Power Supply 2.5V, or 1.8V. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
VDD33_25_MII	6, 13	P	GMII/RGMII/MII Interface Power Supply 3.3V/2.5V .
VDD33_SD30	84	P	SD Power supply 3.3V
VDD1P05	60, 111, 45, 103, 97, 94, 14, 83	P	Digital Core Power Supply 1.05V.
AVDD33_EPHY	121, 72, 5	AP	Ethernet Analog Power Supply 3.3V.
AVDD1P05_EPHY	76, 127, 65, 62	AP	Ethernet Analog Power Supply 1.05V.
AVDD33_BG	61	AP	System Bandgap Power Supply 3.3V.
AVDD1P05_PCIE	56	AP	PCI Express Analog Power Supply 1.05V.
AVDD1P05_PLL	119	AP	PLL Power 1.05V.
AVDD33_USB	118	AP	USB 2.0 Analog Power 3.3V.
AVDD1P05_USB	115	AP	USB 2.0 Analog Power 1.05V.
AVDD33_DDRPLL	112	AP	DDR PLL Analog Power 3.3V
AVDD1P05_DDRPLL	50	AP or NC	DDR PLL Analog Power 1.05V Mode 1(NC): NC, using internal LDO (3.3V->1.05V) Mode 2(AP): input power
GND	E-PAD	G	System GND.
AGND_SPS_DDR	31	AG	Internal SWR_DDR GND
AGND_SPS	35, 36	AG	Internal SWR GND
AGND_USB	58	AG	USB GND.
Internal SWR & LDO			
AVDD33_SPS_DDR	32	AP	Internal SWR_DDR Power Supply 3.3V Input for DDR.
AVDD25_18_SPS_DDR	98	AP (O)	Internal SWR_DDR Output Power for DDR. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
AVDD33_SPS	99, 33	AP	Internal SWR Power Supply 3.3V Input
AVDD1P05_SPS	100, 34	AP (O)	Internal SWR Power Supply 1.05V Output
ENSWR	37	I	Internal SWR Power Supply Output Voltage enable/disable 0: Disable internal SWR 1: Enable internal SWR Note: If using external SWR/LDO, this pin must tie low.
RF & RF Power			
AVDD1P05_AFE	85	AP	Analog 1.05V power supply
AVDD33_X	86	AP	Analog 3.3V power supply
AVDD33_SYN	17	AP	RF 3.3V power supply
AVDD1P05_SYN	18	AP	RF 1.05V power supply
VTSSI_EXT_S0	19	AI	S0_TSSI voltage input
RFIP_S0	20	AI/O	S0 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIN_S0	87	AI/O	

Pin Name	Pin No.	Type	Description
AVDD33_RTX_S0	21	AP	RF 3.3V power supply
RXIO_S0	88	AI	S0 RX LNA input port
AVDD1P05_RTX_S0	22	AP	RF 1.05V power supply
VTSSI_EXT_S1	89	AI	S1 TSSI voltage input
AVDD1P05_RTX_S1	23	AP	RF 1.05V power supply
RXIO_S1	90	AI	S1 RX LNA input port
AVDD33_RTX_S1	24	AP	RF 3.3V power supply
RFIN_S1	91	AI/O	S1 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIP_S1	25	AI/O	
Not Connected Pins			
NC	1, 55	-	Not Connected. Must keep these pin floating .

6.2. Configuration Upon Power On Strapping (RTL8197FNT)

The 1.05V digital core power input pin voltage is up to 0.7V on system power-on. The strap data will be latched after a delay of 160/100 ms.

25MHz XTAL: 160 ms
40MHz XTAL: 100 ms

Table 9. Configuration Upon Power On Strapping (RTL8197FNT)

H/W Pin Name	Configuration Name	Pin No	Description
WBB4	Boot_select[0]	108	boot_select[3:0]: 0000: SPI-NOR-Flash booting (3 byte addressing) 0001: [ROM] SPI-NOR-Flashing (3 byte addressing) 0010: [ROM] SPI-NAND-Flash booting 0011: 0100: 0101: 0110: 0111: 1000: [ROM] Switch booting (Image to DRAM) 1001: 1010: 1011: 1100: 1101: [ROM] Switch booting (Image to SPI-Nor Flash) 1110: SPI-NOR-Flash booting for OLT (3 byte addressing) 1111: loop mode for debug
WBB7	Boot_select[1]	93	
WBB8	Boot_select[2]	27	
P0_TXD3	Boot_select[3]	77	
MF_CS0N	DRAM_TYPE_INV	41	DRAM_TYPE_INV Select: (Referenced by SW) 0: DDR2 1: DDR1
U0_TX	DRAM_FEQ	101	DRAM_FEQ Selection: (Only Referenced by SW) 0: DDR2_400MHz, DDR1_200MHz 1: DDR2_533MHz, DDR1_250MHz
P0_TXCTL	HW_DBG_DISABLE	79	WiFi Debug mode / Enable strap_ctl_sys_dbg_sel 0: Enable 1: Disable
P0_TXD2	ddr_ldo_Sel	7	DDR Power regulator selection: 0: SWR 1: LDO
P0_TXD1	Disable_Load_Efuse_Value	78	Load Efuse Select: (Referenced by SW) 0: enable Load Efuse 1: disable Load Efuse
P0_TXD0	DISABLE_EXT_RSTN	8	External Reset Select: 0: enable 1: disable

H/W Pin Name	Configuration Name	Pin No	Description
MF_CK	sel_40m	96	System Clock Source Select. 0: 25M 1: 40M
PCIE_RSTN	strap_test_mode	44	Chip Test Mode Select. 0: normal_mode 1: TEST_MODE (CP/FT/SCAN)

6.3. Shared I/O Pin Mapping (RTL8197FNT)

Table 10. Shared I/O Pin Mapping – RTL8197FNT

Pin	GPIO		WiFi / PCM	RGMII/MII	I2S	SPI-Nor / SD/ eMMC	EJTAG/ SPI-Nand	LED/SPI	UART	I2C, Reset
96	GPIOA[0]	O				MF_CK	SPI_NAND_CK	SPI0_CLK		I2C0_SCL
102	GPIOA[1]	B				MF_D0	SPI_NAND_D0	SPI0_TXD		I2C0_SDA
30	GPIOA[2]	B				MF_D1	SPI_NAND_D1	SPI0_RXD, SPI0_TRXD		I2C1_SCL / I2C1_SCL_SLV
39	GPIOA[3]	B				MF_RSTN	SPI_NAND_D2	SPI0_CS0N		I2C1_SDA / I2C1_SDA_SLV
41	GPIOA[4]	O				MF_CS0N	SPI_NAND_CS0N			I2C1_SCL
	~~GPIOA[5]~~									
77	GPIOA[6]	O		P0_TXD3	I2S_MCLK			SPI0_CLK		
7	GPIOA[7]	O		P0_TXD2	I2S_SCLK			SPI0_CS0N		
78	GPIOB[0]	O		P0_TXD1	I2S_WS / I2S_SD2_O			SPI0_TXD		I2C1_SCL
80	GPIOB[1]	B		P0_RXC	I2S_SD1_O / I2S_SD1_I / I2S_SD3_O		JTAG_TCK	SPI0_RXD, SPI0_TRXD		I2C1_SDA
12	GPIOB[2]	B	PCM_CLK	P0_RXD3	I2S_MCLK		JTAG_TRSTN	SPI0_TXD_SLV	U2_RTS	
82	GPIOB[3]	B	PCM_FS	P0_RXD2	I2S_SCLK		JTAG_TMS	SPI0_RXD_SLV	U2_TX	
11	GPIOB[4]	B	PCM_TXD	P0_RXD1	I2S_WS		JTAG_TDI	SPI0_CLK_SLV	U2_RX	
81	GPIOB[5]	B	PCM_RXD	P0_RXD0	I2S_SD1_O			SPI0_CS0N_SLV	U2_CTS	
8	GPIOB[6]	O		P0_TXD0			JTAG_TDO	SPI1_CLK	U1_RTS	I2C1_SCL
9	GPIOB[7]	B		P0_TXC	I2S_SD1_I			SPI1_CS0N	U1_RX	I2C1_SDA / I2C0_SCL_SLV
79	GPIOC[0]	O		P0_TXCTL				SPI1_TXD	U1_TX	I2C0_SCL
10	GPIOC[1]	B		P0_RXCTL				SPI1_RXD, SPI1_TRXD	U1_CTS	I2C0_SDA / I2C0_SDA_SLV
	~~GPIOC[2]~~			~~P0_MDC~~						
48	GPIOC[3]	B		P0_MDIO				SPI0_CS0N, SPI1_CS0N		
	~~GPIOC[4]~~									
	~~GPIOC[5]~~									
	~~GPIOC[6]~~									
	~~GPIOC[7]~~									
	~~GPIOD[0]~~									

Pin	GPIO		WiFi / PCM	RGMII/MII	I2S	SPI-Nor / SD/ eMMC	EJTAG/ SPI-Nand	LED/SPI	UART	I2C, Reset
	~~GPIOD[1]~~									
	~~GPIOD[2]~~									
	~~GPIOD[3]~~									
	~~GPIOD[4]~~									
	~~GPIOD[5]~~									
	~~GPIOD[6]~~									
	~~GPIOD[7]~~									
	~~GPIOE[0]~~									
47	GPIOE[1]	B	WBB0							
92	GPIOE[2]	B	WBB1							
46	GPIOE[3]	B	WBB2							
110	GPIOE[4]	B	WBB3							
108	GPIOE[5]	O	WBB4							
	~~GPIOE[6]~~		~~WBB_5~~							
	~~GPIOE[7]~~		~~WBB_6~~							
93	GPIOF[0]	O	WBB7							
27	GPIOF[1]	O	WBB8							
	~~GPIOF[2]~~									
	~~GPIOF[3]~~									
	~~GPIOF[4]~~									
	~~GPIOF[5]~~									
	~~GPIOF[6]~~									
	~~GPIOF[7]~~									
	~~GPIOG[0]~~									
	~~GPIOG[1]~~									
	~~GPIOG[2]~~									
	~~GPIOG[3]~~									
	~~GPIOG[4]~~									
	~~GPIOG[5]~~									
95	GPIOG[6]	B						LED_PORT0		
43	GPIOG[7]	B						LED_PORT1		
28	GPIOH[0]	B						LED_PORT2		
106	GPIOH[1]	B						LED_PORT3		RESETN
42	GPIOH[2]	B						LED_PORT4		
38	GPIOH[3]	B							U0_RX	
101	GPIOH[4]	O							U0_TX	
44	GPIOH[5]	O								PCIE_RSTN

6.4. GPIO Pin During Boot State (RTL8197FNT)

Table 11. GPIO Pin During Boot State – RTL8197FNT

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
96	GPIOA[0]	I	O	Y	internal pull-down only in strap period
102	GPIOA[1]	I	B		internal pull-up
30	GPIOA[2]	I	B		internal pull-up
39	GPIOA[3]	I	B		internal pull-up
41	GPIOA[4]	I	O	Y	internal pull-down only in strap period
	~~GPIOA[5]~~				
77	GPIOA[6]	O	O	Y	internal pull-down only in strap period
7	GPIOA[7]	O	O	Y	internal pull-up only in strap period
78	GPIOB[0]	O	O	Y	internal pull-down only in strap period
80	GPIOB[1]	I	B		internal pull-up
12	GPIOB[2]	I	B		internal pull-up
82	GPIOB[3]	I	B		internal pull-up
11	GPIOB[4]	I	B		internal pull-up
81	GPIOB[5]	I	B		internal pull-up
8	GPIOB[6]	O	O	Y	internal pull-down only in strap period
9	GPIOB[7]	B	B		internal pull-up
79	GPIOC[0]	O	O	Y	internal pull-down only in strap period
10	GPIOC[1]	I	B		internal pull-up
	~~GPIOC[2]~~				
48	GPIOC[3]	B	B		internal pull-up
	~~GPIOC[4]~~				
	~~GPIOC[5]~~				
	~~GPIOC[6]~~				
	~~GPIOC[7]~~				
	~~GPIOD[0]~~				
	~~GPIOD[1]~~				
	~~GPIOD[2]~~				
	~~GPIOD[3]~~				
	~~GPIOD[4]~~				
	~~GPIOD[5]~~				
	~~GPIOD[6]~~				
	~~GPIOD[7]~~				
	~~GPIOE[0]~~				
47	GPIOE[1]	O	B		internal pull-down
92	GPIOE[2]	B	B		internal pull-down
46	GPIOE[3]	B	B		internal pull-down
110	GPIOE[4]	B	B		internal pull-down

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
108	GPIOE[5]	O	O	Y	internal pull-down
	~~GPIOE[6]~~				
	~~GPIOE[7]~~				
93	GPIOF[0]	O	O	Y	internal pull-down
27	GPIOF[1]	O	O	Y	internal pull-down
	~~GPIOF[2]~~				
	~~GPIOF[3]~~				
	~~GPIOF[4]~~				
	~~GPIOF[5]~~				
	~~GPIOF[6]~~				
	~~GPIOF[7]~~				
	~~GPIOG[0]~~				
	~~GPIOG[1]~~				
	~~GPIOG[2]~~				
	~~GPIOG[3]~~				
	~~GPIOG[4]~~				
	~~GPIOG[5]~~				
95	GPIOG[6]	O	B		internal pull-down
43	GPIOG[7]	O	B		internal pull-down
28	GPIOH[0]	O	B		internal pull-down
106	GPIOH[1]	O	B		internal pull-down
42	GPIOH[2]	O	B		internal pull-down
38	GPIOH[3]	I	B		internal pull-up
101	GPIOH[4]	O	O	Y	internal pull-up only in strap period
44	GPIOH[5]	O	O	Y	internal pull-down only in strap period

6.5. Pin Descriptions (RTL8197FN)

Table 12. Pin Descriptions – RTL8197FN DRQFN-128

Pin Name	Pin No.	Type	Description
Clock & Reset			
XI	16	I	25/40MHz External Clock Input.
XO	15	O	25/40MHz Crystal Clock Output.
10/100M Ethernet Physical Layer			
TXOP_P[4:0] TXON_P[4:0]	TXOP_P0: 63 TXON_P0: 122 TXOP_P1: 124 TXON_P1: 66 TXOP_P2: 126 TXON_P2: 68 TXOP_P3: 70 TXON_P3: 71 TXOP_P4: 3 TXON_P4: 74	AO	10/100M Ethernet Physical Layer Transmit Pair. For differential data transmission.
RXIP_P[4:0] RXIN_P[4:0]	RXIP_P0: 64 RXIN_P0: 123 RXIP_P1: 125 RXIN_P1: 67 RXIP_P2: 69 RXIN_P2: 128 RXIP_P3: 73 RXIN_P3: 2 RXIP_P4: 75 RXIN_P4: 4	AI	10/100M Ethernet Physical Layer Receive Pair. For differential data reception.
Ethernet MAC RGMII/MII Interface			
~~P0_MDC~~		~~O~~	~~Management Data Clock.~~
P0_MDIO	48	I_{PU}/O	Management Data I/O.
P0_TXC	9	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
P0_TXCTL	79	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see

Pin Name	Pin No.	Type	Description
P0_TXD[3:0]	P0_TXD0: 8 P0_TXD1: 78 P0_TXD2: 7 P0_TXD3: 77	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXC	80	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXCTL	10	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
P0_RXD[3:0]	P0_RXD0: 81 P0_RXD1: 11 P0_RXD2: 82 P0_RXD3: 12	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
Serial SPI-Nor Flash Control			
MF_CS0N	41	O	SPI Serial Flash Chip Select 0.
MF_RSTN	39	O	SPI Serial Flash Reset
MF_D[1:0]	MF_D0: 102 MF_D1: 30	I/O	SPI Serial Flash Serial Data Input/Output.
MF_CK	96	O	SPI Serial Flash Serial Clock Output.
Serial SPI-Nand Flash Control (Share Pin)			
SPI_NAND_CK	MF_CK	O	SPI Nand Flash Clock Output
SPI_NAND_D[2:0]	SPI_NAND_D0: MF_D0 SPI_NAND_D1: MF_D1 SPI_NAND_D2: MF_RSTN	I/O	SPI Nand Flash Data Input/Output
SPI_NAND_CS0N	MF_CS0N	O	SPI Nand Flash Chip Select 0
~~SPI_NAND_D[3]~~		~~I/O~~	~~SPI Nand Flash Data Input/Output~~
UART			
U0_TX	101	O	Data Transmit Serial Output of UART0.
U0_RX	38	I_{PU}	Data Receive Serial Input of UART0.
UART (Full) (Share Pin)			
U1_TX	P0_TXCTL	O	Data Transmit Serial Output of UART1.
U1_RX	P0_TXC	I_{PU}	Data Receive Serial Input of UART1.
U1_RTS	P0_TXD0	O	Request To Send of UART1.
U1_CTS	P0_RXCTL	I	Clear To Send of UART1.
U2_TX	P0_RXD2	O	Data Transmit Serial Output of UART2.
U2_RX	P0_RXD1	I_{PU}	Data Receive Serial Input of UART2.
U2_RTS	P0_RXD3	O	Request To Send of UART2.
U2_CTS	P0_RXD0	I	Clear To Send of UART2.
SPI (4-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3	O	SPI0 Clock output
SPI0_TXD	MF_D0, P0_TXD1	O	SPI0 Data Transmit

Pin Name	Pin No.	Type	Description
SPI0_RXD	MF_D1, P0_RXC	I	SPI0 Data Receive
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO	O	SPI0 Chip Select 0
SPI1_CLK	P0_TXD0	O	SPI1 Clock output
SPI1_TXD	P0_TXCTL	O	SPI1 Data Transmit
SPI1_RXD	P0_RXCTL	I	SPI1 Data Receive
SPI1_CS0N	P0_TXC, P0_MDIO	O	SPI1 Chip Select 0
SPI (3-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3	O	SPI0 Clock output
SPI0_TRXD	MF_D1, P0_RXC	I/O	SPI0 Data Transmit/Receive
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO	O	SPI0 Chip Select 0
SPI1_CLK	P0_TXD0	O	SPI1 Clock output
SPI1_TRXD	P0_RXCTL	I/O	SPI1 Data Transmit/Receive
SPI1_CS0N	P0_TXC, P0_MDIO	O	SPI1 Chip Select 0
SPI (4-Wire Slave mode) (Share Pin)			
SPI0_CLK_SLV	P0_RXD1	I	SPI0 Slave Mode Clock Input
SPI0_TXD_SLV	P0_RXD3	O	SPI0 Slave Mode Data Transmit
SPI0_RXD_SLV	P0_RXD2	I	SPI0 Slave Mode Data Receive
SPI0_CS0N_SLV	P0_RXD0	I	SPI0 Slave Mode Chip Select 0 Input
PCM (Master Mode) (Share Pin)			
PCM_CLK	P0_RXD3	O	PCM Master Mode Clock Output
PCM_FS	P0_RXD2	O	PCM Master Mode Frame Sync
PCM_TXD	P0_RXD1	O	PCM Master Mode Data Transmit
PCM_RXD	P0_RXD0	I	PCM Master Mode Data Receive
JTAG (Share Pin)			
JTAG_TCK	P0_RXC	I_{PU}	JTAG Test Clock.
JTAG_TMS	P0_RXD2	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	P0_TXD0	O	JTAG Test Data Output.
JTAG_TDI	P0_RXD1	I_{PU}	JTAG Test Data In.
JTAG_TRSTN	P0_RXD3	I_{PU}	JTAG Test Reset.
I2C (Share Pin)			
I2C0_SCL	MF_CK, P0_TXCTL	B	I2C0 Serial Clock Line
I2C0_SDA	MF_D0, P0_RXCTL	B	I2C0 Serial Data Line

Pin Name	Pin No.	Type	Description
I2C1_SCL	MF_D1, MF_CS0N, P0_TXD1, P0_TXD0	B	I2C1 Serial Clock Line
I2C1_SDA	MF_RSTN, P0_RXC, P0_TXC	B	I2C1 Serial Data Line
I2C0_SCL_SLV	P0_TXC	B	I2C0 Slave Serial Clock Line
I2C0_SDA_SLV	P0_RXCTL	B	I2C0 Slave Serial Data Line
I2C1_SCL_SLV	MF_D1	B	I2C1 Slave Serial Clock Line
I2C1_SDA_SLV	MF_RSTN	B	I2C1 Slave Serial Data Line
LED			
LED_PORT[4:0]	LED_PORT[0]: 95 LED_PORT[1]: 43 LED_PORT[2]: 28 LED_PORT[3]: 106 LED_PORT[4]: 42	O	Link or Link/Speed Status (Low Active).
WiFi Digital			
WBB0	47	O	LED for Wlan TRX
WBB[4:1]	WBB1: 92 WBB2: 46 WBB3: 110 WBB4: 108	I/O	Reserved for external RF component control or Wireless Coexistence interface
WBB[8:7]	WBB7: 93 WBB8: 27	I/O	Reserved for external RF component control or Wireless Coexistence interface
GPIO			
-	-	I/O	-
USB Host 2.0 / OTG			
USB_HSDP0	116	AI/O	USB Port0 Host Device Data Plus Pin.
USB_HSDM0	57	AI/O	USB Port0 Host Device Data Minus Pin.
USB_HSDP1	59	AI/O	USB Port1 Host Device Data Plus Pin.
USB_HSDM1	117	AI/O	USB Port1 Host Device Data Minus Pin.
PCI Express Interface			
PCIE_HSON PCIE_HSOP	51, 113	AO	Transmitter Differential Pair.
PCIE_HSIN PCIE_HSIP	54, 53	AI	Receiver Differential Pair.
PCIE_REFCLK_M PCIE_REFCLK_P	52, 114	AO	Reference Clock Differential Pair.
PCIE_RSTN	44	O	PCI Express Reset.
Reference Voltage			
VDD_REF_DDR	104	AI	Voltage Reference 1.25V for DDR1. Voltage Reference 0.9V for DDR2.
VDD_REF_EPHY	120	AO	Voltage Reference 0.6V for Ethernet PHY. 2.5K ohm 1% resister pull down
Power & GND			
VDD33_IO	26, 29	P	Digital I/O Power Supply 3.3V.

Pin Name	Pin No.	Type	Description
VDD25_18_DDRIO	40, 105, 107, 109, 49	P	Memory I/O Power Supply 2.5V, or 1.8V. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
VDD33_25_MII	6, 13	P	GMII/RGMII/MII Interface Power Supply 3.3V/2.5V .
VDD33_SD30	84	P	SD Power supply 3.3V
VDD1P05	60, 111, 45, 103, 97, 94, 14, 83	P	Digital Core Power Supply 1.05V.
AVDD33_EPHY	121, 72, 5	AP	Ethernet Analog Power Supply 3.3V.
AVDD1P05_EPHY	76, 127, 65, 62	AP	Ethernet Analog Power Supply 1.05V.
AVDD33_BG	61	AP	System Bandgap Power Supply 3.3V.
AVDD1P05_PCIE	56	AP	PCI Express Analog Power Supply 1.05V.
AVDD1P05_PLL	119	AP	PLL Power 1.05V.
AVDD33_USB	118	AP	USB 2.0 Analog Power 3.3V.
AVDD1P05_USB	115	AP	USB 2.0 Analog Power 1.05V.
AVDD33_DDRPLL	112	AP	DDR PLL Analog Power 3.3V
AVDD1P05_DDRPLL	50	AP or NC	DDR PLL Analog Power 1.05V Mode 1(NC): NC, using internal LDO (3.3V->1.05V) Mode 2(AP): input power
GND	E-PAD	G	System GND.
AGND_SPS_DDR	31	AG	Internal SWR_DDR GND
AGND_SPS	35, 36	AG	Internal SWR GND
AGND_USB	58	AG	USB GND.
Internal SWR & LDO			
AVDD33_SPS_DDR	32	AP	Internal SWR_DDR Power Supply 3.3V Input for DDR.
AVDD25_18_SPS_DDR	98	AP (O)	Internal SWR_DDR Output Power for DDR. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
AVDD33_SPS	99, 33	AP	Internal SWR Power Supply 3.3V Input
AVDD1P05_SPS	100, 34	AP (O)	Internal SWR Power Supply 1.05V Output
ENSWR	37	I	Internal SWR Power Supply Output Voltage enable/disable 0: Disable internal SWR 1: Enable internal SWR Note: If using external SWR/LDO, this pin must tie low.
RF & RF Power			
AVDD1P05_AFE	85	AP	Analog 1.05V power supply
AVDD33_X	86	AP	Analog 3.3V power supply
AVDD33_SYN	17	AP	RF 3.3V power supply
AVDD1P05_SYN	18	AP	RF 1.05V power supply
VTSSI_EXT_S0	19	AI	S0_TSSI voltage input
RFIP_S0	20	AI/O	S0 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIN_S0	87	AI/O	
AVDD33_RTX_S0	21	AP	RF 3.3V power supply
RXIO_S0	88	AI	S0 RX LNA input port

Pin Name	Pin No.	Type	Description
AVDD1P05_RTX_S0	22	AP	RF 1.05V power supply
VTSSI_EXT_S1	89	AI	S1 TSSI voltage input
AVDD1P05_RTX_S1	23	AP	RF 1.05V power supply
RXIO_S1	90	AI	S1 RX LNA input port
AVDD33_RTX_S1	24	AP	RF 3.3V power supply
RFIN_S1	91	AI/O	S1 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIP_S1	25	AI/O	
Not Connected Pins			
NC	1, 55	-	Not Connected. Must keep these pin floating .

6.6. Configuration Upon Power On Strapping (RTL8197FN)

The 1.05V digital core power input pin voltage is up to 0.7V on system power-on. The strap data will be latched after a delay of 160/100 ms.

25MHz XTAL: 160 ms
40MHz XTAL: 100 ms

Table 13. Configuration Upon Power On Strapping (RTL8197FN)

H/W Pin Name	Configuration Name	Pin No	Description
WBB4	Boot_select[0]	108	boot_select[3:0]: 0000: SPI-NOR-Flash booting (3 byte addressing) 0001: [ROM] SPI-NOR-Flashing (3 byte addressing) 0010: [ROM] SPI-NAND-Flash booting 0011: 0100: 0101: 0110: 0111: 1000: [ROM] Switch booting (Image to DRAM) 1001: 1010: 1011: 1100: 1101: [ROM] Switch booting (Image to SPI-Nor Flash) 1110: SPI-NOR-Flash booting for OLT (3 byte addressing) 1111: loop mode for debug
WBB7	Boot_select[1]	93	
WBB8	Boot_select[2]	27	
P0_TXD3	Boot_select[3]	77	
MF_CS0N	DRAM_TYPE_INV	41	DRAM_TYPE_INV Select: (Referenced by SW) 0: DDR2 1: DDR1
U0_TX	DRAM_FEQ	101	DRAM_FEQ Selection: (Only Referenced by SW) 0: DDR2_400MHz, DDR1_200MHz 1: DDR2_533MHz, DDR1_250MHz
P0_TXCTL	HW_DBG_DISABLE	79	WiFi Debug mode / Enable strap_ctl_sys_dbg_sel 0: Enable 1: Disable
P0_TXD2	ddr_ldo_Sel	7	DDR Power regulator selection: 0: SWR 1: LDO
P0_TXD1	Disable_Load_Efuse_Value	78	Load Efuse Select: (Referenced by SW) 0: enable Load Efuse 1: disable Load Efuse
P0_TXD0	DISABLE_EXT_RSTN	8	External Reset Select: 0: enable 1: disable

H/W Pin Name	Configuration Name	Pin No	Description
MF_CK	sel_40m	96	System Clock Source Select. 0: 25M 1: 40M
PCIE_RSTN	strap_test_mode	44	Chip Test Mode Select. 0: normal_mode 1: TEST_MODE (CP/FT/SCAN)

6.7. Shared I/O Pin Mapping (RTL8197FN)

Table 14. Shared I/O Pin Mapping – RTL8197FN

Pin	GPIO		WiFi / PCM	RGMII/MII	I2S	SPI-Nor / SD/ eMMC	EJTAG/ SPI-Nand	LED/SPI	UART	I2C, Reset
96	GPIOA[0]	O				MF_CK	SPI_NAND_CK	SPI0_CLK		I2C0_SCL
102	GPIOA[1]	B				MF_D0	SPI_NAND_D0	SPI0_TXD		I2C0_SDA
30	GPIOA[2]	B				MF_D1	SPI_NAND_D1	SPI0_RXD, SPI0_TRXD		I2C1_SCL / I2C1_SCL_SLV
39	GPIOA[3]	B				MF_RSTN	SPI_NAND_D2	SPI0_CS0N		I2C1_SDA / I2C1_SDA_SLV
41	GPIOA[4]	O				MF_CS0N	SPI_NAND_CS0N			I2C1_SCL
	~~GPIOA[5]~~									
77	GPIOA[6]	O		P0_TXD3	I2S_MCLK			SPI0_CLK		
7	GPIOA[7]	O		P0_TXD2	I2S_SCLK			SPI0_CS0N		
78	GPIOB[0]	O		P0_TXD1	I2S_WS / I2S_SD2_O			SPI0_TXD		I2C1_SCL
80	GPIOB[1]	B		P0_RXC	I2S_SD1_O / I2S_SD1_I / I2S_SD3_O		JTAG_TCK	SPI0_RXD, SPI0_TRXD		I2C1_SDA
12	GPIOB[2]	B	PCM_CLK	P0_RXD3	I2S_MCLK		JTAG_TRSTN	SPI0_TXD_SLV	U2_RTS	
82	GPIOB[3]	B	PCM_FS	P0_RXD2	I2S_SCLK		JTAG_TMS	SPI0_RXD_SLV	U2_TX	
11	GPIOB[4]	B	PCM_TXD	P0_RXD1	I2S_WS		JTAG_TDI	SPI0_CLK_SLV	U2_RX	
81	GPIOB[5]	B	PCM_RXD	P0_RXD0	I2S_SD1_O			SPI0_CS0N_SLV	U2_CTS	
8	GPIOB[6]	O		P0_TXD0			JTAG_TDO	SPI1_CLK	U1_RTS	I2C1_SCL
9	GPIOB[7]	B		P0_TXC	I2S_SD1_I			SPI1_CS0N	U1_RX	I2C1_SDA / I2C0_SCL_SLV
79	GPIOC[0]	O		P0_TXCTL				SPI1_TXD	U1_TX	I2C0_SCL
10	GPIOC[1]	B		P0_RXCTL				SPI1_RXD, SPI1_TRXD	U1_CTS	I2C0_SDA / I2C0_SDA_SLV
	~~GPIOC[2]~~			~~P0_MDC~~						
48	GPIOC[3]	B		P0_MDIO				SPI0_CS0N, SPI1_CS0N		
	~~GPIOC[4]~~									
	~~GPIOC[5]~~									
	~~GPIOC[6]~~									
	~~GPIOC[7]~~									
	~~GPIOD[0]~~									

Pin	GPIO		WiFi / PCM	RGMII/MII	I2S	SPI-Nor / SD/ eMMC	EJTAG/ SPI-Nand	LED/SPI	UART	I2C, Reset
	~~GPIOD[1]~~									
	~~GPIOD[2]~~									
	~~GPIOD[3]~~									
	~~GPIOD[4]~~									
	~~GPIOD[5]~~									
	~~GPIOD[6]~~									
	~~GPIOD[7]~~									
	~~GPIOE[0]~~									
47	GPIOE[1]	B	WBB0							
92	GPIOE[2]	B	WBB1							
46	GPIOE[3]	B	WBB2							
110	GPIOE[4]	B	WBB3							
108	GPIOE[5]	O	WBB4							
	~~GPIOE[6]~~		~~WBB_5~~							
	~~GPIOE[7]~~		~~WBB_6~~							
93	GPIOF[0]	O	WBB7							
27	GPIOF[1]	O	WBB8							
	~~GPIOF[2]~~									
	~~GPIOF[3]~~									
	~~GPIOF[4]~~									
	~~GPIOF[5]~~									
	~~GPIOF[6]~~									
	~~GPIOF[7]~~									
	~~GPIOG[0]~~									
	~~GPIOG[1]~~									
	~~GPIOG[2]~~									
	~~GPIOG[3]~~									
	~~GPIOG[4]~~									
	~~GPIOG[5]~~									
95	GPIOG[6]	B						LED_PORT0		
43	GPIOG[7]	B						LED_PORT1		
28	GPIOH[0]	B						LED_PORT2		
106	GPIOH[1]	B						LED_PORT3		RESETN
42	GPIOH[2]	B						LED_PORT4		
38	GPIOH[3]	B							U0_RX	
101	GPIOH[4]	O							U0_TX	
44	GPIOH[5]	O								PCIE_RSTN

6.8. GPIO Pin During Boot State (RTL8197FN)

Table 15. GPIO Pin During Boot State – RTL8197FN

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
96	GPIOA[0]	I	O	Y	internal pull-down only in strap period
102	GPIOA[1]	I	B		internal pull-up
30	GPIOA[2]	I	B		internal pull-up
39	GPIOA[3]	I	B		internal pull-up
41	GPIOA[4]	I	O	Y	internal pull-down only in strap period
	~~GPIOA[5]~~				
77	GPIOA[6]	O	O	Y	internal pull-down only in strap period
7	GPIOA[7]	O	O	Y	internal pull-up only in strap period
78	GPIOB[0]	O	O	Y	internal pull-down only in strap period
80	GPIOB[1]	I	B		internal pull-up
12	GPIOB[2]	I	B		internal pull-up
82	GPIOB[3]	I	B		internal pull-up
11	GPIOB[4]	I	B		internal pull-up
81	GPIOB[5]	I	B		internal pull-up
8	GPIOB[6]	O	O	Y	internal pull-down only in strap period
9	GPIOB[7]	B	B		internal pull-up
79	GPIOC[0]	O	O	Y	internal pull-down only in strap period
10	GPIOC[1]	I	B		internal pull-up
	~~GPIOC[2]~~				
48	GPIOC[3]	B	B		internal pull-up
	~~GPIOC[4]~~				
	~~GPIOC[5]~~				
	~~GPIOC[6]~~				
	~~GPIOC[7]~~				
	~~GPIOD[0]~~				
	~~GPIOD[1]~~				
	~~GPIOD[2]~~				
	~~GPIOD[3]~~				
	~~GPIOD[4]~~				
	~~GPIOD[5]~~				
	~~GPIOD[6]~~				
	~~GPIOD[7]~~				
	~~GPIOE[0]~~				
47	GPIOE[1]	O	B		internal pull-down
92	GPIOE[2]	B	B		internal pull-down
46	GPIOE[3]	B	B		internal pull-down
110	GPIOE[4]	B	B		internal pull-down

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
108	GPIOE[5]	O	O	Y	internal pull-down
	~~GPIOE[6]~~				
	~~GPIOE[7]~~				
93	GPIOF[0]	O	O	Y	internal pull-down
27	GPIOF[1]	O	O	Y	internal pull-down
	~~GPIOF[2]~~				
	~~GPIOF[3]~~				
	~~GPIOF[4]~~				
	~~GPIOF[5]~~				
	~~GPIOF[6]~~				
	~~GPIOF[7]~~				
	~~GPIOG[0]~~				
	~~GPIOG[1]~~				
	~~GPIOG[2]~~				
	~~GPIOG[3]~~				
	~~GPIOG[4]~~				
	~~GPIOG[5]~~				
95	GPIOG[6]	O	B		internal pull-down
43	GPIOG[7]	O	B		internal pull-down
28	GPIOH[0]	O	B		internal pull-down
106	GPIOH[1]	O	B		internal pull-down
42	GPIOH[2]	O	B		internal pull-down
38	GPIOH[3]	I	B		internal pull-up
101	GPIOH[4]	O	O	Y	internal pull-up only in strap period
44	GPIOH[5]	O	O	Y	internal pull-down only in strap period

6.9. Pin Descriptions (RTL8197FH)

Table 16. Pin Descriptions – RTL8197FH DRQFN-128

Pin Name	Pin No.	Type	Description
Clock & Reset			
XI	16	I	25/40MHz External Clock Input.
XO	15	O	25/40MHz Crystal Clock Output.
10/100M Ethernet Physical Layer			
TXOP_P[4:0] TXON_P[4:0]	TXOP_P0: 63 TXON_P0: 122 TXOP_P1: 124 TXON_P1: 66 TXOP_P2: 126 TXON_P2: 68 TXOP_P3: 70 TXON_P3: 71 TXOP_P4: 3 TXON_P4: 74	AO	10/100M Ethernet Physical Layer Transmit Pair. For differential data transmission.
RXIP_P[4:0] RXIN_P[4:0]	RXIP_P0: 64 RXIN_P0: 123 RXIP_P1: 125 RXIN_P1: 67 RXIP_P2: 69 RXIN_P2: 128 RXIP_P3: 73 RXIN_P3: 2 RXIP_P4: 75 RXIN_P4: 4	AI	10/100M Ethernet Physical Layer Receive Pair. For differential data reception.
Ethernet MAC RGMII/MII Interface			
P0_MDC_GPIO	LED_PORT[0]	O	Management Data Clock by GPIO Simulation.
P0_MDIO_GPIO	48	I_{PU}/O	Management Data I/O by GPIO Simulation.
P0_TXC	9	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.

Pin Name	Pin No.	Type	Description
P0_TXCTL	79	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_TXD[3:0]	P0_TXD0: 8 P0_TXD1: 78 P0_TXD2: 7 P0_TXD3: 77	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXC	80	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXCTL	10	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
P0_RXD[3:0]	P0_RXD0: 81 P0_RXD1: 11 P0_RXD2: 82 P0_RXD3: 12	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
Serial SPI-Nor Flash Control			
MF_CS0N	41	O	SPI Serial Flash Chip Select 0.
MF_RSTN	39	O	SPI Serial Flash Reset
MF_D[1:0]	MF_D0: 102 MF_D1: 30	I/O	SPI Serial Flash Serial Data Input/Output.
MF_CK	96	O	SPI Serial Flash Serial Clock Output.
Serial SPI-Nand Flash Control (Share Pin)			
SPI_NAND_CK	MF_CK	O	SPI Nand Flash Clock Output
SPI_NAND_D[2:0]	SPI_NAND_D0: MF_D0 SPI_NAND_D1: MF_D1 SPI_NAND_D2: MF_RSTN	I/O	SPI Nand Flash Data Input/Output
SPI_NAND_CS0N	MF_CS0N	O	SPI Nand Flash Chip Select 0
~~SPI_NAND_D[3]~~		~~I/O~~	~~SPI Nand Flash Data Input/Output~~
UART			
U0_TX	101	O	Data Transmit Serial Output of UART0.
U0_RX	38	I_{PU}	Data Receive Serial Input of UART0.
UART (Full) (Share Pin)			
U1_TX	P0_TXCTL	O	Data Transmit Serial Output of UART1.
U1_RX	P0_TXC	I_{PU}	Data Receive Serial Input of UART1.
U1_RTS	P0_TXD0	O	Request To Send of UART1.
U1_CTS	P0_RXCTL	I	Clear To Send of UART1.
U2_TX	P0_RXD2	O	Data Transmit Serial Output of UART2.
U2_RX	P0_RXD1	I_{PU}	Data Receive Serial Input of UART2.
U2_RTS	P0_RXD3	O	Request To Send of UART2.
U2_CTS	P0_RXD0	I	Clear To Send of UART2.

Pin Name	Pin No.	Type	Description
SPI (4-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3	O	SPI0 Clock output
SPI0_TXD	MF_D0, P0_TXD1	O	SPI0 Data Transmit
SPI0_RXD	MF_D1, P0_RXC	I	SPI0 Data Receive
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO	O	SPI0 Chip Select 0
SPI1_CLK	P0_TXD0	O	SPI1 Clock output
SPI1_TXD	P0_TXCTL	O	SPI1 Data Transmit
SPI1_RXD	P0_RXCTL	I	SPI1 Data Receive
SPI1_CS0N	P0_TXC, P0_MDIO	O	SPI1 Chip Select 0
SPI (3-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3	O	SPI0 Clock output
SPI0_TRXD	MF_D1, P0_RXC	I/O	SPI0 Data Transmit/Receive
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO	O	SPI0 Chip Select 0
SPI1_CLK	P0_TXD0	O	SPI1 Clock output
SPI1_TRXD	P0_RXCTL	I/O	SPI1 Data Transmit/Receive
SPI1_CS0N	P0_TXC, P0_MDIO	O	SPI1 Chip Select 0
SPI (4-Wire Slave mode) (Share Pin)			
SPI0_CLK_SLV	P0_RXD1	I	SPI0 Slave Mode Clock Input
SPI0_TXD_SLV	P0_RXD3	O	SPI0 Slave Mode Data Transmit
SPI0_RXD_SLV	P0_RXD2	I	SPI0 Slave Mode Data Receive
SPI0_CS0N_SLV	P0_RXD0	I	SPI0 Slave Mode Chip Select 0 Input
PCM (Master Mode) (Share Pin)			
PCM_CLK	P0_RXD3	O	PCM Master Mode Clock Output
PCM_FS	P0_RXD2	O	PCM Master Mode Frame Sync
PCM_TXD	P0_RXD1	O	PCM Master Mode Data Transmit
PCM_RXD	P0_RXD0	I	PCM Master Mode Data Receive
JTAG (Share Pin)			
JTAG_TCK	P0_RXC	I_{PU}	JTAG Test Clock.
JTAG_TMS	P0_RXD2	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	P0_TXD0	O	JTAG Test Data Output.
JTAG_TDI	P0_RXD1	I_{PU}	JTAG Test Data In.
JTAG_TRSTN	P0_RXD3	I_{PU}	JTAG Test Reset.
I2C (Share Pin)			
I2C0_SCL	MF_CK, P0_TXCTL	B	I2C0 Serial Clock Line

Pin Name	Pin No.	Type	Description
I2C0_SDA	MF_D0, P0_RXCTL	B	I2C0 Serial Data Line
I2C1_SCL	MF_D1, MF_CS0N, P0_TXD1, P0_TXD0	B	I2C1 Serial Clock Line
I2C1_SDA	MF_RSTN, P0_RXC, P0_TXC	B	I2C1 Serial Data Line
I2C0_SCL_SLV	P0_TXC	B	I2C0 Slave Serial Clock Line
I2C0_SDA_SLV	P0_RXCTL	B	I2C0 Slave Serial Data Line
I2C1_SCL_SLV	MF_D1	B	I2C1 Slave Serial Clock Line
I2C1_SDA_SLV	MF_RSTN	B	I2C1 Slave Serial Data Line
LED			
LED_PORT[4:0]	LED_PORT[0]: 95 LED_PORT[1]: 43 LED_PORT[2]: 28 LED_PORT[3]: 106 LED_PORT[4]: 42	O	Link or Link/Speed Status (Low Active).
WiFi Digital			
WBB0	47	O	LED for Wlan TRX
WBB[4:1]	WBB1: 92 WBB2: 46 WBB3: 110 WBB4: 108	I/O	Reserved for external RF component control or Wireless Coexistence interface
WBB[8:7]	WBB7: 93 WBB8: 27	I/O	Reserved for external RF component control or Wireless Coexistence interface
GPIO			
-	-	I/O	-
USB Host 2.0 / OTG			
USB_HSDP0	116	AI/O	USB Port0 Host Device Data Plus Pin.
USB_HSDM0	57	AI/O	USB Port0 Host Device Data Minus Pin.
USB_HSDP1	59	AI/O	USB Port1 Host Device Data Plus Pin.
USB_HSDM1	117	AI/O	USB Port1 Host Device Data Minus Pin.
PCI Express Interface			
PCIE_HSON PCIE_HSOP	51, 113	AO	Transmitter Differential Pair.
PCIE_HSIN PCIE_HSIP	54, 53	AI	Receiver Differential Pair.
PCIE_REFCLK_M PCIE_REFCLK_P	52, 114	AO	Reference Clock Differential Pair.
PCIE_RSTN	44	O	PCI Express Reset.
Reference Voltage			
VDD_REF_DDR	104	AI	Voltage Reference 1.25V for DDR1. Voltage Reference 0.9V for DDR2.
VDD_REF_EPHY	120	AO	Voltage Reference 0.6V for Ethernet PHY. 2.5K ohm 1% resister pull down

Pin Name	Pin No.	Type	Description
Power & GND			
VDD33_IO	26, 29	P	Digital I/O Power Supply 3.3V.
VDD25_18_DDRIO	40, 105, 107, 109, 49	P	Memory I/O Power Supply 2.5V, or 1.8V. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
VDD33_25_MII	6, 13	P	GMII/RGMII/MII Interface Power Supply 3.3V/2.5V .
VDD33_SD30	84	P	SD Power supply 3.3V
VDD1P05	60, 111, 45, 103, 97, 94, 14, 83	P	Digital Core Power Supply 1.05V.
AVDD33_EPHY	121, 72, 5	AP	Ethernet Analog Power Supply 3.3V.
AVDD1P05_EPHY	76, 127, 65, 62	AP	Ethernet Analog Power Supply 1.05V.
AVDD33_BG	61	AP	System Bandgap Power Supply 3.3V.
AVDD1P05_PCIE	56	AP	PCI Express Analog Power Supply 1.05V.
AVDD1P05_PLL	119	AP	PLL Power 1.05V.
AVDD33_USB	118	AP	USB 2.0 Analog Power 3.3V.
AVDD1P05_USB	115	AP	USB 2.0 Analog Power 1.05V.
AVDD33_DDRPLL	112	AP	DDR PLL Analog Power 3.3V
AVDD1P05_DDRPLL	50	AP or NC	DDR PLL Analog Power 1.05V Mode 1(NC): NC, using internal LDO (3.3V->1.05V) Mode 2(AP): input power
GND	E-PAD	G	System GND.
AGND_SPS_DDR	31	AG	Internal SWR_DDR GND
AGND_SPS	35, 36	AG	Internal SWR GND
AGND_USB	58	AG	USB GND.
Internal SWR & LDO			
AVDD33_SPS_DDR	32	AP	Internal SWR_DDR Power Supply 3.3V Input for DDR.
AVDD25_18_SPS_DDR	98	AP (O)	Internal SWR_DDR Output Power for DDR. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
AVDD33_SPS	99, 33	AP	Internal SWR Power Supply 3.3V Input
AVDD1P05_SPS	100, 34	AP (O)	Internal SWR Power Supply 1.05V Output
ENSWR	37	I	Internal SWR Power Supply Output Voltage enable/disable 0: Disable internal SWR 1: Enable internal SWR Note: If using external SWR/LDO, this pin must tie low.
RF & RF Power			
AVDD1P05_AFE	85	AP	Analog 1.05V power supply
AVDD33_X	86	AP	Analog 3.3V power supply
AVDD33_SYN	17	AP	RF 3.3V power supply
AVDD1P05_SYN	18	AP	RF 1.05V power supply
VTSSI_EXT_S0	19	AI	S0_TSSI voltage input
RFIP_S0	20	AI/O	S0 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIN_S0	87	AI/O	

Pin Name	Pin No.	Type	Description
AVDD33_RTX_S0	21	AP	RF 3.3V power supply
RXIO_S0	88	AI	S0 RX LNA input port
AVDD1P05_RTX_S0	22	AP	RF 1.05V power supply
VTSSI_EXT_S1	89	AI	S1 TSSI voltage input
AVDD1P05_RTX_S1	23	AP	RF 1.05V power supply
RXIO_S1	90	AI	S1 RX LNA input port
AVDD33_RTX_S1	24	AP	RF 3.3V power supply
RFIN_S1	91	AI/O	S1 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIP_S1	25	AI/O	
Not Connected Pins			
NC	1, 55	-	Not Connected. Must keep these pin floating .

6.10. Configuration Upon Power On Strapping (RTL8197FH)

The 1.05V digital core power input pin voltage is up to 0.7V on system power-on. The strap data will be latched after a delay of 160/100 ms.

25MHz XTAL: 160 ms
40MHz XTAL: 100 ms

Table 17. Configuration Upon Power On Strapping (RTL8197FH)

H/W Pin Name	Configuration Name	Pin No	Description
WBB4	Boot_select[0]	108	boot_select[3:0]: 0000: SPI-NOR-Flash booting (3 byte addressing) 0001: [ROM] SPI-NOR-Flashing (3 byte addressing) 0010: [ROM] SPI-NAND-Flash booting 0011: 0100: 0101: 0110: 0111: 1000: [ROM] Switch booting (Image to DRAM) 1001: 1010: 1011: 1100: 1101: [ROM] Switch booting (Image to SPI-Nor Flash) 1110: SPI-NOR-Flash booting for OLT (3 byte addressing) 1111: loop mode for debug
WBB7	Boot_select[1]	93	
WBB8	Boot_select[2]	27	
P0_TXD3	Boot_select[3]	77	
MF_CS0N	DRAM_TYPE_INV	41	DRAM_TYPE_INV Select: (Referenced by SW) 0: DDR2 1: DDR1
U0_TX	DRAM_FEQ	101	DRAM_FEQ Selection: (Only Referenced by SW) 0: DDR2_400MHz, DDR1_200MHz 1: DDR2_533MHz, DDR1_250MHz
P0_TXCTL	HW_DBG_DISABLE	79	WiFi Debug mode / Enable strap_ctl_sys_dbg_sel 0: Enable 1: Disable
P0_TXD2	ddr_ldo_Sel	7	DDR Power regulator selection: 0: SWR 1: LDO
P0_TXD1	Disable_Load_Efuse_Value	78	Load Efuse Select: (Referenced by SW) 0: enable Load Efuse 1: disable Load Efuse
P0_TXD0	DISABLE_EXT_RSTN	8	External Reset Select: 0: enable 1: disable

H/W Pin Name	Configuration Name	Pin No	Description
MF_CK	sel_40m	96	System Clock Source Select. 0: 25M 1: 40M
PCIE_RSTN	strap_test_mode	44	Chip Test Mode Select. 0: normal_mode 1: TEST_MODE (CP/FT/SCAN)

6.11. Shared I/O Pin Mapping (RTL8197FH)

Table 18. Shared I/O Pin Mapping – RTL8197FH

Pin	GPIO		WiFi / PCM	RGMII/MII	I2S	SPI-Nor / SD/ eMMC	EJTAG/ SPI-Nand	LED/SPI	UART	I2C, Reset
96	GPIOA[0]	O				MF_CK	SPI_NAND_CK	SPI0_CLK		I2C0_SCL
102	GPIOA[1]	B				MF_D0	SPI_NAND_D0	SPI0_TXD		I2C0_SDA
30	GPIOA[2]	B				MF_D1	SPI_NAND_D1	SPI0_RXD, SPI0_TRXD		I2C1_SCL / I2C1_SCL_SLV
39	GPIOA[3]	B				MF_RSTN	SPI_NAND_D2	SPI0_CS0N		I2C1_SDA / I2C1_SDA_SLV
41	GPIOA[4]	O				MF_CS0N	SPI_NAND_CS0N			I2C1_SCL
	~~GPIOA[5]~~									
77	GPIOA[6]	O		P0_TXD3	I2S_MCLK			SPI0_CLK		
7	GPIOA[7]	O		P0_TXD2	I2S_SCLK			SPI0_CS0N		
78	GPIOB[0]	O		P0_TXD1	I2S_WS / I2S_SD2_O			SPI0_TXD		I2C1_SCL
80	GPIOB[1]	B		P0_RXC	I2S_SD1_O / I2S_SD1_I / I2S_SD3_O		JTAG_TCK	SPI0_RXD, SPI0_TRXD		I2C1_SDA
12	GPIOB[2]	B	PCM_CLK	P0_RXD3	I2S_MCLK		JTAG_TRSTN	SPI0_TXD_SLV	U2_RTS	
82	GPIOB[3]	B	PCM_FS	P0_RXD2	I2S_SCLK		JTAG_TMS	SPI0_RXD_SLV	U2_TX	
11	GPIOB[4]	B	PCM_TXD	P0_RXD1	I2S_WS		JTAG_TDI	SPI0_CLK_SLV	U2_RX	
81	GPIOB[5]	B	PCM_RXD	P0_RXD0	I2S_SD1_O			SPI0_CS0N_SLV	U2_CTS	
8	GPIOB[6]	O		P0_TXD0			JTAG_TDO	SPI1_CLK	U1_RTS	I2C1_SCL
9	GPIOB[7]	B		P0_TXC	I2S_SD1_I			SPI1_CS0N	U1_RX	I2C1_SDA / I2C0_SCL_SLV
79	GPIOC[0]	O		P0_TXCTL				SPI1_TXD	U1_TX	I2C0_SCL
10	GPIOC[1]	B		P0_RXCTL				SPI1_RXD, SPI1_TRXD	U1_CTS	I2C0_SDA / I2C0_SDA_SLV
	~~GPIOC[2]~~									
48	GPIOC[3]	B		P0_MDIO_GPIO				SPI0_CS0N, SPI1_CS0N		
	~~GPIOC[4]~~									
	~~GPIOC[5]~~									
	~~GPIOC[6]~~									
	~~GPIOC[7]~~									
	~~GPIOD[0]~~									

Pin	GPIO		WiFi / PCM	RGMII/MII	I2S	SPI-Nor / SD/ eMMC	EJTAG/ SPI-Nand	LED/SPI	UART	I2C, Reset
	~~GPIOD[1]~~									
	~~GPIOD[2]~~									
	~~GPIOD[3]~~									
	~~GPIOD[4]~~									
	~~GPIOD[5]~~									
	~~GPIOD[6]~~									
	~~GPIOD[7]~~									
	~~GPIOE[0]~~									
47	GPIOE[1]	B	WBB0							
92	GPIOE[2]	B	WBB1							
46	GPIOE[3]	B	WBB2							
110	GPIOE[4]	B	WBB3							
108	GPIOE[5]	O	WBB4							
	~~GPIOE[6]~~		~~WBB_5~~							
	~~GPIOE[7]~~		~~WBB_6~~							
93	GPIOF[0]	O	WBB7							
27	GPIOF[1]	O	WBB8							
	~~GPIOF[2]~~									
	~~GPIOF[3]~~									
	~~GPIOF[4]~~									
	~~GPIOF[5]~~									
	~~GPIOF[6]~~									
	~~GPIOF[7]~~									
	~~GPIOG[0]~~									
	~~GPIOG[1]~~									
	~~GPIOG[2]~~									
	~~GPIOG[3]~~									
	~~GPIOG[4]~~									
	~~GPIOG[5]~~									
95	GPIOG[6]	B		P0_MDC_GPIO				LED_PORT0		
43	GPIOG[7]	B						LED_PORT1		
28	GPIOH[0]	B						LED_PORT2		
106	GPIOH[1]	B						LED_PORT3		RESETN
42	GPIOH[2]	B						LED_PORT4		
38	GPIOH[3]	B							U0_RX	
101	GPIOH[4]	O							U0_TX	
44	GPIOH[5]	O								PCIE_RSTN

6.12. GPIO Pin During Boot State (RTL8197FH)

Table 19. GPIO Pin During Boot State – RTL8197FH

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
96	GPIOA[0]	I	O	Y	internal pull-down only in strap period
102	GPIOA[1]	I	B		internal pull-up
30	GPIOA[2]	I	B		internal pull-up
39	GPIOA[3]	I	B		internal pull-up
41	GPIOA[4]	I	O	Y	internal pull-down only in strap period
	~~GPIOA[5]~~				
77	GPIOA[6]	O	O	Y	internal pull-down only in strap period
7	GPIOA[7]	O	O	Y	internal pull-up only in strap period
78	GPIOB[0]	O	O	Y	internal pull-down only in strap period
80	GPIOB[1]	I	B		internal pull-up
12	GPIOB[2]	I	B		internal pull-up
82	GPIOB[3]	I	B		internal pull-up
11	GPIOB[4]	I	B		internal pull-up
81	GPIOB[5]	I	B		internal pull-up
8	GPIOB[6]	O	O	Y	internal pull-down only in strap period
9	GPIOB[7]	B	B		internal pull-up
79	GPIOC[0]	O	O	Y	internal pull-down only in strap period
10	GPIOC[1]	I	B		internal pull-up
	~~GPIOC[2]~~				
48	GPIOC[3]	B	B		internal pull-up
	~~GPIOC[4]~~				
	~~GPIOC[5]~~				
	~~GPIOC[6]~~				
	~~GPIOC[7]~~				
	~~GPIOD[0]~~				
	~~GPIOD[1]~~				
	~~GPIOD[2]~~				
	~~GPIOD[3]~~				
	~~GPIOD[4]~~				
	~~GPIOD[5]~~				
	~~GPIOD[6]~~				
	~~GPIOD[7]~~				
	~~GPIOE[0]~~				
47	GPIOE[1]	O	B		internal pull-down
92	GPIOE[2]	B	B		internal pull-down
46	GPIOE[3]	B	B		internal pull-down
110	GPIOE[4]	B	B		internal pull-down

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
108	GPIOE[5]	O	O	Y	internal pull-down
	~~GPIOE[6]~~				
	~~GPIOE[7]~~				
93	GPIOF[0]	O	O	Y	internal pull-down
27	GPIOF[1]	O	O	Y	internal pull-down
	~~GPIOF[2]~~				
	~~GPIOF[3]~~				
	~~GPIOF[4]~~				
	~~GPIOF[5]~~				
	~~GPIOF[6]~~				
	~~GPIOF[7]~~				
	~~GPIOG[0]~~				
	~~GPIOG[1]~~				
	~~GPIOG[2]~~				
	~~GPIOG[3]~~				
	~~GPIOG[4]~~				
	~~GPIOG[5]~~				
95	GPIOG[6]	O	B		internal pull-down
43	GPIOG[7]	O	B		internal pull-down
28	GPIOH[0]	O	B		internal pull-down
106	GPIOH[1]	O	B		internal pull-down
42	GPIOH[2]	O	B		internal pull-down
38	GPIOH[3]	I	B		internal pull-up
101	GPIOH[4]	O	O	Y	internal pull-up only in strap period
44	GPIOH[5]	O	O	Y	internal pull-down only in strap period

6.13. Pin Descriptions (RTL8197FS)

Table 20. Pin Descriptions – RTL8197FS DRQFN-128

Pin Name	Pin No.	Type	Description
Clock & Reset			
XI	16	I	25/40MHz External Clock Input.
XO	15	O	25/40MHz Crystal Clock Output.
10/100M Ethernet Physical Layer			
TXOP_P[4] TXON_P[4]	TXOP_P4: 122 TXON_P4: 64	AO	10/100M Ethernet Physical Layer Transmit Pair. For differential data transmission.
RXIP_P[4] RXIN_P[4]	RXIP_P4: 123 RXIN_P4: 65	AI	10/100M Ethernet Physical Layer Receive Pair. For differential data reception.
Ethernet MAC RGMII/MII Interface			
P0_MDC	77	O	Management Data Clock.
P0_MDIO	48	I_{PU}/O	Management Data I/O.
P0_TXC	73	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
P0_TXCTL	2	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_TXD[3:0]	P0_TXD0: 71 P0_TXD1: 70 P0_TXD2: 128 P0_TXD3: 66	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXC	3	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXCTL	74	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
P0_RXD[3:0]	P0_RXD0: 4 P0_RXD1: 75 P0_RXD2: 5 P0_RXD3: 76	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
eMMC Interface			
EMMC_CLK	10	O	eMMC Clock Output
EMMC_CMD	11	B	eMMC Command

Pin Name	Pin No.	Type	Description
EMMC_DAT[7:0]	EMMC_DAT0: 8 EMMC_DAT1: 78 EMMC_DAT2: 83 EMMC_DAT3: 12 EMMC_DAT4: 82 EMMC_DAT5: 81 EMMC_DAT6: 9 EMMC_DAT7: 79	B	eMMC Data Input/Output
EMMC_RSTN	127	O	eMMC Reset
SD Interface (Partial Share Pin)			
SD_CLK	EMMC_CLK	O	SD Clock Output
SD_CMD	EMMC_CMD	B	SD Command
SD_DAT[3:0]	EMMC_DAT[3:0]	B	SD Data Input/Output
SD_CTRL_PWR	EMMC_RSTN	O	Enable/Disable power supply to SD card
SD_WP	67	I	SD Write Protection
SD_CD	69	I	SD Card Detection
Serial SPI-Nor Flash Control			
MF_CS1N	30	O	SPI Serial Flash Chip Select 1.
MF_CS0N	41	O	SPI Serial Flash Chip Select 0.
MF_RSTN	39	O	SPI Serial Flash Reset
MF_D[1:0]	MF_D0: 102 MF_D1: 96	I/O	SPI Serial Flash Serial Data Input/Output.
MF_CK	29	O	SPI Serial Flash Serial Clock Output.
Serial SPI-Nand Flash Control (Share Pin)			
SPI_NAND_CK	MF_CK	O	SPI Nand Flash Clock Output
SPI_NAND_D[2:0]	SPI_NAND_D0: MF_D0 SPI_NAND_D1: MF_D1 SPI_NAND_D2: MF_RSTN	I/O	SPI Nand Flash Data Input/Output
SPI_NAND_CS0N	MF_CS0N	O	SPI Nand Flash Chip Select 0
SPI_NAND_D[3]	MF_CS1N	I/O	SPI Nand Flash Data Input/Output
Parallel P-Nand Flash Control (Share Pin)			
NF_D[7:0]	NF_D0: P0_RXD3 NF_D1: P0_RXD2 NF_D2: P0_RXD1 NF_D3: P0_RXD0 NF_D4: EMMC_DAT0 NF_D5: EMMC_DAT1 NF_D6: EMMC_DAT2 NF_D7: EMMC_DAT3	I/O	Data Input/Output for P-NAND Flash.
NF_CLE	P0_TXD2	O	P-NAND Flash Command Latch Enable.
NF_ALE	P0_TXD3	O	P-NAND Flash Address Latch Enable.
NF_CE0#	P0_RXC	O	P-NAND Flash Chip Enable.
NF_RD#	P0_TXD1	O	P-NAND Flash Read Enable.
NF_WE#	P0_TXCTL	O	P-NAND Flash Write Enable.

Pin Name	Pin No.	Type	Description
NF_WP#	P0_TXD0	O	P-NAND Flash Write Protect.
NF_R/B#	P0_RXCTL	I	P-NAND Flash Ready/Busy Input.
UART			
U0_TX	101	O	Data Transmit Serial Output of UART0.
U0_RX	38	I_{PU}	Data Receive Serial Input of UART0.
UART (Full) (Share Pin)			
U1_TX	P0_TXCTL, EMMC_DAT3, P0_MDIO	O	Data Transmit Serial Output of UART1.
U1_RX	P0_TXC, SD_WP, EMMC_DAT0	I_{PU}	Data Receive Serial Input of UART1.
U1_RTS	P0_TXD0, EMMC_DAT2, P0_MDC	O	Request To Send of UART1.
U1_CTS	P0_RXCTL, SD_CD, EMMC_DAT1	I	Clear To Send of UART1.
U2_TX	P0_RXD2, EMMC_DAT3	O	Data Transmit Serial Output of UART2.
U2_RX	P0_RXD1, EMMC_DAT0	I_{PU}	Data Receive Serial Input of UART2.
U2_RTS	P0_RXD3, EMMC_DAT2	O	Request To Send of UART2.
U2_CTS	P0_RXD0, EMMC_DAT1	I	Clear To Send of UART2.
SPI (4-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3, P0_MDC, EMMC_CLK	O	SPI0 Clock output
SPI0_TXD	MF_D0, P0_TXD1, SD_WP	O	SPI0 Data Transmit
SPI0_RXD	MF_D1, P0_RXC, SD_CD	I	SPI0 Data Receive
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO, EMMC_CMD	O	SPI0 Chip Select 0
SPI0_CS1N	EMMC_RSTN	O	SPI0 Chip Select 1

Pin Name	Pin No.	Type	Description
SPI1_CLK	P0_TXD0, P0_MDC, EMMC_CLK, EMMC_DAT4	O	SPI1 Clock output
SPI1_TXD	P0_TXCTL, SD_WP, EMMC_DAT6	O	SPI1 Data Transmit
SPI1_RXD	P0_RXCTL, SD_CD, EMMC_DAT7	I	SPI1 Data Receive
SPI1_CS0N	P0_TXC, P0_MDIO, EMMC_CMD, EMMC_DAT5	O	SPI1 Chip Select 0
SPI (3-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3, P0_MDC, EMMC_CLK	O	SPI0 Clock output
SPI0_TRXD	MF_D1, P0_RXC, SD_CD	I/O	SPI0 Data Transmit/Receive
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO, EMMC_CMD	O	SPI0 Chip Select 0
SPI0_CS1N	EMMC_RSTN	O	SPI0 Chip Select 1
SPI1_CLK	P0_TXD0, P0_MDC, EMMC_CLK, EMMC_DAT4	O	SPI1 Clock output
SPI1_TRXD	P0_RXCTL, SD_CD, EMMC_DAT7	I/O	SPI1 Data Transmit/Receive
SPI1_CS0N	P0_TXC, P0_MDIO, EMMC_CMD, EMMC_DAT5	O	SPI1 Chip Select 0
SPI (4-Wire Slave mode) (Share Pin)			
SPI0_CLK_SLV	P0_RXD1	I	SPI0 Slave Mode Clock Input
SPI0_TXD_SLV	P0_RXD3	O	SPI0 Slave Mode Data Transmit
SPI0_RXD_SLV	P0_RXD2	I	SPI0 Slave Mode Data Receive
SPI0_CS0N_SLV	P0_RXD0	I	SPI0 Slave Mode Chip Select 0 Input
PCM (Master Mode) (Share Pin)			
PCM_CLK	P0_RXD3, EMMC_DAT4	O	PCM Master Mode Clock Output
PCM_FS	P0_RXD2, EMMC_DAT5	O	PCM Master Mode Frame Sync

Pin Name	Pin No.	Type	Description
PCM_TXD	P0_RXD1, EMMC_DAT6	O	PCM Master Mode Data Transmit
PCM_RXD	P0_RXD0, EMMC_DAT7	I	PCM Master Mode Data Receive
JTAG (Share Pin)			
JTAG_TCK	P0_RXC	I_{PU}	JTAG Test Clock.
JTAG_TMS	P0_RXD2	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	P0_TXD0	O	JTAG Test Data Output.
JTAG_TDI	P0_RXD1	I_{PU}	JTAG Test Data In.
JTAG_TRSTN	P0_RXD3	I_{PU}	JTAG Test Reset.
I2C (Share Pin)			
I2C0_SCL	MF_CK, P0_TXCTL	B	I2C0 Serial Clock Line
I2C0_SDA	MF_D0, P0_RXCTL	B	I2C0 Serial Data Line
I2C1_SCL	MF_D1, MF_CS0N, P0_TXD1, P0_TXD0	B	I2C1 Serial Clock Line
I2C1_SDA	MF_RSTN, P0_RXC, P0_TXC	B	I2C1 Serial Data Line
I2C0_SCL_SLV	P0_TXC	B	I2C0 Slave Serial Clock Line
I2C0_SDA_SLV	P0_RXCTL	B	I2C0 Slave Serial Data Line
I2C1_SCL_SLV	MF_D1	B	I2C1 Slave Serial Clock Line
I2C1_SDA_SLV	MF_RSTN	B	I2C1 Slave Serial Data Line
LED			
LED_PORT[0] LED_PORT[4:2]	LED_PORT0: 43 LED_PORT2: 28 LED_PORT3: 106 LED_PORT4: 42	O	Link or Link/Speed Status (Low Active).
WiFi Digital			
WBB0	47	O	LED for Wlan TRX
WBB[4:1]	WBB1: 92 WBB2: 46 WBB3: 110 WBB4: 108	I/O	Reserved for external RF component control or Wireless Coexistence interface
WBB[8:7]	WBB7: 93 WBB8: 27	I/O	Reserved for external RF component control or Wireless Coexistence interface
GPIO			
-	-	I/O	-
USB Host 2.0 / OTG			
USB_HSDP0	116	AI/O	USB Port0 Host Device Data Plus Pin.
USB_HSDM0	57	AI/O	USB Port0 Host Device Data Minus Pin.
USB_HSDP1	59	AI/O	USB Port1 Host Device Data Plus Pin.
USB_HSDM1	117	AI/O	USB Port1 Host Device Data Minus Pin.

Pin Name	Pin No.	Type	Description
PCI Express Interface			
PCIE_HSON PCIE_HSOP	51, 113	AO	Transmitter Differential Pair.
PCIE_HSIN PCIE_HSIP	54, 53	AI	Receiver Differential Pair.
PCIE_REFCLK_M PCIE_REFCLK_P	52, 114	AO	Reference Clock Differential Pair.
PCIE_RSTN	44	O	PCI Express Reset.
Reference Voltage			
VDD_REF_DDR	104	AI	Voltage Reference 1.25V for DDR1. Voltage Reference 0.9V for DDR2.
VDD_REF_EPHY	120	AO	Voltage Reference 0.6V for Ethernet PHY. 2.5K ohm 1% resister pull down
Power & GND			
VDD33_IO	26, 95	P	Digital I/O Power Supply 3.3V.
VDD25_18_DDRIO	40, 105, 107, 109, 49	P	Memory I/O Power Supply 2.5V, or 1.8V. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
VDD33_25_MII	6, 13, 125	P	GMII/RGMII/MII Interface Power Supply 3.3V/2.5V .
VDD33_SD30	84	P	SD Power supply 3.3V
VDD33_18_SD30	80	P (O)	SD IO Output Power 3.3V/1.8V
VDD1P05	7, 14, 94, 97, 103, 45, 111, 60	P	Digital Core Power Supply 1.05V.
AVDD33_EPHY	121, 72	AP	Ethernet Analog Power Supply 3.3V.
AVDD1P05_EPHY	62, 63	AP	Ethernet Analog Power Supply 1.05V.
AVDD33_BG	61	AP	System Bandgap Power Supply 3.3V.
AVDD1P05_PCIE	56	AP	PCI Express Analog Power Supply 1.05V.
AVDD1P05_PLL	119	AP	PLL Power 1.05V.
AVDD33_USB	118	AP	USB 2.0 Analog Power 3.3V.
AVDD1P05_USB	115	AP	USB 2.0 Analog Power 1.05V.
AVDD33_DDRPLL	112	AP	DDR PLL Analog Power 3.3V
AVDD1P05_DDRPLL	50	AP or NC	DDR PLL Analog Power 1.05V Mode 1(NC): NC, using internal LDO (3.3V->1.05V) Mode 2(AP): input power
GND	E-PAD	G	System GND.
AGND_SPS_DDR	31	AG	Internal SWR_DDR GND
AGND_SPS	35, 36	AG	Internal SWR GND
AGND_USB	58	AG	USB GND.
Internal SWR & LDO			
AVDD33_SPS_DDR	32	AP	Internal SWR_DDR Power Supply 3.3V Input for DDR.
AVDD25_18_SPS_DDR	98	AP (O)	Internal SWR_DDR Output Power for DDR. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
AVDD33_SPS	99, 33	AP	Internal SWR Power Supply 3.3V Input

Pin Name	Pin No.	Type	Description
AVDD1P05_SPS	100, 34	AP (O)	Internal SWR Power Supply 1.05V Output
ENSWR	37	I	Internal SWR Power Supply Output Voltage enable/disable 0: Disable internal SWR 1: Enable internal SWR Note: If using external SWR/LDO, this pin must tie low.
RF & RF Power			
AVDD1P05_AFE	85	AP	Analog 1.05V power supply
AVDD33_X	86	AP	Analog 3.3V power supply
AVDD33_SYN	17	AP	RF 3.3V power supply
AVDD1P05_SYN	18	AP	RF 1.05V power supply
VTSSI_EXT_S0	19	AI	S0_TSSI voltage input
RFIP_S0	20	AI/O	S0 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIN_S0	87	AI/O	
AVDD33_RTX_S0	21	AP	RF 3.3V power supply
RXIO_S0	88	AI	S0 RX LNA input port
AVDD1P05_RTX_S0	22	AP	RF 1.05V power supply
VTSSI_EXT_S1	89	AI	S1 TSSI voltage input
AVDD1P05_RTX_S1	23	AP	RF 1.05V power supply
RXIO_S1	90	AI	S1 RX LNA input port
AVDD33_RTX_S1	24	AP	RF 3.3V power supply
RFIN_S1	91	AI/O	S1 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIP_S1	25	AI/O	
Not Connected Pins			
NC	1, 55, 124, 126, 68	-	Not Connected. Must keep these pin floating .

6.14. Configuration Upon Power On Strapping (RTL8197FS)

The 1.05V digital core power input pin voltage is up to 0.7V on system power-on. The strap data will be latched after a delay of 160/100 ms.

25MHz XTAL: 160 ms
40MHz XTAL: 100 ms

Table 21. Configuration Upon Power On Strapping (RTL8197FS DRQFN-128)

H/W Pin Name	Configuration Name	Pin No	Description
WBB4	Boot_select[0]	108	boot_select[3:0]: 0000: SPI-NOR-Flash booting (3 byte addressing) 0001: [ROM] SPI-NOR-Flashing (3 byte addressing) 0010: [ROM] SPI-NAND-Flash booting 0011: [ROM] Parallel-NAND-Flash booting 0100: [ROM] eMMC 1.8V booting 0101: [ROM] SD booting 0110: 0111: 1000: [ROM] Switch booting (Image to DRAM) 1001: 1010: 1011: 1100: [ROM] eMMC 3.3V booting 1101: [ROM] Switch booting (Image to SPI-Nor Flash) 1110: SPI-NOR-Flash booting for OLT (3 byte addressing) 1111: loop mode for debug
WBB7	Boot_select[1]	93	
WBB8	Boot_select[2]	27	
P0_TXD3	Boot_select[3]	66	
MF_CS0N	DRAM_TYPE_INV	41	DRAM_TYPE_INV Select: (Referenced by SW) 0: DDR2 1: DDR1
U0_TX	DRAM_FEQ	101	DRAM_FEQ Selection: (Only Referenced by SW) 0: DDR2_400MHz, DDR1_200MHz 1: DDR2_533MHz, DDR1_250MHz
P0_TXCTL	HW_DBG_DISABLE	2	WiFi Debug mode / Enable strap_ctl_sys_dbg_sel 0: Enable 1: Disable
P0_TXD2	ddr_ldo_Sel	128	DDR Power regulator selection: 0: SWR 1: LDO
P0_TXD1	Disable_Load_Efuse_Value	70	Load Efuse Select: (Referenced by SW) 0: enable Load Efuse 1: disable Load Efuse
P0_TXD0	DISABLE_EXT_RSTN	71	External Reset Select: 0: enable 1: disable

H/W Pin Name	Configuration Name	Pin No	Description
EMMC_RSTN	SWITCH_PHY_SEL	127	Switch PHY Select: 0: External PHY 1: Embedded PHY
MF_CK	sel_40m	29	System Clock Source Select: 0: 25M 1: 40M
PCIE_RSTN	strap_test_mode	44	Chip Test Mode Select: 0: normal_mode 1: TEST_MODE (CP/FT/SCAN)

6.15. Shared I/O Pin Mapping (RTL8197FS)

Table 22. Shared I/O Pin Mapping (RTL8197FS DRQFN-128)

Pin	GPIO		WiFi / PCM	RGMII/MII	P-Nand	I2S	SPI-Nor / SD/ eMMC	EJTAG / SPI-Nand	LED / SPI	UART	I2C/ Reset
29	GPIOA[0]	O					MF_CK	SPI_NAND_CK	SPI0_CLK		I2C0_SCL
102	GPIOA[1]	B					MF_D0	SPI_NAND_D0	SPI0_TXD		I2C0_SDA
96	GPIOA[2]	B					MF_D1	SPI_NAND_D1	SPI0_RXD, SPI0_TRXD		I2C1_SCL / I2C1_SCL_SLV
39	GPIOA[3]	B					MF_RSTN	SPI_NAND_D2	SPI0_CS0N		I2C1_SDA / I2C1_SDA_SLV
41	GPIOA[4]	O					MF_CS0N	SPI_NAND_CS0N			I2C1_SCL
30	GPIOA[5]	B				I2S_SD3_O	MF_CS1N	SPI_NAND_D3			I2C1_SDA
66	GPIOA[6]	O		P0_TXD3	NF_ALE	I2S_MCLK			SPI0_CLK		
128	GPIOA[7]	O		P0_TXD2	NF_CLE	I2S_SCLK			SPI0_CS0N		
70	GPIOB[0]	O		P0_TXD1	NF_RD#	I2S_WS / I2S_SD2_O			SPI0_TXD		I2C1_SCL
3	GPIOB[1]	B		P0_RXC	NF_CE0#	I2S_SD1_O / I2S_SD1_I / I2S_SD3_O		JTAG_TCK	SPI0_RXD, SPI0_TRXD		I2C1_SDA
76	GPIOB[2]	B	PCM_CLK	P0_RXD3	NF_D0	I2S_MCLK		JTAG_TRSTN	SPI0_TXD_SLV	U2_RTS	
5	GPIOB[3]	B	PCM_FS	P0_RXD2	NF_D1	I2S_SCLK		JTAG_TMS	SPI0_RXD_SLV	U2_TX	
75	GPIOB[4]	B	PCM_TXD	P0_RXD1	NF_D2	I2S_WS		JTAG_TDI	SPI0_CLK_SLV	U2_RX	
4	GPIOB[5]	B	PCM_RXD	P0_RXD0	NF_D3	I2S_SD1_O			SPI0_CS0N_SLV	U2_CTS	
71	GPIOB[6]	O		P0_TXD0	NF_WP#			JTAG_TDO	SPI1_CLK	U1_RTS	I2C1_SCL
73	GPIOB[7]	B		P0_TXC		I2S_SD1_I			SPI1_CS0N	U1_RX	I2C1_SDA / I2C0_SCL_SLV
2	GPIOC[0]	O		P0_TXCTL	NF_WE#				SPI1_TXD	U1_TX	I2C0_SCL
74	GPIOC[1]	B		P0_RXCTL	NF_R/B#				SPI1_RXD, SPI1_TRXD	U1_CTS	I2C0_SDA / I2C0_SDA_SLV
77	GPIOC[2]	B		P0_MDC					SPI0_CLK, SPI1_CLK	U1_RTS	I2C0_SCL / I2C1_SCL
48	GPIOC[3]	B		P0_MDIO					SPI0_CS0N, SPI1_CS0N	U1_TX	I2C0_SDA / I2C1_SDA
127	GPIOC[4]	O					EMMC_RSTN		SPI0_CS1N		
67	GPIOC[5]	B				I2S_WS	SD_WP		SPI0_TXD, SPI1_TXD	U1_RX	
69	GPIOC[6]	B				I2S_SCLK	SD_CD		SPI0_RXD, SPI0_TRXD SPI1_RXD, SPI1_TRXD	U1_CTS	
10	GPIOC[7]	B				I2S_MCLK	EMMC_CLK		SPI0_CLK, SPI1_CLK		
11	GPIOD[0]	B				I2S_SD1_O	EMMC_CMD		SPI0_CS0N, SPI1_CS0N		
8	GPIOD[1]	B			NF_D4	I2S_WS	EMMC_DAT0			U1_RX / U2_RX	
78	GPIOD[2]	B			NF_D5	I2S_SCLK	EMMC_DAT1			U1_CTS / U2_CTS	

Pin	GPIO		WiFi / PCM	RGMII/MII	P-Nand	I2S	SPI-Nor / SD/ eMMC	EJTAG / SPI-Nand	LED / SPI	UART	I2C/ Reset
83	GPIOD[3]	B			NF_D6	I2S_MCLK	EMMC_DAT2			U1_RTS / U2_RTS	
12	GPIOD[4]	B			NF_D7	I2S_SD1_O	EMMC_DAT3			U1_TX / U2_TX	
82	GPIOD[5]	B	PCM_CLK				EMMC_DAT4		SPI1_CLK		
81	GPIOD[6]	B	PCM_FS				EMMC_DAT5		SPI1_CS0N		
9	GPIOD[7]	B	PCM_TXD				EMMC_DAT6		SPI1_TXD		
79	GPIOE[0]	B	PCM_RXD				EMMC_DAT7		SPI1_RXD, SPI1_TRXD		
47	GPIOE[1]	B	WBB0								
92	GPIOE[2]	B	WBB1								
46	GPIOE[3]	B	WBB2								
110	GPIOE[4]	B	WBB3								
108	GPIOE[5]	O	WBB4								
	~~GPIOE[6]~~		~~WBB5~~								
	~~GPIOE[7]~~		~~WBB6~~								
93	GPIOF[0]	O	WBB7								
27	GPIOF[1]	O	WBB8								
	~~GPIOF[2]~~										
	~~GPIOF[3]~~										
	~~GPIOF[4]~~										
	~~GPIOF[5]~~										
	~~GPIOF[6]~~										
	~~GPIOF[7]~~										
	~~GPIOG[0]~~										
	~~GPIOG[1]~~										
	~~GPIOG[2]~~										
	~~GPIOG[3]~~										
	~~GPIOG[4]~~										
	~~GPIOG[5]~~										
43	GPIOG[6]	B							LED_PORT0		
	~~GPIOG[7]~~								~~LED_PORT1~~		
28	GPIOH[0]	B							LED_PORT2		
106	GPIOH[1]	B							LED_PORT3		RESETN
42	GPIOH[2]	B							LED_PORT4		
38	GPIOH[3]	B								U0_RX	
101	GPIOH[4]	O								U0_TX	
44	GPIOH[5]	O									PCIE_RSTN

6.16. GPIO Pin During Boot State (RTL8197FS)

Table 23. GPIO Pin During Boot State - RTL8197FS

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
29	GPIOA[0]	I	O	Y	internal pull-down only in strap period
102	GPIOA[1]	I	B		internal pull-up
96	GPIOA[2]	I	B		internal pull-up
39	GPIOA[3]	I	B		internal pull-up
41	GPIOA[4]	I	O	Y	internal pull-down only in strap period
30	GPIOA[5]	I	B		internal pull-up
66	GPIOA[6]	O	O	Y	internal pull-down only in strap period
128	GPIOA[7]	O	O	Y	internal pull-up only in strap period
70	GPIOB[0]	O	O	Y	internal pull-down only in strap period
3	GPIOB[1]	I	B		internal pull-up
76	GPIOB[2]	I	B		internal pull-up
5	GPIOB[3]	I	B		internal pull-up
75	GPIOB[4]	I	B		internal pull-up
4	GPIOB[5]	I	B		internal pull-up
71	GPIOB[6]	O	O	Y	internal pull-down only in strap period
73	GPIOB[7]	B	B		internal pull-up
2	GPIOC[0]	O	O	Y	internal pull-down only in strap period
74	GPIOC[1]	I	B		internal pull-up
77	GPIOC[2]	I	B		internal pull-up
48	GPIOC[3]	B	B		internal pull-up
127	GPIOC[4]	O	O	Y	internal pull-up only in strap period
67	GPIOC[5]	I	B		internal pull-up
69	GPIOC[6]	I	B		internal pull-up
10	GPIOC[7]	O	B		
11	GPIOD[0]	B	B		internal pull-up
8	GPIOD[1]	B	B		internal pull-up
78	GPIOD[2]	B	B		internal pull-up
83	GPIOD[3]	B	B		internal pull-up
12	GPIOD[4]	B	B		internal pull-up
82	GPIOD[5]	B	B		internal pull-up
81	GPIOD[6]	B	B		internal pull-up
9	GPIOD[7]	B	B		internal pull-up
79	GPIOE[0]	B	B		internal pull-up
47	GPIOE[1]	O	B		internal pull-down
92	GPIOE[2]	B	B		internal pull-down
46	GPIOE[3]	B	B		internal pull-down
110	GPIOE[4]	B	B		internal pull-down

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
108	GPIOE[5]	O	O	Y	internal pull-down
	~~GPIOE[6]~~				
	~~GPIOE[7]~~				
93	GPIOF[0]	O	O	Y	internal pull-down
27	GPIOF[1]	O	O	Y	internal pull-down
	~~GPIOF[2]~~				
	~~GPIOF[3]~~				
	~~GPIOF[4]~~				
	~~GPIOF[5]~~				
	~~GPIOF[6]~~				
	~~GPIOF[7]~~				
	~~GPIOG[0]~~				
	~~GPIOG[1]~~				
	~~GPIOG[2]~~				
	~~GPIOG[3]~~				
	~~GPIOG[4]~~				
	~~GPIOG[5]~~				
43	GPIOG[6]	O	B		internal pull-down
	~~GPIOG[7]~~				
28	GPIOH[0]	O	B		internal pull-down
106	GPIOH[1]	O	B		internal pull-down
42	GPIOH[2]	O	B		internal pull-down
38	GPIOH[3]	I	B		internal pull-up
101	GPIOH[4]	O	O	Y	internal pull-up only in strap period
44	GPIOH[5]	O	O	Y	internal pull-down only in strap period

6.17. Pin Descriptions (RTL8197FB)

Table 24. Pin Descriptions – RTL8197FB

Pin Name	Pin No.	Type	Description
Clock & Reset (2)			
XI	V11	I	25/40MHz External Clock Input.
XO	V10	O	25/40MHz Crystal Clock Output.
10/100M Ethernet Physical Layer (20)			
TXOP_P[4:0] TXON_P[4:0]	TXOP_P0: J1 TXON_P0: J2 TXOP_P1: L1 TXON_P1: L2 TXOP_P2: N1 TXON_P2: N2 TXOP_P3: R1 TXON_P3: R2 TXOP_P4: U1 TXON_P4: U2	AO	10/100M Ethernet Physical Layer Transmit Pair. For differential data transmission.
RXIP_P[4:0] RXIN_P[4:0]	RXIP_P0: K1 RXIN_P0: K2 RXIP_P1: M1 RXIN_P1: M2 RXIP_P2: P1 RXIN_P2: P2 RXIP_P3: T1 RXIN_P3: T2 RXIP_P4: V1 RXIN_P4: V2	AI	10/100M Ethernet Physical Layer Receive Pair. For differential data reception.
Ethernet MAC RGMII/MII Interface (14)			
P0_MDC	R6	O	Management Data Clock.
P0_MDIO	T6	I_{PU}/O	Management Data I/O.
P0_TXC	V5	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
P0_TXCTL	U5	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see

Pin Name	Pin No.	Type	Description
P0_TXD[3:0]	P0_TXD3: V3 P0_TXD2: U3 P0_TXD1: V4 P0_TXD0: U4	O	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXC	V6	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see
P0_RXCTL	U6	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
P0_RXD[3:0]	P0_RXD3: U8 P0_RXD2: V8 P0_RXD1: U7 P0_RXD0: V7	I	Shared for (1) MII Mode (2) RGMII Mode (3) MII PHY Mode. For details see.
eMMC Interface (11)			
EMMC_CLK	V9	O	eMMC Clock Output
EMMC_CMD	U10	B	eMMC Command
EMMC_DAT[7:0]	EMMC_DAT7: T9 EMMC_DAT6: U9 EMMC_DAT5: T10 EMMC_DAT4: T11 EMMC_DAT3: U11 EMMC_DAT2: T12 EMMC_DAT1: T7 EMMC_DAT0: T8	B	eMMC Data Input/Output
EMMC_RSTN	R3	O	eMMC Reset
SD Interface (2) (Partial Share Pin)			
SD_CLK	EMMC_CLK	O	SD Clock Output
SD_CMD	EMMC_CMD	B	SD Command
SD_DAT[3:0]	EMMC_DAT[3:0]	B	SD Data Input/Output
SD_CTRL_PWR	EMMC_RSTN	O	Enable/Disable power supply to SD card
SD_WP	T3	I	SD Write Protection
SD_CD	R4	I	SD Card Detection
Serial SPI-Nor Flash Control (6)			
MF_CS1N	C16	O	SPI Serial Flash Chip Select 1.
MF_CS0N	H16	O	SPI Serial Flash Chip Select 0.
MF_RSTN	D16	O	SPI Serial Flash Reset
MF_D[1:0]	MF_D1: E16 MF_D0: F16	I/O	SPI Serial Flash Serial Data Input/Output.
MF_CK	G16	O	SPI Serial Flash Serial Clock Output.
Serial SPI-Nand Flash Control (Share Pin)			
SPI_NAND_CK	MF_CK	O	SPI Nand Flash Clock Output
SPI_NAND_D[2:0]	SPI_NAND_D0: MF_D0 SPI_NAND_D1: MF_D1 SPI_NAND_D2: MF_RSTN	I/O	SPI Nand Flash Data Input/Output

Pin Name	Pin No.	Type	Description
SPI_NAND_CS0N	MF_CS0N	O	SPI Nand Flash Chip Select 0
SPI_NAND_D[3]	MF_CS1N	I/O	SPI Nand Flash Data Input/Output
Parallel P-Nand Flash Control (Share Pin)			
NF_D[7:0]	NF_D0: P0_RXD3 NF_D1: P0_RXD2 NF_D2: P0_RXD1 NF_D3: P0_RXD0 NF_D4: EMMC_DAT0 NF_D5: EMMC_DAT1 NF_D6: EMMC_DAT2 NF_D7: EMMC_DAT3	I/O	Data Input/Output for P-NAND Flash.
NF_CLE	P0_TXD2	O	P-NAND Flash Command Latch Enable.
NF_ALE	P0_TXD3	O	P-NAND Flash Address Latch Enable.
NF_CE0#	P0_RXC	O	P-NAND Flash Chip Enable.
NF_RD#	P0_TXD1	O	P-NAND Flash Read Enable.
NF_WE#	P0_TXCTL	O	P-NAND Flash Write Enable.
NF_WP#	P0_TXD0	O	P-NAND Flash Write Protect.
NF_R/B#	P0_RXCTL	I	P-NAND Flash Ready/Busy Input.
UART (2)			
U0_TX	K14	O	Data Transmit Serial Output of UART0.
U0_RX	J14	I_{PU}	Data Receive Serial Input of UART0.
UART (Full) (Share Pin)			
U1_TX	P0_TXCTL, EMMC_DAT3, P0_MDIO	O	Data Transmit Serial Output of UART1.
U1_RX	P0_TXC, SD_WP, EMMC_DAT0	I_{PU}	Data Receive Serial Input of UART1.
U1_RTS	P0_TXD0, EMMC_DAT2, P0_MDC	O	Request To Send of UART1.
U1_CTS	P0_RXCTL, SD_CD, EMMC_DAT1	I	Clear To Send of UART1.
U2_TX	P0_RXD2, EMMC_DAT3	O	Data Transmit Serial Output of UART2.
U2_RX	P0_RXD1, EMMC_DAT0	I_{PU}	Data Receive Serial Input of UART2.
U2_RTS	P0_RXD3, EMMC_DAT2	O	Request To Send of UART2.
U2_CTS	P0_RXD0, EMMC_DAT1	I	Clear To Send of UART2.

Pin Name	Pin No.	Type	Description
SPI (4-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3, P0_MDC, EMMC_CLK, WBB9	O	SPI0 Clock output
SPI0_TXD	MF_D0, P0_TXD1, SD_WP, WBB11	O	SPI0 Data Transmit
SPI0_RXD	MF_D1, P0_RXC, SD_CD, WBB12	I	SPI0 Data Receive
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO, EMMC_CMD, WBB10	O	SPI0 Chip Select 0
SPI0_CS1N	EMMC_RSTN, JTAG_TRSTN	O	SPI0 Chip Select 1
SPI1_CLK	P0_TXD0, P0_MDC, EMMC_CLK, EMMC_DAT4	O	SPI1 Clock output
SPI1_TXD	P0_TXCTL, SD_WP, EMMC_DAT6	O	SPI1 Data Transmit
SPI1_RXD	P0_RXCTL, SD_CD, EMMC_DAT7	I	SPI1 Data Receive
SPI1_CS0N	P0_TXC, P0_MDIO, EMMC_CMD, EMMC_DAT5	O	SPI1 Chip Select 0
SPI (3-Wire Master mode) (Share Pin)			
SPI0_CLK	MF_CK, P0_TXD3, P0_MDC, EMMC_CLK, WBB9	O	SPI0 Clock output
SPI0_TRXD	MF_D1, P0_RXC, SD_CD, WBB12	I/O	SPI0 Data Transmit/Receive

Pin Name	Pin No.	Type	Description
SPI0_CS0N	MF_RSTN, P0_TXD2, P0_MDIO, EMMC_CMD, WBB10	O	SPI0 Chip Select 0
SPI0_CS1N	EMMC_RSTN, JTAG_TRSTN	O	SPI0 Chip Select 1
SPI1_CLK	P0_TXD0, P0_MDC, EMMC_CLK, EMMC_DAT4	O	SPI1 Clock output
SPI1_TRXD	P0_RXCTL, SD_CD, EMMC_DAT7	I/O	SPI1 Data Transmit/Receive
SPI1_CS0N	P0_TXC, P0_MDIO, EMMC_CMD, EMMC_DAT5	O	SPI1 Chip Select 0
SPI (4-Wire Slave mode) (Share Pin)			
SPI0_CLK_SLV	P0_RXD1	I	SPI0 Slave Mode Clock Input
SPI0_TXD_SLV	P0_RXD3	O	SPI0 Slave Mode Data Transmit
SPI0_RXD_SLV	P0_RXD2	I	SPI0 Slave Mode Data Receive
SPI0_CS0N_SLV	P0_RXD0	I	SPI0 Slave Mode Chip Select 0 Input
PCM (Master Mode) (Share Pin)			
PCM_CLK	P0_RXD3, EMMC_DAT4, JTAG_TMS	O	PCM Master Mode Clock Output
PCM_FS	P0_RXD2, EMMC_DAT5, JTAG_TCK	O	PCM Master Mode Frame Sync
PCM_TXD	P0_RXD1, EMMC_DAT6, JTAG_TDO	O	PCM Master Mode Data Transmit
PCM_RXD	P0_RXD0, EMMC_DAT7, JTAG_TDI	I	PCM Master Mode Data Receive
JTAG (5)			
JTAG_TCK	N16	I_{PU}	JTAG Test Clock.
JTAG_TMS	M15	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	M16	O	JTAG Test Data Output.
JTAG_TDI	N15	I_{PU}	JTAG Test Data In.
JTAG_TRSTN	P15	I_{PU}	JTAG Test Reset.
JTAG (Share Pin)			
JTAG_TCK	P0_RXC	I_{PU}	JTAG Test Clock.
JTAG_TMS	P0_RXD2	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	P0_TXD0	O	JTAG Test Data Output.
JTAG_TDI	P0_RXD1	I_{PU}	JTAG Test Data In.

Pin Name	Pin No.	Type	Description
JTAG_TRSTN	P0_RXD3	I_{PU}	JTAG Test Reset.
I2C (Share Pin)			
I2C0_SCL	MF_CK, P0_TXCTL	B	I2C0 Serial Clock Line
I2C0_SDA	MF_D0, P0_RXCTL	B	I2C0 Serial Data Line
I2C1_SCL	MF_D1, MF_CS0N, P0_TXD1, P0_TXD0	B	I2C1 Serial Clock Line
I2C1_SDA	MF_RSTN, P0_RXC, P0_TXC	B	I2C1 Serial Data Line
I2C0_SCL_SLV	P0_TXC	B	I2C0 Slave Serial Clock Line
I2C0_SDA_SLV	P0_RXCTL	B	I2C0 Slave Serial Data Line
I2C1_SCL_SLV	MF_D1	B	I2C1 Slave Serial Clock Line
I2C1_SDA_SLV	MF_RSTN	B	I2C1 Slave Serial Data Line
LED (5)			
LED_PORT[4:0]	LED_PORT0: H15 LED_PORT1: J15 LED_PORT2: K15 LED_PORT3: L15 LED_PORT4: G15	O	Link or Link/Speed Status (Low Active).
WiFi Digital (13)			
WBB0	U13	O	LED for Wlan TRX
WBB[12:1]	WBB12: U18 WBB11: V17 WBB10: U17 WBB9: T16 WBB8: N17 WBB7: R16 WBB6: P17 WBB5: N18 WBB4: P16 WBB3: V18 WBB2: U16 WBB1: U15	I/O	Reserved for external RF component control or Wireless Coexistence interface
GPIO (3)			
GPIO_0	T4	I/O	GPIO Port G[3]
GPIO_1	R5	I/O	GPIO Port G[4]
GPIO_2	T5	I/O	GPIO Port G[5]
USB Host 2.0 / OTG (4)			
USB_HSDP0	G2	AI/O	USB Port0 Host Device Data Plus Pin.
USB_HSDM0	G1	AI/O	USB Port0 Host Device Data Minus Pin.
USB_HSDP1	H2	AI/O	USB Port1 Host Device Data Plus Pin.
USB_HSDM1	H1	AI/O	USB Port1 Host Device Data Minus Pin.

Pin Name	Pin No.	Type	Description
PCI Express Interface (7)			
PCIE_HSON PCIE_HSOP	D1, D2	AO	Transmitter Differential Pair.
PCIE_HSIN PCIE_HSIP	F1, F2	AI	Receiver Differential Pair.
PCIE_REFCLK_M PCIE_REFCLK_P	E1, E2	AO	Reference Clock Differential Pair.
PCIE_RSTN	M17	O	PCI Express Reset.
Reference Voltage (2)			
VDD_REF_DDR	C15	AI	Voltage Reference 1.25V for DDR1. Voltage Reference 0.9V for DDR2.
VDD_REF_EPHY	J5	AO	Voltage Reference 0.6V for Ethernet PHY. 2.5K ohm 1% resister pull down
Power & GND (93)			
VDD33_IO	D15,F15	P	Digital I/O Power Supply 3.3V.
VDD25_18_DDRIO	C6, C7, C9, C10, C13, C14	P	Memory I/O Power Supply 2.5V, or 1.8V. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
VDD33_25_MII	R7, R8	P	GMII/RGMII/MII Interface Power Supply 3.3V/2.5V .
VDD33_SD30	R11	P	SD Power supply 3.3V
VDD33_18_SD30	R10	P (O)	SD IO Output Power 3.3V/1.8V
VDD1P05	C5, C8, C12, D14, E15, P10	P	Digital Core Power Supply 1.05V.
AVDD33_EPHY	J3, J4, L4, N4, P4	AP	Ethernet Analog Power Supply 3.3V.
AVDD1P05_EPHY	H3, K3, L3, N3, P3	AP	Ethernet Analog Power Supply 1.05V.
AVDD33_BG	K5	AP	System Bandgap Power Supply 3.3V.
AVDD1P05_PCIE	E3	AP	PCI Express Analog Power Supply 1.05V.
AVDD1P05_PLL	G4	AP	PLL Power 1.05V.
AVDD33_USB	D4	AP	USB 2.0 Analog Power 3.3V.
AVDD1P05_USB	E4	AP	USB 2.0 Analog Power 1.05V.
AVDD33_DDRPLL	C3	AP	DDR PLL Analog Power 3.3V
AVDD1P05_DDRPLL	C4	AP or NC	DDR PLL Analog Power 1.05V Mode 1(NC): NC, using internal LDO (3.3V->1.05V) Mode 2(AP): input power

Pin Name	Pin No.	Type	Description
GND	D3, D5, D6, D7, D8, D9, D10, D11, D12, D13, E9, E10, F3 G3, G7, G8, G9, G10, G11, G12, H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10 L7, L8, L9, L10, L12 M3, M4, M7, M8, M9, M11, M12, P9, R9, R17, V12, U14	G	System GND.
AGND_SPS_DDR	J17, J18	AG	Internal SWR_DDR GND
AGND_SPS	L17, L18	AG	Internal SWR GND
AGND_USB	F4	AG	USB GND.
Internal SWR & LDO (8)			
AVDD33_SPS_DDR	J16	AP	Internal SWR_DDR Power Supply 3.3V Input for DDR.
AVDD25_18_SPS_DDR	H18, H17	AP (O)	Internal SWR_DDR Output Power for DDR. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
AVDD33_SPS	K16, L16	AP	Internal SWR Power Supply 3.3V Input
AVDD1P05_SPS	K17, K18	AP (O)	Internal SWR Power Supply 1.05V Output
ENSWR	M18	I	Internal SWR Power Supply Output Voltage enable/disable 0: Disable internal SWR 1: Enable internal SWR Note: If using external SWR/LDO, this pin must tie low.
Realtek Internal Test Pin (3)			
RTT	H4	AO	Reserved for Realtek Internal use. Must be left floating.
RTT1	K4	AO	Reserved for Realtek Internal use. Must be left floating.
AGPIO	V13	AI/O	Reserved for Realtek Internal use. Must be left floating.
RF & RF Power (16)			
AVDD1P05_AFE	M10	AP	Analog 1.05V power supply
AVDD33_X	R12	AP	Analog 3.3V power supply
AVDD33_SYN	T13	AP	RF 3.3V power supply
AVDD1P05_SYN	R13	AP	RF 1.05V power supply
VTSSI_EXT_S0	U12	AI	S0_TSSI voltage input
RFIP_S0	V14	AI/O	S0 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIN_S0	V15	AI/O	
AVDD33_RTX_S0	R14	AP	RF 3.3V power supply

Pin Name	Pin No.	Type	Description
RXIO_S0	V16	AI	S0 RX LNA input port
AVDD1P05_RTX_S0	T14	AP	RF 1.05V power supply
VTSSI_EXT_S1	T17	AI	S1 TSSI voltage input
AVDD1P05_RTX_S1	T15	AP	RF 1.05V power supply
RXIO_S1	T18	AI	S1 RX LNA input port
AVDD33_RTX_S1	R15	AP	RF 3.3V power supply
RFIN_S1	R18	AI/O	S1 RX/TX differential input/output ports connected to ANT by matching network and LC balun
RFIP_S1	P18	AI/O	
DDR (49)			
DDR_A[15:0]	DDR_A15: A6 DDR_A14: A3 DDR_A13: A7 DDR_A12: A2 DDR_A11: B7 DDR_A10: C1 DDR_A9: B3 DDR_A8: B8 DDR_A7: B2 DDR_A6: A8 DDR_A5: B1 DDR_A4: B9 DDR_A3: A1 DDR_A2: B6 DDR_A1: B4 DDR_A0: A9	O	DDR1/DDR2 Address bus bit
DDR_DQ[15:0]	DDR_DQ15: A16 DDR_DQ14: D17 DDR_DQ13: B15 DDR_DQ12: E18 DDR_DQ11: E17 DDR_DQ10: A15 DDR_DQ9: D18 DDR_DQ8: B16 DDR_DQ7: A14 DDR_DQ6: F17 DDR_DQ5: B13 DDR_DQ4: B18 DDR_DQ3: B17 DDR_DQ2: A13 DDR_DQ1: C17 DDR_DQ0: B14	I/O	DDR1/DDR2 Data bus bit
DDR_LDQS	G18	O	DDR1/DDR2 Differential Lower Data Strobe Corresponds to DDR_DQ[7:0].
DDR_LDQS#	G17	O	DDR1/DDR2 Differential Lower Data Strobe Corresponds to DDR_DQ[7:0].
DDR_UDQS	A18	O	DDR1/DDR2 Differential Upper Data Strobe Corresponds to D[15:8].
DDR_UDQS#	A17	O	DDR1/DDR2 Differential Upper Data Strobe Corresponds to D[15:8].
DDR_LDQM	F18	O	DDR1/DDR2 Lower Data Mask Output Corresponds to D[7:0]

Pin Name	Pin No.	Type	Description
DDR_UDQM	C18	O	DDR1/DDR2 Upper Data Mask Output Corresponds to D[15:8]
DDR_DCLK	A12	O	DDR1/DDR2 Differential Clock +.
DDR_DCLK#	B12	O	DDR1/DDR2 Differential Clock -.
DDR_CKE	A11	O	DDR1/DDR2 Clock Enable.
DDR_ODT	B11	O	DDR1/DDR2 On-Die Termination. ODT (registered HIGH) enables termination resistance internal to the DDR DRAM.
DDR_RAS#	A10	O	DDR1/DDR2 Raw Address Strobe (RAS)
DDR_CS#	C11	O	DDR1/DDR2 Chip Select
DDR_CAS#	B10	O	DDR1/DDR2 Column Address Strobe (CAS).
DDR_WE#	A5	O	Write Enable for DDR DRAM
DDR_BS[2:0]	DDR_BS2: C2 DDR_BS1: B5 DDR_BS0: A4	O	DDR1/DDR2 Chip Bank Select
Not Connected Pins (3)			
NC	L11, K11, K12	-	Not Connected. Must keep these pin floating .

Total Ball Number: 268

- Clock & Reset (2)
- 10/100M Ethernet Physical Layer (16)
- Ethernet MAC RGMII/MII Interface (14)
- eMMC Interface (11)
- SD Interface (2) (Partial Share Pin)
- Serial SPI Flash Control (6)
- UART (2)
- JTAG (5)
- LED (5)
- WiFi Digital (13)
- GPIO (3)
- USB Host 2.0 / OTG (4)
- PCI Express Interface (7)
- Reference Voltage (2)
- Power & GND (93)
- SWR & LDO (8)
- Realtek Internal Test Pin (3)
- RF & RF Power (16)
- DDR (49)
- Not Connected Pins (3)

6.18. Configuration Upon Power On Strapping (RTL8197FB)

The 1.05V digital core power input pin voltage is up to 0.7V on system power-on. The strap data will be latched after a delay of 160/100 ms.

25MHz XTAL: 160 ms
40MHz XTAL: 100 ms

Table 25. Configuration Upon Power On Strapping (RTL8197FB)

H/W Pin Name	Configuration Name	Pin No	Description
WBB4	Boot_select[0]	P16	boot_select[3:0]: 0000: SPI-NOR-Flash booting (3 byte addressing) 0001: [ROM] SPI-NOR-Flashing (3 byte addressing) 0010: [ROM] SPI-NAND-Flash booting 0011: [ROM] Parallel-NAND-Flash booting 0100: [ROM] eMMC 1.8V booting 0101: [ROM] SD booting 0110: 0111: 1000: [ROM] Switch booting (Image to DRAM) 1001: 1010: 1011: 1100: [ROM] eMMC 3.3V booting 1101: [ROM] Switch booting (Image to SPI-Nor Flash) 1110: SPI-NOR-Flash booting for OLT (3 byte addressing) 1111: loop mode for debug
WBB7	Boot_select[1]	R16	
WBB8	Boot_select[2]	N17	
P0_TXD3	Boot_select[3]	V3	
MF_CS0N	DRAM_TYPE_INV	H16	DRAM_TYPE_INV Select: (Referenced by SW) 0: DDR2 1: DDR1
U0_TX	DRAM_FEQ	K14	DRAM_FEQ Selection: (Only Referenced by SW) 0: DDR2_400MHz, DDR1_200MHz 1: DDR2_533MHz, DDR1_250MHz
P0_TXCTL	HW_DBG_DISABLE	U5	WiFi Debug mode / Enable strap_ctl_sys_dbg_sel 0: Enable 1: Disable
P0_TXD2	ddr_ldo_Sel	U3	DDR Power regulator selection: 0: SWR 1: LDO
P0_TXD1	Disable_Load_Efuse_Value	V4	Load Efuse Select: (Referenced by SW) 0: enable Load Efuse 1: disable Load Efuse
P0_TXD0	DISABLE_EXT_RSTN	U4	External Reset Select: 0: enable 1: disable

H/W Pin Name	Configuration Name	Pin No	Description
EMMC_RSTN	SWITCH_PHY_SEL	R3	Switch PHY Select: 0: External PHY 1: Embedded PHY
MF_CK	sel_40m	G16	System Clock Source Select: 0: 25M 1: 40M
PCIE_RSTN	strap_test_mode	M17	Chip Test Mode Select: 0: normal_mode 1: TEST_MODE (CP/FT/SCAN)
GPIO_1	mii_rx_dly[0] / NAFC_ECC[0]	R5	Nand Flash Controller ECC Selection. NAFC_ECC[2:0]: 000: 6, 001: 12, 010: 16, 011: 24 100: 40, 101: 43, 110: 65, 111: 72 MII RX Delay Selection. mii_rx_dly[2:0]
GPIO_2	mii_rx_dly[1] / NAFC_ECC[1]	T5	
JTAG_TCK	mii_rx_dly[2] / NAFC_ECC[2]	N16	
JTAG_TDO	mii_tx_dly[0]	M16	MII TX Delay Selection. mii_tx_dly[0]
WBB10	mii_mode[0]	U17	MII Mode Selection. mii_mode[1:0]: 01= MII-PHY, 00= MII-MAC mode 11= GMII-MAC, 10= RGMII mode
WBB9	mii_mode[1]	T16	

6.19. Shared I/O Pin Mapping (RTL8197FB)

Table 26. Shared I/O Pin Mapping (RTL8197FB)

Pin	GPIO		WiFi / PCM	RGMII/MII	P-Nand	I2S	SPI-Nor / SD/ eMMC	EJTAG / SPI-Nand	LED / SPI	UART	I2C, Reset
G16	GPIOA[0]	O					MF_CK	SPI_NAND_CK	SPI0_CLK		I2C0_SCL
F16	GPIOA[1]	B					MF_D0	SPI_NAND_D0	SPI0_TXD		I2C0_SDA
E16	GPIOA[2]	B					MF_D1	SPI_NAND_D1	SPI0_RXD, SPI0_TRXD		I2C1_SCL / I2C1_SCL_SLV
D16	GPIOA[3]	B					MF_RSTN	SPI_NAND_D2	SPI0_CS0N		I2C1_SDA / I2C1_SDA_SLV
H16	GPIOA[4]	O					MF_CS0N	SPI_NAND_CS0N			I2C1_SCL
C16	GPIOA[5]	B				I2S_SD3_O	MF_CS1N	SPI_NAND_D3			I2C1_SDA
V3	GPIOA[6]	O		P0_TXD3	NF_ALE	I2S_MCLK			SPI0_CLK		
U3	GPIOA[7]	O		P0_TXD2	NF_CLE	I2S_SCLK			SPI0_CS0N		
V4	GPIOB[0]	O		P0_TXD1	NF_RD#	I2S_WS / I2S_SD2_O			SPI0_TXD		I2C1_SCL
V6	GPIOB[1]	B		P0_RXC	NF_CE0#	I2S_SD1_O / I2S_SD1_I / I2S_SD3_O		JTAG_TCK	SPI0_RXD, SPI0_TRXD		I2C1_SDA
U8	GPIOB[2]	B	PCM_CLK	P0_RXD3	NF_D0	I2S_MCLK		JTAG_TRSTN	SPI0_TXD_SLV	U2_RTS	
V8	GPIOB[3]	B	PCM_FS	P0_RXD2	NF_D1	I2S_SCLK		JTAG_TMS	SPI0_RXD_SLV	U2_TX	
U7	GPIOB[4]	B	PCM_TXD	P0_RXD1	NF_D2	I2S_WS		JTAG_TDI	SPI0_CLK_SLV	U2_RX	
V7	GPIOB[5]	B	PCM_RXD	P0_RXD0	NF_D3	I2S_SD1_O			SPI0_CS0N_SLV	U2_CTS	
U4	GPIOB[6]	O		P0_TXD0	NF_WP#			JTAG_TDO	SPI1_CLK	U1_RTS	I2C1_SCL
V5	GPIOB[7]	B		P0_TXC		I2S_SD1_I			SPI1_CS0N	U1_RX	I2C1_SDA / I2C0_SCL_SLV
U5	GPIOC[0]	O		P0_TXCTL	NF_WE#				SPI1_TXD	U1_TX	I2C0_SCL
U6	GPIOC[1]	B		P0_RXCTL	NF_R/B#				SPI1_RXD, SPI1_TRXD	U1_CTS	I2C0_SDA / I2C0_SDA_SLV
R6	GPIOC[2]	B		P0_MDC					SPI0_CLK, SPI1_CLK	U1_RTS	I2C0_SCL / I2C1_SCL
T6	GPIOC[3]	B		P0_MDIO					SPI0_CS0N, SPI1_CS0N	U1_TX	I2C0_SDA / I2C1_SDA
R3	GPIOC[4]	O					EMMC_RSTN		SPI0_CS1N		
T3	GPIOC[5]	B				I2S_WS	SD_WP		SPI0_TXD, SPI1_TXD	U1_RX	
R4	GPIOC[6]	B				I2S_SCLK	SD_CD		SPI0_RXD, SPI0_TRXD SPI1_RXD, SPI1_TRXD	U1_CTS	
V9	GPIOC[7]	B				I2S_MCLK	EMMC_CLK		SPI0_CLK, SPI1_CLK		
U10	GPIOD[0]	B				I2S_SD1_O	EMMC_CMD		SPI0_CS0N, SPI1_CS0N		
T8	GPIOD[1]	B			NF_D4	I2S_WS	EMMC_DAT0			U1_RX / U2_RX	
T7	GPIOD[2]	B			NF_D5	I2S_SCLK	EMMC_DAT1			U1_CTS / U2_CTS	
T12	GPIOD[3]	B			NF_D6	I2S_MCLK	EMMC_DAT2			U1_RTS / U2_RTS	

Pin	GPIO		WiFi / PCM	RGMII/MII	P-Nand	I2S	SPI-Nor / SD/ eMMC	EJTAG / SPI-Nand	LED / SPI	UART	I2C, Reset
U11	GPIOD[4]	B			NF_D7	I2S_SD1_O	EMMC_DAT3			U1_TX / U2_TX	
T11	GPIOD[5]	B	PCM_CLK				EMMC_DAT4		SPI1_CLK		
T10	GPIOD[6]	B	PCM_FS				EMMC_DAT5		SPI1_CS0N		
U9	GPIOD[7]	B	PCM_TXD				EMMC_DAT6		SPI1_TXD		
T9	GPIOE[0]	B	PCM_RXD				EMMC_DAT7		SPI1_RXD, SPI1_TRXD		
U13	GPIOE[1]	B	WBB0								
U15	GPIOE[2]	B	WBB1								
U16	GPIOE[3]	B	WBB2								
V18	GPIOE[4]	B	WBB3								
P16	GPIOE[5]	O	WBB4								
N18	GPIOE[6]	B	WBB5								
P17	GPIOE[7]	B	WBB6								
R16	GPIOF[0]	O	WBB7								
N17	GPIOF[1]	O	WBB8								
T16	GPIOF[2]	O	WBB9						SPI0_CLK		
U17	GPIOF[3]	O	WBB10						SPI0_CS0N		
V17	GPIOF[4]	B	WBB11						SPI0_TXD		
U18	GPIOF[5]	B	WBB12						SPI0_RXD, SPI0_TRXD		
P15	GPIOF[6]	B						JTAG_TRSTN	SPI0_CS1N		
N16	GPIOF[7]	O	PCM_FS					JTAG_TCK			
M15	GPIOG[0]	B	PCM_CLK					JTAG_TMS			
N15	GPIOG[1]	B	PCM_RXD					JTAG_TDI			
M16	GPIOG[2]	O	PCM_TXD					JTAG_TDO			
T4	GPIOG[3]	B									GPIO_0
R5	GPIOG[4]	O									GPIO_1
T5	GPIOG[5]	O									GPIO_2
H15	GPIOG[6]	B							LED_PORT0		
J15	GPIOG[7]	B							LED_PORT1		
K15	GPIOH[0]	B							LED_PORT2		
L15	GPIOH[1]	B							LED_PORT3		RESETN
G15	GPIOH[2]	B							LED_PORT4		
J14	GPIOH[3]	B								U0_RX	
K14	GPIOH[4]	O								U0_TX	
M17	GPIOH[5]	O									PCIE_RSTN

6.20. GPIO Pin During Boot State (RTL8197FB)

Table 27. GPIO Pin During Boot State - RTL8197FB

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
G16	GPIOA[0]	I	O	Y	internal pull-down only in strap period
F16	GPIOA[1]	I	B		internal pull-up
E16	GPIOA[2]	I	B		internal pull-up
D16	GPIOA[3]	I	B		internal pull-up
H16	GPIOA[4]	I	O	Y	internal pull-down only in strap period
C16	GPIOA[5]	I	B		internal pull-up
V3	GPIOA[6]	O	O	Y	internal pull-down only in strap period
U3	GPIOA[7]	O	O	Y	internal pull-up only in strap period
V4	GPIOB[0]	O	O	Y	internal pull-down only in strap period
V6	GPIOB[1]	I	B		internal pull-up
U8	GPIOB[2]	I	B		internal pull-up
V8	GPIOB[3]	I	B		internal pull-up
U7	GPIOB[4]	I	B		internal pull-up
V7	GPIOB[5]	I	B		internal pull-up
U4	GPIOB[6]	O	O	Y	internal pull-down only in strap period
V5	GPIOB[7]	B	B		internal pull-up
U5	GPIOC[0]	O	O	Y	internal pull-down only in strap period
U6	GPIOC[1]	I	B		internal pull-up
R6	GPIOC[2]	I	B		internal pull-up
T6	GPIOC[3]	B	B		internal pull-up
R3	GPIOC[4]	O	O	Y	internal pull-up only in strap period
T3	GPIOC[5]	I	B		internal pull-up
R4	GPIOC[6]	I	B		internal pull-up
V9	GPIOC[7]	O	B		
U10	GPIOD[0]	B	B		internal pull-up
T8	GPIOD[1]	B	B		internal pull-up
T7	GPIOD[2]	B	B		internal pull-up
T12	GPIOD[3]	B	B		internal pull-up
U11	GPIOD[4]	B	B		internal pull-up
T11	GPIOD[5]	B	B		internal pull-up
T10	GPIOD[6]	B	B		internal pull-up
U9	GPIOD[7]	B	B		internal pull-up
T9	GPIOE[0]	B	B		internal pull-up
U13	GPIOE[1]	O	B		internal pull-down
U15	GPIOE[2]	B	B		internal pull-down
U16	GPIOE[3]	B	B		internal pull-down
V18	GPIOE[4]	B	B		internal pull-down

Pin	GPIO	HW Default Direction	Support Direction	Strap ?	During Boot state (Before SW Control)
P16	GPIOE[5]	O	O	Y	internal pull-down
N18	GPIOE[6]	B	B		internal pull-down
P17	GPIOE[7]	B	B		internal pull-down
R16	GPIOF[0]	O	O	Y	internal pull-down
N17	GPIOF[1]	O	O	Y	internal pull-down
T16	GPIOF[2]	O	O	Y	internal pull-down
U17	GPIOF[3]	O	O	Y	internal pull-up
V17	GPIOF[4]	B	B		internal pull-up
U18	GPIOF[5]	B	B		internal pull-up
P15	GPIOF[6]	I	B		internal pull-up
N16	GPIOF[7]	I	O	Y	internal pull-down
M15	GPIOG[0]	I	B		internal pull-up
N15	GPIOG[1]	I	B		internal pull-up
M16	GPIOG[2]	O	O	Y	internal pull-down only in strap period
T4	GPIOG[3]	I	B		internal pull-up
R5	GPIOG[4]	O	O	Y	internal pull-down only in strap period
T5	GPIOG[5]	O	O	Y	internal pull-down only in strap period
H15	GPIOG[6]	O	B		internal pull-down
J15	GPIOG[7]	O	B		internal pull-down
K15	GPIOH[0]	O	B		internal pull-down
L15	GPIOH[1]	O	B		internal pull-down
G15	GPIOH[2]	O	B		internal pull-down
J14	GPIOH[3]	I	B		internal pull-up
K14	GPIOH[4]	O	O	Y	internal pull-up only in strap period
M17	GPIOH[5]	O	O	Y	internal pull-down only in strap period

7. Register & DRAM Address Summary

7.1. The Mapping relationship

BUS	Virtual Address	Physical Address	*Size*	IP Function
Sheipa	0xA000_0000	0x0000_0000	256MB	RAM
	0xAFFF_FFFF	0x0FFF_FFFF		
	0xB000_0000	0x1000_0000	128MB	SPI NOR Flash
	0xB7FF_FFFF	0x17FF_FFFF		
LX0	0xB800_0000	0x1800_0000	1.25KB	System register
	0xB800_04FF	0x1800_04FF		
	0xB800_0600	0x1800_0600	256B	IIC
	0xB800_06FF	0x1800_06FF		
	0xB800_0700	0x1800_0700	256B	efuse_ctrl
	0xB800_07FF	0x1800_07FF		
	0xB800_0800	0x1800_0800	2KB	System register
	0xB800_0FFF	0x1800_0FFF		
	0xB800_2000	0x1800_2000	4KB	UART(x16)
	0xB800_2FFF	0x1800_2FFF		
	0xB800_3000	0x1800_3000	0.125KB	Interrupt controller0
	0xB800_307F	0x1800_307F		
	0xB800_3080	0x1800_3080	0.125KB	Interrupt controller1
	0xB800_30FF	0x1800_30FF		
	0xB800_3100	0x1800_3100	0.125KB	Timer(x4)(#0, #1, #2, #3), Watchdog
	0xB800_317F	0x1800_317F		
	0xB800_3300	0x1800_3300	0.25KB	systerm misc0
	0xB800_337F	0x1800_337F		
	0xB800_3380	0x1800_3380	0.25KB	systerm misc1
	0xB800_33FF	0x1800_33FF		
	0xB800_3500	0x1800_3500	0.25KB	GPIO0
	0xB800_357F	0x1800_357F		
	0xB800_3580	0x1800_3580	0.25KB	GPIO1

	0xB800_35FF	0x1800_35FF		
	0xB801_0000	0x1801_0000	8KB	Switch CPORT
	0xB801_1FFF	0x1801_1FFF		
	0xB801_9000	0x1801_9000	4KB	NFBI
	0xB801_9FFF	0x1801_9FFF		
	0xB801_A000	0x1801_A000	1KB	parallel NAND flash
	0xB801_A3FF	0x1801_A3FF		
	0xB801_A600	0x1801_A600	512B	flash ecc
	0xB801_A7FF	0x1801_A7FF		
	0xBB00_0000	0x1B00_0000	32MB	Chip application specific space(Switch Core)
	0xBCFF_FFFF	0x1CFF_FFFF		
LX1	0xB800_8000	0x1800_8000	4KB	PCM
	0xB800_8FFF	0x1800_8FFF		
	0xB800_C000	0x1800_C000	16KB	Security engine
	0xB800_FFFF	0x1800_FFFF		
	0xB801_F000	0x1801_F000	4KB	I2S
	0xB801_FFFF	0x1801_FFFF		
	0xB801_5000	0x1801_5000	4KB	SD3.0/MMC/SDIO
	0xB801_5FFF	0x1801_5FFF		
	0xB801_6000	0x1801_6000	4KB	eMMC
	0xB801_6FFF	0x1801_6FFF		
LX2				
	0xB814_0200	0x1814_0200	0.25KB	USB2 MAC Control Registers
	0xB814_02FF	0x1814_02FF		
	0xB814_0300	0x1814_0300	0.25KB	USB2 OTG Control Registers
	0xB814_03FF	0x1814_03FF		
	0xB8B0_1000	0x18B0_1000	4KB	PCIE0 Extended Reg
	0xB8B0_1FFF	0x18B0_1FFF		

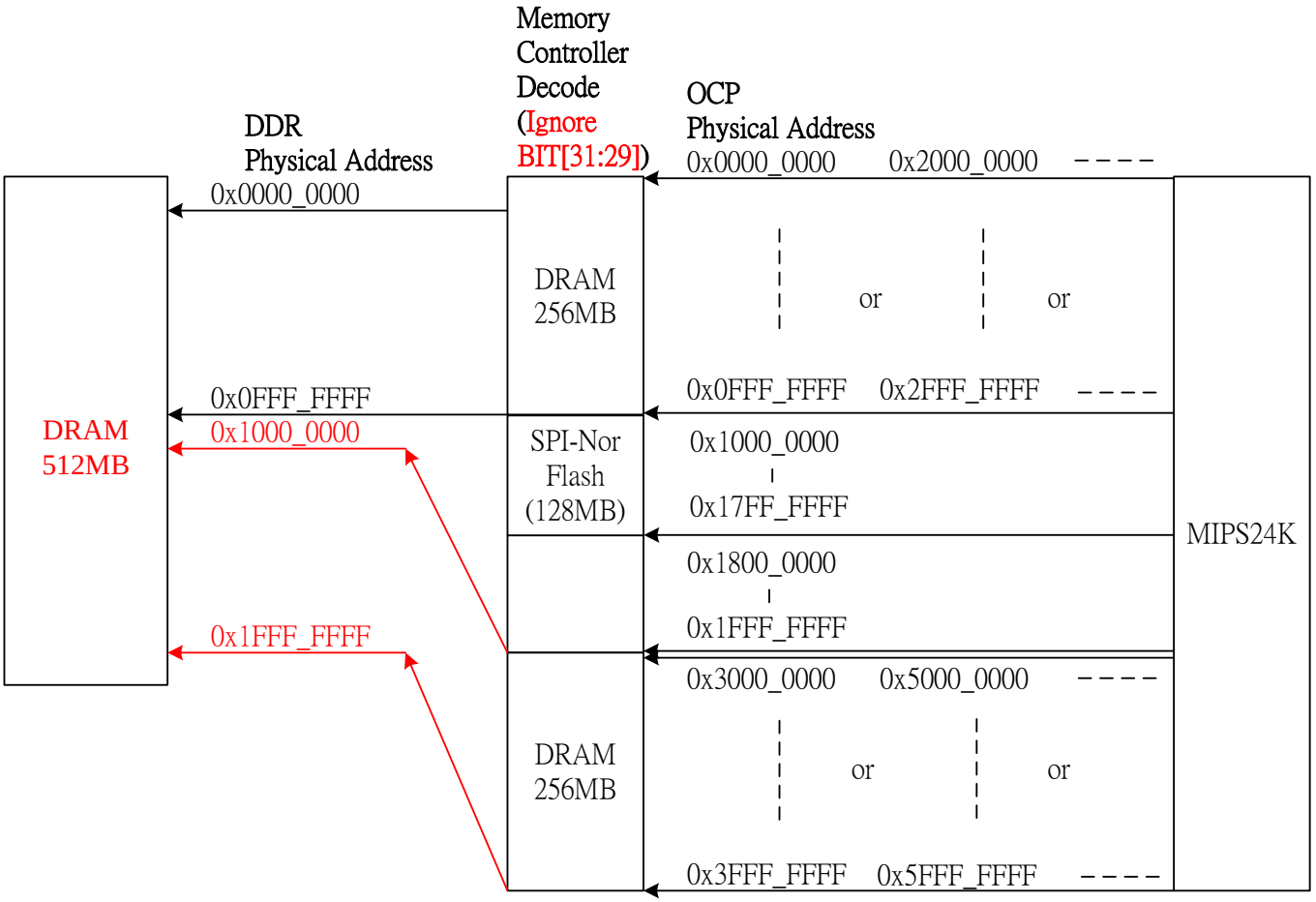
Sheipa	0xB814_2000	0x1814_2000	4KB	Sheipa RXI-310 DRAM Controller
	0xB814_2FFF	0x1814_2FFF		
	0xB814_3000	0x1814_3000	4KB	Sheipa RXI-310 SPI Contorller
	0xB814_3FFF	0x1814_3FFF		
	0xB814_4000	0x1814_4000	4KB	Sheipa PMU Controller and cpu/sheipa sram controll signal
	0xB814_4FFF	0x1814_4FFF		
	0xB814_5000	0x1814_5000	4KB	Sheipa RXI-310 Bus Controller
	0xB814_5FFF	0x1814_5FFF		
	0xB814_6000	0x1814_6000	4KB	Sheipa DDR DFI controller (digital part)
	0xB814_6FFF	0x1814_6FFF		
	0xB816_0000	0x1816_0000	128KB	Sheipa DDR training pattern
	0xB817_FFFF	0x1817_FFFF		
TLP pcie_rc0	0xB8B0_0000	0x18B0_0000	4KB	PCIE0 DBI
	0xB8B0_0FFF	0x18B0_0FFF		
	0xB8B1_0000	0x18B1_0000	4KB	PCIE0 CFG0
	0xB8B1_0FFF	0x18B1_0FFF		
	0xB8B1_1000	0x18B1_1000	4KB	PCIE0 CFG1
	0xB8B1_1FFF	0x18B1_1FFF		
	0xB8B1_2000	0x18B1_2000	4KB	PCIE0 MSG
	0xB8B1_2FFF	0x18B1_2FFF		
	0xB8C0_0000	0x18C0_0000	1MB	PCIE0 IO
	0xB8CF_FFFF	0x18CF_FFFF		
	0xB900_0000	0x1900_0000	8MB	PCIE0 MEM
	0xB97F_FFFF	0x197F_FFFF		

AHB GDMA	0xB801_B000	0x1801_B000	1KB	DW_GDMA
	0xB801_B3FF	0x1801_B3FF		
APB SPI 1	0xB801_C000	0x1801_C000	256B	DW_SPI_1
	0xB801_C0FF	0x1801_C0FF		
APB SPI 2	0xB801_C100	0x1801_C100	256B	DW_SPI_2
	0xB801_C1FF	0x1801_C1FF		
APB I2C 1	0xB801_D000	0x1801_D000	256B	DW_I2C_1
	0xB801_D0FF	0x1801_D0FF		
APB I2C 2	0xB801_D100	0x1801_D100	256B	DW_I2C_2
	0xB801_D1FF	0x1801_D1FF		
AHB OHCI	0xB802_0000	0x1802_0000	4KB	USB2 OHCI
	0xB802_0FFF	0x1802_0FFF		
AHB EHCI	0xB802_1000	0x1802_1000	4KB	USB2 EHCI
	0xB802_1FFF	0x1802_FFFF		
AHB USB2 OTG	0xB803_0000	0x1803_0000	64KB	USB2 OTG

	0xB803_FFFF	0x1803_FFFF		
APB UART 1	0xB814_7000	0x1814_7000	1KB	rt_uart_1
	0xB814_73FF	0x1814_73FF		
APB UART 2	0xB814_7400	0x1814_7400	1KB	rt_uart_2
	0xB814_77FF	0x1814_77FF		
APB UART 3	0xB814_7800	0x1814_7800	1KB	rt_uart_3
	0xB814_7BFF	0x1814_7BFF		
APB TIMER 1	0xB814_8000	0x1814_8000	256B	DW_timers
	0xB814_80FF	0x1814_80FF		
APB4 WIFI	0xB864_0000	0x1864_0000	256KB	WIFI
	0xB867_FFFF	0x1867_FFFF		
LX0 Switch Core	0xBB00_0000	0x1B00_0000	32MB	Chip application specific space(Switch Core)
	0xBCFF_FFFF	0x1CFF_FFFF		
Sheipa	0xBD00_0000	0x1D00_0000	32MB	Reserved
	0xBEFF_FFFF	0x1EFF_FFFF		
	0xBF00_0000	0x1F00_0000	12MB	Reserved
	0xBFBF_FFFF	0xBFBF_FFFF		
	0xBFC0_0000	0x1FC0_0000	1MB	Sheipa Boot ROM
	0xBFCF_FFFF	0x1FCF_FFFF		
	0xBFD0_0000	0x1FD0_0000	1MB	ROM
	0xBFDF_FFFF	0x1FDF_FFFF		
	0xBFE0_0000	0x1FE0_0000	2MB	SRAM
	0xBFFF_FFFF	0x1FFF_FFFF		

Table 28. System map for each bus

7.2. DRAM Map



MAX DRAM Size is 512 MB, because memory controller will ignore address[31:29]

Figure 15. DRAM Map

7.3. DRAM Max Size Support

8197F DRAM interface only support 1 chip select.

DRAM Data bit width 16 => Max Size 256MB
- One 256MB/16bit DRAM ASIC

DRAM Data bit width 8 => Max Size 512MB
- Two 256MB/8bit DRAM ASIC

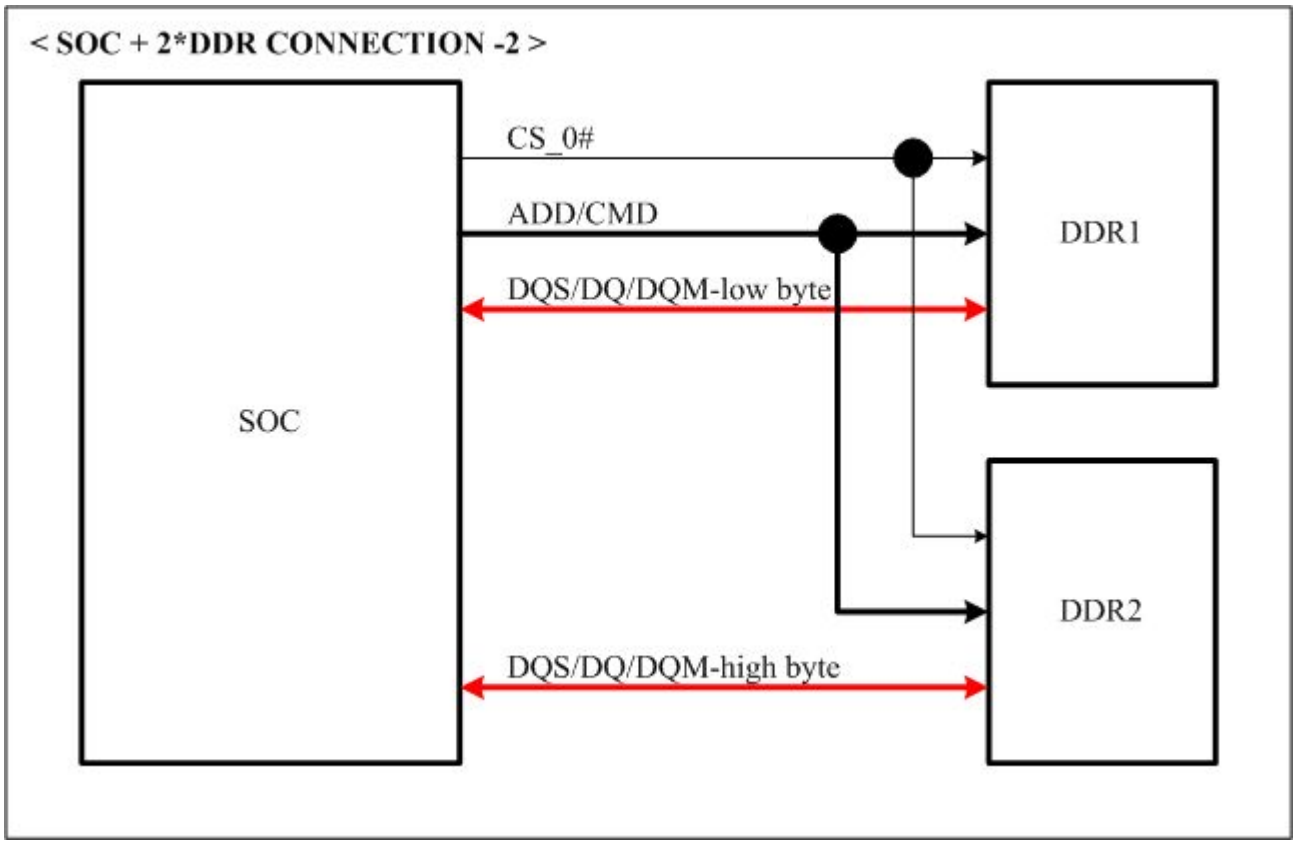


Figure 16. Two DRAM ASIC Support

In general, DDR2 Max Size is 256MB by Vendor provided.
But 8197F can use 2 DRAM ASIC to support Max 512MB (2 x 256MB, data bit width: 8)

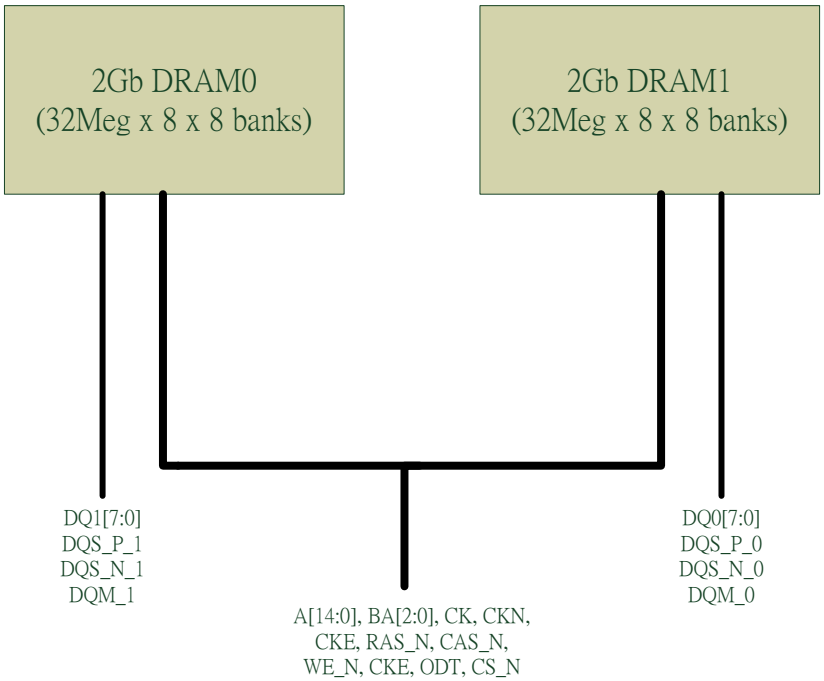


Figure 17. DRAM Max Size Support

8. Shared Mode I/O Pin Mux Control Register

Shared Mode pins configuration control register is controlled by the following registers

Base Address: 0xB800_0000 (Virtual Address), 0x1800_0000 (Physical Address)

0800h	REG_PINMUX_00				
	[31:28]	R/W	1	BIT_REG_IOCFG_P0TXD0	Pinmux selection 0000:MII 0001:JTAG 0010:NAND 0011:SPI1 0100:UART1 0101:II2C1 0110:XOUT 0111:PWM 1000:GPIOB[6] 1001:DBG
	[27:24]	R/W	0	BIT_REG_IOCFG_P0TXD1	Pinmux selection 0000:MII 0001:NAND 0010:SPI0 0011:I2C1 0100:IIS 0101:IISA 0110:XOUT 0111:PWM 1000:GPIOB[0] 1001:DBG
	[23:20]	R/W	0	BIT_REG_IOCFG_P0TXD2	Pinmux selection 0000:MII 0001:NAND 0010:SPI0 0011:IIS 0100:XOUT 0101:PWM 0110:GPIOA[7]

					0111:DBG
	[19:16]	R/W	0	BIT_REG_IOCFG_P0TXD3	Pinmux selection 0000:MII 0001:NAND 0010:SPI0 0011:IIS 0100:PWM 0101:GPIOA[6] 0110:DBG
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
0804h	REG_PINMUX_01				
	[31:28]	R/W	0	BIT_REG_IOCFG_P0RXD0	Pinmux selection 0000:MII 0001:NAND 0010:SPI0 0011:UART2 0100:IIS 0101:PCM 0110:EVENT 0111:GPIOB[5] 1000:DBG

	[27:24]	R/W	1	BIT_REG_IOCFG_P0RXD1	Pinmux selection 0000:MII 0001:JTAG 0010:NAND 0011:SPI0 0100:UART2 0101:IIS 0110:PCM 0111:EVENT 1000:GPIOB[4] 1001:DBG
	[23:20]	R/W	1	BIT_REG_IOCFG_P0RXD2	Pinmux selection 0000:MII 0001:JTAG 0010:NAND 0011:SPI0 0100:UART2 0101:IIS 0110:PCM 0111:EVENT 1000:GPIOB[3] 1001:DBG
	[19:16]	R/W	1	BIT_REG_IOCFG_P0RXD3	Pinmux selection 0000:MII 0001:JTAG 0010:NAND 0011:SPI0 0100:UART2 0101:IIS 0110:PCM 0111:EVENT 1000:GPIOB[2] 1001:DBG
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved

	[3:0]	R/W	0	--	Reserved
0808h	REG_PINMUX_02				
	[31:28]	R/W	0	--	Reserved
	[27:24]	R/W	0	BIT_REG_IOCFG_P0TXC	Pinmux selection 0000:MII 0001:NAND 0010:SPI1 0011:UART1 0100:IIS 0101:I2C1 0110:I2C0 0111:EVENT 1000:GPIOB[7] 1001:DBG
	[23:20]	R/W	0	BIT_REG_IOCFG_P0TXCTL	Pinmux selection 0000:MII 0001:NAND 0010:SPI1 0011:UART1 0100:I2C0 0101:PWM 0110:GPIOC[0] 0111:DBG
	[19:16]	R/W	1	BIT_REG_IOCFG_P0RXC	Pinmux selection 0000:MII 0001:JTAG 0010:NAND 0011:SPI0 0100:SPI0_3W 0101:I2C1 0110:IISV 0111:IIS 1000:IISA 1001:PWM 1010:GPIOB[1] 1011:DBG

	[15:12]	R/W	0	BIT_REG_IOCFG_P0RXCTL	Pinmux selection 0000:MII 0001:NAND 0010:SPI1 0011:SPI1_3W 0100:UART1 0101:I2C0 0110:PWM 0111:GPIOC[1] 1000:DBG
	[11:8]	R/W	0	BIT_REG_IOCFG_P0MDC	Pinmux selection 0000:MII 0001:SPI0 0010:SPI1 0011:I2C0 0100:I2C1 0101:UART1 0110:GPIOC[2] 0111:DBG
	[7:4]	R/W	0	BIT_REG_IOCFG_P0MDIO	Pinmux selection 0000:MII 0001:SPI0 0010:SPI1 0011:I2C0 0100:I2C1 0101:UART1 0110:GPIOC[3] 0111:DBG
	[3:0]	R/W	0	--	Reserved
080Ch	REG_PINMUX_03				
	[31:28]	R/W	0	--	Reserved
	[27:24]	R/W	0	--	Reserved
	[23:20]	R/W	0	--	Reserved
	[19:16]	R/W	0	--	Reserved
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved

	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
0810h	REG_PINMUX_04				
	[31:28]	R/W	0	--	Reserved
	[27:24]	R/W	0	--	Reserved
	[23:20]	R/W	0	--	Reserved
	[19:16]	R/W	0	--	Reserved
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
0814h	REG_PINMUX_05				
	[31:28]	R/W	0	--	Reserved
	[27:24]	R/W	0	--	Reserved
	[23:20]	R/W	0	--	Reserved
	[19:16]	R/W	0	--	Reserved
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
0818h	REG_PINMUX_06				
	[31:28]	R/W	0	BIT_REG_IOCFG_MFD0	Pinmux selection 0000:ROM (not nfbi_boot , not spi boot) 0000:NFBI (with nfbi_boot) 0000:SPINOR (with spii_boot) 0001:NFBI 0010:SPINOR 0011:SPINAND 0100:IIS 0101:I2C0 0110:UART1 0111:SPI0 1000:GPIOA[1]

					1001:DBG
	[27:24]	R/W	0	BIT_REG_IOCFG_MFD1	Pinmux selection 0000:ROM (not nfbi_boot , not spi boot) 0000:NFBI (with nfbi_boot) 0000:SPINOR (with spii_boot) 0001:NFBI 0010:SPINOR 0011:SPINAND 0100:IISA 0101:IISV 0110:I2C1 0111:I2C1_S 1000:UART1 1001:SPI0 1010:SPI0_3W 1011:GPIOA[2] 1100:DBG
	[23:20]	R/W	0	--	Reserved
	[19:16]	R/W	0	--	Reserved
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved

081Ch	REG_PINMUX_07				
	[31:28]	R/W	0	BIT_REG_IOCFG_MFCK	Pinmux selection 0000:ROM (not nfbi_boot , not spi boot) 0000:NFBI (with nfbi_boot) 0000:SPINOR (with spii_boot) 0001:NFBI 0010:SPINOR 0011:SPINAND 0100:IIS 0101:I2C0 0110:UART1 0111:SPI0 1000:GPIOA[0] 1001:DBG
	[27:24]	R/W	0	BIT_REG_IOCFG_MFCS0	Pinmux selection 0000:ROM (not nfbi_boot , not spi boot) 0000:NFBI (with nfbi_boot) 0000:SPINOR (with spii_boot) 0001:NFBI 0010:SPINOR 0011:SPINAND 0100:IIS 0101:I2C1 0110:XOUT 0111:GPIOA[4] 1000:DBG

	[23:20]	R/W	0	BIT_REG_IOCFG_MFCS1	Pinmux selection 0000:ROM (not nfbi_boot , not spi boot) 0000:NFBI (with nfbi_boot) 0000:SPINOR (with spii_boot) 0001:NFBI 0010:SPINOR 0011:SPINAND 0100:IIS 0101:I2C1 0110:GPIOA[5] 0111:DBG
	[19:16]	R/W	0	BIT_REG_IOCFG_MFRST	Pinmux selection 0000:ROM (not nfbi_boot , not spi boot) 0000:NFBI (with nfbi_boot) 0000:SPINOR (with spii_boot) 0001:NFBI 0010:SPINOR 0011:SPINAND 0100:IIS 0101:I2C1 0110:UART1 0111:SPI0 1000:GPIOA[3] 1001:DBG
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
0820h	REG_PINMUX_08				

	[31:28]	R/W	1	BIT_REG_IOCFG_JTAG_CLK	Pinmux selection 0000:WLAN 0001:JTAG 0010:PCM 0011:UART1 0100:IIS 0101:PWM 0110:GPIOF[7] 0111:DBG
	[27:24]	R/W	1	BIT_REG_IOCFG_JTAG_RST	Pinmux selection 0000:WLAN 0001:JTAG 0010:SPI0 0011:IISA 0100:IISV 0101:XOUT 0110:GPIOF[6] 0111:DBG
	[23:20]	R/W	1	BIT_REG_IOCFG_JTAG_TMS	Pinmux selection 0000:WLAN 0001:JTAG 0010:PCM 0011:UART1 0100:PWM 0101:XOUT 0110:GPIOG[0] 0111:DBG
	[19:16]	R/W	1	BIT_REG_IOCFG_JTAG_TDI	Pinmux selection 0000:WLAN 0001:JTAG 0010:PCM 0011:UART1 0100:IIS 0101:I2C0 0110:PWM 0111:GPIOG[1]

					1000:DBG
	[15:12]	R/W	1	BIT_REG_IOCFG_JTAG_TDO	Pinmux selection 0000:WLAN 0001:JTAG 0010:PCM 0011:UART1 0100:IIS 0101:I2C0 0110:PWM 0111:GPIOG[2] 1000:DBG
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	BIT_REG_IOCFG_PCIE	Pinmux selection 0000:PCIE 0001:GPIOH[5] 0010:DBG
0824h	REG_PINMUX_09				
	[31:28]	R/W	0	BIT_REG_IOCFG_GPIO0	Pinmux selection 0000:USBH 0001:LOWV 0010:GPIOG[3] 0011:DBG
	[27:24]	R/W	0	BIT_REG_IOCFG_GPIO1	Pinmux selection 0000:USBH 0001:GPIOG[4] 0010:DBG

	[23:20]	R/W	1	BIT_REG_IOCFG_GPIO2	Pinmux selection 0000:GPIOG[5] 0001:DBG
	[19:16]	R/W	0	--	Reserved
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
0828h	REG_PINMUX_10				
	[31:28]	R/W	0	--	Reserved
	[27:24]	R/W	0	--	Reserved
	[23:20]	R/W	0	--	Reserved
	[19:16]	R/W	0	--	Reserved
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
082Ch	REG_PINMUX_11				
	[31:28]	R/W	0	--	Reserved
	[27:24]	R/W	0	--	Reserved
	[23:20]	R/W	0	--	Reserved
	[19:16]	R/W	0	--	Reserved
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
0830h	REG_PINMUX_12				
	[31:28]	R/W	0	BIT_REG_IOCFG_U0_TX	Pinmux selection 0000:UART 0001:GPIOH[4]
	[27:24]	R/W	0	BIT_REG_IOCFG_U0_RX	Pinmux selection 0000:UART 0001:GPIOH[3]
	[23:20]	R/W	0	--	Reserved
	[19:16]	R/W	0	--	Reserved

	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
0834h	REG_PINMUX_13				
	[31:28]	R/W	0011	BIT_REG_IOCFG_LED_S0	Pinmux selection 0000:LED 0001:PWM 0010:VP 0011:GPIOG[6] 0100:DBG
	[27:24]	R/W	0011	BIT_REG_IOCFG_LED_S1	Pinmux selection 0000:LED 0001:PWM 0010:VP 0011:GPIOG[7] 0100:DBG
	[23:20]	R/W	0011	BIT_REG_IOCFG_LED_S2	Pinmux selection 0000:LED 0001:PWM 0010:XOUT 0011:GPIOH[0]
	[19:16]	R/W	0010	BIT_REG_IOCFG_LED_S3	Pinmux selection 0000:LED 0001:PWM 0010:GPIOH[1] 0011:DBG
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
0838h	REG_PINMUX_14				

	[31:28]	R/W	0010	BIT_REG_IOCFG_LED_P0	Pinmux selection 0000:LED 0001:MIIM 0010:GPIOH[2] 0011:DBG
	[27:24]	R/W	0	--	Reserved
	[23:20]	R/W	0	--	Reserved
	[19:16]	R/W	0	--	Reserved
	[15:12]	R/W	0	--	Reserved
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved
083Ch	REG_PINMUX_15				
	[31:28]	R/W	0	BIT_REG_IOCFG_MMC_D0	Pinmux selection 0000:MMC 0001:IIS 0010:UART1 0011:UART2 0100:NAND 0101:GPIOD[1] 0110:DBG
	[27:24]	R/W	0	BIT_REG_IOCFG_MMC_D1	Pinmux selection 0000:MMC 0001:IIS 0010:UART1 0011:UART2 0100:NAND 0101:GPIOD[2] 0110:DBG
	[23:20]	R/W	0	BIT_REG_IOCFG_MMC_D2	Pinmux selection 0000:MMC 0001:IIS 0010:UART1 0011:UART2 0100:NAND

					0101:GPIOD[3] 0110:DBG
	[19:16]	R/W	0	BIT_REG_IOCFG_MMC_D3	Pinmux selection 0000:MMC 0001:IIS 0010:UART1 0011:UART2 0100:NAND 0101:GPIOD[4] 0110:DBG
	[15:12]	R/W	0	BIT_REG_IOCFG_MMC_D4	Pinmux selection 0000:MMC 0001:SPI1 0010:IISV 0011:IISA 0100:UART1 0101:PCM 0110:PWM 0111:GPIOD[5] 1000:DBG
	[11:8]	R/W	0	BIT_REG_IOCFG_MMC_D5	Pinmux selection 0000:MMC 0001:SPI1 0010:IIS 0011:UART1 0100:PCM 0101:PWM 0110:GPIOD[6] 0111:DBG

	[7:4]	R/W	0	BIT_REG_IOCFG_MMC_D6	Pinmux selection 0000:MMC 0001:SPI1 0010:I2C0 0011:I2C0_S 0100:UART1 0101:PCM 0110:PWM 0111:GPIOD[7] 1000:DBG
	[3:0]	R/W	0	BIT_REG_IOCFG_MMC_D7	Pinmux selection 0000:MMC 0001:SPI1 0010:SPI1_3W 0011:I2C0 0100:UART1 0101:PCM 0110:PWM 0111:GPIOE[0] 1000:DBG
0840h	REG_PINMUX_16				
	[31:28]	R/W	0	--	Reserved
	[27:24]	R/W	0	--	Reserved
	[23:20]	R/W	0	--	Reserved
	[19:16]	R/W	0	BIT_REG_IOCFG_MMC_RST	Pinmux selection 0000:MMC 0001:SPI0 0010:GPIOC[4] 0011:DBG

	[15:12]	R/W	0	BIT_REG_IOCFG_MMC_WP	Pinmux selection 0000:MMC 0001:SPI0 0010:SPI1 0011:IIS 0100:UART1 0101:EVENT 0110:GPIOC[5] 0111:DBG
	[11:8]	R/W	0	BIT_REG_IOCFG_MMC_CD	Pinmux selection 0000:MMC 0001:SPI0 0010:SPI0_3W 0011:SPI1 0100:SPI1_3W 0101:IIS 0110:UART1 0111:EVENT 1000:GPIOC[6] 1001:DBG
	[7:4]	R/W	0	BIT_REG_IOCFG_MMC_CLK	Pinmux selection 0000:MMC 0001:SPI0 0010:SPI1 0011:IIS 0100:EVENT 0101:GPIOC[7] 0110:DBG
	[3:0]	R/W	0	BIT_REG_IOCFG_MMC_CMD	Pinmux selection 0000:MMC 0001:SPI0 0010:SPI1 0011:IIS 0100:EVENT 0101:GPIOD[0] 0110:DBG

0844h	REG_PINMUX_17				
	[31:28]	R/W	0	BIT_REG_IOCFG_WBB0	Pinmux selection 0000:WLAN 0001:GPIOE[1] 0010:DBG
	[27:24]	R/W	0	BIT_REG_IOCFG_WBB1	Pinmux selection 0000:WLAN 0001:GPIOE[2] 0010:DBG
	[23:20]	R/W	0	BIT_REG_IOCFG_WBB2	Pinmux selection 0000:WLAN 0001:GPIOE[3] 0010:DBG
	[19:16]	R/W	0	BIT_REG_IOCFG_WBB3	Pinmux selection 0000:WLAN 0001:GPIOE[4] 0010:DBG
	[15:12]	R/W	0	BIT_REG_IOCFG_WBB4	Pinmux selection 0000:WLAN 0001:GPIOE[5] 0010:DBG
	[11:8]	R/W	0	BIT_REG_IOCFG_WBB5	Pinmux selection 0000:WLAN 0001:GPIOE[6] 0010:DBG
	[7:4]	R/W	0	BIT_REG_IOCFG_WBB6	Pinmux selection 0000:WLAN 0001:GPIOE[7] 0010:DBG
	[3:0]	R/W	0	BIT_REG_IOCFG_WBB7	Pinmux selection 0000:WLAN 0001:GPIOF[0] 0010:DBG
0848h	REG_PINMUX_18				

	[31:28]	R/W	0	BIT_REG_IOCFG_WBB8	Pinmux selection 0000:WLAN 0001:XOUT 0010:GPIOF[1] 0011:DBG
	[27:24]	R/W	0	BIT_REG_IOCFG_WBB9	Pinmux selection 0000:WLAN 0001:SPI0 0010:IIS 0011:EVENT 0100:GPIOF[2] 0101:DBG
	[23:20]	R/W	0	BIT_REG_IOCFG_WBB10	Pinmux selection 0000:WLAN 0001:SPI0 0010:IIS 0011:EVENT 0100:GPIOF[3] 0101:DBG
	[19:16]	R/W	0	BIT_REG_IOCFG_WBB11	Pinmux selection 0000:WLAN 0001:SPI0 0010:IIS 0011:I2C1 0100:EVENT 0101:XOUT 0110:GPIOF[4] 0111:DBG
	[15:12]	R/W	0	BIT_REG_IOCFG_WBB12	Pinmux selection 0000:WLAN 0001:SPI0 0010:SPI0_3W 0011:IIS 0100:I2C1 0101:EVENT 0110:GPIOF[5]

					0111:DBG
	[11:8]	R/W	0	--	Reserved
	[7:4]	R/W	0	--	Reserved
	[3:0]	R/W	0	--	Reserved

9. Switch Core Control

9.1. Global Port Control Register

9.1.1. Global Port Control Register Address Mapping (Base:0xBB80_4000)

The RTL8197F provides an MDC/MDIO (Management Data Clock/Management Data Input/Output) interface to access external PHYs. As the MDC/MDIO interface is relatively slow, the access is divided into command and status registers.

Table 29. Global Port Control Register Address Mapping (Base: 0xBB80_4000)

Offset	Size (byte)	Name	Description
04	4	MDCIOCR	MDC/MDIO Command Register.
08	4	MDCIOSR	MDC/MDIO Status Register.

9.1.2. Global MDC/MDIO Command Register (0xBB80_4004)

Table 30. Global MDC/MDIO Command Register (0xBB80-4004)

Reg.bit	Name	Description	Mode	Default
31	COMMAND	MDC/MDIO Command Type. 0: Read Access 1: Write Access *Note: The procedure to access the internal/ external PHY via the MDC/MDIO interface is as follows:* *1. Define the PHY address (PHYADD), register address (REGADD)* *2. Define the write data content for write command (WRDATA)* *3. Identify the command type (COMMAND)* *4. Get the command execution status (STATUS) and read data content (RDATA)*	RW	0B
30:29	-	Reserved.	-	-
28:24	PHYADD[4:0]	PHY Address of MDC/MDIO Command.	RW	00000B
23:21	-	Reserved.	-	-
20:16	REGADD[4:0]	Register Address of MDC/MDIO Command.	RW	00000B
15:0	WRDATA[15:0]	Write Data of MDC/MDIO Command.	RW	0000H

9.1.3. Global MDC/MDIO Status Register (0xBB80_4008)

Table 31. Global MDC/MDIO Status Register (0xBB80_4008)

Reg.bit	Name	Description	Mode	Default
31	STATUS	MDC/MDIO Command in Process Status. 0: Process done 1: In progress	R	0000B
30	Read error	MII management frame reading error Detect a read/write turn around bit error .	R	0B
29:16	-	Reserved.	-	-

Reg.bit	Name	Description	Mode	Default
15:0	RDATA	Read Data Result of MDC/MDIO Command.	R	0B

9.1.4. Global Frame Filtering Control Register Address Mapping (Base:0xBB80_4000)

Table 32. Global Frame Filtering Control Register Address Mapping (Base: 0xBB80_4000)

Offset	Size (byte)	Name	Description
44	4	BSCR	Broadcast Storm Control Register.

9.1.5. Global Broadcast Storm Control Register (0xBB80_4044)

Per-port broadcast storm traffic utilization is a global parameter that is defined by BCSC_CNT[14:0] in the Broadcast Storm Control Register (0xBB80-4044). Broadcast storm control can be enabled/disabled on a per-port basis, and the broadcast traffic definition is user configurable.

Table 33. Global Broadcast Storm Control Register (0xBB80_4044)

Reg.bit	Name	Description	Mode	Default
31:15	-	Reserved.	-	-
14:0	BCSC_CNT[14:0]	Broadcast Storm Control Rate Configuration. Defines the per-port-based broadcast storm control valid accumulated byte count in each default time interval 25ms/2.5ms/0.25ms for 10M/100M/1000M (the time interval will auto update for different port link speeds). For BCSC_BCNT[14:0] value=N. The % max rate=N/30360*100%. The storm packet types (broadcast or multicast) can be selected by BCSC_Types[2:0] in Port Configuration Register.	RW	0

Note: When Broadcast Storm Control is enabled, every 25ms, each port will limit the max incoming byte counts of broadcast, multicast, or unknown-unicast packets to 3 counts maximum. Other excessive packets within the duration time will be dropped.

9.2. Per-Port Configuration Register

All five switch port interfaces of the RTL8197F can be individually configured as either 10/100Mbps UTP or RGMII/GMII/MII via Port Interface Control registers.

The port ability properties, e.g., auto negotiation, port speed, duplex, flow control, can be configured via the Per-Port Configuration Register.

Table 34. Per-Port Configuration Register Address Mapping (Base: 0xBB80_4100)

Offset	Size (byte)	Name	Description
00	4	PITCR	Port Interface Type Control Register.
04	4	PCRP0	Port Configuration Register of Port 0.
08	4	PCRP1	Port Configuration Register of Port 1.
0C	4	PCRP2	Port Configuration Register of Port 2.
10	4	PCRP3	Port Configuration Register of Port 3.
14	4	PCRP4	Port Configuration Register of Port 4.
1C	4	PCRP6	Port Configuration Register of Port 6 (Ext. P0).
20	4	PCRP7	Port Configuration Register of Port 7 (Ext. P1).
24	4	PCRP8	Port Configuration Register of Port 8 (Ext. P2).
28	4	PSRP0	Port Status Register of Port 0.
2C	4	PSRP1	Port Status Register of Port 1.
30	4	PSRP2	Port Status Register of Port 2.
34	4	PSRP3	Port Status Register of Port 3.
38	4	PSRP4	Port Status Register of Port 4.
40	4	PSRP6	Port Status Register of Port 6.
44	4	PSRP7	Port Status Register of Port 7.
48	4	PSRP8	Port Status Register of Port 8.
4C	4	P0GMIICR	Port-0 GMII Configuration Register.

9.2.1. Port Interface Type Control Register (0xBB80_4100)

Table 35. Port Interface Type Control Register (0xBB80_4100)

Reg.bit	Name	Description	Mode	Default
31:10	-	Reserved.	-	-
9:8	Reserved		R	00B
9:8	Port4_TypeCfg[1:0]	Port 4 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
7:6	Port3_TypeCfg[1:0]	Port 3 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
5:4	Port2_TypeCfg[1:0]	Port 2 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
3:2	Port1_TypeCfg[1:0]	Port 1 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
1:0	Port0_TypeCfg[1:0]	Port 0 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01 : GMII/MII/RGMII interface 10 :Reserved 11 : reserved	RW	00B

9.2.2. Port Configuration Register of Port N (N=0~4)

Table 36. Port Configuration Register of Port N (N=0~4)

Reg.bit	Name	Description	Mode	Default
31	ByPassTCRC	1: Do not recalculate CRC for frame ; Do not recalculate CRC for L2/L3/L4 modified frame. 0: Recalculate CRC for frame ; Recalculate CRC for L2/L3/L4 modified frame.	RW	0B
30:26	ExtPHYID[4:0]	External PHY ID Assign for PHY MII Register Polling Addressing. Identifies the external PHY ID for MDC/MDIO polling addressing. Only valid for ports 0 and port 5. The value should be modied to avoid being the same as embedded PHY's ID and should not set as 0x0. (Note that PHY ID value 0x0 is not valid for normal PHY setting , because value 0x0 is broadcast PHY ID)	RW	Port0~5=0x10~0x15
5	EnForceMode	Enable Port Property (Link/Speed/Duplex/Flow Control) to be Set by Force Mode. 0: Disable (enable Auto-Negotiation) In this mode, the port link/speed/duplex /flow control setting is based on the MDC/MDIO polling result. 1: Enable (Force Mode) (Disable Auto-Negotiation) In this mode, the port speed/duplex /flow control setting is set by the force mode control bits in this register. Note that the method of determining the link status depends on the PollinkStatus setting. In this mode MDC/MDIO polling of the external PHY access for this Giga port will be disabled.	RW	0
24	PollinkStatus	Polling PHY Link Status {EnForceMode, PollinkStatus}. 00, 01: Enable Auto-Negotiation 10: ForceMode. Disables Auto-Negotiation (this mode should be set for MAC-to-MAC connection) 11: ForceMode with polling link status. Disables Auto-Negotiation but polls the PHY's link status	RW	0
23	ForceLink	Force Link-Up or Link-Down Setting. Available Only If {EnForceMode, PollinkStatus}=10. 0: Force link down 1: Force link up *Note: If {EnForceMode, PollinkStatus}=11, the link status information is derived from PHY register 1 via the ASIC's auto-polling mechanism.*	RW	0

Reg.bit	Name	Description	Mode	Default
22:18	FrcAbi_AnAbi_sel	If EnForceMode=1, FrcAbi_AnAbi_sel is used to indicate the force mode operation for MAC or PHY mode operations. FrcAbi_AnAbi_sel[0]: ForceDuplex 1: Force FULL duplex 0: Force HALF duplex FrcAbi_AnAbi_sel[2:1]: ForceSpeed 00: Force 10Mbps 01: Force 100Mbps 10: Reserved 11: Reserved FrcAbi_AnAbi_sel[4:3]: Reserved. If EnForceMode=0, FrcAbi_AnAbi_sel is used to indicate Auto-Negotiation advertising ability. FrcAbi_AnAbi_sel[0]: 10Mbps Half-duplex FrcAbi_AnAbi_sel[1]: 10Mbps Full-duplex FrcAbi_AnAbi_sel[2]: 100Mbps Half-duplex FrcAbi_AnAbi_sel[3]: 100Mbps Full-duplex FrcAbi_AnAbi_sel[4]: Reserved	RW	5'b11111 for port#0~4
17:16	PauseFlowControl[1:0] (ADVERTISE_ PAUSEABY)	If EnForceMode=1, this register controls PAUSE flow control. 0: Enable TX pause ability 1: Enable RX pause ability If EnForceMode=0, the PHY advertises PAUSE flow control. 0: PAUSE operation for full duplex links 1: Asymmetric PAUSE operation for full duplex links	RW	2'b11
15:12	-	Reserved	-	-
11:9	BCSC_Types[2:0]	Broadcast Storm Control Packet Types Selection. When Broadcast storm control is enabled, the control packet types can be selected. Bit[0]: Enable control for broadcast packets Bit[1]: Enable control for multicast packet Bit[2]: Reserved 0: Disable 1: Enable When Bit[3:0] are set as '000', the port's broadcast storm function is disabled.	RW	0B
8	EnBCSC	Enable Broadcast Storm Control. 0: Disable 1: Enable When enabled, the broadcast storm control rate and control packet type should be defined in the broadcast storm control register.	RW	0B

<table>
<tr><th>Reg.bit</th><th>Name</th><th>Description</th><th>Mode</th><th>Default</th></tr>
<tr><td>7</td><td>EnLoopBack</td><td>Enable MAC – PHY Interface for MII Loopback.
Enable internal and external loopback. Sets the MAC as an internal loopback, and sets the PHY side as an external loopback.
0: Disable 1: Enable</td><td>RW</td><td>0B</td></tr>
<tr><td>6</td><td>DisBKP</td><td>Per-Port Disable Backpressure Function for Half Duplex Mode.
1: Disable 0: Enable</td><td>RW</td><td>0B</td></tr>
<tr><td>5:4</td><td>STP_PortST[1:0]</td><td>Spanning Tree Protocol Port State Control.
00: Disable State 01: Blocking/Listen State
10: Learning State 11: Forwarding State
<table>
<tr><th>802.1d Port State</th><th>Pass Received Non-BPDU Frames</th><th>Pass Received BPDU Frames</th><th>Learning Station Location Into Address Database</th></tr>
<tr><td>Disabled</td><td>No</td><td>No</td><td>No</td></tr>
<tr><td>Blocking</td><td>No</td><td>Yes</td><td>No</td></tr>
<tr><td>Listening</td><td>No</td><td>Yes</td><td>No</td></tr>
<tr><td>Learning</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>Forwarding</td><td>Yes</td><td>Yes</td><td>Yes</td></tr>
</table></td><td>RW</td><td>11</td></tr>
<tr><td>3</td><td>MAC S/W Reset</td><td>MAC S/W Reset supports a method to reset the MAC by software. It can reset the circuit in the RXC and TXC domain via an active-low signal. To reset the MAC, software should write a 1 following the writing of a 0 .
0: Reset state
1: Normal state</td><td>RW</td><td>1</td></tr>
<tr><td>2:1</td><td>AcptMaxLen[1:0]</td><td>Configures the Maximum Acceptable Packet Length Supported.
This control is valid only when jumbo packet accept is disabled on a port.
00: 1536 bytes
01: 1552 bytes
10: 9k bytes (jumbo packet: 9216 bytes)
11: 16k-14 bytes (jumbo packet: 16370 bytes)</td><td>RW</td><td>00B</td></tr>
<tr><td>0</td><td>EnablePHYIf</td><td>Enable PHY Interface.
The bit controls the MAC vs. PHY interface, irrelevant as to whether the port interface is UTP or GMII/RGMII/MII modes.
0: Disable
When disabled, the PHY interface will be isolated from the MAC. Packets will not be transmitted or received to/from the PHY to/from the MAC interface (internal GMII/MII interface).
1: Enable</td><td>RW</td><td>0B</td></tr>
</table>

9.2.3. Port Status Register of Port N (N=0~4)

Table 37. Port Status Register of Port N (N=0~4)

Reg.bit	Name	Description	Mode	Default
31:14	-	Reserved.	-	-
13:12	EEE Status[1:0]	Port Link Status. In NWay Mode, the status shown is that of PHY local and PHY remote ability. In Force mode, the status is the configuration result of the force mode configuration registers. Bit 1: Reserved Bit 0: 100M EEE ability	R	0
11:9	-	Reserved.	-	-
8	LinkDownEventFlag	Port Link Down Event Detection Monitor Flag 0: Idle 1: Link Down event detected When the Port link status changes from link-up to link-down, the flag bit will be latched as '1' until read to clear and updated to the new status.	Latch, RW	0
7:0	PortStatus[7:0]	Port Link Status In an NWay Mode port, the status shown is that of PHY local and PHY remote ability. In Force mode, the status is the configuration result of the force mode configuration registers. This report is valid for UTP or GMII/RGMII Interface mode. Bit 7: NWay Enable (link by auto-negotiation) Bit 6: RX PAUSE ability Bit 5: TX PAUSE ability Bit 4: LinkUp Bit 3: Duplex Bit 2: Reserved Bit [1:0] LinkSpeed[1:0] LinkSpeed[1:0]: 00: 10M 01: 100M 10: Reserved 11: Reserved	R	0

9.2.4. Port0_GMII Configuration Register

Table 38. Port-0 GMII Configuration Register (0x BB80414C)

Reg.bit	Name	Description	Mode	Default
n.31: n.27	Reserved		R/W	0
n26	cf_txcputag	Enable Tx CPU tag	R/W	0
n25	cf_cputag_en	Enable CPU tag	R/W	0

Reg.bit	Name	Description	Mode	Default
n.24: n.23	CFG_GMAC[1:0]	GMII Port MAC interface Mode Configuration. The register default reflect the HW power on strapping value of H/W pin "CFG_GMAC[1:0]" . The register can be update by the host . **CFG_GMAC[1:0]** = 00 = RGMII mode , 01 = GMII/MII MAC mode , 10 = GMII/MII PHY mode , 11 = Reserved (Design Note: The GMAC interface mode change could not cause the system crashed)	R/W	0
n22	TurboMII	0: MII 1: Turbo MII	RW	0
n.21: n.20	Reserved		R/W	0
n.19: n.18	cf_sel_rgtxc_offset	RGMII TXC phase offset selection: 2'b00: offset 0ns 2'b01: offset 0.5ns 2'b10: offset 1.0ns 2'b11: offset 1.5ns	R/W	0
n.17: n.8	MediaTypeAddr[9:0]	MediaTypeStatus Register bit location address MediaTypeAddr[9:5]=RegA[4:0] (REG address) MediaTypeAddr[4:0]=BitLA[4:0] (Bit location address) **Note:** This bit is valid and be used only when the Gigabit PHY MII Register 15 report both 1000Base-T and 1000Base-X capability. This configuration bits direct RTL865xC to identify the correct link media type . The value is depend on the Gigabit PHY chip.	R/W	0x37D
n.7	FiberMTB_polarity	Fiber Media Type defined bit polarity To define the MediaTypeStatus Register bit definition. To tell the system whether "0 = Fiber mode" or "1 = fiber mode" are defined in the register that MediaTypeAddr[9:0] addressed . If write 0, it means that "0 = Fiber mode"; If write 1, it means that "1 = Fiber mode".	R/W	0
n.6	Conf_done	Port0 configuration is done to enable the frame reception and transmission.	R/W	0
n.5	cf_rgm_lp_en	Configure to enable RGMII LP mode.	R/W	0

Reg.bit	Name	Description	Mode	Default
n.4	RGMII_Tcomp[0]	RGMII Output Timing compensation control Add internal output delay to GTXC to implement the TXD setup time and hold time required spec for the receiver side. (1). For GMII mode: RGMII_Tcomp[0] : 1 : GTXC inverted output. (180 degree phase shift) 0 : notmal GTXC (2). For RGMII mode: 1 : GTXC delay 2 ns. 0 : normal NOTE: The delay timing value will be update based on IC the P&R result.	R/W	1'b0
n.3	Reserved			
n.2: n.0	RGMII_Rcomp[2:0]	GMII/RGMII Input Timing compensation control Add internal input delay to RXC to implement the RXD setup time and hold time required spec at the input side. GMII i/f --- GMII_Rcomp[2]([1:0] are useless) 0= 0ns 1= 4ns (use negative edge of RXC) RGMII i/f --- RGMII_Rcomp[2:0] 000 = 0.0 ns 001 = 0.5 ns 010 = 1.0 ns ….. 111= 3.5 ns	R/W	3'b000

9.3. Switch LED Control Register

9.3.1. LED Topology Operation

The RTL8197F supports single Color LED displays topology. Below Table illustrates all combinations of LED topologies.

Table 39. Display Arrangement of Each DIRECT LED Mode

LED	LED Mode=DIRECT 0	LED Mode=DIRECT 1	LED Mode=DIRECT 2
Off	link down	10M Linkup	10M/ 100M Linkup
On	10M/100M/1000M Linkup	100M/1000M Linkup	1000M Linkup
Fast Blink	Act	Act	Act
Slow Blink (if EEE LED enable)	LPI	LPI	LPI

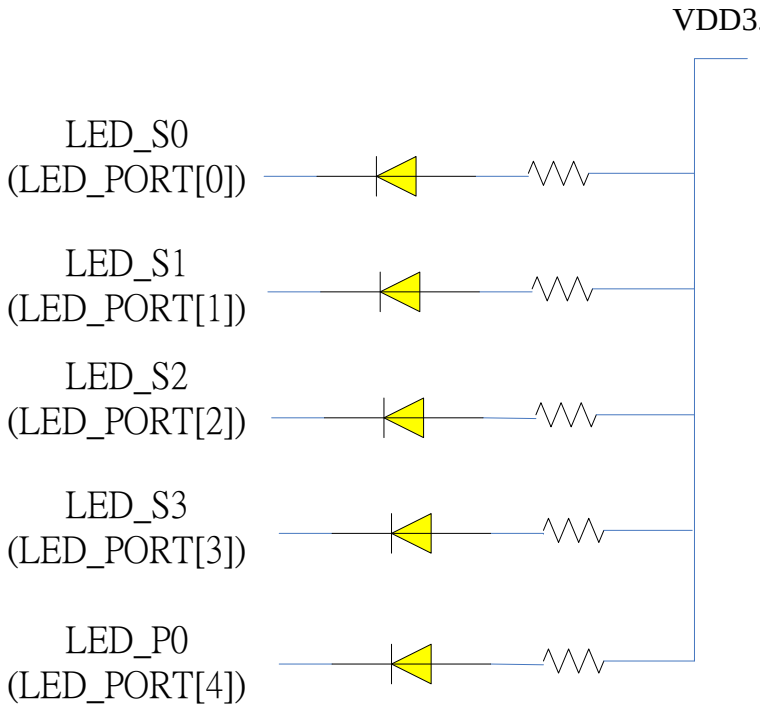


Figure 18. Single-Color LED interconnections

9.3.2. LED Control Register Address Mapping (Base: 0xBB80_4300)

Table 40. LED Control Register Address Mapping (Base: 0xBB80_4300)

Offset	Size (byte)	Name	Description
00	4	LEDCR0	LED Control Register 0.
04	4	LEDCR1	LED Control Register 1.
0C	4	LEDBCR	LED Blinking Control Register.
10	4	EEELCR	EEE LED Configuration Register.
14	4	DIRECTLCR	DIRECT Mode LED Configuration Register.

9.3.3. LED Control Register 0 (0xBB80_4300)

Table 41. LED Control Register 0 (0xBB80_4300)

Reg.bit	Name	Description	Mode	Default
31:22	-	Reserved.	-	-
21:20	LedTopology	LED Topology Selection. Selects the Scan mode of LED topology. 00: Reserved 01: Reserved 10: Direct mode Topology 11: Reserved	RW	0B

Reg.bit	Name	Description	Mode	Default
19:18	P0_LedDefSel[1:0]	Select P0 LED Display Mode Definition. Selects LED bit display definition. 00: Mode Direct 0 01: Mode Direct 1 10: Reserved 11: Reserved	RW	00B
17:16	P1_LedDefSel[1:0]	Select P1 LED Display Mode Definition.	RW	00B
15:14	P2_LedDefSel[1:0]	Select P2 LED Display Mode Definition.	RW	00B
13:12	P3_LedDefSel[1:0]	Select P3 LED Display Mode Definition.	RW	00B
11:10	P4_LedDefSel[1:0]	Select P4 LED Display Mode Definition.	RW	00B
9:8	-	Reserved.	-	-
7	DisLEDBlinking	Disable LED Initial Blinking. 0: Enable LED blinking 1: Disable LED blinking	RW	0B
6	BlinkTime	0: 40ms 1: 120ms	RW	0B
5	-	Reserved.	-	-
4:2	CPUCtrlMask[2:0]	CPU Control LED Masking. When any bit of CPUCtrlMask[2:0] is 0b, it means the corresponding LED is controlled by internal circuit. Conversely, when any bit of CPUCtrlMask[2:0] is 1b, the corresponding LED is controlled by CPU and the indication is controlled by CPUCtrlPort. 0: LED is controlled by internal circuit 1: LED is controlled by CPU CPUCtrlMask[2:0] are mapped to LED[2:0] respectively. The developer could make a specific LED display a designated mode through CPUCtrlPort without influencing other LEDs. The other LEDs will still operate with the LedTopology, EnBiColor, and LedType settings. This setting effects all ports.	RW	000B
1:0	-	Reserved.	-	-

9.3.4. LED Control Register 1 (0xBB80_4304)

Table 42. LED Control Register 1 (0xBB80_4304)

Reg.bit	Name	Description	Mode	Default
31:21	-	Reserved.	-	-
20:18	CPUCtrlPort0[2:0]	CPU Control Manner for Port 0. CPUCtrlPort0[2:0] are mapped to LED[2:0] respectively. Only valid when CPUCtorlMask bit is 1b. only LED0 is available. 0: LED off 1: LED on	RW	000B
17:15	CPUCtrlPort1[2:0]	CPU Control Mode for Port 1.	RW	000B
14:12	CPUCtrlPort2[2:0]	CPU Control Mode for Port 2.	RW	000B
11:9	CPUCtrlPort3[2:0]	CPU Control Mode for Port 3.	RW	000B
8:6	CPUCtrlPort4[2:0]	CPU Control Mode for Port 4.	RW	000B

Reg.bit	Name	Description	Mode	Default
5:0	-	Reserved.	-	-

9.3.5. LED Blinking Control Register (0xBB80_430C)

Table 43. LED Blinking Control Register (0xBB80_430C)

Reg.bit	Name	Description	Mode	Default
31:20	-	Reserved.	-	-
19:17	LEDBlinkP0[2:0]	CPU Controls the LED to Blink for Port 0. LEDBlinkP0[2:0] are mapped to LED[2:0] respectively. Only valid when CPUCtorlMask bit is 1b. only LED0 is available. 0: Disable LED blinking 1: Enable LED blinking When LED blinking is enabled, no matter whether the designated LED is on or off, the designated LED will be forced to start blinking until the CPU disables it.	RW	000B
16:14	LEDBlinkP1[2:0]	CPU Controls the LED to Blink for Port 1.	RW	000B
13:11	LEDBlinkP2[2:0]	CPU Controls the LED to Blink for Port 2.	RW	000B
10:8	LEDBlinkP3[2:0]	CPU Controls the LED to Blink for Port 3.	RW	000B
7:5	LEDBlinkP4[2:0]	CPU Controls the LED to Blink for Port 4.	RW	000B
4:0	-	Reserved.	-	-

9.3.6. EEE LED Configuration Register (0xBB80_4310)

Table 44. EEE LED Configuration Register (0xBB80_4310)

Reg.bit	Name	Description	Mode	Default
31:16	-	Reserved.	-	0
15:11	LPI_SBTOFF[4:0]	LPI Slow Blink Timer OFF-Period Time (Unit=100ms). Default=2000ms.	RW	0x14
10:6	LPI_SBTON[4:0]	LPI Slow Blink Timer ON-Period Time (Unit=100ms). Default=400ms.	RW	0x4
5:2	LPI_MT[3:0]	LPI Mask Off Time (Unit=100ms). To define the LED mask off time in a LPI LED state. Default=600ms.	RW	0xA
1	En10MLP	Enable 10Mbps port to show low power driving indication on LPI LED (same as the 10/100M port). 0: Disable 1: Enable	RW	0
0	enLPILED	Enable EEE LED Display Ability. 1: Enable 0: Disable *Note: When set to 1, the LPI LED display feature will remain disabled until after detecting a port has been linked-up for longer than 5 seconds.*	RW	0

9.3.7. Direct Mode LED Configuration Register (0xBB80_4314)

Table 45. Direct Mode LED Configuration Register (0xBB80_4314)

Reg.bit	Name	Description	Mode	Default
31	LEDOnPolarity	0: Normal Mode (LED output is Low active) 1: Reverse Mode (LED output is High active)	RW	0B
30:28	LEDBlinkTime	Blink Timer Period Time for All Port (Unit 40ms). 000: No blink 001: 40ms 010: 80ms 011: 120ms 100: 160ms 101: 200ms 110: 240ms 111: 280ms	RW	001B
27:18	-	Reserved.	-	-
17:15	LEDOnScaleP0[2:0]	Select the LED Turn On Scale for Port 0. 000: 12% 001: 25% 010: 37% 011: 50% 100: 62% 101: 75% 110: 87% 111: 100%	RW	111B
14:12	LEDOnScaleP1[2:0]	Select the LED Turn On Scale for Port 1.	RW	111B
11:9	LEDOnScaleP2[2:0]	Select the LED Turn On Scale for Port 2.	RW	111B
8:6	LEDOnScaleP3[2:0]	Select the LED Turn On Scale for Port 3.	RW	111B
5:3	LEDOnScaleP4[2:0]	Select the LED Turn On Scale for Port 4.	RW	111B
2:0	-	Reserved.	-	-

9.4. MIB Counters

This section describes the MIB counter provided by RTL8197F. The supported MIB counter includes MIB-II (RFC 1213), Ethernet-like MIB (RFC 3635), Interface Group MIB (RFC 2863), RMON MIB group 1,2,3,9 (RFC 2819), Bridge MIB (RFC 1493) and Bridge MIB Extension (RFC 2674). Each MIB counter associates with each physical port (include GMII port) and is divided into three types, which are In Counters, Out Counters and whole system Counters respectively. Table 8.1, 8.2, 8.3 and 8.4 define the registers for In/Out counters in each physical port.

Table 46. MIB Control Register Address Mapping (Base address: 0xBB80-1000)

Offset	Size (byte)	Name	Description	Field
000	4	MIBCR	MIB Control Register	

Table 47. MIB Control Register

Reg.bit	Name	Description	Mode	Default
n.31-n.19	Reserved		W/R	0x0
n.18	SysCounterReStart	Write '1' to reset Whole System Counter and restart counting	W/R	0x0
n.17	InCounterReStart_P8	Write '1' to reset all the inCounters and restart counting for port 8.	W/R	0x0
n.16	OutCounterReStart_P8	Write '1' to reset all the outCounters and restart counting for port 8.	W/R	0x0
n.15	InCounterReStart_P7	Write '1' to reset all the inCounters and restart counting for port 7.	W/R	0x0
n.14	OutCounterReStart_P7	Write '1' to reset all the outCounters and restart counting for port 7.	W/R	0x0
n.13	InCounterReStart_P6	Write '1' to reset all the inCounters and restart counting for port 6.	W/R	0x0
n.12	OutCounterReStart_P6	Write '1' to reset all the outCounters and restart counting for port 6.	W/R	0x0
n.11	InCounterReStart_P5	Write '1' to reset all the inCounters and restart counting for port 5.	W/R	0x0
n.10	OutCounterReStart_P5	Write '1' to reset all the outCounters and restart counting for port 5.	W/R	0x0
n.9	InCounterReStart_P4	Write '1' to reset all the inCounters and restart counting for port 4.	W/R	0x0
n.8	OutCounterReStart_P4	Write '1' to reset all the outCounters and restart counting for port 4.	W/R	0x0
n.7	InCounterReStart_P3	Write '1' to reset all the inCounters and restart counting for port 3.	W/R	0x0
n.6	OutCounterReStart_P3	Write '1' to reset all the outCounters and restart counting for port 3.	W/R	0x0
n.5	InCounterReStart_P2	Write '1' to reset all the inCounters and restart counting for port 2.	W/R	0x0
n.4	OutCounterReStart_P2	Write '1' to reset all the outCounters and restart counting for port 2.	W/R	0x0
n.3	InCounterReStart_P1	Write '1' to reset all the inCounters and restart counting for port 1.	W/R	0x0
n.2	OutCounterReStart_P1	Write '1' to reset all the outCounters and restart counting for port 1.	W/R	0x0
n.1	InCounterReStart_P0	Write '1' to reset all the inCounters and restart counting for port 0.	W/R	0x0
n.0	OutCounterReStart_P0	Write '1' to reset all the outCounters and restart counting for port 0.	W/R	0x0

Table 48. Whole System Counter Register Address Mapping (Base address: 0xBB80-1000)

Offset	Size (byte)	Name	Description	Field
080	4	dot1dTpLearnedEntryDiscards	Ref.	
084	4	EtherStatsCpuEventPkt		

Table 49. In Counter Register Address Mapping (Base address: 0xBB80-1000)

Offset	Size (byte)	Name	Description	Field
100	8	ifInOctets_P0		
108	4	ifInUcastPkts_P0		
10C	8	etherStatsOctets_P0		
114	4	etherStatsUndersizePkts_P0		
118	4	etherStatsFragments_P0		
11C	4	etherStatsPkts64Octets_P0		
120	4	etherStatsPkts65to127Octets_P0		
124	4	etherStatsPkts128to255Octets_P0		
128	4	etherStatsPkts256to511Octets_P0		
12C	4	etherStatsPkts512to1023Octets_P0		
130	4	etherStatsPkts1024to1518Octets_P0		
134	4	etherStatsOversizePkts_P0		
138	4	EtherStatsJabbers_P0		
13C	4	etherStatsMulticastPkts_P0		
140	4	etherStatsBroadcastPkts_P0		
144	4	dot1dTpPortInDiscards_P0		
148	4	etherStatsDropEvents_P0		
14C	4	dot3StatsFCSErrors_P0		
150	4	dot3StatsSymbolErrors_P0		
154	4	dot3ControlInUnknownOpcodes_P0		
158	4	dot3InPauseFrames_P0		
15C	4	inRxdvCnt_P0		
160	4	QMdiscardCnt_P0		
164 ~17C		Reserved		
180	8	ifInOctets_P1		
188	4	ifInUcastPkts_P1		
18C	8	etherStatsOctets_P1		
194	4	etherStatsUndersizePkts_P1		
198	4	etherStatsFragments_P1		
19C	4	etherStatsPkts64Octets_P1		
1A0	4	etherStatsPkts65to127Octets_P1		
1A4	4	etherStatsPkts128to255Octets_P1		
1A8	4	etherStatsPkts256to511Octets_P1		
1AC	4	etherStatsPkts512to1023Octets_P1		
1B0	4	etherStatsPkts1024to1518Octets_P1		

Offset	Size (byte)	Name	Description	Field
1B4	4	etherStatsOversizePkts_P1		
1B8	4	EtherStatsJabbers_P1		
1BC	4	etherStatsMulticastPkts_P1		
1C0	4	etherStatsBroadcastPkts_P1		
1C4	4	dot1dTpPortInDiscards_P1		
1C8	4	etherStatsDropEvents_P1		
1CC	4	dot3StatsFCSErrors_P1		
1D0	4	dot3StatsSymbolErrors_P1		
1D4	4	dot3ControlInUnknownOpcodes_P1		
1D8	4	dot3InPauseFrames_P1		
1DC	4	inRxdvCnt_P1		
1E0	4	QMdiscardCnt_P1		
1E4 ~1FC		Reserved		
200	8	ifInOctets_P2		
208	4	ifInUcastPkts_P2		
20C	8	etherStatsOctets_P2		
214	4	etherStatsUndersizePkts_P2		
218	4	etherStatsFragments_P2		
21C	4	etherStatsPkts64Octets_P2		
220	4	etherStatsPkts65to127Octets_P2		
224	4	etherStatsPkts128to255Octets_P2		
228	4	etherStatsPkts256to511Octets_P2		
22C	4	etherStatsPkts512to1023Octets_P2		
230	4	etherStatsPkts1024to1518Octets_P2		
234	4	etherStatsOversizePkts_P2		
238	4	etherStatsJabbers_P2		
23C	4	etherStatsMulticastPkts_P2		
240	4	etherStatsBroadcastPkts_P2		
244	4	dot1dTpPortInDiscards_P2		
248	4	etherStatsDropEvents_P2		
24C	4	dot3StatsFCSErrors_P2		
250	4	dot3StatsSymbolErrors_P2		
254	4	dot3ControlInUnknownOpcodes_P2		
258	4	dot3InPauseFrames_P2		
25C	4	inRxdvCnt_P2		
260	4	QMdiscardCnt_P2		
264 ~27C		Reserved		
280	8	ifInOctets_P3		
288	4	ifInUcastPkts_P3		
28C	8	etherStatsOctets_P3		
294	4	etherStatsUndersizePkts_P3		
298	4	etherStatsFragments_P3		

Offset	Size (byte)	Name	Description	Field
29C	4	etherStatsPkts64Octets_P3		
2A0	4	etherStatsPkts65to127Octets_P3		
2A4	4	etherStatsPkts128to255Octets_P3		
2A8	4	etherStatsPkts256to511Octets_P3		
2AC	4	etherStatsPkts512to1023Octets_P3		
2B0	4	etherStatsPkts1024to1518Octets_P3		
2B4	4	etherStatsOversizePkts_P3		
2B8	4	etherStatsJabbers_P3		
2BC	4	etherStatsMulticastPkts_P3		
2C0	4	etherStatsBroadcastPkts_P3		
2C4	4	dot1dTpPortInDiscards_P3		
2C8	4	etherStatsDropEvents_P3		
2CC	4	dot3StatsFCSErrors_P3		
2D0	4	dot3StatsSymbolErrors_P3		
2D4	4	dot3ControlInUnknownOpcodes_P3		
2D8	4	dot3InPauseFrames_P3		
2DC	4	inRxdvCnt_P3		
2E0	4	QMdiscardCnt_P3		
2E4 ~2FC		Reserved		
300	8	ifInOctets_P4		
308	4	ifInUcastPkts_P4		
30C	8	etherStatsOctets_P4		
314	4	etherStatsUndersizePkts_P4		
318	4	etherStatsFragments_P4		
31C	4	etherStatsPkts64Octets_P4		
320	4	etherStatsPkts65to127Octets_P4		
324	4	etherStatsPkts128to255Octets_P4		
328	4	etherStatsPkts256to511Octets_P4		
32C	4	etherStatsPkts512to1023Octets_P4		
330	4	etherStatsPkts1024to1518Octets_P4		
334	4	etherStatsOversizePkts_P4		
338	4	etherStatsJabbers_P4		
33C	4	etherStatsMulticastPkts_P4		
340	4	etherStatsBroadcastPkts_P4		
344	4	dot1dTpPortInDiscards_P4		
348	4	etherStatsDropEvents_P4		
34C	4	dot3StatsFCSErrors_P4		
350	4	dot3StatsSymbolErrors_P4		
354	4	dot3ControlInUnknownOpcodes_P4		
358	4	dot3InPauseFrames_P4		
35C	4	inRxdvCnt_P4		
360	4	QMdiscardCnt_P4		

Offset	Size (byte)	Name	Description	Field
364 ~37C		Reserved		
380	8	ifInOctets_P5		
388	4	ifInUcastPkts_P5		
38C	8	etherStatsOctets_P5		
394	4	etherStatsUndersizePkts_P5		
398	4	etherStatsFragments_P5		
39C	4	etherStatsPkts64Octets_P5		
3A0	4	etherStatsPkts65to127Octets_P5		
3A4	4	etherStatsPkts128to255Octets_P5		
3A8	4	etherStatsPkts256to511Octets_P5		
3AC	4	etherStatsPkts512to1023Octets_P5		
3B0	4	etherStatsPkts1024to1518Octets_P5		
3B4	4	etherStatsOversizePkts_P5		
3B8	4	etherStatsJabbers_P5		
3BC	4	etherStatsMulticastPkts_P5		
3C0	4	etherStatsBroadcastPkts_P5		
3C4	4	dot1dTpPortInDiscards_P5		
3C8	4	etherStatsDropEvents_P5		
3CC	4	dot3StatsFCSErrors_P5		
3D0	4	dot3StatsSymbolErrors_P5		
3D4	4	dot3ControlInUnknownOpcodes_P5		
3D8	4	dot3InPauseFrames_P5		
3DC	4	inRxdvCnt_P5		
3E0	4	QMdiscardCnt_P5		
3E4 ~3FC		Reserved		
400	8	ifInOctets_Ext0		
408	4	ifInUcastPkts_ Ext0		
40C	8	etherStatsOctets_ Ext0		
414	4	etherStatsUndersizePkts_ Ext0		
418	4	etherStatsFragments_ Ext0	X	
41C	4	etherStatsPkts64Octets_ Ext0		
420	4	etherStatsPkts65to127Octets_ Ext0		
424	4	etherStatsPkts128to255Octets_ Ext0		
428	4	etherStatsPkts256to511Octets_ Ext0		
42C	4	etherStatsPkts512to1023Octets_ Ext0		
430	4	etherStatsPkts1024to1518Octets_ Ext0		
434	4	etherStatsOversizePkts_ Ext0		
438	4	etherStatsJabbers_ Ext0		
43C	4	EtherStatsMulticastPkts_ Ext0		
440	4	etherStatsBroadcastPkts_ Ext0		
444	4	dot1dTpPortInDiscards_Ext0		
448	4	etherStatsDropEvents_Ext0		

Offset	Size (byte)	Name	Description	Field
44C	4	dot3StatsFCSErrors_ Ext0		
450	4	dot3StatsSymbolErrors_ Ext0	X	
454	4	dot3ControlInUnknownOpcodes_ Ext0		
458	4	dot3InPauseFrames_ Ext0		
45C	4	inRxdvCnt_Ext0		
460	4	QMdiscardCnt_Ext0		
464 ~47C		Reserved		
480	8			
488	4			
48C	8			
494	4			
498	4			
49C	4			
4A0	4			
4A4	4			
4A8	4			
4AC	4			
4B0	4			
4B4	4			
4B8	4			
4BC	4			
4C0	4			
4C4	4			
4C8	4			
4CC	4			
4D0	4			
4D4	4			
4D8	4			
4DC ~4FC				
500	8			
508	4			
50C	8			
514	4			
518	4			
51C	4			
520	4			
524	4			
528	4			
52C	4			
530	4			
534	4			
538	4			

Offset	Size (byte)	Name	Description	Field
53C	4			
540	4			
544	4			
548	4			
54C	4			
550	4			
554	4			
558	4			

Table 50. Out Counter Register Address Mapping (Base address: 0xBB80-1000)

Offset	Size (byte)	Name	Description	Field
800	8	ifOutOctets_P0		
808	4	ifOutUcastPkts_P0		
80C	4	ifOutMulticastPkts_P0		
810	4	ifOutBroadcastPkts_P0		
814	4	ifOutDiscards_P0		
818	4	dot3StatsSingleCollisionFrames_P0		
81C	4	dot3StatsMultipleCollisionFrames_P0		
820	4	dot3StatsDeferredTransmissions_P0		
824	4	dot3StatsLateCollisions_P0		
828	4	dot3StatsExcessiveCollisions_P0		
82C	4	dot3OutPauseFrames_P0		
~~830~~	~~4~~			
834	4	etherStatsCollisions_P0		
880	8	ifOutOctets_P1		
888	4	ifOutUcastPkts_P1		
88C	4	ifOutMulticastPkts_P1		
890	4	ifOutBroadcastPkts_P1		
894	4	ifOutDiscards_P1		
898	4	dot3StatsSingleCollisionFrames_P1		
89C	4	dot3StatsMultipleCollisionFrames_P1		
8A0	4	dot3StatsDeferredTransmissions_P1		
8A4	4	dot3StatsLateCollisions_P1		
8A8	4	dot3StatsExcessiveCollisions_P1		
8AC	4	dot3OutPauseFrames_P1		
~~8B0~~	4			
8B4	4	etherStatsCollisions_P1		
900	8	ifOutOctets_P2		
908	4	ifOutUcastPkts_P2		

Offset	Size (byte)	Name	Description	Field
90C	4	ifOutMulticastPkts_P2		
910	4	ifOutBroadcastPkts_P2		
914	4	ifOutDiscards_P2		
918	4	dot3StatsSingleCollisionFrames_P2		
91C	4	dot3StatsMultipleCollisionFrames_P2		
920	4	dot3StatsDeferredTransmissions_P2		
924	4	dot3StatsLateCollisions_P2		
928	4	dot3StatsExcessiveCollisions_P2		
92C	4	dot3OutPauseFrames_P2		
~~930~~	~~4~~			
934	4	etherStatsCollisions_P2		
980	8	ifOutOctets_P3		
988	4	ifOutUcastPkts_P3		
98C	4	ifOutMulticastPkts_P3		
990	4	ifOutBroadcastPkts_P3		
994	4	ifOutDiscards_P3		
998	4	dot3StatsSingleCollisionFrames_P3		
99C	4	dot3StatsMultipleCollisionFrames_P3		
9A0	4	dot3StatsDeferredTransmissions_P3		
9A4	4	dot3StatsLateCollisions_P3		
9A8	4	dot3StatsExcessiveCollisions_P3		
9AC	4	dot3OutPauseFrames_P3		
~~9B0~~	~~4~~			
9B4	4	etherStatsCollisions_P3		
A00	8	ifOutOctets_P4		
A08	4	ifOutUcastPkts_P4		
A0C	4	ifOutMulticastPkts_P4		
A10	4	ifOutBroadcastPkts_P4		
A14	4	ifOutDiscards_P4		
A18	4	dot3StatsSingleCollisionFrames_P4		
A1C	4	dot3StatsMultipleCollisionFrames_P4		
A20	4	dot3StatsDeferredTransmissions_P4		
A24	4	dot3StatsLateCollisions_P4		
A28	4	dot3StatsExcessiveCollisions_P4		
A2C	4	dot3OutPauseFrames_P4		
~~A30~~	~~4~~			
A34	4	etherStatsCollisions_P4		
A80	8	ifOutOctets_P5		
A88	4	ifOutUcastPkts_P5		
A8C	4	ifOutMulticastPkts_P5		
A90	4	ifOutBroadcastPkts_P5		
A94	4	ifOutDiscards_P5		
A98	4	dot3StatsSingleCollisionFrames_P5		
A9C	4	dot3StatsMultipleCollisionFrames_P5		

Offset	Size (byte)	Name	Description	Field
AA0	4	dot3StatsDeferredTransmissions_P5		
AA4	4	dot3StatsLateCollisions_P5		
AA8	4	dot3StatsExcessiveCollisions_P5		
AAC	4	dot3OutPauseFrames_P5		
~~AB0~~	~~4~~			
AB4	4	etherStatsCollisions_P5		
B00	8	ifOutOctets_Ext0		
B08	4	IfOutUcastPkts_Ext0		
B0C	4	ifOutMulticastPkts_Ext0		
B10	4	ifOutBroadcastPkts_Ext0		
B14	4	ifOutDiscards_Ext0		
B18	4	dot3StatsSingleCollisionFrames_Ext0	X	
B1C	4	dot3StatsMultipleCollisionFrames_Ext0	X	
B20	4	dot3StatsDeferredTransmissions_Ext0	X	
B24	4	dot3StatsLateCollisions_Ext0	X	
B28	4	dot3StatsExcessiveCollisions_Ext0	X	
B2C	4	dot3OutPauseFrames_Ext0		
~~B30~~	~~4~~			
B34	4	etherStatsCollisions_ Ext0	X	
B80	8			
B88	4			
B8C	4			
B90	4			
B94	4			
B98	4			
B9C	4			
BA0	4			
BA4	4			
BA8	4			
BAC	4			
BB0	4			
BB4	4			
C00	8			
C08	4			
C0C	4			
C10	4			
C14	4			
C18	4			
C1C	4			
C20	4			
C24	4			
C28	4			
C2C	4			

Offset	Size (byte)	Name	Description	Field
C30	4			
C34	4			

Table 51. Whole System Counter Register

Reg.bit	Name	Description	Mode	Default
n.31-n.0	dot1dTpLearnedEntryDiscards		R	00000000H
n.31-n.0	etherStatsCpuEvent		R	00000000H

Table 52. In Counter Register

Reg.bit	Name	Description	Mode	Default
n63.-n0	ifInOctets		R	00000000H
n31.-n0	IfInUcastPkts		R	00000000H
n63.-n0	EtherStatsOctets		R	00000000H
n31.-n0	etherStatsUndersizePkts		R	00000000H
n31.-n0	etherStatsFragments		R	00000000H
n31.-n0	etherStatsPkts64Octets		R	00000000H
n31.-n0	etherStatsPkts65to127Octets		R	00000000H
n31.-n0	etherStatsPkts127to255Octets		R	00000000H
n31.-n0	etherStatsPkts256to511Octets		R	00000000H
n31.-n0	etherStatsPkts512to1023Octets		R	00000000H
n31.-n0	etherStatsPkts1024to1518Octets		R	00000000H
n31.-n0	etherStatsOversizePkts		R	00000000H
n31.-n0	EtherStatsJabbers		R	00000000H
n31.-n0	etherStatsMulticastPkts		R	00000000H
n31.-n0	etherStatsBroadcastPkts		R	00000000H
n31.-n0	etherStatsDropEvents		R	00000000H
n31.-n0	dot1dTpPortInDiscards		R	00000000H
n31.-n0	dot3StatsFCSErrors		R	00000000H
n31.-n0	dot3StatsSymbolErrors		R	00000000H
n31.-n0	dot3ControlInUnknownOpcodes		R	00000000H
n31.-n0	dot3InPauseFrames		R	00000000H

Table 53. Out Counter Register

Reg.bit	Name	Description	Mode	Default
n.63-n.0	ifOutOctets		R	00000000H
n.31-n.0	ifOutUcastPkts		R	00000000H
n.31-n.0	ifOutMulticastPkts		R	00000000H
n.31-n.0	ifOutBroadcastPkts		R	00000000H
n.31-n.0	ifOutDiscards		R	00000000H
n.31-n.0	dot3StatsSingleCollisionFrames		R	00000000H
n.31-n.0	dot3StatsMultipleCollisionFrames		R	00000000H
n.31-n.0	dot3StatsDeferredTransmissions		R	00000000H
n.31-n.0	dot3StatsLateCollisions		R	00000000H

Reg.bit	Name	Description	Mode	Default
n.31-n.0	dot3StatsExcessiveCollisions		R	00000000H
n.31-n.0	dot3OutPauseFrames		R	00000000H
~~n.31-n.0~~	~~dot1dBasePortDelayExceededDiscards~~		~~R~~	~~00000000H~~
n.31-n.0	etherStatsCollisions		R	00000000H

Table 54. The Definition of MIB Counter

Name	*condition*	*From*	*Framing*	*CRC*	*Definition*	*Check*
ifInOctets (64-bit)	frame size ≥ 64 bytes (include PASUE frame !)	**DA**	**Good**	**Good**	The total number of octets in received ***valid***[1] frames on the interface, including MAC header and FCS, but not the preamble, start of frame or extension octets.	**V**
ifInUcastPkts (32-bit)	frame size ≥ 64 bytes	**DA**	**G**	**G**	The number of received ***valid***[1] unicast packets.	V
etherStatsOctets (64-bit)	frame size > 0 byte	**DA**	**X**	X	The total number of octets in ***all***[2] received frames on the interface, including MAC header and FCS, but not the preamble, start of frame or extension octets.	V
etherStatsUndersizePkts (32-bit)	frame size < 64 bytes	**DA**	**G**	**G**	The number of received ***valid***[1] packets whose size are less than 64 bytes, including MAC header and FCS, excluding preamble and SFD.	**V**
etherStatsFragments (32-bit)	frame size < 64 bytes	**DA**	**B**	**B**	The number of received ***invalid***[3] packets whose size are less than 64 bytes, including MAC header and FCS, excluding preamble and SFD.	V
etherStatsPkts64Octets (32-bit)	frame size = 64 bytes	**DA**	**X**	**X**	The number of ***all***[2]received packets whose size are exactly 64 bytes, including MAC header and FSC, excluding preamble and SFD.	V
etherStatsPkts65to127Octets (32-bit)	65 ≤ frame size ≤ 127	**DA**	**X**	**X**	The number of ***all***[2]received packets whose size are between 65 ~ 127 bytes, including MAC header and FSC, excluding preamble and SFD.	V
etherStatsPkts128to255Octets (32-bit)	128 ≤ frame size ≤ 255	**DA**	**X**	**X**	The number of ***all***[2]received packets whose size are between 128 ~ 255 bytes, including MAC header and FSC, excluding preamble and SFD.	V
etherStatsPkts256to511Octets (32-bit)	256 ≤ frame size ≤ 511	**DA**	**X**	**X**	The number of ***all***[2]received packets whose size are between 256 ~ 511 bytes, including MAC header and FSC, excluding preamble and SFD.	V
etherStatsPkts512to1023Octets (32-bit)	512 ≤ frame size ≤ 1023	**DA**	**X**	**X**	The number of ***all***[2]received packets whose size are between 512 ~ 1023 bytes, including MAC header and FSC, excluding preamble and SFD.	V
etherStatsPkts1024toOversizeOctets (32-bit)	1024 ≤ frame size ≤ ***OversizeOctets (N***[5]***)***	**DA**	**X**	**X**	The number of ***all***[2]received packets whose size are between 1024 ~ ***N***[5] bytes, including MAC header and FSC, excluding preamble and SFD.	V
etherStatsOversizePkts (32-bit)	frame size > ***N***[5]	**DA**	**G**	**G**	The number of received valid rames whose size are more than ***N***[5] bytes, including MAC header and FCS, but excluding preamble and SFD.	V
EtherStatsJabbers (32-bit)	frame size > ***N***[5]	**DA**	**B**	**B**	The number of ***invalid***[3] packets whose size are more than ***N***[6] bytes with BAD FCSor alignment error, including MAC header and FCS, excluding preamble and SFD.	V
etherStatsMulticastPkts (32-bit)	frame size ≥ 64 byte Layer 2 multicast packets with ether type != 0x8808 exclude PAUSE frame	**DA**	**G**	**G**	The number of ***valid***[1]received multicast packets, excluding ***MAC Control Frame***[4].	V
etherStatsBroadcastPkts (32-bit)	frame size ≥ 64 byte DA = broadcast address	**DA**	**G**	**G**	The number of ***valid***[1]received broadcast packets.	V
EtherStatsDropEvents (32-bit)	frame size ≥ 64 bytes AND was dropt due to flow control drop emcheme .	***X***	**G**	**G**	The number of ***valid***[1]packets dropped due to lack of resource. (packet was dropt due to the buffer flow control drop mecheme).	V

	~~In full duplex mode , flow control is trigger but still receive packets .~~ ~~In half duplex, no buffers~~					
dot1dTpPortInDiscards (32-bit)	frame size ≥ 64 bytes drop case of : {Ingress rule fail. Egress rule fail. Source blocking …} exclude PAUSE frame , and EtherStatsDropEvents	***DA***	**G**	**G**	The number of ***valid***[1] frames discarded by forwarding process. (Note : It exclude the drop event of ***EtherStatsDropEvents)***	V
dot3StatsFCSErrors (32-bit)	frame size > 0 byte	***DA***	**G**	**B**	The number of received frames with FCS errors.	V
dot3StatsFrameTooLongs (32-bit)	frame size > ***N***[5] = therStatsOversizePkts + etherStatsJabbers	***DA***	**X**	**X**	The number of received frames that exceed max permitted frame size.	V
dot3StatsSymbolErrors (32-bit)	fame size > 0 byte	***DA***	**X**	**X**	The number of frames with symbol errors.	V
dot3ControlInUnknownOpcodes (32-bit)	frame size > 0 byte MAC control frame with opcode ≠ 0x0001	***DA***	**G**	**G**	The number of received ***MAC Control Frames***[4] ~~(DA=0x01-80-C2-00-00-01)~~ (EtherType=0x8808) with an unknown opcode.	V
dot3InPauseFrames (32-bit)	fame size > 0 byte DA = 01-80-C2-00-00-01 EtherType=88-08 , Opcode=00-01	***DA***	**G**	**G**	The number of received PAUSE frames. (The InPauseframe packet will not be counted in other MIBs)	V
ifOutOctets (64-bit)	Byte of all frame size ≥ 64 bytes (include PASUE frame !)	***DA***	**G**	**G**	The number of bytes in ***valid***[1]transmitted frames, including MAC header and FCS, excluding preamble and SFD.	V
ifOutUcastPkts (32-bit)	frame size ≥ 64 bytes	***DA***	**G**	**G**	The number of transmitted unicast packets, including discarded or not sent (never happen in fact).	V
ifOutMulticastPkts (32-bit)	exclude PAUSE frame	***DA***	**G**	**G**	The number of transmitted multicast packets, including discarded or not sent (never happen in fact), excluding ***MAC Conftrol Frame***[4] (here Pause Frame).	V
ifOutBroadcastPkts (32-bit)	frame size ≥ 0 byte DA = broadcast address	***DA***	**G**	**G**	The number of transmitted broadcast packets, including discarded or not sent (never happen in fact).	V
ifOutDiscards (32-bit) ***[do not implement !!]***	Drop due to RED mecheme .	***X***	**G**	**G**	The number of outbound packets dropped due to lack of resource.	x
dot3StatsSingleCollisionFrames (32-bit)		***X***	***X***	***X***	A count of frames that are involved in a single collision and are subsequently transmitted successfully.	V
dot3StatsMultipleCollisionFrames (32-bit)		***X***	***X***	***X***	A count of frames that are involved in more than one collision and are subsequently transmitted successfully.	V
dot3StatsDeferredTransmissions (32-bit)	Only occurs in half-duplex mode.	***X***	**G**	**G**	A count of frames for which the first transmission attempt on a particular interface is delayed because the medium is busy (half duplex).	V
dot3StatsLateCollisions (32-bit)	Collision detect on latter than 512bit time during a packet transmission.	***X***	***X***	***X***	The number of times that a collision is detected on a particular interface later than one slotTime into the transmission of a packet.	V
dot3StatsExcessiveCollisions (32-bit)	Collision for a packet exceedes 16 times.	***X***	***X***	***X***	A count of frames for which transmission on a particular interface exceeds 16 collisions (>16 collisons).	V
dot3OutPauseFrames (32-bit)	fame size > 0 byte DA = 01-80-C2-00-00-01 EtherType=88-08 , Opcode=00-01	***DA***	**G**	**G**	A count of ***MAC control frames***[4] transmitted on this interface with an opcode indicating the PAUSE operation.	V
		~~***X***~~	~~**G**~~	~~**G**~~		~~X~~
etherStatsCollisions (32-bit)	Collision count	***X***	***X***	***X***	The number of collisions experienced in a port during packet transmissions.	V

dot1dTpLearnedEntryDiscard (32-bit)	4-way full and replace an existed entry. apply to all Filtering Database. should be ***valid***[1] frame.	***DA***	**G**	**G**	The total number of forwarding database entries which have been or would have been learnt, but have been discarded due to lack of space to store them in the forwarding database.	V
TBD						
ipInReceives (32-bit)					The total number of input datagrams received from interfaces, including those received in error.	
ipInHdrErrors (32-bit)					The number of input datagrams discarded due to errors in their IP headers, including bad checksums, version number mismatch, other format errors, time-to-live exceeded, errors discovered in processing their IP options, etc.	
ipInAddrErrors (32-bit)					The number of input datagrams discarded because the IP address in their IP header's destination field was not a valid address to be received at this entity. This ount includes invalid addresses (e.g., 0.0.0.0) and addresses of unsupported Classes (e.g., Class E). For entities which are not IP Gateways and therefore do not forward datagrams, this counter includes datagrams discarded because the destination address was not a local address.	
ipForwDatagrams (32-bit)					The number of input datagrams for which this entity was not their final IP destination, as a result of which an attempt was made to find a route to forward them to that final destination. In entities which do not act as IP Gateways, this counter will include only those packets which were Source-Routed via this entity, and the Source-Route option processing was successful.	
ipInDiscards (32-bit)					The number of input IP datagrams for which no problems were encountered to prevent their continued processing, but which were discarded (e.g., for lack of buffer space). Note that this counter does not include any datagrams discarded while awaiting re-assembly.	
ipOutDiscards (32-bit)					The number of output IP datagrams for which no problem was encountered to prevent their transmission to their destination, but which were discarded (e.g., for lack of buffer space). Note that this counter would include datagrams counted in ipForwDatagrams if any such packets met this (discretionary) discard criterion.	
ipOutNoRoutes (32-bit)					The number of IP datagrams discarded because no route could be found to transmit them to their destination. Note that this counter includes any packets counted in ipForwDatagrams which meet this `no-route' criterion. Note that this includes any datagarms which a host cannot route because all of its default gateways are down.	
ipFragOKs (32-bit)					he number of IP datagrams that have been successfully fragmented at this entity.	

Note 1: Valid frame is a frame with no CRC error and no alignment error.
Note 2: All frame means a frame is either a valid or invalid frame.
Note 3: Invalid frame is a frame with CRC or alignment error.
Note 4: The ether type of MAC Control Frame is 0x8808. . Ref. IEEE 802.3, 2002. Section 31.4.
Note 5: N=1518 for untagged frame, otherwise N=1522 for vlan tagged frame.
Note 5: P= system permited maxacceptable packet lengthj, It is defined by the system register .

Design Note :

(1) that the *dot3StatsFrameTooLongs* should be implemented as an indirectly supported MIB Counter, such as *dot3StatsFrameTooLongs = etherStatsOversizePkts + etherStatsJabbers*.

(2) the received valid pause frame will only trigger the dot3InPauseFrames conter, and will not be counted in other MIB counters. :

Table 55. MIB Counter Mapping

RTL8197F MIB	*Ethernet-Like MIB RFC 3635*	*Bridge MIB RFC 1493/2674*	*MIB II/Interface Group RFC 1213/2863*	*RMON MIB RFC 2819*
ifInOctets			*ifInOctets*	
ifInUcastPkts			*ifInUcastPkts*	
etherStatsOctets				*etherStatsOctets*
etherStatsUndersizePkts				*etherStatsUndersizePkts*
etherStatsFragments				*etherStatsFragments*
etherStatsPkts64Octets				*etherStatsPkts64Octets*
etherStatsPkts65to127Octets				*etherStatsPkts65to127Octets*
etherStatsPkts128to255Octets				*etherStatsPkts128to255Octets*
etherStatsPkts256to511Octets				*etherStatsPkts256to511Octets*
etherStatsPkts512to1023Octets				*etherStatsPkts512to1023Octets*
etherStatsPkts1024to1518Octets				*etherStatsPkts1024to1518Octets*
etherStatsOversizePkts				*etherStatsOversizePkts*
etherStatsJabbers				*etherStatsJabbers*
etherStatsMulticastPkts				*etherStatsMulticastPkts*
etherStatsBroadcastPkts				*etherStatsBroadcastPkts*
etherStatsDropEvents				*etherStatsDropEvents*
Dot1dTpPortInDiscards		*dot1dTpPortInDiscards*		
dot3StatsFCSErrors	*dot3StatsFCSErrors*			
dot3StatsFrameTooLongs	*dot3StatsFrameTooLongs*			
Dot3StatsSymbolErrors	*dot3StatsSymbolErrors*			
dot3ControlInUnknownOpcodes	*dot3ControlInUnknownOpcodes*			
dot3InPauseFrames	*dot3InPauseFrames*			
ifOutOctets			*ifOutOctets*	
ifOutUcastPkts			*ifOutUcastPkts*	
ifOutMulticastPkts			*ifOutMulticastPkts*	
ifOutBroadcastPkts			*ifOutBroadcastPkts*	
ifOutDiscards			*ifOutDiscards*	
dot3StatsSingleCollisionFrames	*dot3StatsSingleCollisionFrames*			
dot3StatsMultipleCollisionFrames	*dot3StatsMultipleCollisionFrames*			
dot3StatsDeferredTransmissions	*dot3StatsDeferredTransmissions*			
dot3StatsLateCollisions	*dot3StatsLateCollisions*			
dot3StatsExcessiveCollisions	*dot3StatsExcessiveCollisions*			
dot3OutPauseFrames	*dot3OutPauseFrames*			
~~***dot1dBasePortDelayExceedEdDiscards***~~				
etherStatsCollisions				*etherStatsCollisions*
dot1dTpLearnedEntryDiscard		*dot1dTpLearnedEntryDiscard*		

ipInReceives	*ipInReceives*
ipInHdrErrors	*ipInHdrErrors*
ipInAddrErrors	*ipInAddrErrors*
ipForwDatagrams	*ipForwDatagrams*
ipInDiscards	*ipInDiscards*
ipOutDiscards	*ipOutDiscards*
ipOutNoRoutes	*ipOutNoRoutes*
ipFragOKs	*ipFragOKs*

9.5. QoS Function Register

9.5.1. QoS Function Control Register

Table 56. QoS Function Control Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
00	4	QOSFCR	QoS Function Control Register	

Table 57. QoS Function Control Register

Reg.bit	Name	Description	Mode	Default
n.31-n.1	Reserved			
n.0	BWC_withPIFG	Bandwidth Control Include/exclude Preamble & IFG (20bytes) 0: exclude, 1: include	W/R	0B

9.5.2. Ingress Bandwidth Control

Table 58. Ingress Bandwidth Control Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
04	4	IBCR0	Ingress Bandwidth Control Register 0.	
08	4	IBCR1	Ingress Bandwidth Control Register 1.	
0C	4	IBCR2	Ingress Bandwidth Control Register 2.	
10	4	Reserved		

Table 59. Ingress Bandwidth Control Register 0 (BB80-4704)

Reg.bit	Name	Description	Mode	Default
n.31-n.16	BWC_P1[15:0]	Port 1 Bandwidth Control,	W/R	0000H
n.15-n.0	BWC_P0[15:0]	Port 0 Bandwidth Control, unit: 1Kbps (K=1024) 0 : BW= full rate (line rate) N : BW=N*16Kbps. Note: MSB bits need refer to 0xBB80-4710	W/R	0000H

Table 60. Ingress Bandwidth Control Register 1 (BB80-4708)

Reg.bit	Name	Description	Mode	Default
n.31-n.16	BWC_P3[15:0]	Port 3 Bandwidth Control,	W/R	0000H

Reg.bit	Name	Description	Mode	Default
n.15-n.0	BWC_P2[15:0]	Port 2 Bandwidth Control, unit: 1Kbps (K=1024) 0 : BW= full rate (line rate) N : BW=N*16Kbps. Note: MSB bits need refer to 0xBB80-4710	W/R	0000H

Table 61. Ingress Bandwidth Control Register 2 (BB80-470C)

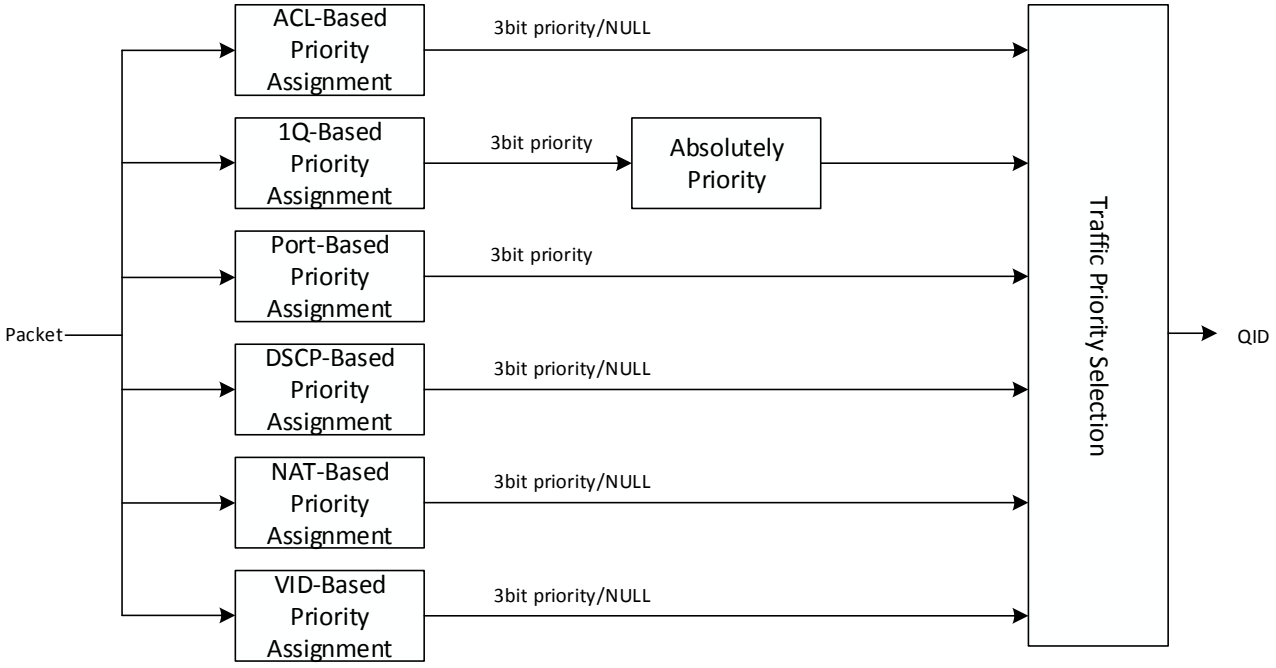
Reg.bit	Name	Description	Mode	Default
n.31-n.16	BWC_P5[15:0]	Port 5 Bandwidth Control,	W/R	0000H
n.15-n.0	BWC_P4[15:0]	Port 4 Bandwidth Control, unit: 1Kbps (K=1024) 0 : BW= full rate (line rate) N : BW=N*16Kbps. Note: MSB bits need refer to 0xBB80-4710	W/R	0000H

Table 62. Ingress Bandwidth Control Register 3 (BB80-4710)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	Reserved			0000H
n.23-n.20	BWC_P5[19:16]	Port 5 Bandwidth Control	W/R	0000H
n.19-n.16	BWC_P4[19:16]	Port 4 Bandwidth Control	W/R	0000H
n.15-n.12	BWC_P3[19:16]	Port 3 Bandwidth Control	W/R	0000H
n.11-n.8	BWC_P2[19:16]	Port 2 Bandwidth Control	W/R	0000H
n.7-n.4	BWC_P3[19:16]	Port 1 Bandwidth Control	W/R	0000H
n.3-n.0	BWC_P0[19:16]	Port 0 Bandwidth Control	W/R	0000H

9.5.3. Packet Priority Assignment Control Register

Packet Priority Assignment is a mechanism used to assign an outgoing packet to an output queue. In RTL8197F, there are six output queues provided per port. Each outgoing packet should be assigned to and queued into one of these output queues. RTL8197F provides five Priority Assignments and each Priority Assignments may or may not assign a pseudo QID (pQID) to a received packet. A received packet finally should be assigned only one pQID through the pQID selection mechanism. Once a pQID is derived for a received packet, the pQID will map to a output QID and the packet will be queued in the output queue. Following figure describes the whole procedure for the packet priority assignment:



9.5.3.1 Port-Based Priority Assignment Register

Table 63. Port Based Priority Control Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
14	4	PBPCR	Port Based Priority Control Register	

Table 64. Port Based Priority Control Register

Reg.bit	Name	Description	Mode	Default
n.31-n.27	Reserved			
n.26-n.24	PBPRI_P8[2:0]	Port Based Priority assign for port 8 (extension port 2)	W/R	000B
n.23-n.21	PBPRI_P7[2:0]	Port Based Priority assign for port 7 (extension port 1)	W/R	000B
n.20-.18	PBPRI_P6[2:0]	Port Based Priority assign for port 6 (extension port 0)	W/R	000B
n.17-n.15	PBPRI_P5[2:0]	Port Based Priority assign for port 5	W/R	000B
n.14-n.12	PBPRI_P4[2:0]	Port Based Priority assign for port 4	W/R	000B
n.11-n.9	PBPRI_P3[2:0]	Port Based Priority assign for port 3	W/R	000B
n.8-n.6	PBPRI_P2[2:0]	Port Based Priority assign for port 2	W/R	000B
n.5-n.3	PBPRI_P1[2:0]	Port Based Priority assign for port 1	W/R	000B
n.2-n.0	PBPRI_P0[2:0]	Port Based Priority assign for port 0	W/R	000B

9.5.3.2 1Q-Based Priority Assignment Register

1Q Based Priority Assignment is the same as the IEEE 802.1P priority. Each received packet is assigned to a 3-bit priority according to its VLAN tag priority. If the packet is an untagged packet, the 3-bit priority is assigned

by Port and Protocol Based Priority. If the packet doesn't match any Port and Protocol Based VLAN, a default port priority is assigned. For the Port and Protocol Based Priority and Default Port Priority configuration, please refer to the Port and Protocol Based VLAN and Port-Based VLAN sections.

After a 3-bit prioriy is derived from the VLAN Tag, Port and Protocol priority or default port priority, the 3-bit priority is still needed to be used to map to an pseudo output queue ID. The mapping table is defined in user priority to traffic class mapping table, which is shown as following figure.

	Priority to QID mapping table						1Q priority to system linear priority transfer mapping
	Number of Available Traffic Classes(Queue number)						
Priority	1	2	3	4	5	6	8
0(default)	Queue 0	Queue 0	Queue 0	Queue 1	Queue 1	Queue 1	Priority 2
1	Queue 0	Queue 0	Queue 0	Queue 0	Queue 0	Queue 0	Priority 0
2	Queue 0	Queue 0	Queue 0	Queue 0	Queue 0	Queue 0	Priority 1
3	Queue 0	Queue 0	Queue 0	Queue 1	Queue 1	Queue 2	Priority 3
4	Queue 0	Queue 5	Queue 1	Queue 2	Queue 2	Queue 3	Priority 4
5	Queue 0	Queue 5	Queue 1	Queue 2	Queue 3	Queue 4	Priority 5
6	Queue 0	Queue 5	Queue 5	Queue 5	Queue 5	Queue 5	Priority 6
7	Queue 0	Queue 5	Queue 5	Queue 5	Queue 5	Queue 5	Priority 7

Figure 19. user priority to traffic class mapping table

Figure above is recommended by IEEE 802.1P and can be configured through the User Priority to Traffic Class Mapping Control Register, which is shown in below Tables.

Table 65. User Priority to Traffic Class Mapping Control Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
18	4	UPTCMCR0	User Priority to Traffic Class Mapping for 1 output queue	
1C	4	UPTCMCR1	User Priority to Traffic Class Mapping for 2 output queues	
20	4	UPTCMCR2	User Priority to Traffic Class Mapping for 3 queues	
24	4	UPTCMCR3	User Priority to Traffic Class Mapping for 4 queues	
28	4	UPTCMCR4	User Priority to Traffic Class Mapping for 5 queues	
2C	4	UPTCMCR5	User Priority to Traffic Class Mapping for 6 queues	
30	4	8021Q2LTM	802.1Q priority to linear priority Transfer mapping.	

Table 66. UPTCMCR0 Control Register (0xBB80-4718)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	Reserved			
n.23-n.21	1QMPRI7	1 traffic class Output QID mapping for priority level 7	W/R	000B
n.20-n.18	1QMPRI6	1 traffic class Output QID mapping for priority level 6	W/R	000B
n.17-n.15	1QMPRI5	1 traffic class Output QID mapping for priority level 5	W/R	000B
n.14-n.12	1QMPRI4	1 traffic class Output QID mapping for priority level 4	W/R	000B
n.11-n.9	1QMPRI3	1 traffic class Output QID mapping for priority level 3	W/R	000B
n.8-n.6	1QMPRI2	1 traffic class Output QID mapping for priority level 2	W/R	000B
n.5-n.3	1QMPRI1	1 traffic class Output QID mapping for priority level 1	W/R	000B
n.2-n.0	1QMPRI0	1 traffic class Output QID mapping for priority level 0	W/R	000B

Table 67. UPTCMCR1 Control Register (0xBB80-471C)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	Reserved			
n.23-n.21	2QMPRI7	2 traffic class Output QID mapping for priority level 7	W/R	101B
n.20-n.18	2QMPRI6	2 traffic class Output QID mapping for priority level 6	W/R	101B
n.17-n.15	2QMPRI5	2 traffic class Output QID mapping for priority level 5	W/R	101B
n.14-n.12	2QMPRI4	2 traffic class Output QID mapping for priority level 4	W/R	101B
n.11-n.9	2QMPRI3	2 traffic class Output QID mapping for priority level 3	W/R	000B
n.8-n.6	2QMPRI2	2 traffic class Output QID mapping for priority level 2	W/R	000B
n.5-n.3	2QMPRI1	2 traffic class Output QID mapping for priority level 1	W/R	000B
n.2-n.0	2QMPRI0	2 traffic class Output QID mapping for priority level 0	W/R	000B

Table 68. UPTCMCR2 Control Register (0xBB80-4720)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	Reserved			
n.23-n.21	3QMPRI7	3 traffic class Output QID mapping for priority level 7	W/R	101B
n.20-n.18	3QMPRI6	3 traffic class Output QID mapping for priority level 6	W/R	101B
n.17-n.15	3QMPRI5	3 traffic class Output QID mapping for priority level 5	W/R	001B
n.14-n.12	3QMPRI4	3 traffic class Output QID mapping for priority level 4	W/R	001B
n.11-n.9	3QMPRI3	3 traffic class Output QID mapping for priority level 3	W/R	000B
n.8-n.6	3QMPRI2	3 traffic class Output QID mapping for priority level 2	W/R	000B
n.5-n.3	3QMPRI1	3 traffic class Output QID mapping for priority level 1	W/R	000B
n.2-n.0	3QMPRI0	3 traffic class Output QID mapping for priority level 0	W/R	000B

Table 69. UPTCMCR3 Control Register (0xBB80-4724)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	Reserved			
n.23-n.21	4QMPRI7	4 traffic class Output QID mapping for priority level 7	W/R	101B
n.20-n.18	4QMPRI6	4 traffic class Output QID mapping for priority level 6	W/R	101B
n.17-n.15	4QMPRI5	4 traffic class Output QID mapping for priority level 5	W/R	010B
n.14-n.12	4QMPRI4	4 traffic class Output QID mapping for priority level 4	W/R	010B

Reg.bit	Name	Description	Mode	Default
n.11-n.9	4QMPRI3	4 traffic class Output QID mapping for priority level 3	W/R	001B
n.8-n.6	4QMPRI2	4 traffic class Output QID mapping for priority level 2	W/R	000B
n.5-n.3	4QMPRI1	4 traffic class Output QID mapping for priority level 1	W/R	000B
n.2-n.0	4QMPRI0	4 traffic class Output QID mapping for priority level 0	W/R	001B

Table 70. UPTCMCR4 Control Register (0xBB80-4728)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	Reserved			
n.23-n.21	5QMPRI7	5 traffic class Output QID mapping for priority level 7	W/R	101B
n.20-n.18	5QMPRI6	5 traffic class Output QID mapping for priority level 6	W/R	101B
n.17-n.15	5QMPRI5	5 traffic class Output QID mapping for priority level 5	W/R	011B
n.14-n.12	5QMPRI4	5 traffic class Output QID mapping for priority level 4	W/R	010B
n.11-n.9	5QMPRI3	5 traffic class Output QID mapping for priority level 3	W/R	001B
n.8-n.6	5QMPRI2	5 traffic class Output QID mapping for priority level 2	W/R	000B
n.5-n.3	5QMPRI1	5 traffic class Output QID mapping for priority level 1	W/R	000B
n.2-n.0	5QMPRI0	5 traffic class Output QID mapping for priority level 0	W/R	001B

Table 71. UPTCMCR5 Control Register (0xBB80-472C)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	Reserved			
n.23-n.21	6QMPRI7	6 traffic class Output QID mapping for priority level 7	W/R	101B
n.20-n.18	6QMPRI6	6 traffic class Output QID mapping for priority level 6	W/R	101B
n.17-n.15	6QMPRI5	6 traffic class Output QID mapping for priority level 5	W/R	100B
n.14-n.12	6QMPRI4	6 traffic class Output QID mapping for priority level 4	W/R	011B
n.11-n.9	6QMPRI3	6 traffic class Output QID mapping for priority level 3	W/R	010B
n.8-n.6	6QMPRI2	6 traffic class Output QID mapping for priority level 2	W/R	000B
n.5-n.3	6QMPRI1	6 traffic class Output QID mapping for priority level 1	W/R	000B
n.2-n.0	6QMPRI0	6 traffic class Output QID mapping for priority level 0	W/R	001B

Table 72. 802.1Q priority to linear priority Transfer mapping. (0xBB80-4730)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	Reserved			
n.23-n.21	8021Q2LTMPRI7	8 level linear priority mapping for 802.1Q priority level 7	W/R	111B
n.20-n.18	8021Q2LTMPRI6	8 level linear priority mapping for 802.1Q priority level 6	W/R	110B
n.17-n.15	8021Q2LTMPRI5	8 level linear priority mapping for 802.1Q priority level 5	W/R	101B
n.14-n.12	8021Q2LTMPRI4	8 level linear priority mapping for 802.1Q priority level 4	W/R	100B
n.11-n.9	8021Q2LTMPRI3	8 level linear priority mapping for 802.1Q priority level 3	W/R	011B
n.8-n.6	8021Q2LTMPRI2	8 level linear priority mapping for 802.1Q priority level 2	W/R	001B
n.5-n.3	8021Q2LTMPRI1	8 level linear priority mapping for 802.1Q priority level 1	W/R	000B
n.2-n.0	8021Q2LTMPRI0	8 level linear priority mapping for 802.1Q priority level 0	W/R	010B

9.5.3.3 DSCP-Based Priority Assignment Register

Table 73. DSCP Priority Control Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
34	4	DSCPCR0	DSCP Priority Control Register 0	
38	4	DSCPCR1	DSCP Priority Control Register 1	
3C	4	DSCPCR2	DSCP Priority Control Register 2	
40	4	DSCPCR3	DSCP Priority Control Register 3	
44	4	DSCPCR4	DSCP Priority Control Register 4	
48	4	DSCPCR5	DSCP Priority Control Register 5	
4C	4	DSCPCR6	DSCP Priority Control Register 6	

Table 74. DSCP Priority Control Register 0 (0xBB80-4734)

Reg.bit	Name	Description	Mode	Default
n.31-n.30	Reserved			
n.29-n.27	DSCP9_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.26-n.24	DSCP8_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.23-n.21	DSCP7_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.20-n.18	DSCP6_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.17-n.15	DSCP5_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.14-n.12	DSCP4_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.11-n.9	DSCP3_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.8-n.6	DSCP2_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.5-n.3	DSCP1_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.2-n.0	DSCP0_Pri[2:0]	DSCP code point priority assignment.	W/R	001B

Table 75. DSCP Priority Control Register 1 (0xBB80-4738)

Reg.bit	Name	Description	Mode	Default
n.31-n.30	Reserved			
n.29-n.27	DSCP19_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.26-n.24	DSCP18_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.23-n.21	DSCP17_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.20-n.18	DSCP16_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.17-n.15	DSCP15_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.14-n.12	DSCP14_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.11-n.9	DSCP13_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.8-n.6	DSCP12_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.5-n.3	DSCP11_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.2-n.0	DSCP10_Pri[2:0]	DSCP code point priority assignment.	W/R	001B

Table 76. DSCP Priority Control Register 2 (0xBB80-473C)

Reg.bit	Name	Description	Mode	Default
n.31-n.30	Reserved			

Reg.bit	Name	Description	Mode	Default
n.29-n.27	DSCP29_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.26-n.24	DSCP28_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.23-n.21	DSCP27_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.20-n.18	DSCP26_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.17-n.15	DSCP25_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.14-n.12	DSCP24_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.11-n.9	DSCP23_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.8-n.6	DSCP22_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.5-n.3	DSCP21_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.2-n.0	DSCP20_Pri[2:0]	DSCP code point priority assignment.	W/R	001B

Table 77. DSCP Priority Control Register 3 (0xBB80-4740)

Reg.bit	Name	Description	Mode	Default
n.31-n.30	Reserved			
n.29-n.27	DSCP39_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.26-n.24	DSCP38_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.23-n.21	DSCP37_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.20-n.18	DSCP36_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.17-n.15	DSCP35_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.14-n.12	DSCP34_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.11-n.9	DSCP33_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.8-n.6	DSCP32_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.5-n.3	DSCP31_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.2-n.0	DSCP30_Pri[2:0]	DSCP code point priority assignment.	W/R	001B

Table 78. DSCP Priority Control Register 4 (0xBB80-4744)

Reg.bit	Name	Description	Mode	Default
n.31-n.30	Reserved			
n.29-n.27	DSCP49_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.26-n.24	DSCP48_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.23-n.21	DSCP47_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.20-n.18	DSCP46_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.17-n.15	DSCP45_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.14-n.12	DSCP44_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.11-n.9	DSCP43_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.8-n.6	DSCP42_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.5-n.3	DSCP41_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.2-n.0	DSCP40_Pri[2:0]	DSCP code point priority assignment.	W/R	001B

Table 79. DSCP Priority Control Register 5 (0xBB80-4748)

Reg.bit	Name	Description	Mode	Default
n.31-n.30	Reserved			

Reg.bit	Name	Description	Mode	Default
n.29-n.27	DSCP59_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.26-n.24	DSCP58_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.23-n.21	DSCP57_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.20-n.18	DSCP56_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.17-n.15	DSCP55_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.14-n.12	DSCP54_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.11-n.9	DSCP53_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.8-n.6	DSCP52_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.5-n.3	DSCP51_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.2-n.0	DSCP50_Pri[2:0]	DSCP code point priority assignment.	W/R	001B

Table 80. DSCP Priority Control Register 6 (0xBB80-474C)

Reg.bit	Name	Description	Mode	Default
n.31-n.30	Reserved			
n.29-n.27	Reserved		W/R	001B
n.26-n.24	Reserved		W/R	001B
n.23-n.21	Reserved		W/R	001B
n.20-n.18	Reserved		W/R	001B
n.17-n.15	Reserved		W/R	001B
n.14-n.12	Reserved		W/R	001B
n.11-n.9	DSCP63_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.8-n.6	DSCP62_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.5-n.3	DSCP61_Pri[2:0]	DSCP code point priority assignment.	W/R	001B
n.2-n.0	DSCP60_Pri[2:0]	DSCP code point priority assignment.	W/R	001B

9.5.3.4 Queue ID Decision Priority Control Register

Because each priority assignment may assign a 3-bit priority to a received packet, this may result in ambiguous due to more than one priority assigned to an outgoing packet. To avoid this ambiguous, there is only one output queue decision derived from above five Priority Assignments can be taken. Which priority should be taken is based on the Output Queue Decision Priority Register, which is shown in Table 2.2.6.1 and Table 2.2.6.2.

Table 81. Queue ID Decision Priority Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
50	4	QIDDPCR	Queue decision priority Control Register	

Each traffic could be classified to a traffic class to map to a target priority queue ID by different priority information. The queue ID decision table provide a scheme to select the target QID.

In the table, each filed (4 bit) define the selection priority among these different priority information . The selection scheme is check from the MSB bit to LSB bit, the MSB bit own a higher selection priority .

Table 82. Queue ID Decision Priority Control Register (0xBB80-4750)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	Reserved			
n.23-n.20	cf_vid_pri[3:0]	VID based priority selection	W/R	0001B
n.19-n.16	NAPT_PRI[3:0]	Output queue decision priority assign for NAPT Based Priority	W/R	0001B
n.15-n.12	ACL_PRI[3:0]	Output queue decision priority assign for ACL Based Priority	W/R	0001B
n.11-n.8	DSCP_PRI[3:0]	Output queue decision priority assign for DSCP Based Priority	W/R	0001B
n.7- n.4	8021QBP_PRI[3:0]	Output queue decision priority assign for 1Q Based Priority	W/R	0001B
n.3-n.0	PBP_PRI[3:0]	Output queue decision priority assign for Port Based Priority The final QID of a packet on the output port is decide based on the Matrix table. PBP_PRIO[3:0] : MSB is with the higher comparison priority level than LSB. If the MSB bit with '1' but the priority is not exist, then the decision rule will follow the next bit configuration to make decision again. Bit value 1 = enable compare. 0 = disable compare.	W/R	0001B

9.5.3.5 Output Queue Number Control Register

Table 83. Output Queue Number Control Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
54	4	QNUMCR	Queue Number Control Register.	

Table 84. Output Queue Number Control Register (0xBB80-4754)

Reg.bit	Name	Description	Mode	Default
n.31-n.21	Reserved			
n.20-n.18	P6QNum[2:0]	The number of output queue for port 6. (CPU port)	W/R	001B
n.17-n.15	P5QNum[2:0]	The number of output queue for port 5.	W/R	001B
n.14-n.12	P4QNum[2:0]	The number of output queue for port 4.	W/R	001B
n.11-n.9	P3QNum [2:0]	The number of output queue for port 3.	W/R	001B
n.8-n.6	P2QNum [2:0]	The number of output queue for port 2.	W/R	001B
n.5- n.3	P1QNum [2:0]	The number of output queue for port 1.	W/R	001B
n.2-n.0	P0QNum [2:0]	The number of output queue for port 0. 000: 1 Output Queue, 001: 2 Output Queue 010: 3 Output Queue, 011: 4 Output Queue 100: 5 Output Queue, 101: 6 Output Queue 110: 7 Output Queue, 111: 8 Output Queue	W/R	001B

9.5.3.6 CPU port Queue ID vs. Traffic Class Assignment Control Register

CPU port support 6 internal queues. The CPU port Queue ID vs. traffic mapping is based on the Destination port ID and priority information . And it use the different configuration set from other 6 physical port. The mapping support the one physical port (CPU) to separate the different logical port (extension port) traffic to queued in different queue with different weighting control. The logical port could service at different egress rate that controlled by the queue Rate Guarantee Control registers.

Table 85. CPU port Queue Control Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
58	4	CPUQIDMCR0	CPU port QID Mapping Control Register 0 (DP=include CPU)	
5C	4	CPUQIDMCR1	CPU port QID Mapping Control Register 1 (DP=Ext0)	
60	4	CPUQIDMCR2	CPU port QID Mapping Control Register 2 (DP=Ext1)	
64	4	CPUQIDMCR3	CPU port QID Mapping Control Register 3 (DP=Ext2)	
68	4	CPUQIDMCR4	CPU port QID Mapping Control Register 4 (DP= multi-port of Ext port)	

Table 86. CPU port QID Mapping Control Register 0 (0xBB80-4758)

Reg.bit	Name	Description	Mode	Default
n.31	Reserved	Reserved		
n.30-n.28	CPUPri7QIDM[2:0]	{DP=include CPU ,priority = 7} vs. QID Mapping	W/R	000B
n.27	Reserved		W/R	000B
n.26-n.24	CPUPri6QIDM[2:0]	{DP= include CPU ,priority = 6} vs. QID Mapping	W/R	000B
n.23	Reserved		W/R	000B
n.22-n.20	CPUPri5QIDM[2:0]	{DP= include CPU ,priority = 5} vs. QID Mapping	W/R	000B
n.19	Reserved		W/R	000B
n.18-n.16	CPUPri4QIDM[2:0]	{DP= include CPU ,priority = 4} vs. QID Mapping	W/R	000B
n.15	Reserved		W/R	000B
n.14-n.12	CPUPri3QIDM[2:0]	{DP= include CPU ,priority = 3} vs. QID Mapping	W/R	000B
n.11	Reserved		W/R	000B
n.10-n.8	CPUPri2QIDM[2:0]	{DP= include CPU ,priority = 2} vs. QID Mapping	W/R	000B
n.7	Reserved		W/R	000B
n.6-n.4	CPUPri1QIDM[2:0]	{DP= include CPU ,priority = 1} vs. QID Mapping	W/R	000B
n.3	Reserved		W/R	000B
n.2-n.0	CPUPri0QIDM[2:0]	{DP= include CPU ,priority = 0} vs. QID Mapping	W/R	000B

Table 87. CPU port QID Control Register 1 (0xBB80-475C)

Reg.bit	Name	Description	Mode	Default
n.31	Reserved	Reserved		

Reg.bit	Name	Description	Mode	Default
n.30-n.28	EXT0Pri7QIDM[2:0]	{DP=EXT0 ,priority = 7} vs. QID Mapping	W/R	000B
n.27	Reserved		W/R	000B
n.26-n.24	EXT0Pri6QIDM[2:0]	{DP= EXT0,priority = 6} vs. QID Mapping	W/R	000B
n.23	Reserved		W/R	000B
n.22-n.20	EXT0Pri5QIDM[2:0]	{DP= EXT0,priority = 5} vs. QID Mapping	W/R	000B
n.19	Reserved		W/R	000B
n.18-n.16	EXT0Pri4QIDM[2:0]	{DP= EXT0,priority = 4} vs. QID Mapping	W/R	000B
n.15	Reserved		W/R	000B
n.14-n.12	EXT0Pri3QIDM[2:0]	{DP= EXT0,priority = 3} vs. QID Mapping	W/R	000B
n.11	Reserved		W/R	000B
n.10-n.8	EXT0Pri2QIDM[2:0]	{DP= EXT0,priority = 2} vs. QID Mapping	W/R	000B
n.7	Reserved		W/R	000B
n.6-n.4	EXT0Pri1QIDM[2:0]	{DP= EXT0,priority = 1} vs. QID Mapping	W/R	000B
n.3	Reserved		W/R	000B
n.2-n.0	EXT0Pri0QIDM[2:0]	{DP= EXT0,priority = 0} vs. QID Mapping	W/R	000B

Table 88. CPU port QID Control Register 2 (0xBB80-4760)

Reg.bit	Name	Description	Mode	Default
n.31	Reserved	Reserved		
n.30-n.28	EXT1Pri7QIDM[2:0]	{DP= EXT1 ,priority = 7} vs. QID Mapping	W/R	000B
n.27	Reserved		W/R	000B
n.26-n.24	EXT1Pri6QIDM[2:0]	{DP= EXT1,priority = 6} vs. QID Mapping	W/R	000B
n.23	Reserved		W/R	000B
n.22-n.20	EXT1Pri5QIDM[2:0]	{DP= EXT1,priority = 5} vs. QID Mapping	W/R	000B
n.19	Reserved		W/R	000B
n.18-n.16	EXT1Pri4QIDM[2:0]	{DP= EXT1,priority = 4} vs. QID Mapping	W/R	000B
n.15	Reserved		W/R	000B
n.14-n.12	EXT1Pri3QIDM[2:0]	{DP= EXT1,priority = 3} vs. QID Mapping	W/R	000B
n.11	Reserved		W/R	000B
n.10-n.8	EXT1Pri2QIDM[2:0]	{DP= EXT1,priority = 2} vs. QID Mapping	W/R	000B
n.7	Reserved		W/R	000B
n.6-n.4	EXT1Pri1QIDM[2:0]	{DP= EXT1,priority = 1} vs. QID Mapping	W/R	000B
n.3	Reserved		W/R	000B
n.2-n.0	EXT1Pri0QIDM[2:0]	{DP= EXT1,priority = 0} vs. QID Mapping	W/R	000B

Table 89. CPU port QID Control Register 3 (0xBB80-4764)

Reg.bit	Name	Description	Mode	Default
n.31	Reserved	Reserved		
n.30-n.28	EXT2Pri7QIDM[2:0]	{DP= EXT2 , priority = 7} vs. QID Mapping	W/R	000B
n.27	Reserved		W/R	000B
n.26-n.24	EXT2Pri6QIDM[2:0]	{DP= EXT2 ,priority = 6} vs. QID Mapping	W/R	000B
n.23	Reserved		W/R	000B
n.22-n.20	EXT2Pri5QIDM[2:0]	{DP= EXT2 , priority = 5} vs. QID Mapping	W/R	000B

Reg.bit	Name	Description	Mode	Default
n.19	Reserved		W/R	000B
n.18-n.16	EXT2Pri4QIDM[2:0]	{DP= EXT2 ,priority = 4} vs. QID Mapping	W/R	000B
n.15	Reserved		W/R	000B
n.14-n.12	EXT2Pri3QIDM[2:0]	{DP= EXT2 ,priority = 3} vs. QID Mapping	W/R	000B
n.11	Reserved		W/R	000B
n.10-n.8	EXT2Pri2QIDM[2:0]	{DP= EXT2,priority = 2} vs. QID Mapping	W/R	000B
n.7	Reserved		W/R	000B
n.6-n.4	EXT2Pri1QIDM[2:0]	{DP= EXT2,priority = 1} vs. QID Mapping	W/R	000B
n.3	Reserved		W/R	000B
n.2-n.0	EXT2Pri0QIDM[2:0]	{DP= EXT2,priority = 0} vs. QID Mapping	W/R	000B

Table 90. CPU port QID Control Register 4 (0xBB80-4768)

Reg.bit	Name	Description	Mode	Default
n.31	Reserved	Reserved		
n.30-n.28	multiEXTPri7QIDM[2:0]	{DP=multi-port of Ext port , priority = 7} vs. QID Mapping	W/R	000B
n.27	Reserved		W/R	000B
n.26-n.24	MultiEXTPri6QIDM[2:0]	{DP= multi-port of Ext port, priority = 6} vs. QID Mapping	W/R	000B
n.23	Reserved		W/R	000B
n.22-n.20	MultiEXTPri5QIDM[2:0]	{DP= multi-port of Ext port, priority = 5} vs. QID Mapping	W/R	000B
n.19	Reserved		W/R	000B
n.18-n.16	MultiEXTPri4QIDM[2:0]	{DP= multi-port of Ext port, priority = 4} vs. QID Mapping	W/R	000B
n.15	Reserved		W/R	000B
n.14-n.12	MultiEXTPri3QIDM[2:0]	{DP= multi-port of Ext port, priority = 3} vs. QID Mapping	W/R	000B
n.11	Reserved		W/R	000B
n.10-n.8	MultiEXTPri2QIDM[2:0]	{DP= multi-port of Ext port, priority = 2} vs. QID Mapping	W/R	000B
n.7	Reserved		W/R	000B
n.6-n.4	MultiEXTPri1QIDM[2:0]	{DP= multi-port of Ext port, priority = 1} vs. QID Mapping	W/R	000B
n.3	Reserved		W/R	000B
n.2-n.0	MultiEXTPri0QIDM[2:0]	{DP= multi-port of Ext port, priority = 0} vs. QID Mapping	W/R	000B

9.5.4. 802.1p Remarking

Table 91. 802.1P Remarking Control Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
6C	4	8021PRMCR	802.1P Remarking Control Register	

Table 92. 802.1P Remarking Control Register (0xBB80-476C)

Reg.bit	Name	Description	Mode	Default
n.31-n.24	8021PRM_EN[7:0]	Enable/Disable 802.1P Remarking for destination output port[7:0] 0: Disable, 1: Enable. 8021PRM _EN[8:0] map to port {extenPort[2:0], port[5:0] }; Do not include CPU port.	W/R	0B
n.23-n.21	8021PRM7[2:0]	New 3-bit priority for system parsed priority 7 When a port's 802.1P remarking function is enabled, any packet that was parsed as priority value =7 will be remark the 802.1p priority information as the value that defined by 8021PRM7[2:0] .	W/R	111B
n.20-n.18	8021PRM6[2:0]	New 3-bit priority for system parsed priority 6	W/R	110B
n.17-n.15	8021PRM5[2:0]	New 3-bit priority for system parsed priority 5	W/R	101B
n.14-n.12	8021PRM4[2:0]	New 3-bit priority for system parsed priority 4	W/R	100B
n.11-n.9	8021PRM3[2:0]	New 3-bit priority for system parsed priority 3	W/R	011B
n.8-n.6	8021PRM2[2:0]	New 3-bit priority for system parsed priority 2	W/R	010B
n.5-n.3	8021PRM1[2:0]	New 3-bit priority for system parsed priority 1	W/R	001B
n.2-n.0	8021PRM0[2:0]	New 3-bit priority for system parsed priority 0	W/R	000B

9.5.5. DSCP Remarking

Table 93. DSCP Remarking Control Register Address Mapping (Base = 0xBB80-4700)

Offset	Size (byte)	Name	Description	Field
70	4	DSCPRM0	DSCP Remarking Control Register 0	
74	4	DSCPRM1	DSCP Remarking Control Register 1	
78	4	RLRC	Remarking Layer Rule Control	

Table 94. DSCP Remarking Control Register 0 (0xBB80-4770)

Reg.bit	Name	Description	Mode	Default
n.31	8021PRM_EN[8]	Enable/Disable 802.1P Remarking for destination output port[8] 0: Disable, 1: Enable.	W/R	0
n.30	reserved			
n.29-n.24	DSCPRM4[5:0]	New 6-bit DSCP value for system parsed 3-bit priority 4	W/R	101110B
n.23-n.18	DSCPRM3[5:0]	New 6-bit DSCP value for system parsed 3-bit priority 3	W/R	000000B
n.17-n.12	DSCPRM2[5:0]	New 6-bit DSCP value for system parsed 3-bit priority 2	W/R	000000B
n.11-n.6	DSCPRM1[5:0]	New 6-bit DSCP value for system parsed 3-bit priority 1	W/R	000000B
n.5-n.0	DSCPRM0[5:0]	New 6-bit DSCP value for system parsed 3-bit priority 0	W/R	000000B

Table 95. DSCP Remarking Control Register 1 (0xBB80-4774)

Reg.bit	Name	Description	Mode	Default
n.31-n.23	DSCPRM_EN[8:0]	Enable/Disable DSCP Remark for destination output port [8:0] 0: Disable, 1: Enable DSCPRM_EN[8:0] map to port {extenPort[2:0], port[5:0] } Do not include CPU port.	W/R	0B
n.22-n.18	Reserved			
n.17-n.12	DSCPRM7[5:0]	New 6-bit DSCP value for system parsed 3-bit priority 7 When a port's DSCP remarking function is enabled, any packet that was parsed as priority value =7 will be remark the 802.1p priority information as the value that defined by DSCPRM7[5:0] .	W/R	101110B
n.11-n.6	DSCPRM6[5:0]	New 6-bit DSCP value for system parsed 3-bit priority 6	W/R	101110B
n.5-n.0	DSCPRM5[5:0]	New 6-bit DSCP value for system parsed 3-bit priority 5	W/R	101110B

Table 96. Remarking Layer Rule Control (0xBB80-4778)

Reg.bit	Name	Description	Mode	Default
n.5-n.3	RMLC_DSCP[2:0]	Remarking Layer Control : Bit0 RML[0] : enL2Remarking Bit1 RML[1] : enL3Remarking Bit2 RML[2] : enL4Remarking 0 = disable. 1 = enable.	W/R	0B
n.2-n.0	RMLC_8021P[2:0]	Remarking Layer Control : Bit0 RML[0] : enL2Remarking Bit1 RML[1] : enL3Remarking Bit2 RML[2] : enL4Remarking 0 = disable. 1 = enable.	W/R	0B

9.6. VLAN Control Register

9.6.1. VLAN Control Register

Table 97. VLAN Control Register Address Mapping (Base = 0xBB80-4A00)

Offset	Size (byte)	Name	Description	Field
00	4	VCR0	VLAN Control Register	
04	4	VCR1	VLAN Control Register (reserved)	

Table 98. VLAN Control Register 0 (0xBB80-4A00)

Reg.bit	Name	Description	Mode	Default
n.31	En1QtagVIDignore	Enable 1Q Tag VID ignore of VLAN. 1 = enable ignore 1Q VLAN Tag VID. 0 = acknowledge 1Q VLAN Tag VID . When 1Q Tag ignore is set, then (1).VLAN VID should not classify based on the packet's 1Q Tag information . but the 802.1p priority information should be considered. (2).Ignore the VLAN table entry tag/untag control, all egress packet will be handle by "Don't touch" the 1Q Tag field on the output port.	R/W	0B
n.30-n.27	Reserved			
n.26-n.25	P8_AcptFType[1:0]	Accept frame Type for VLAN ingress control of port #8. AcptFType[1:0] 00 = Admit all frame. 01 = Admit 802.1Q VLAN Tagged frame only. 10 = Admit un-tag frame + priority-tag frame. Port mapping : P[0]~P[8] is map to : port 0,1,2,3,4 , MII port, extension port 0,1,2 .	R/W	0B
n.24-n.23	P7_AcptFType[1:0]	Accept frame Type for VLAN ingress control of port #7.	R/W	0B
n.22-n.21	P6_AcptFType[1:0]	Accept frame Type for VLAN ingress control of port #6.	R/W	0B
n.20-n.19	P5_AcptFType[1:0]	Accept frame Type for VLAN ingress control of port #5.	R/W	0B
n.18-n.17	P4_AcptFType[1:0]	Accept frame Type for VLAN ingress control of port #4.	R/W	0B
n.16-n.15	P3_AcptFType[1:0]	Accept frame Type for VLAN ingress control of port #3.	R/W	0B
n.14-n.13	P2_AcptFType[1:0]	Accept frame Type for VLAN ingress control of port #2.	R/W	0B
n.12-n.11	P1_AcptFType[1:0]	Accept frame Type for VLAN ingress control of port #1.	R/W	0B
n.10-n.9	P0_AcptFType[1:0]	Accept frame Type for VLAN ingress control of port #0.	R/W	0B
n.8-n.0	EnVlanInF[8:0]	Enable Vlan Ingress filtering (bit map). 0: Disable Vlan Ingress filtering 1: Enable Vlan Ingress filtering A VLAN configuration should exist, even if in L2 only. If a VLAN configuration does not exist, the packet will be dropped under any condition. VLAN ingress filtering is based on MBR (Memory-based Reasoning).	R/W	111111111 B

Table 99. VLAN Control Register 1 (0xBB80-4A04)

Reg.bit	Name	Description	Mode	Default
n.31-n.0	Reserved			

9.6.2. Port-Based VLAN

Table 100. Port Based VLAN Control Register Address Mapping (Base = 0xBB80-4A00)

Offset	Size (byte)	Name	Description	Field
08	4	PVCR0	Port based VLAN Control Register 0	
0C	4	PVCR1	Port based VLAN Control Register 1	
10	4	PVCR2	Port based VLAN Control Register 2	
14	4	PVCR3	Port based VLAN Control Register 3	
18	4	PVCR4	Port based VLAN Control Register 4	

Table 101. Port Based VLAN Control Register 0 (0xBB80-4A08)

Reg.bit	Name	Description	Mode	Default
n.31	Reserved			
n.30-n.28	DPRIOP1[2:0]	Default Port priority for port 1	R/W	0x0
n.27-n.16	PVIDP1[11:0]	Default PVID for port 1	R/W	0x001
n.15	Reserved			
n.14-n.12	DPRIOP0[2:0]	Default Port priority for port 0	R/W	0x0
n.11-n.0	PVIDP0[11:0]	Default PVID for port 0	R/W	0x001

Table 102. Port Based VLAN Control Register 1 (0xBB80-4A0C)

Reg.bit	Name	Description	Mode	Default
n.31	Reserved			
n.30-n.28	DPRIOP3[2:0]	Default Port priority for port 3	R/W	0x0
n.27-n.16	PVIDP3[11:0]	Default PVID for port 3	R/W	0x001
n.15	Reserved			
n.14-n.12	DPRIOP2[2:0]	Default Port priority for port 2	R/W	0x0
n.11-n.0	PVIDP2[11:0]	Default PVID for port 2	R/W	0x001

Table 103. Port Based VLAN Control Register 2 (0xBB80-4A10)

Reg.bit	Name	Description	Mode	Default
n.31	Reserved			
n.30-n.28	DPRIOP5[2:0]	Default Port priority for port 5	R/W	0x0
n.27-n.16	PVIDP5[11:0]	Default PVID for port 5	R/W	0x001
n.15	Reserved			
n.14-n.12	DPRIOP4[2:0]	Default Port priority for port 4	R/W	0x0
n.11-n.0	PVIDP4[11:0]	Default PVID for port 4	R/W	0x001

Table 104. Port Based VLAN Control Register 3 (0xBB80-4A14)

Reg.bit	Name	Description	Mode	Default
n.31	Reserved			
n.30-n.28	DPRIOP7[2:0]	Default Port priority for port 7	R/W	0x0
n.27-n.16	PVIDP7[11:0]	Default PVID for port 7	R/W	0x001
n.15	Reserved			

Reg.bit	Name	Description	Mode	Default
n.14-n.12	DPRIOPP6[2:0]	Default Port priority for port 6	R/W	0x0
n.11-n.0	PVIDP6[11:0]	Default PVID for port 6	R/W	0x001

Table 105. Port Based VLAN Control Register 4 (0xBB80-4A18)

Reg.bit	Name	Description	Mode	Default
n.31-n.15	Reserved			
n.14-n.12	DPRIOP8[2:0]	Default Port priority for port 8	R/W	0x0
n.11-n.0	PVIDP8[11:0]	Default PVID for port 8	R/W	0x001

9.7. Multicast Table

9.7.1. IPv4 Multicast Table (256 entries + 32 entries CAM)

Multicast functionality is performed in the RTL8197F via the multicast table shown in 錯誤! 找不到參照來源。.

Table 106. IPv4 Multicast Table Bit Assignment

Field	Name	Description	Bit	Bit Allocation
SIP(32)	Source IP	Source IP	31:0	W0: 31:0
DIP(28)	Destination IP	Destination IP (1110xxxxxxxxxxxx)	59:32	W1: 27:0
SPA(4)	Source Port	Source Port Address	63:60	W1: 31:28
MBR(6)	Member Port	Multicast port mask	69:64	W2: 5:0
ExtMBR(3)	Extension Member Port	Multicast port mask for external member ports 2~0.	72:70	W2: 8:6
EXTIP(4)	External IP table Index	If the destination port is external interface, the NAT is required. This field represents the translation external IP. For 8651B, this represents LSB 3 bits of IP index.	76:73	W2: 12:9
VALID(1)	Valid	Valid	77	W2: 13
CPU(1)	To CPU	Multicast to CPU	78	W2: 14
Age(3)	Age timer	5 seconds per unit	81:79	W2: 17:15
DIF(3)	Destination Interface	Destination Interface index	84:82	W2: 20:18

9.7.2. IPv6 Multicast Table (256 entries)

Table 107. IPv6 Multicast Table Bit Assignment

Field	Name	Description	Bit	Bit Allocation
SIP(128)	Source IP	Source IP	127:0	W3: ~ W0:
DIP(124)	Destination IP	Destination IP (1110xxxxxxxxxxxx)	251:128	W6: ~ W4: W7: 27:0
SPA(4)	Source Port	Source Port Address	255:252	W7: 31:28
MBR(6)	Member Port	Multicast port mask	261:256	W8: 5:0
ExtMBR(3)	Extension Member Port	Multicast port mask for external member ports 2~0.	264:262	W8: 8:6
6RDEG(1)	6rd egress	When a packet match 6RDEG=1 in an entry, After the lookup it will take the 6RD egress, and then add the IPv4 header.	265	W8: 9
6RD_IDX(3)	6rd table index	When process 6rd egress, it search the corresponded 6RD table entry, and then lookup the related IPv4 header data .	268:267	W8: 12:10
VALID(1)	Valid	Valid	269	W8: 13
CPU(1)	To CPU	Multicast to CPU	270	W8: 14
Age(3)	Age timer	5 seconds per unit	273:271	W8: 17:15

9.8. L4 NAT (1K-Entry)

Table 108. L4 TCP/UDP Table Entry Description

Field	Name	Description	Bit	Bit Allocation
INTIP(32)	Internal IP	Internal IP	31:0	W0: 31:0
VALID(1)	Valid	Valid bit(just part of). Should combine with Dedicate bit.	32	W1:0
COL(1)	Collision	**Collision bit for hash1** The bit is asserted if the Hash1 collision occurs on this entry. Once this bit is set, the auto-learn function in the entry is deactivated.	33	W1:1
AGE(6)	Aging time	Aging timer Note: Once aged out, both the 'VALID' and 'D' bits are cleared if 'STATIC' is not set. Software has to set the 'STATIC' bit to protect a hash-2 entry.	39:34	W1:7:2
OFFSET(6)	Offset for L4 port translation	This field lets CPU diverse the port translation. The translated port = [Offset(6), Hash Table Index (10)] This field is used for CPU and ASIC forwarding co-work.	45:40	W1:13:8
C2(1)	Collision bit for Hash2	Collision bit for hash2. The bit is asserted if the Hash2 collision occurs on this entry.	46	W1:14
D(1)	Dedicated	If {Valid,D}=11, the external IP is based on SelIPoffset0, external port is based on [Offset(6),SelEIDX(10)] and has index is calculated from RTL865xB's new 3 tuple based hash algorithm.(hash2) If {Valid,D}=10, this entry uses RTL8651's 5-tuple hashing algorithm.(hash1) If {Valid,D}=01, this entry is extended for SPI use.	47	W1: 15
STATIC(1)	Static entry	1: Static entry. Entry was configured by software. Never auto deleted. 0: Dynamic entry, Entry was auto learnt by ASIC. May be auto deleted if auto deleted feature enabled.	48	W1:16
INTPRT(16)	Internal L4 port	Internal L4 port	64:49	
TCPFLG(3)	TCP flag status	If {Valid,D}=10,01 and ! enhance-hash1: TCP flag to achieve dynamic aging timer control If {Valid,D}=11: or enhance-hash1 TCP flags are reused for other purposes Quiet = TCPFLG[2], 1: don't trap SYN/FIN/RST on this entry 0: Trap all SYN/FIN/RST to software Directional = TCPFLG[1], 1: this connection uses 2 entries. 0:This connection is bi-directional. Outbound=TCPFLG[0],	67:65	

		Don’ t care: If Directional=0 1: this entry is for outbound direction 0: this entry is for inbound direction		
TCP(1)	TCP entry?	1: TCP entry 0: UDP entry	68	
SelIPoffset(4)	Selected IP Offset	If {Valid,D}=11: Selected External IP table offset based on routing domain decision. If the route does not assign a domain, this value is used as a direct index (instead of an offset). Note that the assigned NextHop table index in the External IP table is used to get the MAC and PPPoE information. If {Valid,D}=10: Don’ t care	72:69	
SelEIDX(10)	Selected Entry Index	If {V,D}=11 (hash2) or enhance-hash1 Selected L4 table Entry index for inbound flow If {V,D}=10 (Hash1) and ! enhance-hash1 if STATIC=1and SelEIDX[0]=1, SelEIDX[5:1] assigns NextHop table index. Otherwise, all 10 bits reserved.	82:73	
PriValid(1)	Priority Vlaid ?	0: Invalid 1: Valid	83	
Prioirty(3)	Priority	Output Priority Selection	86:84	

10. I2S

10.1. I2S Description

10.1.1. I2S Interface

I2S (Inter-IC Sound) is a standard communication structure used in new digital audio systems. Previously digital audio signals in the consumer audio market were processed by a number of VLSI ICs. The I2S standardized communication structure increases system flexibility.

10.1.2. I2S audio Standard

Figure 9. shows a sample I2S Mono-Out/Audio-Out Interface Configuration and Figure 10. shows a sample I2S 5.1 channel Audio-Out Interface Configuration

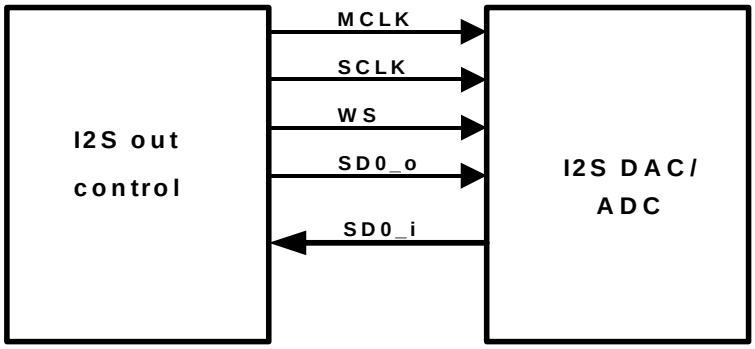


Figure 20. I2S Mono-Out/Audio-Out Interface Configuration

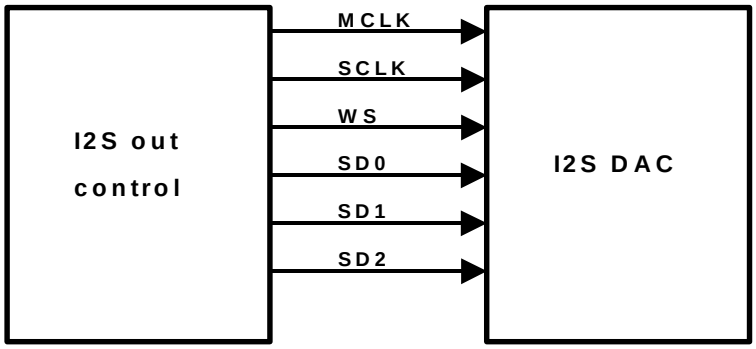


Figure 21. I2S 5.1 channel Audio-Out Interface Configuration

- WS clock is the defined sampling rate frequency
- SCLK is chosen to be 64x or 32x sampling rate frequency, which means maximum 32 bit per each channel sample is supported
- For MCLK, typically a 256x sampling rate frequency is supported. Table 109, page 207 shows a sample

clock configuration

Table 109. I2S Sample Clock Configuration

Signal Line	Description	
SCLK(24bit)/(32bit)	Frequency	Sampling Rate
	24.576 MHz	384.0 kHz
	12.288 MHz	192.0 kHz
	6.144 MHz	96.0 kHz
	3.072 MHz	48.0 kHz
	2.048 MHz	32.0 kHz
	1.536 MHz	24.0 kHz
	1.024 MHz	16.0 kHz
	0.512 MHz	8.0 kHz
SCLK(16bit)	Frequency	Sampling Rate
	12.288 MHz	384.0 kHz
	6.144 MHz	192.0 kHz
	3.072 MHz	96.0 kHz
	1.536 MHz	48.0 kHz
	1.024 MHz	32.0 kHz
	0.768 MHz	24.0 kHz
	0.512 MHz	16.0 kHz
	0.256 MHz	8.0 kHz
MCLK(24bit)/(32bit) (MCLK = 4SCLK if 256x sampling rate frequency is chosen)	Frequency	Sampling Rate
	98.304 MHz	384.0 kHz
	49.152 MHz	192.0 kHz
	24.576 MHz	96.0 kHz
	12.288 MHz	48.0 kHz
	8.192 MHz	32.0 kHz
	6.144 MHz	24.0 kHz
	4.096 MHz	16.0 kHz
	2.048 MHz	8.0 kHz
MCLK(16bit) (MCLK = 8SCLK if 256x sampling rate frequency is chosen)	98.304 MHz	384.0 kHz
	49.152 MHz	192.0 kHz
	24.576 MHz	96.0 kHz
	12.288 MHz	48.0 kHz
	8.192 MHz	32.0 kHz
	6.144 MHz	24.0 kHz
	4.096 MHz	16.0 kHz
	2.048 MHz	8.0 kHz
WS: (WS = 1/64SCLK)->24bit/32bit (WS = 1/32 SCLK)->16bit	WS = 0 to transmit channel 1 (ch0,2,4) WS = 1 to transmit channel 2 (ch1,3,5)	

SD0_o (output)	Transmitted the audio PCM data in channel[1:0] Serial data is transmitted in 2's complement with MSB first and synchronized with the trailing (HIGH to LOW) edge of clock signal
SD1 (output)	Transmitted the audio PCM data in channel[3:2] Serial data is transmitted in 2's complement with MSB first and synchronized with the trailing (HIGH to LOW) edge of clock signal
SD2 (output)	Transmitted the audio PCM data in channel[5:4] Serial data is transmitted in 2's complement with MSB first and synchronized with the trailing (HIGH to LOW) edge of clock signal
SD0_i (input)	Received the mono/audio PCM data in channel[1:0] Serial data is transmitted in 2's complement with MSB first and synchronized with the trailing (HIGH to LOW) edge of clock signal

10.2. Clock Type

- SCLK: 6.144MHz, 3.072MHz, 2.048Mz, 1.536MHz, 1.024MHz , 0.512MHz , 0.256MHZ
- MCLK: 24.576Mhz, 12.288Mz, 8.192MHz, 6.144MHz , 4.096Mhz , 2.048Mhz
- WS (Sample Rate): 384K,192K,96K, 64K,48K, 32K, 24K, 16K,12K, 8K
- WS (Sample Rate): 176.4KHz, 88.2KHz, 58.8KHz 44.1KHz, 29KHz, 22.05KHz, 14.7KHz, 11.025KHz, 7.35KHz
- MCLK=8SCLK=256WS (16-bit)
- MCLK=4SCLK=256WS (24bit)
- MCLK=4SCLK=256WS (32bit)

10.3. Features

- Sample Bit for mono : 16-bit, 32-bit
- Sample bit for stereo & 5.1channel : 16 bit ,24bit,32bit
- Sample rate: 8K,12K,16K,24K,32K,48K,64K,96K,192K ,384KHz
- I2S Throughput: 0.512Mbps(16K*32bit)~24.576Mbps(384K*64bit)
- I2S Channel Num: MONO, stereo , 5.1channel
- Maximum Page Number: 4
- Maximum Page Size: 16K-byte
- Supports MONO and Stereo TX or RX, and TX&RX mode
- Support 5.1 TX mode(DAC), not support RX(ADC) mode

10.4. FIFO Allocation

10.4.1. Mono Channel (FIFO)

Table 110. Mono Channel (FIFO)

Sample Size=16 Bits	
(MSB)Bit 31 to 16	**Bit 15 to 0 (LSB)**
Mono Channel (1)	Mono Channel (2)
Mono Channel (3)	Mono Channel (4)
Mono Channel (5)	Mono Channel (6)
Mono Channel (7)	Mono Channel (8)
Mono Channel (9)	Mono Channel (10)
Mono Channel (11)	Mono Channel (12)
Mono Channel (13)	Mono Channel (14)
Mono Channel (15)	Mono Channel (16)

Sample Size=32 Bits
(MSB)Bit 31 to 0(LSB)
Mono Channel (1)
Mono Channel (2)
Mono Channel (3)
Mono Channel (4)
Mono Channel (5)
Mono Channel (6)
Mono Channel (7)
Mono Channel (8)

10.4.2. Stereo Channel (FIFO)

Table 111. Stereo Channel (FIFO)

Sample Size=16 Bits	
(MSB)Bit 31 to 16	**Bit 15 to 0 (LSB)**
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel

Sample Size=24 Bits	
(MSB)Bit 31 to 24	**Bit 23 to 0 (LSB)**
8’b0	Left Channel
8’b0	Right Channel
8’b0	Left Channel
8’b0	Right Channel
8’b0	Left Channel
8’b0	Right Channel
8’b0	Left Channel
8’b0	Right Channel

Sample Size=32 Bits
(MSB)Bit 31 to 0(LSB)
Left Channel
Right Channel
Left Channel
Right Channel
Left Channel
Right Channel
Left Channel
Right Channel

10.4.3. 5.1 Channel (FIFO)

Table 112. 5.1 Channel (FIFO)

Sample Size=16 Bits	
(MSB)Bit 31 to 16	**Bit 15 to 0 (LSB)**
Left Channel (A)	Right Channel (A)
Left Channel (B)	Right Channel (B)
Left Channel (C)	Right Channel (C)
Left Channel (A)	Right Channel (A)
Left Channel (B)	Right Channel (B)
Left Channel (C)	Right Channel (C)
Left Channel (A)	Right Channel (A)
Left Channel (B)	Right Channel (B)

Sample Size=24 Bits	
(MSB)Bit 31 to 24	**Bit 23 to 0 (LSB)**
8’b0	Left Channel(A)
8’b0	Left Channel(B)
8’b0	Left Channel(C)
8’b0	Right Channel(A)

Sample Size=24 Bits	
(MSB)Bit 31 to 24	**Bit 23 to 0 (LSB)**
8’b0	Right Channel(B)
8’b0	Right Channel(C)
8’b0	Left Channel(A)
8’b0	Left Channel(B)

Sample Size=32 Bits
(MSB)Bit 31 to 0(LSB)
Left Channel(A)
Left Channel(B)
Left Channel(C)
Right Channel(A)
Right Channel(B)
Right Channel(C)
Left Channel(A)
Left Channel(B)

10.5. I2S Register Address Mapping (Base: 0xB801_F000)

Table 113. I2S Register Address Mapping (Base: 0xB801_F000)

Offset	Size (Byte)	Mode	Tag	Description
0x00	4	RW	IIS_CR	I2S Control Register.
0x04	4	RW	PAGE_PTR_TX	TX Page Pointer Register.
0x08	4	RW	PAGE_PTR_RX	RX Page Pointer Register.
0x0C	4	RW	PAGE_SIZE PAGE_NUM_SR	Page Size and Sample Rate Setting Register. The used page number can be configured from 1 to 4 (default is 2).
0x10	4	RW	P0OKIE_TX P1OKIE_TX P2OKIE_TX P3OKIE_TX BUFUNAVA_IE_TX	TX Interrupt Enable Register.
0x14	4	R	P0OKIP_TX P1OKIP_TX P2OKIP_TX P3OKIP_TX BUFUNAVA_IP_TX	TX Interrupt Status Register.
0x18	4	RW	P0OKIE_RX P1OKIE_RX P2OKIE_RX P3OKIE_RX BUFUNAVA_IE_RX	RX Interrupt Enable Register.
0x1C	4	R	P0OKIP_RX P1OKIP_RX P2OKIP_RX P3OKIP_RX BUFUNAVA_IP_RX	RX Interrupt Status Register.
0x20	4	RW	POWN_TX	TX Page 0 Own Bit.
0x24	4	RW	P1WN_TX	TX Page 1 Own Bit.
0x28	4	RW	P2WN_TX	TX Page 2 Own Bit.
0x2C	4	RW	P3WN_TX	TX Page 3 Own Bit.
0x30	4	RW	POWN_RX	RX Page 0 Own Bit.
0x34	4	RW	P1WN_RX	RX Page 1 Own Bit.
0x38	4	RW	P2WN_RX	RX Page 2 Own Bit.
0x3C	4	RW	P3WN_RX	RX Page 3 Own Bit.

10.5.1. I2S Control Register (0xB801_F000)

Table 114. I2S Control Register (0xB801_F000)

Reg.bit	Name	Description	Mode	Default
31	SW_RSTN	0: SW reset (this reset will clear FIFO, reset to memory 1st address, but not clear ISR. The last pending interrupt must be cleared before re-enabling I2S) 1: No SW reset	RW	0x1B
30:29	WL	Word Length 0 (00) - 16bits 1 (01) – 24bits 2 (10) – 32bits 3 (11) – unused (error)	RW	0B
28:13	-	Reserved.	-	-
12	BYTE_SWAP	Byte swap for big endian or little endian 0: Disable for big endian 1: Enable for little endian	RW	0B
11	SCK_SWAP	Invert sck 0: Disable 1: Enable	RW	0B
10	DACLRSWAP	Controls whether the DAC Appears on the 'Right' or 'Left' Phase of the WS Clock. 0: Left phase 1: Right phase	RW	0B
9:8	FORMAT	Digital Interface Format. 0 (00): I^2S 1 (01): Left justified 2 (10): Right justified	RW	0B
7	LOOP_BACK	Internal Testing.	RW	0B
6	WL	Word Length. 0: 16 bits 1: Reserved	RW	0B
5	EDGE_SW	Edge Switch.(only for 16 bit mode) 0: Negative edge 1: Positive edge	RW	0B
4:3	Audio_Mono	Audio_mono 0 (00) – stereo audio 1 (01) – 5.1 audio 2 (10) – mono	RW	0B
2:1	TX_RX_ACT	Tx_act 00: RX path 01: TX path 10: TX_RX path Bi-direction audio/voice application (not involve 5.1 audio)	RW	0B
0	IIS_EN	I2S Enable. 0: Disable 1: Enable	R/W	0B

10.5.2. TX Page Pointer Register (0xB801_F004)

Table 115. TX Page Pointer Register (0xB801_F004)

Reg.bit	Name	Description	Mode	Default
31:2	PAGE_PTR_TX	TX Page Pointer. This is a physical address with word-align limitation.	RW	0H

10.5.3. RX Page Pointer Register (0xB801_F008)

Table 116. RX Page Pointer Register (0xB801_F008)

Reg.bit	Name	Description	Mode	Default
31:2	PAGE_PTR_RX	RX Page Pointer. This is a physical address with word-align limitation.	RW	0H

10.5.4. Page Size and Sample Rate Setting Register (0xB801_F00C)

Table 117. Page Size and Sample Rate Setting Register (0xB801_F00C)

Reg.bit	Name	Description	Mode	Default
11:0	PAGE_SIZE	Page size (word unit)	RW	0B
13:12	PAGE_NUM	Page number	RW	0B
17:14	SR	Sample rate 0000=8KHz /7.35K, 0001=12KHz /11.025K 0010=16KHz /14.7K 0011=24KHz /22.05KHz 0100=32KHz /29.4KHz 0101=48KHz /44.1KHz 0110=64KHz /58.8KHz 0111=96KHz /88.2KHz 1000=192KHz /176.4KHz 1001=384KHz Others=reserved	RW	0101B
18	CLK_SWITCH	CLK_iis switch 0: clk_iis=98.304MHz 1: clk_iis=45.1584MHz	RW	0B

10.5.5. TX Interrupt Enable Register (0xB801_F010)

Table 118. TX Interrupt Enable Register (0xB801_F010)

Reg.bit	Name	Description	Mode	Default
0	P0OKIE_TX	TX Page 0 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
1	P1OKIE_TX	TX Page 1 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B

2	P2OKIE_TX	TX Page 2 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
3	P3OKIE_TX	TX Page 3 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
4	PAGEUNAVA_IE_TX	TX Page 0 Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
5	PAGEUNAVA_IE_TX	TX Page 1 Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
6	PAGEUNAVA_IE_TX	TX Page 2 Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
7	PAGEUNAVA_IE_TX	TX Page 3 Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
8	FIFO_EMPTY_IE_TX	TX FIFO Empty Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B

10.5.6. TX Interrupt Status Register (0xB801_F014)

Table 119. TX Interrupt Status Register (0xB801_F014)

Reg.bit	Name	Description	Mode	Default
0	P0OKIP_TX	TX Page 0 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
1	P1OKIP_TX	TX Page 1 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
2	P2OKIP_TX	TX Page 2 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
3	P3OKIP_TX	TX Page 3 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
4	PAGEUNAVA_IP_TX	TX Page 0 Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
5	PAGEUNAVA_IP_TX	TX Page 1 Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
6	PAGEUNAVA_IP_TX	TX Page 2 Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
7	PAGEUNAVA_IP_TX	TX Page 3 Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
8	FIFO_EMPTY_IP_TX	TX FIFO Empty Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B

10.5.7. RX Interrupt Enable Register (0xB801_F018)

Table 120. RX Interrupt Enable Register (0xB801_F018)

Reg.bit	Name	Description	Mode	Default
0	P0OKIE_RX	RX Page 0 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B

1	P1OKIE_RX	RX Page 1 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
2	P2OKIE_RX	RX Page 2 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
3	P3OKIE_RX	RX Page 3 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
4	PAGEUNAVA_IE_RX	RX Page 0 Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
5	PAGEUNAVA_IE_RX	RX Page 1 Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
6	PAGEUNAVA_IE_RX	RX Page 2 Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
7	PAGEUNAVA_IE_RX	RX Page 3 Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
8	FIFO_FULL_IE_RX	RX FIFO Full Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B

10.5.8. RX Interrupt Status Register (0xB801_F01C)

Table 121. RX Interrupt Status Register (0xB801_F01C)

Reg.bit	Name	Description	Mode	Default
0	P0OKIP_RX	RX Page 0 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
1	P1OKIP_RX	RX Page 1 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
2	P2OKIP_RX	RX Page 2 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
3	P3OKIP_RX	RX Page 3 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
4	PAGEUNAVA_IP_RX	RX Page 0 Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
5	PAGEUNAVA_IP_RX	RX Page 1 Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
6	PAGEUNAVA_IP_RX	RX Page 2 Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
7	PAGEUNAVA_IP_RX	RX Page 3 Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
8	FIFO_FULL_IP_RX	RX FIFO Full Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B

10.5.9. TX Page 0 Own Bit (0xB801_F020)

Table 122. TX Page 0 Own Bit (0xB801_F020)

Reg.bit	Name	Description	Mode	Default
31	P0OWN_TX	TX Page 0 Own Bit. 0: Page 0 owned by CPU 1: Page 0 owned by I2S controller	RW	0B

10.5.10. TX Page 1 Own Bit (0xB801_F024)

Table 123. TX Page 1 Own Bit (0xB801_F024)

Reg.bit	Name	Description	Mode	Default
31	P1OWN_TX	TX Page 1 Own Bit. 0: Page 1 owned by CPU 1: Page 1 owned by I2S controller	RW	0B

10.5.11. TX Page 2 Own Bit (0xB801_F028)

Table 124. TX Page 2 Own Bit (0xB801_F028)

Reg.bit	Name	Description	Mode	Default
31	P2OWN_TX	TX Page 2 Own Bit. 0: Page 2 owned by CPU 1: Page 2 owned by I2S controller	RW	0B

10.5.12. TX Page 3 Own Bit (0xB801_F02C)

Table 125. TX Page 3 Own Bit (0xB801_F02C)

Reg.bit	Name	Description	Mode	Default
31	P3OWN_TX	TX Page 3 Own Bit. 0: Page 3 owned by CPU 1: Page 3 owned by I2S controller	RW	0B

10.5.13. RX Page 0 Own Bit (0xB801_F030)

Table 126. RX Page 0 Own Bit (0xB801_F030)

Reg.bit	Name	Description	Mode	Default
31	P0OWN_RX	RX Page 0 Own Bit. 0: Page 0 owned by CPU 1: Page 0 owned by I2S controller	RW	0B

10.5.14. RX Page 1 Own Bit (0xB801_F034)

Table 127. RX Page 1 Own Bit (0xB801_F034)

Reg,bit	Name	Description	Mode	Default
31	P1OWN_RX	RX Page 1 Own Bit. 0: Page 1 owned by CPU 1: Page 1 owned by I2S controller	RW	0B

10.5.15. RX Page 2 Own Bit (0xB801_F038)

Table 128. RX Page 2 Own Bit (0xB801_F038)

Reg.bit	Name	Description	Mode	Default
31	P2OWN_RX	RX Page 2 Own Bit. 0: Page 2 owned by CPU 1: Page 2 owned by I2S controller	RW	0B

10.5.16. RX Page 3 Own Bit (0xB801_F03C)

Table 129. RX Page 3 Own Bit (0xB801_F03C)

Reg.bit	Name	Description	Mode	Default
31	P3OWN_RX	RX Page 3 Own Bit. 0: Page 3 owned by CPU 1: Page 3 owned by I2S controller	RW	0B

11. PCM

11.1. PCM Description

11.1.1. PCM Interface

PCM (Pulse Code Modulation) interface is a kind of TDM(Time-Division Multiplexing) bus used in voice systems. In the PCM interface, multi-channels data can betransmitting and receiving over a common signal.

11.1.2. PCM Voice Standard

Figure 11. shows a sample PCM Interface Configuration

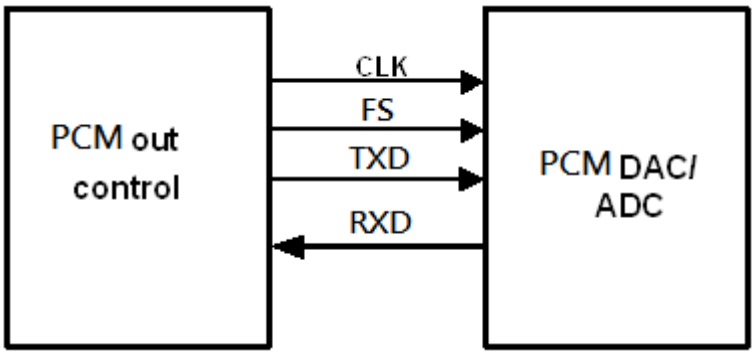


Figure 22. PCM Interface Configuration

- 2.048MHz clock signal
- 8k Hz FS signal
- 32 timeslots for 8-bit PCM data (in 16-bit linear mode PCM, support 16 independent channels)

11.2. Features

- Support 16 independent channels for VOIP application
- Flexible timing control
- Support A law/ μ law companding and 16 bit linear mode
- Support narrow band/wide band for 8K/16K sample rate

11.3. PCM Register Address Mapping (Base: 0xB800_8000)

Table 130. PCM Register Address Mapping (Base: 0xB800_8000)

Address	Size (byte)	Name	Description
0x0	4	PCMCR	PCM interface Control Register
0x4	4	PACHCNR03	PCM interface A Channel0-3 specific Control Register
0x8	4	PATSR03	PCM interface A Channel0-3 Time Slot Assignment Register.
0xc	4	PABSIZE03	PCM interface A Channel0-3 Buffer Size register
0x10	4	CH0ATXBSA	PCM interface A Channel 0 TX buffer starting address pointer.
0x14	4	CH1ATXBSA	PCM interface A Channel 1 TX buffer starting address pointer.
0x18	4	CH2ATXBSA	PCM interface A Channel 2 TX buffer starting address pointer.
0x1c	4	CH3ATXBSA	PCM interface A Channel 3 TX buffer starting address pointer.
0x20	4	CH0ARXBSA	PCM interface A Channel 0 RX buffer starting address pointer.
0x24	4	CH1ARXBSA	PCM interface A Channel 1 RX buffer starting address pointer.
0x28	4	CH2ARXBSA	PCM interface A Channel 2 RX buffer starting address pointer.
0x2c	4	CH3ARXBSA	PCM interface A Channel 3 RX buffer starting address pointer.
0x30	4	PAIMR03	PCM interface A Channel0-3 Interrupt Mask Register
0x34	4	PAISR03	PCM interface A Channel0-3 Interrupt Status Register
0x38	4	PACHCNR47	PCM interface A Channel4-7 specific Control Register
0x3c	4	PATSR47	PCM interface A Channel4-7 Time Slot Assignment Register.
0x40	4	PABSIZE47	PCM interface A Channel4-7 Buffer Size register
0x44	4	CH4ATXBSA	PCM interface A Channel 4 TX buffer starting address pointer.
0x48	4	CH5ATXBSA	PCM interface A Channel 5 TX buffer starting address pointer.
0x4c	4	CH6ATXBSA	PCM interface A Channel 6 TX buffer starting address pointer.
0x50	4	CH7ATXBSA	PCM interface A Channel 7 TX buffer starting address pointer.
0x54	4	CH4ARXBSA	PCM interface A Channel 4 RX buffer starting address pointer.
0x58	4	CH5ARXBSA	PCM interface A Channel 5 RX buffer starting address pointer.
0x5c	4	CH6ARXBSA	PCM interface A Channel 6 RX buffer starting address pointer.
0x60	4	CH7ARXBSA	PCM interface A Channel 7 RX buffer starting address pointer.
0x64	4	PAIMR47	PCM interface A Channel4-7 Interrupt Mask Register
0x68	4	PAISR47	PCM interface A Channel4-7 Interrupt Status Register
0x6c	4	PACHCNR811	PCM interface A Channel8-11 specific Control Register
0x70	4	PATSR811	PCM interface A Channel8-11 Time Slot Assignment Register.
0x74	4	PABSIZE811	PCM interface A Channel8-11 Buffer Size register
0x78	4	CH8ATXBSA	PCM interface A Channel 8 TX buffer starting address pointer.
0x7c	4	CH9ATXBSA	PCM interface A Channel 9 TX buffer starting address pointer.
0x80	4	CH10ATXBSA	PCM interface A Channel 10 TX buffer starting address pointer.
0x84	4	CH11ATXBSA	PCM interface A Channel 11 TX buffer starting address pointer.
0x88	4	CH8ARXBSA	PCM interface A Channel 8 RX buffer starting address pointer.
0x8c	4	CH9ARXBSA	PCM interface A Channel 9 RX buffer starting address pointer.
0x90	4	CH10ARXBSA	PCM interface A Channel 10 RX buffer starting address pointer.
0x94	4	CH11ARXBSA	PCM interface A Channel 11 RX buffer starting address pointer.
0x98	4	PAIMR811	PCM interface A Channel8-11 Interrupt Mask Register
0x9c	4	PAISR811	PCM interface A Channel8-11 Interrupt Status Register
0xa0	4	PACHCNR1215	PCM interface A Channel8-11 specific Control Register
0xa4	4	PATSR1215	PCM interface A Channel8-11 Time Slot Assignment Register.

0xa8	4	PABSIZE1215	PCM interface A Channel8-11 Buffer Size register
0xac	4	CH12ATXBSA	PCM interface A Channel 12 TX buffer starting address pointer.
0xb0	4	CH13ATXBSA	PCM interface A Channel 13 TX buffer starting address pointer.
0xb4	4	CH14ATXBSA	PCM interface A Channel 14 TX buffer starting address pointer.
0xb8	4	CH15ATXBSA	PCM interface A Channel 15 TX buffer starting address pointer.
0xbc	4	CH12ARXBSA	PCM interface A Channel 12 RX buffer starting address pointer.
0xc0	4	CH13ARXBSA	PCM interface A Channel 13 RX buffer starting address pointer.
0xc4	4	CH14ARXBSA	PCM interface A Channel 14 RX buffer starting address pointer.
0xc8	4	CH15ARXBSA	PCM interface A Channel 15 RX buffer starting address pointer.
0xcc	4	PAIMR1215	PCM interface A Channel 12-15 Interrupt Mask Register
0xd0	4	PAISR1215	PCM interface A Channel 12-15 Interrupt Status Register
0xd4	4	PAINTMAP	PCM interface A Channel 0-15 Interrupt mapping
0xd8	4	PAWTSR03	PCM interface A Channel0-3 wideband Time Slot Assignment Register. (if narrowband don't care)
0xdc	4	PAWTSR74	PCM interface A Channel4-7 wideband Time Slot Assignment Register. (if narrowband don't care)
0xe0	4	BUFOWCHK	PCM RX buffer data overwrite indicate.

11.3.1. PCM Control Register (0xB800_8000)

Table 131. PCM control register

Bit	Bit Name	Description	R/W	InitValue
31:18		Reserved	R	x
17	ENDIAN	ENDIAN_SWAP 1:enable 0:disable		
16	ISILBE	ISI loop back mode enable 1:enable 0:disable		
15	ZSILBE	ZSI loop back mode enable(when ISI loopback enable(bit16), this bit don't care) 1 : enable 0. disalbe	R/W	0
14	C0ILBE	Internal loop back enable 0: disable 1: enable when loop back enabled, data from channel x TX FIFO is transmitted to TXD and also loop backed to RX FIFO	R/W	0
13	Linear_mode	Linear mode enable 0: enable compender 1: linear mode	R/W	0
12	PCMAE	PCM interface A Enable. 0: disable 1: enable 1→0 reset all logic and registers to initial state	R/W	0
11	-	Reserved	R/W	x
10	-	Reserved	R/W	x
9	FSINV	PCM interface A Frame synchronization invert.	R/W	0

		0: PCM0FS high active. 1: PCM0FS low active.		
8	-	Reserved	R/W	0
7:0	FCNT	Frame counter (0~255) is triggered by PCMclk between framesync	R	0

11.3.2. PCM interface Channels0-3 Specific Control Register(0xB800_8004)

Table 132. Channels0-3 Specific Control Register

Bit	Bit Name	Description	R/W	InitValue
[31:28]	CH0_SLIC_sel	Channel0 SLIC chip select. SLIC0~15	R/W	0
27	CH0band	Channel0 narrow band /wide band select. 0: narrow band 1: wide band	R/W	0
26	CH0μA	Channel 0 μ law/ A law select. 0: μ law 1: A law	R/W	0
25	CH0TE	Channel 0 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
24	CH0RE	Channel 0 Receiver Enable 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[23:20]	CH1_SLIC_sel	Channel1 SLIC chip select. SLIC0~15	R/W	0
19	CH1band	Channel1 narrow band /wide band select. 0: narrow band 1: wide band	R/W	0
18	CH1μA	Channel 1 μ law/ A law select. 0: μ law 1: A law	R/W	0
17	CH1TE	Channel 1 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
16	CH1RE	Channel 1 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[15:12]	CH2_SLIC_sel	Channel2 SLIC chip select. SLIC0~15	R/W	0
11	CH2band	Channel2 narrow band /wide band select. 0: narrow band 1: wide band	R/W	0
10	CH2μA	Channel 2 μ law/ A law select. 0: μ law 1: A law	R/W	0
9	CH2TE	Channel 2 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
8	CH2RE	Channel 2 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[7:4]	CH3_SLIC_sel	Channel3 SLIC chip select. SLIC0~15	R/W	0

3	CH3band	Channel3 narrow band /wide band select. 0: narrow band 1: wide band	R/W	0
2	CH3μA	Channel 3 μ law/ A law select. 0: μ law 1: A law	R/W	0
1	CH3TE	Channel 3 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
0	CH3RE	Channel 3 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0

11.3.3. PCM interface Channels4-7 Specific Control Register (0xB800_8038)

Table 133. Channels4-7 Specific Control Register

Bit	Bit Name	Description	R/W	InitValue
[31:28]	CH4_SLIC_sel	Channel4 SLIC chip select. SLIC0~15	R/W	0
27	CH4band	Channel4 narrow band /wide band select. 0: narrow band 1: wide band	R/W	0
26	CH4μA	Channel 4 μ law/ A law select. 0: μ law 1: A law	R/W	0
25	CH4TE	Channel 4 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
24	CH4RE	Channel 4 Receiver Enable 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[23:20]	CH5_SLIC_sel	Channel5 SLIC chip select. SLIC0~15	R/W	0
19	CH5band	Channel5 narrow band /wide band select. 0: narrow band 1: wide band	R/W	0
18	CH5μA	Channel 5 μ law/ A law select. 0: μ law 1: A law	R/W	0
17	CH5TE	Channel 5 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
16	CH5RE	Channel 5 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[15:12]	CH6_SLIC_sel	Channel6 SLIC chip select. SLIC0~15	R/W	0
11	CH6band	Channel6 narrow band /wide band select. 0: narrow band 1: wide band	R/W	0
10	CH6μA	Channel 6 μ law/ A law select. 0: μ law 1: A law	R/W	0

9	CH6TE	Channel 6 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
8	CH6RE	Channel 6 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[7:4]	CH7_SLIC_sel	Channel7 SLIC chip select. SLIC0~15	R/W	0
3	CH07and	Channel7 narrow band /wide band select. 0: narrow band 1: wide band	R/W	0
2	CH7μA	Channel 7 μ law/ A law select. 0: μ law 1: A law	R/W	0
1	CH7TE	Channel 7 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
0	CH7RE	Channel 7 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0

11.3.4. PCM interface Channels8-11 Specific Control Register (0xB800_806C)

Table 134. Channels8-11 Specific Control Register

Bit	Bit Name	Description	R/W	InitValue
[31:28]	CH8_SLIC_sel	Channel8 SLIC chip select. SLIC0~15	R/W	0
27	reserved	Reserved	R	X
26	CH8μA	Channel 8 μ law/ A law select. 0: μ law 1: A law	R/W	0
25	CH8TE	Channel 8 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
24	CH8RE	Channel 8 Receiver Enable 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[23:20]	CH9_SLIC_sel	Channel9 SLIC chip select. SLIC0~15	R/W	0
19	reserved	Reserved	R	X
18	CH9μA	Channel 9 μ law/ A law select. 0: μ law 1: A law	R/W	0
17	CH9TE	Channel 9 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
16	CH9RE	Channel 9 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[15:12]	CH10_SLIC_sel	Channel10 SLIC chip select. SLIC0~15	R/W	0
11	reserved	Reserved	R	X
10	CH10μA	Channel 10 μ law/ A law select.	R/W	0

		0: μ law 1: A law		
9	CH10TE	Channel 10 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
8	CH10RE	Channel 10 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[7:4]	CH11_SLIC_sel	Channel11 SLIC chip select. SLIC0~15	R/W	0
3	reserved	Reserved	R	X
2	CH11μA	Channel 11 μ law/ A law select. 0: μ law 1: A law	R/W	0
1	CH11TE	Channel 11 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
0	CH11RE	Channel 11 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0

11.3.5. PCM interface Channels12-15 Specific Control Register (0xB800_80A0)

Table 135. Channels12-15 Specific Control Register

Bit	Bit Name	Description	R/W	InitValue
[31:28]	CH12_SLIC_sel	Channel12 SLIC chip select. SLIC0~15	R/W	0
27	reserved	Reserved	R	X
26	CH12μA	Channel 12 μ law/ A law select. 0: μ law 1: A law	R/W	0
25	CH12TE	Channel 12 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
24	CH12RE	Channel 12 Receiver Enable 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[23:20]	CH13_SLIC_sel	Channel13 SLIC chip select. SLIC0~15	R/W	0
19	reserved	Reserved	R	X
18	CH13μA	Channel 13 μ law/ A law select. 0: μ law 1: A law	R/W	0
17	CH13TE	Channel 13 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
16	CH13RE	Channel 13 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[15:12]	CH14_SLIC_sel	Channel14 SLIC chip select. SLIC0~15	R/W	0

11	reserved	Reserved	R	X
10	CH14μA	Channel 14 μ law/ A law select. 0: μ law 1: A law	R/W	0
9	CH14TE	Channel 14 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
8	CH14RE	Channel 14 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0
[7:4]	CH15_SLIC_sel	Channel15 SLIC chip select. SLIC0~15	R/W	0
3	reserved	Reserved	R	X
2	CH15μA	Channel 15 μ law/ A law select. 0: μ law 1: A law	R/W	0
1	CH15TE	Channel 15 Transmitter Enable. 0: disable 1: enable 1→0 reset transmit logic to initial state	R/W	0
0	CH15RE	Channel 15 Receiver Enable. 0: disable 1: enable 1→0 reset receive logic to initial state	R/W	0

11.3.6. PCM interface A channel0-3 FIFO Time Slot Assignment Register (0xB800_8008)

Table 136. channel0-3 FIFO Time Slot Assignment Register

Bit	Bit Name	Description	R/W	InitValue
31:29		Reserved	R	0b000
28:24	CH0TSA	PCM interface A time slot assignment for channel 0 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
23:21		Reserved	R	0b000
20:16	CH1TSA	PCM interface A time slot assignment for channel 1 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
15:13		Reserved	R	0b000
12:8	CH2TSA	PCM interface A time slot assignment for channel 2 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
7:5		Reserved	R	0b000
4:0	CH3TSA	PCM interface A time slot assignment for channel 3 RX/TX FIFO.	R/W	0b00000

		Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed		

11.3.7. PCM interface A channel4-7 FIFO Time Slot Assignment Register (0xB800_803C)

Table 137. channel4-7 FIFO Time Slot Assignment Register

Bit	Bit Name	Description	R/W	InitValue
31:29		Reserved	R	0b000
28:24	CH4TSA	PCM interface A time slot assignment for channel 4 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
23:21		Reserved	R	0b000
20:16	CH5TSA	PCM interface A time slot assignment for channel 5 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
15:13		Reserved	R	0b000
12:8	CH6TSA	PCM interface A time slot assignment for channel 6 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
7:5		Reserved	R	0b000
4:0	CH7TSA	PCM interface A time slot assignment for channel 7 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000

11.3.8. PCM interface A channel8-11 FIFO Time Slot Assignment Register (0xB800_8070)

Table 138. channel8-11 FIFO Time Slot Assignment Register

Bit	Bit Name	Description	R/W	InitValue
31:29		Reserved	R	0b000
28:24	CH8TSA	PCM interface A time slot assignment for channel 8 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000

23:21		Reserved	R	0b000
20:16	CH9TSA	PCM interface A time slot assignment for channel 9 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
15:13		Reserved	R	0b000
12:8	CH10TSA	PCM interface A time slot assignment for channel 10 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
7:5		Reserved	R	0b000
4:0	CH11TSA	PCM interface A time slot assignment for channel 11 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000

11.3.9. PCM interface A channel12-15 FIFO Time Slot Assignment Register (0xB800_80A4)

Table 139. channel12-15 FIFO Time Slot Assignment Register

Bit	Bit Name	Description	R/W	InitValue
31:29		Reserved	R	0b000
28:24	CH12TSA	PCM interface A time slot assignment for channel 12 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
23:21		Reserved	R	0b000
20:16	CH13TSA	PCM interface A time slot assignment for channel 13 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
15:13		Reserved	R	0b000
12:8	CH14TSA	PCM interface A time slot assignment for channel 14 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
7:5		Reserved	R	0b000
4:0	CH15TSA	PCM interface A time slot assignment for channel 15 RX/TX FIFO. Slot0..slot31	R/W	0b00000

		If configured as 16 bit linear mode, only even number time slot is allowed		

11.3.10. PCM interface Channels RX Buffer starting Address Pointer Register (BASE : 0xB800_8000, OFFESET : 0x20~0x2C, 0x54~0x60, 0x88~0x94, 0xBC~0xC8)

Table 140. PCM interface Channels RX Buffer starting Address Pointer Register

Bit	Bit Name	Description	R/W	InitValue
31:2	BufPtr	Physical Buffer starting address. The buffer address must word aligned.	R/W	X
1	P1OWN	Page1 own bit, S/W only can set “1”, cannot clear it ”0”. 1: page1 owned by PCM controller 0: page1 owned by CPU	R/W	0b00
0	P0OWN	Page0 own bit, S/W only can set “1”, cannot clear it ”0”. 1: page0 owned by PCM controller 0: page0 owned by CPU	R/W	0

11.3.11. PCM interface Channels TX Buffer starting Address Pointer Register (BASE : 0xB800_8000, OFFESET : 0x10~0x1C, 0x44~0x50, 0x78~0x84, 0xAC~0xB8)

Table 141. PCM interface Channels TX Buffer starting Address Pointer Register

Bit	Bit Name	Description	R/W	InitValue
31:2	BufPtr	Physical Buffer starting address. The buffer address must word aligned.	R/W	X
1	P1OWN	Page1 own bit 1: page1 owned by PCM controller 0: page1 owned by CPU	R/W	0b00
0	P0OWN	Page0 own bit 1: page0 owned by PCM controller 0: page0 owned by CPU	R/W	0

11.3.12. PCM interface channel0-3 Buffer Size Register (0xB800_800C)

Table 142. PCM interface channel0-3 Buffer Size Register

Bit	Bit Name	Description	R/W	InitValue
31:24	CH0BSIZE	Channel 0 buffer size in unit of 4(n+1) bytes.	R/W	0
23:16	CH1BSIZE	Channel 1 buffer size in unit of 4(n+1) bytes.	R/W	0
15:8	CH2BSIZE	Channel 2 buffer size in unit of 4(n+1) bytes.	R/W	0
7:0	CH3BSIZE	Channel 3 buffer size in unit of 4(n+1) bytes.	R/W	0

11.3.13. PCM interface channel4-7 Buffer Size Register (0xB800_8040)

Table 143. PCM interface channel4-7 Buffer Size Register

Bit	Bit Name	Description	R/W	InitValue
31:24	CH4BSIZE	Channel 4 buffer size in unit of 4(n+1) bytes.	R/W	0
23:16	CH5BSIZE	Channel 5 buffer size in unit of 4(n+1) bytes.	R/W	0
15:8	CH6BSIZE	Channel 6 buffer size in unit of 4(n+1) bytes.	R/W	0
7:0	CH7BSIZE	Channel 7 buffer size in unit of 4(n+1) bytes.	R/W	0

11.3.14. PCM interface channel8-11 Buffer Size Register (0xB800_8074)

Table 144. PCM interface channel8-11 Buffer Size Register

Bit	Bit Name	Description	R/W	InitValue
31:24	CH8BSIZE	Channel 8 buffer size in unit of 4(n+1) bytes.	R/W	0
23:16	CH9BSIZE	Channel 9 buffer size in unit of 4(n+1) bytes.	R/W	0
15:8	CH10BSIZE	Channel 10 buffer size in unit of 4(n+1) bytes.	R/W	0
7:0	CH11BSIZE	Channel 11 buffer size in unit of 4(n+1) bytes.	R/W	0

11.3.15. PCM interface channel12-15 Buffer Size Register (0xB800_80A8)

Table 145. PCM interface channel12-15 Buffer Size Register

Bit	Bit Name	Description	R/W	InitValue
31:24	CH12BSIZE	Channel 12 buffer size in unit of 4(n+1) bytes.	R/W	0
23:16	CH13BSIZE	Channel 13 buffer size in unit of 4(n+1) bytes.	R/W	0
15:8	CH14BSIZE	Channel 14 buffer size in unit of 4(n+1) bytes.	R/W	0
7:0	CH15BSIZE	Channel 15 buffer size in unit of 4(n+1) bytes.	R/W	0

11.3.16. PCM interface channel0-3 Interrupt Mask Register (0xB800_8030)

Table 146. PCM interface channel0-3 Interrupt Mask Register

Bit	Bit Name	Description	R/W	InitValue
31	CH0P0TOKIE	Channel 0 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
30	CH0P1TOKIE	Channel 0 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
29	CH0P0ROKIE	Channel 0 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
28	CH0P1ROKIE	Channel 0 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0

27	CH0TBP0UAIE	Channel 0 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
26	CH0TBP1UAIE	Channel 0 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
25	CH0RBP0UAIE	Channel 0 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
24	CH0RBP1UAIE	Channel 0 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
23	CH1P0TOKIE	Channel 1 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
22	CH1P1TOKIE	Channel 1 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
21	CH1P0ROKIE	Channel 1 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
20	CH1P1ROKIE	Channel 1 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
19	CH1TBP0UAIE	Channel 1 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
18	CH1TBP1UAIE	Channel 1 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
17	CH1RBP0UAIE	Channel 1 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
16	CH1RBP1UAIE	Channel 1 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
15	CH2P0TOKIE	Channel 2 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
14	CH2P1TOKIE	Channel 2 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
13	CH2P0ROKIE	Channel 2 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
12	CH2P1ROKIE	Channel 2 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
11	CH2TBP0UAIE	Channel 2 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
10	CH2TBP1UAIE	Channel 2 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
9	CH2RBP0UAIE	Channel 2 Receive Buffer Page0 Unavailable Interrupt Enable.	R/W	0

		0: disable 1: enable		
8	CH2RBP1UAIE	Channel 2 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
7	CH3P0TOKIE	Channel 3 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
6	CH3P1TOKIE	Channel 3 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
5	CH3P0ROKIE	Channel 3 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
4	CH3P1ROKIE	Channel 3 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
3	CH3TBP0UAIE	Channel 3 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
2	CH3TBP1UAIE	Channel 3 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
1	CH3RBP0UAIE	Channel 3 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
0	CH3RBP1UAIE	Channel 3 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0

11.3.17. PCM interface channel4-7 Interrupt Mask Register (0xB800_8064)

Table 147. PCM interface channel4-7 Interrupt Mask Register

Bit	Bit Name	Description	R/W	InitValue
31	CH4P0TOKIE	Channel 4 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
30	CH4P1TOKIE	Channel 4 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
29	CH4P0ROKIE	Channel 4 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
28	CH4P1ROKIE	Channel 4 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
27	CH4TBP0UAIE	Channel 4 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
26	CH4TBP1UAIE	Channel 4 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
25	CH4RBP0UAIE	Channel 4 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
24	CH4RBP1UAIE	Channel 4 Receive Buffer Page1 Unavailable	R/W	0

		Interrupt Enable. 0: disable 1: enable		
23	CH5P0TOKIE	Channel 5 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
22	CH5P1TOKIE	Channel 5 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
21	CH5P0ROKIE	Channel 5 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
20	CH5P1ROKIE	Channel 5 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
19	CH5TBP0UAIE	Channel 5 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
18	CH5TBP1UAIE	Channel 5 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
17	CH5RBP0UAIE	Channel 5 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
16	CH1RBP1UAIE	Channel 1 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
15	CH6P0TOKIE	Channel 6 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
14	CH6P1TOKIE	Channel 6 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
13	CH6P0ROKIE	Channel 6 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
12	CH6P1ROKIE	Channel 6 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
11	CH6TBP0UAIE	Channel 6 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
10	CH6TBP1UAIE	Channel 6 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
9	CH6RBP0UAIE	Channel 6 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
8	CH6RBP1UAIE	Channel 6 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
7	CH7P0TOKIE	Channel 7 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
6	CH7P1TOKIE	Channel 7 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
5	CH7P0ROKIE	Channel 7 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0

4	CH7P1ROKIE	Channel 7 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
3	CH7TBP0UAIE	Channel 7 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
2	CH7TBP1UAIE	Channel 7 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
1	CH7RBP0UAIE	Channel 7 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
0	CH7RBP1UAIE	Channel 7 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0

11.3.18. PCM interface channel8-11 Interrupt Mask Register (0xB800_8098)

Table 148. PCM interface channel8-11 Interrupt Mask Register

Bit	Bit Name	Description	R/W	InitValue
31	CH8P0TOKIE	Channel 8 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
30	CH8P1TOKIE	Channel 8 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
29	CH8P0ROKIE	Channel 8 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
28	CH8P1ROKIE	Channel 8 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
27	CH8TBP0UAIE	Channel 8 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
26	CH8TBP1UAIE	Channel 8 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
25	CH8RBP0UAIE	Channel 8 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
24	CH8RBP1UAIE	Channel 8 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
23	CH9P0TOKIE	Channel 9 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
22	CH9P1TOKIE	Channel 9 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
21	CH9P0ROKIE	Channel 9 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
20	CH9P1ROKIE	Channel 9 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0

19	CH9TBP0UAIE	Channel 9 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
18	CH9TBP1UAIE	Channel 9 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
17	CH9RBP0UAIE	Channel 9 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
16	CH9RBP1UAIE	Channel 9 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
15	CH10P0TOKIE	Channel 10 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
14	CH10P1TOKIE	Channel 10 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
13	CH10P0ROKIE	Channel 10 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
12	CH10P1ROKIE	Channel 10 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
11	CH10TBP0UAIE	Channel 10 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
10	CH10TBP1UAIE	Channel 10 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
9	CH10RBP0UAIE	Channel 10 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
8	CH10RBP1UAIE	Channel 10 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
7	CH11P0TOKIE	Channel 11 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
6	CH11P1TOKIE	Channel 11 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
5	CH11P0ROKIE	Channel 11 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
4	CH11P1ROKIE	Channel 11 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
3	CH11TBP0UAIE	Channel 11 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
2	CH11TBP1UAIE	Channel 11 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
1	CH11RBP0UAIE	Channel 11 Receive Buffer Page0 Unavailable Interrupt Enable.	R/W	0

		0: disable 1: enable		
0	CH11RBP1UAIE	Channel 11 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0

11.3.19. PCM interface channel12-15 Interrupt Mask Register (0xB800_80CC)

Table 149. PCM interface channel12-15 Interrupt Mask Register

Bit	Bit Name	Description	R/W	InitValue
31	CH12P0TOKIE	Channel 12 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
30	CH12P1TOKIE	Channel 12 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
29	CH12P0ROKIE	Channel 12 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
28	CH12P1ROKIE	Channel 12 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
27	CH12TBP0UAIE	Channel 12 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
26	CH12TBP1UAIE	Channel 12 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
25	CH12RBP0UAIE	Channel 12 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
24	CH12RBP1UAIE	Channel 12 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
23	CH13P0TOKIE	Channel 13 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
22	CH13P1TOKIE	Channel 13 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
21	CH13P0ROKIE	Channel 13 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
20	CH13P1ROKIE	Channel 13 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
19	CH13TBP0UAIE	Channel 13 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
18	CH13TBP1UAIE	Channel 13 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
17	CH13RBP0UAIE	Channel 13 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
16	CH13RBP1UAIE	Channel 13 Receive Buffer Page1	R/W	0

		Unavailable Interrupt Enable. 0: disable 1: enable		
15	CH14P0TOKIE	Channel 14 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
14	CH14P1TOKIE	Channel 14 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
13	CH14P0ROKIE	Channel 14 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
12	CH14P1ROKIE	Channel 14 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
11	CH14TBP0UAIE	Channel 14 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
10	CH14TBP1UAIE	Channel 14 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
9	CH14RBP0UAIE	Channel 14 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
8	CH14RBP1UAIE	Channel 14 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
7	CH15P0TOKIE	Channel 15 TX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
6	CH15P1TOKIE	Channel 15 TX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
5	CH15P0ROKIE	Channel 15 RX page 0 OK Interrupt Enable. 0: disable 1: enable	R/W	0
4	CH15P1ROKIE	Channel 15 RX page 1 OK Interrupt Enable. 0: disable 1: enable	R/W	0
3	CH15TBP0UAIE	Channel 15 Transmit Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
2	CH15TBP1UAIE	Channel 15 Transmit Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
1	CH15RBP0UAIE	Channel 15 Receive Buffer Page0 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0
0	CH15RBP1UAIE	Channel 15 Receive Buffer Page1 Unavailable Interrupt Enable. 0: disable 1: enable	R/W	0

11.3.20. PCM interface channel0-3 Interrupt Status Register (0xB800_8034)

Table 150. PCM interface channel0-3 Interrupt Status Register

Bit	Bit Name	Description	R/W	InitValue

31	CH0TXP0IP	Channel 0 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
30	CH0TXP1IP	Channel 0 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
29	CH0RXP0IP	Channel 0 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
28	CH0RXP1P	Channel 0 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
27	CH0TXP0UA	Channel 0 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
26	CH0TXP1UA	Channel 0 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
25	CH0RXP0UA	Channel 0 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
24	CH0RXP1UA	Channel 0 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
23	CH1TXP0IP	Channel 1 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
22	CH1TXP1IP	Channel 1 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
21	CH1RXP0IP	Channel 1 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
20	CH1RXP1IP	Channel 1 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
19	CH1TXP0UA	Channel 1 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
18	CH1TXP1UA	Channel 1 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
17	CH1RXP0UA	Channel 1 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
16	CH1RXP1UA	Channel 1 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
15	CH2TXP0IP	Channel 2 TXPage0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
14	CH2TXP1IP	Channel 2 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
13	CH2RXP0IP	Channel 2 RXPage0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
12	CH2RXP1IP	Channel 2 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0

11	CH2TXP0UA	Channel 2 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
10	CH2TXP1UA	Channel 2 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
9	CH2RXP0UA	Channel 2 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
8	CH2RXP1UA	Channel 2 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
7	CH3TXP0IP	Channel 3 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt. Write ‘1’ to clear the interrupt.	R/W	0b0
6	CH3TXP1IP	Channel 3 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
5	CH3RXP0IP	Channel 3 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt. Write ‘1’ to clear the interrupt.	R/W	0b0
4	CH3RXP1IP	Channel 2 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
3	CH3TXP0UA	Channel 3 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
2	CH3TXP1UA	Channel 3 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
1	CH3RXP0UA	Channel 3 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
0	CH3RXP1UA	Channel 3 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0

11.3.21. PCM interface channel4-7 Interrupt Status Register (0xB800_8068)

Table 151. PCM interface channel4-7 Interrupt Status Register

Bit	Bit Name	Description	R/W	InitValue
31	CH4TXP0IP	Channel 4 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
30	CH4TXP1IP	Channel 4 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
29	CH4RXP0IP	Channel 4 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
28	CH4RXP1P	Channel 4 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0

27	CH4TXP0UA	Channel 4 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
26	CH4TXP1UA	Channel 4 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
25	CH4RXP0UA	Channel 4 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
24	CH4RXP1UA	Channel 4 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
23	CH5TXP0IP	Channel 5 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
22	CH5TXP1IP	Channel 5 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
21	CH5RXP0IP	Channel 5 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
20	CH5RXP1IP	Channel 5 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
19	CH5TXP0UA	Channel 5 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
18	CH5TXP1UA	Channel 5 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
17	CH5RXP0UA	Channel 5 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
16	CH5RXP1UA	Channel 5 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
15	CH6TXP0IP	Channel 6 TXPage0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
14	CH6TXP1IP	Channel 6 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
13	CH6RXP0IP	Channel 6 RXPage0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
12	CH6RXP1IP	Channel 6 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
11	CH6TXP0UA	Channel 6 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
10	CH6TXP1UA	Channel 6 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
9	CH6RXP0UA	Channel 6 Receive Buffer Page0 Unavailable Interrupt Pending flag.	R/W	0b0

		Write ‘1’ to clear the interrupt.		
8	CH6RXP1UA	Channel 6 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
7	CH7TXP0IP	Channel 7 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt. Write ‘1’ to clear the interrupt.	R/W	0b0
6	CH7TXP1IP	Channel 7 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
5	CH7RXP0IP	Channel 7 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt. Write ‘1’ to clear the interrupt.	R/W	0b0
4	CH7RXP1IP	Channel 7 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
3	CH7TXP0UA	Channel 7 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
2	CH7TXP1UA	Channel 7 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
1	CH7RXP0UA	Channel 7 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
0	CH7RXP1UA	Channel 7 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0

11.3.22. PCM interface channel8-11 Interrupt Status Register (0xB800_809C)

Table 152. PCM interface channel8-11 Interrupt Status Register

Bit	Bit Name	Description	R/W	InitValue
31	CH8TXP0IP	Channel 8 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
30	CH8TXP1IP	Channel 8 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
29	CH8RXP0IP	Channel 8 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
28	CH8RXP1P	Channel 8 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
27	CH8TXP0UA	Channel 8 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
26	CH8TXP1UA	Channel 8 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
25	CH8RXP0UA	Channel 8 Receive Buffer Page0 Unavailable Interrupt Pending flag.	R/W	0b0

		Write ‘1’ to clear the interrupt.		
24	CH8RXP1UA	Channel 8 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
23	CH9TXP0IP	Channel 9 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
22	CH9TXP1IP	Channel 9 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
21	CH9RXP0IP	Channel 9 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
20	CH9RXP1IP	Channel 9 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
19	CH9TXP0UA	Channel 9 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
18	CH9TXP1UA	Channel 9 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
17	CH9RXP0UA	Channel 9 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
16	CH9RXP1UA	Channel 9 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
15	CH10TXP0IP	Channel 10 TXPage0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
14	CH10TXP1IP	Channel 10 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
13	CH10RXP0IP	Channel 10 RXPage0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
12	CH10RXP1IP	Channel 10 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
11	CH10TXP0UA	Channel 10 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
10	CH10TXP1UA	Channel 10 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
9	CH10RXP0UA	Channel 10 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
8	CH10RXP1UA	Channel 10 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
7	CH11TXP0IP	Channel 11 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt. Write ‘1’ to clear the interrupt.	R/W	0b0
6	CH11TXP1IP	Channel 11 TX Page1 Interrupt Pending flag.	R/W	0b0

		Write ‘1’ to clear the interrupt.		
5	CH11RXP0IP	Channel 11 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt. Write ‘1’ to clear the interrupt.	R/W	0b0
4	CH11RXP1IP	Channel 11 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
3	CH11TXP0UA	Channel 11 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
2	CH11TXP1UA	Channel 11 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
1	CH11RXP0UA	Channel 11 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
0	CH11RXP1UA	Channel 11 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0

11.3.23. PCM interface channel12-15 Interrupt Status Register (0xB800_80D0)

Table 153. PCM interface channel12-15 Interrupt Status Register

Bit	Bit Name	Description	R/W	InitValue
31	CH12TXP0IP	Channel 12 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
30	CH12TXP1IP	Channel 12 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
29	CH12RXP0IP	Channel 12 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
28	CH12RXP1P	Channel 12 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
27	CH12TXP0UA	Channel 12 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
26	CH12TXP1UA	Channel 12 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
25	CH12RXP0UA	Channel 12 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
24	CH12RXP1UA	Channel 12 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
23	CH13TXP0IP	Channel 13 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
22	CH13TXP1IP	Channel 13 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0

21	CH13RXP0IP	Channel 13 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
20	CH13RXP1IP	Channel 13 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
19	CH13TXP0UA	Channel 13 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
18	CH13TXP1UA	Channel 13 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
17	CH13RXP0UA	Channel 13 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
16	CH13RXP1UA	Channel 13 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
15	CH14TXP0IP	Channel 14 TXPage0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
14	CH14TXP1IP	Channel 14 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
13	CH14RXP0IP	Channel 14 RXPage0 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
12	CH14RXP1IP	Channel 14 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
11	CH14TXP0UA	Channel 14 Transmit Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
10	CH14TXP1UA	Channel 14 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
9	CH14RXP0UA	Channel 14 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
8	CH14RXP1UA	Channel 14 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
7	CH15TXP0IP	Channel 15 TX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt. Write ‘1’ to clear the interrupt.	R/W	0b0
6	CH15TXP1IP	Channel 15 TX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
5	CH15RXP0IP	Channel 15 RX Page0 Interrupt Pending flag. Write ‘1’ to clear the interrupt. Write ‘1’ to clear the interrupt.	R/W	0b0
4	CH15RXP1IP	Channel 15 RX Page1 Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
3	CH15TXP0UA	Channel 15 Transmit Buffer Page0 Unavailable Interrupt Pending flag.	R/W	0b0

		Write ‘1’ to clear the interrupt.		
2	CH15TXP1UA	Channel 15 Transmit Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
1	CH15RXP0UA	Channel 15 Receive Buffer Page0 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0
0	CH15RXP1UA	Channel 15 Receive Buffer Page1 Unavailable Interrupt Pending flag. Write ‘1’ to clear the interrupt.	R/W	0b0

11.3.24. PCM interface channel0-15 Interrupt mapping Register (0xB800_80D4)

Table 154. PCM interface channel0-15 Interrupt mapping Register

Bit	Bit Name	Description	R/W	InitValue
31:16		Reserved	R	0b000
15	CH0 INTMAP	Channel 0 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
14	CH1 INTMAP	Channel 1 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
13	CH2 INTMAP	Channel 2 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
12	CH3 INTMAP	Channel 3 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
11	CH4 INTMAP	Channel 4 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
10	CH5 INTMAP	Channel 5 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
9	CH6 INTMAP	Channel 6 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
8	CH7 INTMAP	Channel 7 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
7	CH8 INTMAP	Channel 8 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
6	CH9 INTMAP	Channel 9 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
5	CH10 INTMAP	Channel 10 interrupt mapping	R/W	0

		0: interrupt 0 1: interrupt 1		
4	CH11 INTMAP	Channel 11 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
3	CH12 INTMAP	Channel 12 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
2	CH13 INTMAP	Channel 13 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
1	CH14 INTMAP	Channel 14 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0
0	CH15 INTMAP	Channel 15 interrupt mapping 0: interrupt 0 1: interrupt 1	R/W	0

11.3.25. PCM interface A channel0-3 wideband FIFO Time Slot Assignment Register (0xB800_80D8)

Table 155. PCM interface A channel0-3 wideband FIFO Time Slot Assignment Register

Bit	Bit Name	Description	R/W	InitValue
31:29		Reserved	R	0b000
28:24	CH0WTSA	PCM interface A time slot assignment for channel 0 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
23:21		Reserved	R	0b000
20:16	CH1WTSA	PCM interface A time slot assignment for channel 1 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
15:13		Reserved	R	0b000
12:8	CH2WTSA	PCM interface A time slot assignment for channel 2 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
7:5		Reserved	R	0b000
4:0	CH3WTSA	PCM interface A time slot assignment for channel 3 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000

11.3.26. PCM interface A channel4-7 wideband FIFO Time Slot Assignment Register (0xB800_80DC)

Table 156. PCM interface A channel4-7 wideband FIFO Time Slot Assignment Register

Bit	Bit Name	Description	R/W	InitValue
31:29		Reserved	R	0b000
28:24	CH4WTSA	PCM interface A time slot assignment for channel 4 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
23:21		Reserved	R	0b000
20:16	CH5WTSA	PCM interface A time slot assignment for channel 5 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
15:13		Reserved	R	0b000
12:8	CH6WTSA	PCM interface A time slot assignment for channel 6 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000
7:5		Reserved	R	0b000
4:0	CH7WTSA	PCM interface A time slot assignment for channel 7 RX/TX FIFO. Slot0..slot31 If configured as 16 bit linear mode, only even number time slot is allowed	R/W	0b00000

11.3.27. PCM interface A channel15-0 RX Buffer data overwrite indicated Register (0xB800_80E0)

Table 157. PCM interface A channel15-0 RX Buffer data overwrite indicated Register

Bit	Bit Name	Description	R/W	InitValue
31:16		Reserved	R	0b000
15	CH15OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
14	CH14OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
13	CH13OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
12	CH12OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
11	CH11OVERW	PCM RX buffer data overwrite indicate.	R/W	0b0

		Write ‘1’ to clear the status.		
10	CH10OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
9	CH9OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
8	CH8OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
7	CH7OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
6	CH6OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
5	CH5OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
4	CH4OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
3	CH3OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
2	CH2OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
1	CH1OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0
0	CH0OVERW	PCM RX buffer data overwrite indicate. Write ‘1’ to clear the status.	R/W	0b0

12. Security Engine

12.1. Architecture

12.1.1. Feature

- Operation modes:
  (1) Encryption/Decryption only.
  (2) Authentication only.
  (3) Authentication then Encryption/Decryption.
  (4) Encryption/Decryption then Authentication.

- Encryption/Decryption algorithms:
  (1) DES with ECB/CBC mode.
  (2) 3DES with ECB/CBC mode.
  (3) AES-128 with ECB/CBC/CTR mode.
  (4) AES-192 with ECB/CBC/CTR mode.
  (5) AES-256 with ECB/CBC/CTR mode.

- Authentication algorithms:
  (1) HMAC with MD5 hash function.
  (2) HMAC with SHA-1 hash function.
  (3) HMAC with SHA-2 (SHA-224 or SHA-256) hash function.
  (4) MD5 hash only.
  (5) SHA-1 hash only.
  (6) SHA-2 (SHA-224 or SHA-256) hash only

- Support packet length up to 16383 bytes:
- Support discrete memory allocation multiple frames packet, each frame address and length is byte alignment.
- Support source and destination descriptor ring, each up to 256 descriptors.

13. MISC Controls

13.1. Interrupt Control

The RTL8197F provides 14 hardware-interrupt inputs, IRQ2 to IRQ15. The Global Interrupt Mask Register (GIMR) enables/disables an interrupt coming from the Timer, USB, UART, WiFi, Switch Core, GPIO, or Timer modules. The Global Interrupt Status Register (GISR) shows the pending interrupt status. The Interrupt Routing Register (IRR) controls the mapping from the interrupt source to IRQ 2~15.

Table 158. Interrupt Control Register Address Mapping (Base = 0xB800-3000)

Offset	Size (byte)	Name	Description	Field
00	4	GIMR	Global interrupt mask register.	
04	4	GISR	Global interrupt status register.	
08	4	IRR0	Interrupt routing register 0	
0C	4	IRR1	Interrupt routing register 1	
10	4	IRR2	Interrupt routing register 2	
14	4	IRR3	Interrupt routing register 3	
18				
1C				
20	4	GIMR2	Global interrupt mask register. 2	
24	4	GISR2	Global interrupt status register 2.	
28	4	IRR4	Interrupt routing register 4	
2C	4	IRR5	Interrupt routing register 5	
30	4	IRR6	Interrupt routing register 6	
34	4	IRR7	Interrupt routing register 7	

13.1.1. Global Interrupt Mask Register (GIMR) (0xb800-3000)

Table 159. Global Interrupt Mask Register (GIMR) (0xB800-3000)

Bit	Bit Name	Description	R/W	InitVal
31	GISR2_IE	GISR2 interrupt enable	R/W	0
30	DW_I2C_0_IE	Design ware I2C 0. Interrupt enable	R/W	0
29	WLAN_MAC_IE		R/W	0
28	USB0_WAKE_IE	USB0 wake up interrupt enable	R/W	0
27	CPU_WAKE_IE	CPU wake up interrupt enable	R/W	0
26	I2S_IE	I2S interrupt enable	R/W	0
25	USB1_WAKE_IE	USB1 wake up interrupt enable.	R/W	0
24	EFUSE_CTRL_IE		R/W	0
23	DW_SSI_0_IE	Design ware SSI 0. Interrupt enable	R/W	0
22	DHC_NAND_IE	NAND Ctrl interrupt enable	R/W	0
21	PCIE0_IE	PCIE port 0 host interface interrupt enable	R/W	0
20	SECURITY_IE	Security Engine interrupt enable	R/W	0
19	PCM_IE	PCM interface interrupt enable	R/W	0
18	NFBI_IE	NFBI interrupt enable.	R/W	0
17	GPIO_EFGH_IE	GPIO Port E,F,G,H interrupt enable	R/W	0
16	GPIO_ABCD_IE	GPIO Port A,B,C,D interrupt enable.	R/W	0
15	SW_IE	Switch Core interrupt enable.	R/W	0
14	SD30_IE	SD30 interrupt enable	R/W	0
13	USB_H_IE	USB 2.0 Host interrupt enable.	R/W	0
12	USB_O_IE	USB 2.0 OTG interrupt enable.	R/W	0
11	DW_APB_TIMER_IE	Design ware apb timer interrupt enable.	R/W	0
10	TC3_IE	Timers/Counters #3 interrupt enable.	R/W	0
9	DW_UART_0_IE	Design ware UART 0. Interrupt enable	R/W	0
8	DW_GDMA_IE	Design ware GDMA. Interrupt enable	R/W	0
7	TC0_IE	Timers/Counters #0 interrupt enable.	R/W	0
6			R/W	0
5			R/W	0
4			R/W	0
3			R/W	0
2	POK33V_L_IE	EPHY POR detect interrupt enable.	R/W	0
1			R/W	0
0			R/W	0

13.1.2. Global Interrupt Status Register (GISR) (0xB800-3004)

Table 160. Global Interrupt Status Register (GISR) (0xB800-3004)

Bit	Bit Name	Description	R/W	InitVal
31	GISR2_IP	GISR2 interrupt pending flag	R	0
30	DW_I2C_0_IP	Design ware I2C 0. Interrupt pending flag	R	0
39	WLAN_MAC_IP		R	0
28	USB0_WAKE_IP	USB0 wake up interrupt pending flag	R	0
27	CPU_WAKE_IP	CPU wake up interrupt pending flag	R	0
26	I2S_IP	I2S interrupt pending flag	R	0
25	USB1_WAKE_IP	USB1 wake up interrupt pending flag.	R	0
24	EFUSE_CTRL_IP		R	0
23	DW_SSI_0_IP	Design ware SSI 0. Interrupt pending flag	R	0
22	DHC_NAND_IP	NAND Ctrl interrupt pending flag	R	0
21	PCIE0_IP	PCIE port 0 host interface interrupt pending flag	R	0
20	SECURITY_IP	Security Engine interrupt pending flag	R	0
19	PCM_IP	PCM interface interrupt pending flag	R	0
18	NFBI_IP	NFBI interrupt pending flag.	R	0
17	GPIO_EFGH_IP	GPIO Port E,F,G,H interrupt pending flag	R	0
16	GPIO_ABCD_IP	GPIO Port A,B,C,D interrupt pending flag.	R	0
15	SW_IP	Switch Core interrupt pending flag.	R	0
14	SD30_IP	SD30 interrupt pending flag	R	0
13	USB_H_IP	USB 2.0 Host interrupt pending flag.	R	0
12	USB_O_IP	USB 2.0 OTG interrupt pending flag.	R	0
11	DW_APB_TIMER_IP	Design ware apb timer interrupt pending flag.	R	0
10	TC3_IP	Timers/Counters #3 interrupt pending flag.	R	0
9	DW_UART_0_IP	Design ware UART 0. Interrupt pending flag	R	0
8	DW_GDMA_IP	Design ware GDMA. Interrupt pending flag	R	0
7	TC0_IP	Timers/Counters #0 interrupt pending flag.	R	0
6			R/WC	0
5			R/WC	0
4			R/WC	0
3			R/WC	0
2	POK33V_L_IP	EPHY POR detect interrupt pending flag.	R/WC	0
1			R/WC	0
0			R/WC	0

13.1.3. Interrupt Routing Register 0 (IRR0) (0xB800-3008)

Table 161. Interrupt Routing Register 0 (IRR0) (0xB800-3008)

Bit	Bit Name	Description	R/W	InitVal
n.31-n.28	GISR_bit_7[3:0]	GISR_bit_7 Interrupt route select	R/W	0
n.27-n.24	GISR_bit_6[3:0]	GISR_bit_6 Interrupt route select	R/W	0
n.23-n.20	GISR_bit_5[3:0]	GISR_bit_5 Interrupt route select	R/W	0
n.19-n.16	GISR_bit_4[3:0]	GISR_bit_4 Interrupt route select	R/W	0
n.15-n.12	GISR_bit_3[3:0]	GISR_bit_3 Interrupt route select	R/W	0
n.11-n.8	GISR_bit_2[3:0]	GISR_bit_2 Interrupt route select	R/W	0
n.7-n.4	GISR_bit_1[3:0]	GISR_bit_1 Interrupt route select	R/W	0
n.3-n.0	GISR_bit_0[3:0]	GISR_bit_0 Interrupt route select	R/W	0

13.1.4. Interrupt Routing Register 1 (IRR1) (0xB800-300C)

Table 162. Interrupt Routing Register 1 (IRR1) (0xB800-300C)

Bit	Bit Name	Description	R/W	InitVal
n.31-n.28	GISR_bit_15[3:0]	GISR_bit_15 Interrupt route select	R/W	0
n.27-n.24	GISR_bit_14[3:0]	GISR_bit_14 Interrupt route select	R/W	0
n.23-n.20	GISR_bit_13[3:0]	GISR_bit_13 Interrupt route select	R/W	0
n.19-n.16	GISR_bit_12[3:0]	GISR_bit_12 Interrupt route select	R/W	0
n.15-n.12	GISR_bit_11[3:0]	GISR_bit_11 Interrupt route select	R/W	0
n.11-n.8	GISR_bit_10[3:0]	GISR_bit_10 Interrupt route select	R/W	0
n.7-n.4	GISR_bit_9[3:0]	GISR_bit_9 Interrupt route select	R/W	0
n.3-n.0	GISR_bit_8[3:0]	GISR_bit_8 Interrupt route select	R/W	0

13.1.5. Interrupt Routing Register 2 (IRR2) (0xB800-3010)

Table 163. Interrupt Routing Register 2 (IRR2) (0xB800-3010)

Bit	Bit Name	Description	R/W	InitVal
n.31-n.28	GISR_bit_23[3:0]	GISR_bit_23 Interrupt route select	R/W	0
n.27-n.24	GISR_bit_22[3:0]	GISR_bit_22 Interrupt route select	R/W	0
n.23-n.20	GISR_bit_21[3:0]	GISR_bit_21 Interrupt route select	R/W	0
n.19-n.16	GISR_bit_20[3:0]	GISR_bit_20 Interrupt route select	R/W	0
n.15-n.12	GISR_bit_19[3:0]	GISR_bit_19 Interrupt route select	R/W	0
n.11-n.8	GISR_bit_18[3:0]	GISR_bit_18 Interrupt route select	R/W	0
n.7-n.4	GISR_bit_17[3:0]	GISR_bit_17 Interrupt route select	R/W	0
n.3-n.0	GISR_bit_16[3:0]	GISR_bit_16 Interrupt route select	R/W	0

13.1.6. Interrupt Routing Register 3 (IRR3) (0xB800-3014)

Table 164. Interrupt Routing Register 3 (IRR3) (0xB800-3014)

Bit	Bit Name	Description	R/W	InitVal
n.31-n.28	GISR_bit_31[3:0]	GISR_bit_31 Interrupt route select	R/W	0
n.27-n.24	GISR_bit_30[3:0]	GISR_bit_30 Interrupt route select	R/W	0
n.23-n.20	GISR_bit_29[3:0]	GISR_bit_29 Interrupt route select	R/W	0
n.19-n.16	GISR_bit_28[3:0]	GISR_bit_28 Interrupt route select	R/W	0
n.15-n.12	GISR_bit_27[3:0]	GISR_bit_27 Interrupt route select	R/W	0
n.11-n.8	GISR_bit_26[3:0]	GISR_bit_26 Interrupt route select	R/W	0
n.7-n.4	GISR_bit_25[3:0]	GISR_bit_25 Interrupt route select	R/W	0
n.3-n.0	GISR_bit_24[3:0]	GISR_bit_24 Interrupt route select	R/W	0

13.1.7. Global Interrupt Mask Register 2 (GIMR2) (0xb800-3020)

Table 165. Global Interrupt Mask Register 2 (GIMR2) (0xB800-3020)

Bit	Bit Name	Description	R/W	InitVal
31	LX2_S_BTRDY_IE	LBC 2 slave bus time ready time-out interrupt enable.	R/W	0
30	LX1_S_BTRDY_IE	LBC 1 slave bus time ready time-out interrupt enable.	R/W	0
29	LX0_S_BTRDY_IE	LBC 0 slave bus time ready time-out interrupt enable.	R/W	0
28	LX2_BTRDY_IE	LBC 2 bus time ready time-out interrupt enable.	R/W	0
27	LX1_BTRDY_IE	LBC 1 bus time ready time-out interrupt enable.	R/W	0
26	LX0_BTRDY_IE	LBC 0 bus time ready time-out interrupt enable.	R/W	0
25	LX2_BFRAME_IE	LBC 2 bus frame time-out interrupt enable.	R/W	0
24	LX1_BFRAME_IE	LBC 1 bus frame time-out interrupt enable.	R/W	0
23	LX0_BFRAME_IE	LBC 0 bus frame time-out interrupt enable.	R/W	0
22			R/W	0
21			R/W	0
20			R/W	0
19			R/W	0
18	DPI_DLL_IE	DDR PLL controller. Interrupt enable	R/W	0
17	RXI300_IE	RXI300 BUS controller. Interrupt enable	R/W	0
16	RXI310_SPIC_IE	RXI310 SPI NOR flash controller. Interrupt enable	R/W	0
15	CPU_SI_TIMER_IE	CPU Timer. Interrupt enable	R/W	0
14	CPU_SI_PC_IE	CPU Performance Counter. Interrupt enable	R/W	0
13			R/W	0
12			R/W	0
11			R/W	0
10	SWR_DDR_OVER_LOAD_IE	SWR ddr ldo over load interrupt enable	R/W	0
9	Spi_flashecc_IE	Spi_flahecc Interrupt enable	R/W	0
8	Spi_nand_IE	Spi nand Interrupt enable	R/W	0
7	DW_UART_2_IE	Design ware UART 2. Interrupt enable	R/W	0
6	DW_UART_1_IE	Design ware UART 1. Interrupt enable	R/W	0
5	DW_SSI_1_IE	Design ware SSI 1. Interrupt enable	R/W	0
4			R/W	0
3	DW_I2C_1_IE	Design ware I2C 1. Interrupt enable	R/W	0
2			R/W	0
1	TC2_IE	Timers/Counters #2 interrupt enable.	R/W	0
0	TC1_IE	Timers/Counters #1 interrupt enable.	R/W	0

13.1.8. Global Interrupt Status Register 2(GISR2) (0xB800-3024)

Table 166. Global Interrupt Status Register 2 (GISR2) (0xB800-3024)

Bit	Bit Name	Description	R/W	InitVal
31	LX2_S_BTRDY_IP	LBC 2 slave bus time ready time-out interrupt pending flag	R/WC	0
30	LX1_S_BTRDY_IP	LBC 1 slave bus time ready time-out interrupt pending flag	R/WC	0
39	LX0_S_BTRDY_IP	LBC 0 slave bus time ready time-out interrupt pending flag	R/WC	0
28	LX2_BTRDY_IP	LBC 2 bus time ready time-out interrupt pending flag	R/WC	0
27	LX1_BTRDY_IP	LBC 1 bus time ready time-out interrupt pending flag	R/WC	0
26	LX0_BTRDY_IP	LBC 0 bus time ready time-out interrupt pending flag	R/WC	0
25	LX2_BFRAME_IP	LBC 2 bus frame time-out interrupt pending flag	R/WC	0
24	LX1_BFRAME_IP	LBC 1 bus frame time-out interrupt pending flag	R/WC	0
23	LX0_BFRAME_IP	LBC 0 bus frame time-out interrupt pending flag	R/WC	0
22			R/WC	0
21			R/WC	0
20			R/WC	0
19			R/WC	0
18	DPI_DLL_IP	DDR PLL controller. Interrupt pending flag	R	0
17	RXI300_IP	RXI300 BUS controller. Interrupt pending flag	R	0
16	RXI310_SPIC_IP	RXI310 SPI NOR flash controller. Interrupt pending flag	R	0
15	CPU_SI_TIMER_IP	CPU Timer. Interrupt pending flag	R	0
14	CPU_SI_PC_IP	CPU Performance Counter. Interrupt pending flag	R	0
13			R	0
12			R	0
11			R	0
10	SWR_DDR_OVER_LOAD_IP	SWR ddr ldo over load interrupt pending flag	R	0
9	Spi_flashecc_IP	Spi_flahecc Interrupt pending flag	R	0
8	Spi_nand_IP	Spi nand Interrupt pending flag	R	0
7	DW_UART_2_IP	Design ware UART 2. Interrupt pending flag	R	0
6	DW_UART_1_IP	Design ware UART 1. Interrupt pending flag	R	0
5	DW_SSI_1_IP	Design ware SSI 1. Interrupt pending flag	R	0
4			R	0
3	DW_I2C_1_IP	Design ware I2C 1. Interrupt pending flag	R	0
2			R	0
1	TC2_IP	Timers/Counters #2 interrupt pending flag.	R	0
0	TC1_IP	Timers/Counters #1 interrupt pending flag.	R	0

13.1.9. Interrupt Routing Register 4 (IRR4) (0xB800-3028)

Table 167. Interrupt Routing Register 4 (IRR4) (0xB800-3028)

Bit	Bit Name	Description	R/W	InitVal
n.31-n.28	GISR2_bit_7[3:0]	GISR2_bit_7 Interrupt route select	R/W	0
n.27-n.24	GISR2_bit_6[3:0]	GISR2_bit_6 Interrupt route select	R/W	0
n.23-n.20	GISR2_bit_5[3:0]	GISR2_bit_5 Interrupt route select	R/W	0
n.19-n.16	GISR2_bit_4[3:0]	GISR2_bit_4 Interrupt route select	R/W	0
n.15-n.12	GISR2_bit_3[3:0]	GISR2_bit_3 Interrupt route select	R/W	0
n.11-n.8	GISR2_bit_2[3:0]	GISR2_bit_2 Interrupt route select	R/W	0
n.7-n.4	GISR2_bit_1[3:0]	GISR2_bit_1 Interrupt route select	R/W	0
n.3-n.0	GISR2_bit_0[3:0]	GISR2_bit_0 Interrupt route select	R/W	0

13.1.10. Interrupt Routing Register 5 (IRR5) (0xB800-302C)

Table 168. Interrupt Routing Register 5 (IRR5) (0xB800-302C)

Bit	Bit Name	Description	R/W	InitVal
n.31-n.28	GISR2_bit_15[3:0]	GISR2_bit_15 Interrupt route select	R/W	0
n.27-n.24	GISR2_bit_14[3:0]	GISR2_bit_14 Interrupt route select	R/W	0
n.23-n.20	GISR2_bit_13[3:0]	GISR2_bit_13 Interrupt route select	R/W	0
n.19-n.16	GISR2_bit_12[3:0]	GISR2_bit_12 Interrupt route select	R/W	0
n.15-n.12	GISR2_bit_11[3:0]	GISR2_bit_11 Interrupt route select	R/W	0
n.11-n.8	GISR2_bit_10[3:0]	GISR2_bit_10 Interrupt route select	R/W	0
n.7-n.4	GISR2_bit_9[3:0]	GISR2_bit_9 Interrupt route select	R/W	0
n.3-n.0	GISR2_bit_8[3:0]	GISR2_bit_8 Interrupt route select	R/W	0

13.1.11. Interrupt Routing Register 6 (IRR6) (0xB800-3030)

Table 169. Interrupt Routing Register 6 (IRR6) (0xB800-3030)

Bit	Bit Name	Description	R/W	InitVal
n.31-n.28	GISR2_bit_23[3:0]	GISR2_bit_23 Interrupt route select	R/W	0
n.27-n.24	GISR2_bit_22[3:0]	GISR2_bit_22 Interrupt route select	R/W	0
n.23-n.20	GISR2_bit_21[3:0]	GISR2_bit_21 Interrupt route select	R/W	0
n.19-n.16	GISR2_bit_20[3:0]	GISR2_bit_20 Interrupt route select	R/W	0
n.15-n.12	GISR2_bit_19[3:0]	GISR2_bit_19 Interrupt route select	R/W	0
n.11-n.8	GISR2_bit_18[3:0]	GISR2_bit_18 Interrupt route select	R/W	0
n.7-n.4	GISR2_bit_17[3:0]	GISR2_bit_17 Interrupt route select	R/W	0
n.3-n.0	GISR2_bit_16[3:0]	GISR2_bit_16 Interrupt route select	R/W	0

13.1.12. Interrupt Routing Register 7 (IRR7) (0xB800-3034)

Table 170. Interrupt Routing Register 7 (IRR7) (0xB800-3034)

Bit	Bit Name	Description	R/W	InitVal
n.31-n.28	GISR2_bit_31[3:0]	GISR2_bit_31 Interrupt route select	R/W	0
n.27-n.24	GISR2_bit_30[3:0]	GISR2_bit_30 Interrupt route select	R/W	0
n.23-n.20	GISR2_bit_29[3:0]	GISR2_bit_29 Interrupt route select	R/W	0
n.19-n.16	GISR2_bit_28[3:0]	GISR2_bit_28 Interrupt route select	R/W	0
n.15-n.12	GISR2_bit_27[3:0]	GISR2_bit_27 Interrupt route select	R/W	0
n.11-n.8	GISR2_bit_26[3:0]	GISR2_bit_26 Interrupt route select	R/W	0
n.7-n.4	GISR2_bit_25[3:0]	GISR2_bit_25 Interrupt route select	R/W	0
n.3-n.0	GISR2_bit_24[3:0]	GISR2_bit_24 Interrupt route select	R/W	0

13.2. Timer & Watchdog

The chip provides four sets of hardware timers and one watchdog timer. Each timer can be configured to timer mode or counter mode. Counter mode means the timer only times-out once. The initial time-out values are configured via TC0DATA and TC1DATA. The current count values are shown in TC0CNT and TC1CNT. The Clock Division Base Register (CDBR) defines the base clock for counting, and is based on a multiple of the system clock. The Timer/Counter Interrupt Register (TCIR) controls the interrupt resulting from a timer time-out. The Watchdog timer is controlled by the Watchdog Timer Control Register (WDTCNR).

13.2.1. Timer 0,1,2,3 Control Address Mapping (Base: 0xB800_3100)

Table 171. Timer Control Address Mapping (Base: 0xB800_3100)

Offset	Size (byte)	Name	Description
0x00	4	TC0DATA	Timer/Counter 0 Data Register. It specifies the time-out duration.
0x04	4	TC1DATA	Timer/Counter 1 Data Register. It specifies the time-out duration.
0x08	4	TC0CNT	Timer/Counter 0 Count Register.
0x0C	4	TC1CNT	Timer/Counter 1 Count Register.
0x10	4	TCCNR	Timer/Counter Control Register.
0x14	4	TCIR	Timer/Counter Interrupt Register.
0x18	4	CDBR	Clock Division Base Register.
0x1C	4	WDTCNR	Watchdog Timer Control Register.
0x20	4	TC2DATA	Timer/Counter 2 Data Register. It specifies the time-out duration.
0x24	4	TC3DATA	Timer/Counter 3 Data Register. It specifies the time-out duration.
0x28	4	TC2CNT	Timer/Counter 2 Count Register.
0x2C	4	TC3CNT	Timer/Counter 3 Count Register.

13.2.2. Timer/Counter 0 Data Register (0xB800_3100)

Table 172. Timer/Counter 0 Data Register (0xB800_3100)

Bit	Name	Description	RW	Default
31:4	TC0Data[27:0]	The Timer or Counter Initial Value. Counter values of 0 and 1 are not allowed.	RW	0H
3:0	-	Reserved.	-	-

13.2.3. Timer/Counter 1 Data Register (0xB800_3104)

Table 173. Timer/Counter 1 Data Register (0xB800_3104)

Bit	Name	Description	RW	Default
31:4	TC1Data[27:0]	The Timer or Counter Initial Value. Counter values of 0 and 1 are not allowed.	RW	0H
3:0	-	Reserved.	-	-

13.2.4. Timer/Counter 0 Counter Register (0xB800_3108)

Table 174. Timer/Counter 0 Counter Register (0xB800_3108)

Bit	Name	Description	RW	Default
31:4	TC0Value[27:0]	The Timer or Counter Value. Count incremented by 1 from 0.	R	-
3:0	-	Reserved.	-	-

13.2.5. Timer/Counter 1 Counter Register (0xB800_310C)

Table 175. Timer/Counter 1 Counter Register (0xB800_310C)

Bit	Name	Description	RW	Default
31:4	TC1Value[27:0]	The Timer or Counter Value. Count incremented by 1 from 0.	R	-
3:0	-	Reserved.	-	-

13.2.6. Timer/Counter Control Register (0xB800_3110)

Table 176. Timer/Counter Control Register (0xB800_3110)

Bit	Bit Name	Description	RW	Default
31	TC0En	Timer/Counter 0 Enable.	RW	0
30	TC0Mode	Timer/Counter 0 Mode. 0: Counter mode 1: Timer mode When Mitigation&Timer0 is asserted, this bit should be set to 1 to ensure normal processing.	RW	0
29	TC1En	Timer/Counter 1 Enable.	RW	0
28	TC1Mode	Timer/Counter 1 Mode. 0: Counter mode 1: Timer mode When Mitigation&Timer1 is asserted, this bit should be set to 1 to ensure normal processing.	RW	0
27	TC2En	Timer/Counter 2 Enable.	RW	0

Bit	Bit Name	Description	RW	Default
26	TC2Mode	Timer/Counter 2 Mode. 0: Counter mode 1: Timer mode When Mitigation&Timer2 is asserted, this bit should be set to 1 to ensure normal processing.	RW	0
25	TC3En	Timer/Counter 3 Enable.	RW	0
24	TC3Mode	Timer/Counter 3 Mode. 0: Counter mode 1: Timer mode When Mitigation&Timer3 is asserted, this bit should be set to 1 to ensure normal processing.	RW	0
23: 0	-	Reserved.	RW	0

13.2.7. Timer/Counter Interrupt Register (0xB800_3114)

Table 177. Timer/Counter Interrupt Register (0xB800_3114)

Bit	Bit Name	Description	RW	Default
31	TC0IE	Timer/Counter 0 Interrupt Enable.	RW	0
30	TC1IE	Timer/Counter 1 Interrupt Enable. When Mitigation&Timer1 is asserted, this bit should be set as 0 to assure normal processing.	RW	0
29	TC0IP	Timer/Counter 0 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
28	TC1IP	Timer/Counter 1 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
27	TC2IE	Timer/Counter 2 Interrupt Enable.	RW	0
26	TC3IE	Timer/Counter 3 Interrupt Enable. When Mitigation&Timer1 is asserted, this bit should be set as 0 to assure normal processing.	RW	0
25	TC2IP	Timer/Counter 2 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
24	TC3IP	Timer/Counter 3 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
23:0	-	Reserved.	RW	0

13.2.8. Clock Division Base Register (0xB800_3118)

Table 178. Clock Division Base Register (0xB800_3118)

Bit	Name	Description	RW	Default
31:16	DivFactor[16:0]	Clock Source Division Factor. Assume DivFactor=N, then Base clock=System_clock (Peripheral Lexra Bus)/N. Both values 0x0000 and 0x0001 disable the clock.	RW	0x0000
15:0	-	Reserved.	-	-

13.2.9. Watchdog Timer Control Register (0xB800_311C)

Table 179. Watchdog Timer Control Register (0xB800_311C)

Bit	Name	Description	RW	Default
31:24	WDTE[7:0]	Watchdog Enable. When these bits are set to 0xA5, the watchdog timer stops. Other values will enable the watchdog timer and cause a system reset when an overflow signal occurs.	W	0xA5
23	WDTCLR	Watchdog Clear. Write a 1 to clear the up-count watchdog counter.	W	0
22:21	OVSEL[1:0]	Lower Overflow Select Bits. These bits specify the overflow condition when the watchdog timer counts to the value. The watchdog timer is based on the base clock defined by CDBR. 00: 2^{15} 01: 2^{16} 10: 2^{17} 11: 2^{18}	RW	00
20	WatchDogIND	Watchdog Event Indicator. 0: A Watchdog RESET did not occur (POWER-ON or PIN RESET) 1: A Watchdog RESET occurred Write '1' to clear.	RW	0
19	NRFRstType	NOR Flash Reset Command Type Selection. When the watchdog event is active and WatchDogIND=1, It will cause the memory controller to reboot and issue a Flash reset command. The command type should be pre-defined by this control bit. 0: AMD NOR Flash reset command Type 1: Intel NOR Flash reset command Type *Note: This bit should not be reset by watchdog reset.* This bit has been taken over by System_Register hw_strap (Offset: 0xB800_0008h~B800_000bh, RW) Initial value: 0xff00_1410 Reg.bit[19] Strap register without PAD: Indicates NOR flash reset type	RW	0
18:17	OVSEL[3:2]	Higher Overflow Select Bits. These bits specify the overflow condition when the watchdog timer counts to the value. The watchdog timer is based on the base clock defined by CDBR. There are a total of 24 watchdog bits. Condition values are the OVSEL[3:0] 0000: 2^{15} 0001: 2^{16} 0010: 2^{17} 0011: 2^{18} 0100: 2^{19} 0101: 2^{20} 0110: 2^{21} 0111: 2^{22} 1000: 2^{23} 1001: 2^{24}	RW	0

Bit	Name	Description	RW	Default
16:0	-	Reserved.	-	-

13.2.10. Timer/Counter 2 Data Register (0xB800_3120)

Table 180. Timer/Counter 2 Data Register (0xB800_3120)

Bit	Name	Description	RW	Default
31:4	TC2Data[27:0]	The Timer or Counter Initial Value. Counter values of 0 and 1 are not allowed.	RW	0H
3:0	-	Reserved.	-	-

13.2.11. Timer/Counter 3 Data Register (0xB800_3124)

Table 181. Timer/Counter 3 Data Register (0xB800_3124)

Bit	Name	Description	RW	Default
31:4	TC3Data[27:0]	The Timer or Counter Initial Value. Counter values of 0 and 1 are not allowed.	RW	0H
3:0	-	Reserved.	-	-

13.2.12. Timer/Counter 2 Counter Register (0xB800_3128)

Table 182. Timer/Counter 2 Counter Register (0xB800_3128)

Bit	Name	Description	RW	Default
31:4	TC2Value[27:0]	The Timer or Counter Value. Count incremented by 1 from 0.	R	-
3:0	-	Reserved.	-	-

13.2.13. Timer/Counter 3 Counter Register (0xB800_312C)

Table 183. Timer/Counter 3 Counter Register (0xB800_312C)

Bit	Name	Description	RW	Default
31:4	TC3Value[27:0]	The Timer or Counter Value. Count incremented by 1 from 0.	R	-
3:0	-	Reserved.	-	-

13.3. APB Timer & PWM & Event

Total 8 generic timers.
4 PWMs
4 Events

13.3.1. Architecture

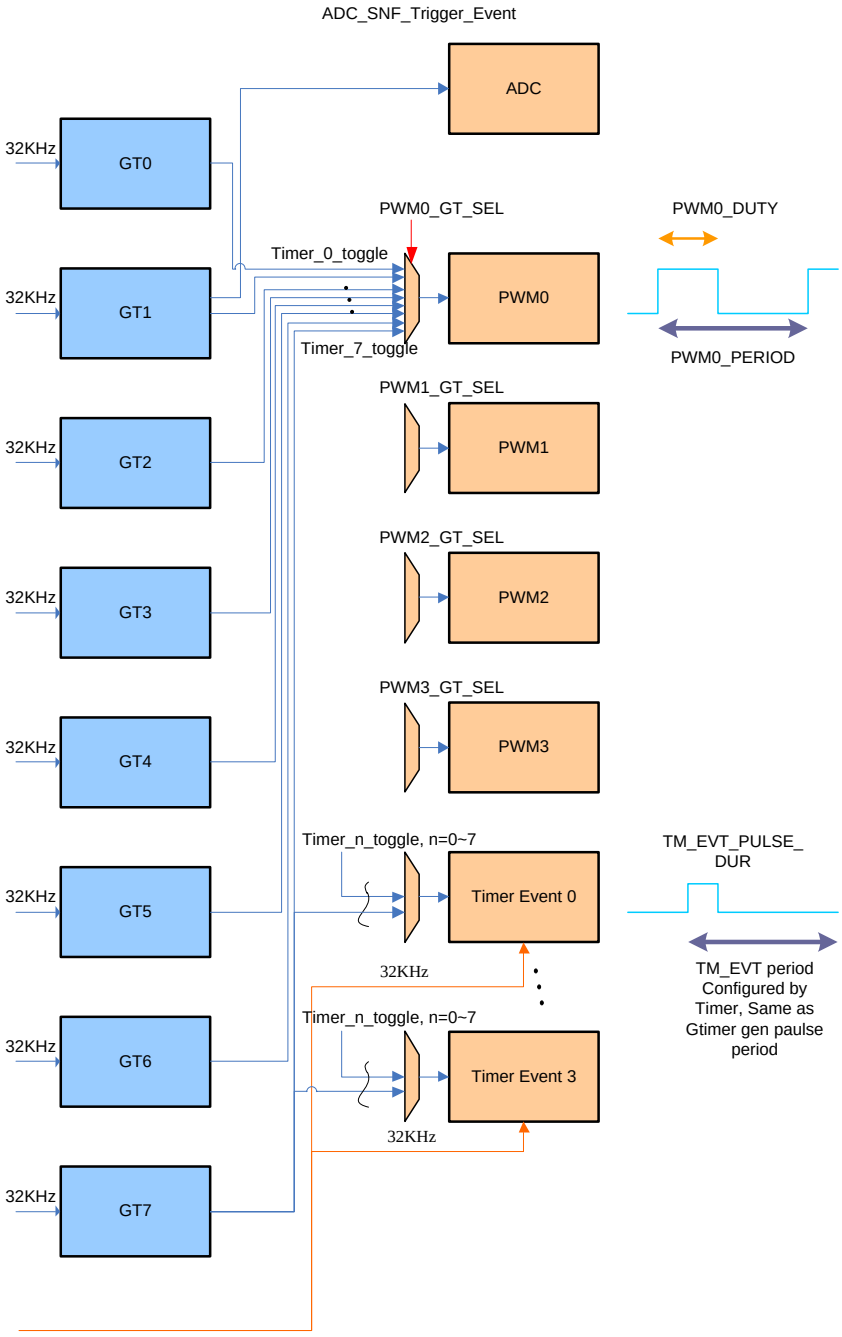


Figure 23. Architecture of Gtimer and PWM and Timer event

13.3.2. Control Register

REG_PERI _PWM0_CTRL [31:0]: GTIMER PWM0 Control Register (0xB800_0200)

REG_GT_PWM0_CTRL Register Definition

Bit	Access	INI	Symbol	Description
31	R/W	0	BIT_PERI_PWM0_EN	Enable PWM0
30:27	--	--	RSVD	RSVD
26:24	R/W	2	BIT_PERI_PWM0_GT_SEL	0: GTIMER 0 1: GTIMER 1 … 7: GTIMER 7 Etc.
23:22	--	--	RSVD	RSVD
21:12	R/W	0	BIT_PERI_PWM0_DUTY	The on-duty duration of PWM pulse. The time unit is configured from GTIMER specified by BIT_PWM0_GT_SEL field.
11:10	--	--	RSVD	RSVD
9:0	R/W	0	BIT_PERI_PWM0_PERIOD	The period of PWM pulse. The time unit is configured from GTIMER specified by BIT_PWM0_GT_SEL field.

REG_PERI _PWM1_CTRL [31:0]: GTIMER PWM1 Control Register (0xB800_0204)

REG_GT_PWM1_CTRL Register Definition

Bit	Access	INI	Symbol	Description
31	R/W	0	BIT_PERI_PWM0_EN	Enable PWM0
30:27	--	--	RSVD	RSVD
26:24	R/W	2	BIT_PERI_PWM1_GT_SEL	0: GTIMER 0 1: GTIMER 1 … 7: GTIMER 7 Etc.
23:22	--	--	RSVD	RSVD
21:12	R/W	0	BIT_PERI_PWM01_DUTY	The on-duty duration of PWM pulse. The time unit is configured from GTIMER specified by BIT_PWM0_GT_SEL field.
11:10	--	--	RSVD	RSVD
9:0	R/W	0	BIT_PERI_PWM1_PERIOD	The period of PWM pulse. The time unit is configured from GTIMER specified by BIT_PWM0_GT_SEL field.

REG_PERI _PWM2_CTRL [31:0]: GTIMER PWM2 Control Register (0xB800_0208)

REG_GT_PWM2_CTRL Register Definition

Bit	Access	INI	Symbol	Description
31	R/W	0	BIT_PERI_PWM2_EN	Enable PWM2
30:27	--	--	RSVD	RSVD
26:24	R/W	2	BIT_PERI_PWM2_GT_SEL	0: GTIMER 0

				1: GTIMER 1 … 7: GTIMER 7 Etc.
23:22	--	--	RSVD	RSVD
21:12	R/W	0	BIT_PERI_PWM2_DUTY	The on-duty duration of PWM pulse. The time unit is configured from GTIMER specified by BIT_PWM0_GT_SEL field.
11:10	--	--	RSVD	RSVD
9:0	R/W	0	BIT_PERI_PWM2_PERIOD	The period of PWM pulse. The time unit is configured from GTIMER specified by BIT_PWM2_GT_SEL field.

REG_PERI _PWM3_CTRL [31:0]: GTIMER PWM3 Control Register (0xB800_020C)

REG_GT_PWM3_CTRL Register Definition

Bit	Access	INI	Symbol	Description
31	R/W	0	BIT_PERI_PWM3_EN	Enable PWM3
30:27	--	--	RSVD	RSVD
26:24	R/W	2	BIT_PERI_PWM3_GT_SEL	0: GTIMER 0 1: GTIMER 1 … 7: GTIMER 7 Etc.
23:22	--	--	RSVD	RSVD
21:12	R/W	0	BIT_PERI_PWM3_DUTY	The on-duty duration of PWM pulse. The time unit is configured from GTIMER specified by BIT_PWM0_GT_SEL field.
11:10	--	--	RSVD	RSVD
9:0	R/W	0	BIT_PERI_PWM3_PERIOD	The period of PWM pulse. The time unit is configured from GTIMER specified by BIT_PWM3_GT_SEL field.

REG_PERI _TIM_EVT_CTRL [31:0]: GTIMER Event Control Register (0xB800_0210)

REG_TIM_EVENT_CTRL Register Definition

Bit	Access	INI	Symbol	Description
31	R/W	0	BIT_GT_EVT3_EN	Enable timer event
30:28	R/W	0	BIT_GT_EVT3_SRC_SEL	0: timer event from timer 0 7: timer event from timer 7
27:24	R/W	0	BIT_GT_EVT3_PULSE_DUR	The event timer output pulse duration 0: 32us 1: 64us 2: 128us 3: 256us
23	R/W	0	BIT_GT_EVT2_EN	Enable timer event
22:20	R/W	0	BIT_GT_EVT2_SRC_SEL	0: timer event from timer 0 7: timer event from timer 7
19:16	R/W	0	BIT_GT_EVT2_PULSE_DUR	The event timer output pulse duration 0: 32us 1: 64us 2: 128us

				3: 256us
15	R/W	0	BIT_GT_EVT1_EN	Enable timer event
14:12	R/W	0	BIT_GT_EVT1_SRC_SEL	0: timer event from timer 0 7: timer event from timer 7
11:8	R/W	0	BIT_GT_EVT1_PULSE_DUR	The event timer output pulse duration 0: 32us 1: 64us 2: 128us 3: 256us
7	R/W	0	BIT_GT_EVT0_EN	Enable timer event
6:4	R/W	0	BIT_GT_EVT0_SRC_SEL	0: timer event from timer 0 7: timer event from timer 7
3:0	R/W	0	BIT_GT_EVT0_PULSE_DUR	The event timer output pulse duration 0: 32us 1: 64us 2: 128us 3: 256us

REG_PERI _EXT_TIMER_EN [31:0]: GTIMER external timer count enable Register (0xB800_0214)

REG_GT_EXT_TIMER_EN Register Definition

Bit	Access	INI	Symbol	Description
31:1	R/W	0	RSVD	RSVD
0	R/W	0	BIT_GT_EXT_TIMER_EN	Enable external timer count

13.3.3. Operation Spec

13.3.3.1 PWM HW Operation Flow

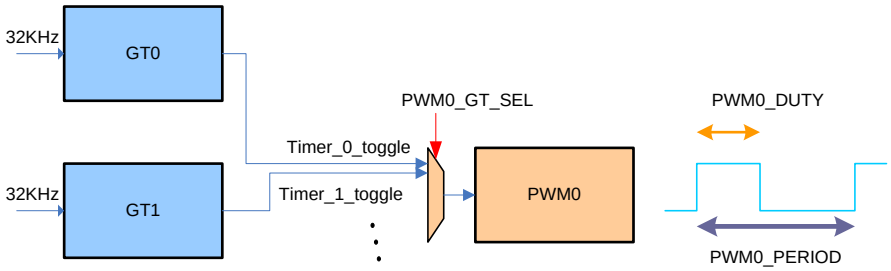


Figure 24. PWM Operation

PWM generator can select a Gtimer as its counting source. It can be configured with period and duty cycle specified by PWM0_PERIOD and PWM0_DUTY register. The tick unit is specified by Gtimer selected.

13.3.3.2 Timer Event HW Operation Flow

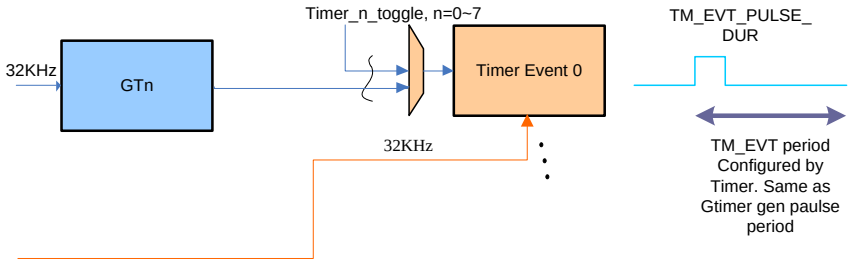


Figure 25. Timer Event Operation

The G-timer can be configured to output toggle signal to indicate the timer timeout event.

13.4. GPIO Control

The RTL8197F provides eight sets of General Purpose Input/Output (GPIO) pins (GPIO A, B, C, D, E, F, G, H). Each GPIO pin may be configured as an input or output pin. The GPIO DATA register may be used to control GPIO pin signals. The GPIO pins are shared with some peripheral pins, and the type of peripheral can affect the attributes of the shared pins. All GPIO sets can be used to generate interrupt and an interrupt mask and status register are provided. The GPIO control registers are defined in the following table.

Note :

that the detail available GPIO pin should refer to Shared I/O Pin Mapping information in Pin Description Chapter.

13.4.1. GPIO Register Set (0xB800_3500)

Table 184. GPIO Register Set (0xB800_3500)

Offset	Size (Byte)	Name	Description
0x08	4	PABCD_DIR	Port A, B, C, D Direction Register
0x0C	4	PABCD_DAT	Port A, B, C, D Data Register
0x10	4	PABCD_ISR	Port A, B, C, D Interrupt Status Register
0x14	4	PAB_IMR	Port A, B Interrupt Mask Register
0x18	4	PCD_IMR	Port C, D Interrupt Mask Register
0x24	4	PEFGH_DIR	Port E, F, G, H Direction Register
0x28	4	PEFGH_DAT	Port E, F, G, H Data Register
0x2C	4	PEFGH_ISR	Port E, F, G, H Interrupt Status Register
0x30	4	PEF_IMR	Port E, F Interrupt Mask Register
0x34	4	PGH_IMR	Port G, H Interrupt Mask Register

13.4.2. GPIO Port A, B, C, D Direction Register (PABCD_DIR) (0xB800_3508)

Table 185. GPIO Port A, B, C, D Direction Register (PABCD_DIR) (0xB800_3508)

Bit	Name	Description	Mode	Default
31:24	DRC_D[7:0]	Pin Direction Configuration of Port D 0: Configured as input pin 1: Configured as output pin	RW	00H
23:16	DRC_C[7:0]	Pin Direction Configuration of Port C 0: Configured as input pin 1: Configured as output pin	RW	00H
15:8	DRC_B[7:0]	Pin Direction Configuration of Port B 0: Configured as input pin 1: Configured as output pin	RW	00H
7:0	DRC_A[7:0]	Pin Direction Configuration of Port A 0: Configured as input pin 1: Configured as output pin	RW	00H

13.4.3. Port A, B, C, D Data Register (PABCD_DAT) (0xB800_350C)

Table 186. Port A, B, C, D Data Register (PABCD_DAT) (0xB800_350C)

Bit	Name	Description	Mode	Default
31:24	PD_D[7:0]	Pin Data of Port D 0: Data=0 1: Data=1	RW	00H
23:16	PD_C[7:0]	Pin Data of Port C 0: Data=0 1: Data=1	RW	00H
15:8	PD_B[7:0]	Pin Data of Port B 0: Data=0 1: Data=1	RW	00H
7:0	PD_A[7:0]	Pin Data of Port A 0: Data=0 1: Data=1	RW	00H

13.4.4. Port A, B, C, D Interrupt Status Register (PABCD_ISR) (0xB800_3510)

Table 187. Port A, B, C, D Interrupt Status Register (PABCD_ISR) (0xB800_3510)

Bit	Name	Description	Mode	Default
31:24	IPS_D[7:0]	Interrupt Pending Status of Port D. Write '1' to clear the interrupt	RW	00H
23:16	IPS_C[7:0]	Interrupt Pending Status of Port C. Write '1' to clear the interrupt	RW	00H
15:8	IPS_B[7:0]	Interrupt Pending Status of Port B. Write '1' to clear the interrupt	RW	00H
7:0	IPS_A[7:0]	Interrupt Pending Status of Port A. Write '1' to clear the interrupt	RW	00H

13.4.5. Port A, B Interrupt Mask Register (PAB_IMR) (0xB800_3514)

Table 188. Port A, B Interrupt Mask Register (PAB_IMR) (0xB800_3514)

Bit	Name	Description	Mode	Default
31:30	PB7_IM[1:0]	PortB.7 Interrupt Mode	RW	00B
29:28	PB6_IM[1:0]	PortB.6 Interrupt Mode	RW	00B
27:26	PB5_IM[1:0]	PortB.5 Interrupt Mode	RW	00B
25:24	PB4_IM[1:0]	PortB.4 Interrupt Mode	RW	00B
23:22	PB3_IM[1:0]	PortB.3 Interrupt Mode	RW	00B
21:20	PB2_IM[1:0]	PortB.2 Interrupt Mode	RW	00B
19:18	PB1_IM[1:0]	PortB.1 Interrupt Mode	RW	00B
17:16	PB0_IM[1:0]	PortB.0 Interrupt Mode	RW	00B
15:14	PA7_IM[1:0]	PortA.7 Interrupt Mode	RW	00B
13:12	PA6_IM[1:0]	PortA.6 Interrupt Mode	RW	00B
11:10	PA5_IM[1:0]	PortA.5 Interrupt Mode	RW	00B
9:8	PA4_IM[1:0]	PortA.4 Interrupt Mode	RW	00B
7:6	PA3_IM[1:0]	PortA.3 Interrupt Mode	RW	00B

Bit	Name	Description	Mode	Default
5:4	PA2_IM[1:0]	PortA.2 Interrupt Mode	RW	00B
3:2	PA1_IM[1:0]	PortA.1 Interrupt Mode	RW	00B
1:0	PA0_IM[1:0]	PortA.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

13.4.6. Port C, D Interrupt Mask Register (PCD_IMR) (0xB800_3518)

Table 189. Port C, D Interrupt Mask Register (PCD_IMR) (0xB800_3518)

Bit	Name	Description	Mode	Default
31:30	PD7_IM[1:0]	PortD.7 Interrupt Mode	RW	00B
29:28	PD6_IM[1:0]	PortD.6 Interrupt Mode	RW	00B
27:26	PD5_IM[1:0]	PortD.5 Interrupt Mode	RW	00B
25:24	PD4_IM[1:0]	PortD.4 Interrupt Mode	RW	00B
23:22	PD3_IM[1:0]	PortD.3 Interrupt Mode	RW	00B
21:20	PD2_IM[1:0]	PortD.2 Interrupt Mode	RW	00B
19:18	PD1_IM[1:0]	PortD.1 Interrupt Mode	RW	00B
17:16	PD0_IM[1:0]	PortC.0 Interrupt Mode	RW	00B
15:14	PC7_IM[1:0]	PortC.7 Interrupt Mode	RW	00B
13:12	PC6_IM[1:0]	PortC.6 Interrupt Mode	RW	00B
11:10	PC5_IM[1:0]	PortC.5 Interrupt Mode	RW	00B
9:8	PC4_IM[1:0]	PortC.4 Interrupt Mode	RW	00B
7:6	PC3_IM[1:0]	PortC.3 Interrupt Mode	RW	00B
5:4	PC2_IM[1:0]	PortC.2 Interrupt Mode	RW	00B
3:2	PC1_IM[1:0]	PortC.1 Interrupt Mode	RW	00B
1:0	PC0_IM[1:0]	PortC.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

13.4.7. GPIO Port E, F, G, H Direction Register (PEFGH_DIR) (0xB800_3524)

Table 190. GPIO Port E, F, G, H Direction Register (PEFGH_DIR) (0xB800_3524)

Bit	Name	Description	Mode	Default
31:24	DRC_H[7:0]	Pin Direction Configuration of Port H 0: Configured as input pin 1: Configured as output pin	RW	00H
23:16	DRC_G[7:0]	Pin Direction Configuration of Port G 0: Configured as input pin 1: Configured as output pin	RW	00H
15:8	DRC_F[7:0]	Pin Direction Configuration of Port F 0: Configured as input pin 1: Configured as output pin	RW	00H
7:0	DRC_E[7:0]	Pin Direction Configuration of Port E 0: Configured as input pin 1: Configured as output pin	RW	00H

13.4.8. Port E, F, G, H Data Register (PEFGH_DAT) (0xB800_3528)

Table 191. Port E, F, G, H Data Register (PEFGH_DAT) (0xB800_3528)

Bit	Name	Description	Mode	Default
31:24	PD_H[7:0]	Pin Data of Port H 0: Data=0 1: Data=1	RW	00H
23:16	PD_G[7:0]	Pin Data of Port G 0: Data=0 1: Data=1	RW	00H
15:8	PD_F[7:0]	Pin Data of Port F 0: Data=0 1: Data=1	RW	00H
7:0	PD_E[7:0]	Pin Data of Port E 0: Data=0 1: Data=1	RW	00H

13.4.9. Port E, F, G, H Interrupt Status Register (PEFGH_ISR) (0xB800_352C)

Table 192. Port E, F, G, H Interrupt Status Register (PEFGH_ISR) (0xB800_352C)

Bit	Name	Description	Mode	Default
31:24	IPS_H[7:0]	Interrupt Pending Status of Port H. Write '1' to clear the interrupt	RW	00H
23:16	IPS_G[7:0]	Interrupt Pending Status of Port G. Write '1' to clear the interrupt	RW	00H
15:8	IPS_F[7:0]	Interrupt Pending Status of Port F. Write '1' to clear the interrupt	RW	00H
7:0	IPS_E[7:0]	Interrupt Pending Status of Port E. Write '1' to clear the interrupt	RW	00H

13.4.10. Port E, F Interrupt Mask Register (PEF_IMR) (0xB800_3530)

Table 193. Port E, F Interrupt Mask Register (PEF_IMR) (0xB800_3530)

Bit	Name	Description	Mode	Default
31:30	PF7_IM[1:0]	PortF.7 Interrupt Mode	RW	00B
29:28	PF6_IM[1:0]	PortF.6 Interrupt Mode	RW	00B
27:26	PF5_IM[1:0]	PortF.5 Interrupt Mode	RW	00B
25:24	PF4_IM[1:0]	PortF.4 Interrupt Mode	RW	00B
23:22	PF3_IM[1:0]	PortF.3 Interrupt Mode	RW	00B
21:20	PF2_IM[1:0]	PortF.2 Interrupt Mode	RW	00B
19:18	PF1_IM[1:0]	PortF.1 Interrupt Mode	RW	00B
17:16	PF0_IM[1:0]	PortF.0 Interrupt Mode	RW	00B
15:14	PE7_IM[1:0]	PortE.7 Interrupt Mode	RW	00B
13:12	PE6_IM[1:0]	PortE.6 Interrupt Mode	RW	00B
11:10	PE5_IM[1:0]	PortE.5 Interrupt Mode	RW	00B
9:8	PE4_IM[1:0]	PortE.4 Interrupt Mode	RW	00B
7:6	PE3_IM[1:0]	PortE.3 Interrupt Mode	RW	00B
5:4	PE2_IM[1:0]	PortE.2 Interrupt Mode	RW	00B
3:2	PE1_IM[1:0]	PortE.1 Interrupt Mode	RW	00B

Bit	Name	Description	Mode	Default
1:0	PE0_IM[1:0]	PortE.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

13.4.11. Port G, H Interrupt Mask Register (PGH_IMR) (0xB800_3534)

Table 194. Port G, H Interrupt Mask Register (PGH_IMR) (0xB800_3534)

Bit	Name	Description	Mode	Default
31:30	PH7_IM[1:0]	PortH.7 Interrupt Mode	RW	00B
29:28	PH6_IM[1:0]	PortH.6 Interrupt Mode	RW	00B
27:26	PH5_IM[1:0]	PortH.5 Interrupt Mode	RW	00B
25:24	PH4_IM[1:0]	PortH.4 Interrupt Mode	RW	00B
23:22	PH3_IM[1:0]	PortH.3 Interrupt Mode	RW	00B
21:20	PH2_IM[1:0]	PortH.2 Interrupt Mode	RW	00B
19:18	PH1_IM[1:0]	PortH.1 Interrupt Mode	RW	00B
17:16	PH0_IM[1:0]	PortH.0 Interrupt Mode	RW	00B
15:14	PG7_IM[1:0]	PortG.7 Interrupt Mode	RW	00B
13:12	PG6_IM[1:0]	PortG.6 Interrupt Mode	RW	00B
11:10	PG5_IM[1:0]	PortG.5 Interrupt Mode	RW	00B
9:8	PG4_IM[1:0]	PortG.4 Interrupt Mode	RW	00B
7:6	PG3_IM[1:0]	PortG.3 Interrupt Mode	RW	00B
5:4	PG2_IM[1:0]	PortG.2 Interrupt Mode	RW	00B
3:2	PG1_IM[1:0]	PortG.1 Interrupt Mode	RW	00B
1:0	PG0_IM[1:0]	PortG.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

14. Electrical Characteristics

14.1. Clock Signal Timing

14.1.1. Crystal Clock Timing

Table 195. Crystal and OSC board configuration

	Crystal						External Frequency Reference				
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Remark
Frequency	-	25	-	-	40	-	-	25 or 40	-	MHz	
Frequency tolerance initial and over temperature	-20	-	+20	-20	-	+20	-20	-	+20	ppm	Without trimming
ESR	-	-	25	-	-	25	-	-	-	Ω	
Load capacitance	-	12	-	-	12	-	-	-	-	pF	
C1	8.2	10	12	6	8.2	10	-	-	-	pF	Depends on frequency offset
C2	-	22	-	-	27	-	-	-	-	pF	
Rin	-	2	-	-	2	-	-	-	-	Mohm	
Shunt capacitance	-	-	3	-	-	3	-	-	-	pF	
Drive level	-	-	300	-	-	300	-	-	-	uW	
Input voltage	-	-	-	-	-	-	0.9	-	1.2	V_{p-p}	AC couple input, connect to XI
Input AC couple cap.	-	-	-	-	-	-	0.1	-	-	nF	connect to XI

Duty cycle	-	-	-	-	-	-	40	50	60	%	

Note 1. The PCB parasitic capacitance on OSC_IN and OSC_OUT to ground must be smaller than 3pF, otherwise C1 must be less than 10pF/25MHz (or 8.2pF/40MHz).

Note 2. The variations of C1, C2, Rin values must be less than +/-5%.

Note 3: This value could be an oscillator input or a series resonant frequency from a crystal. If used as an oscillator input, tie to the crystal input pin and leave the crystal output pin disconnected.

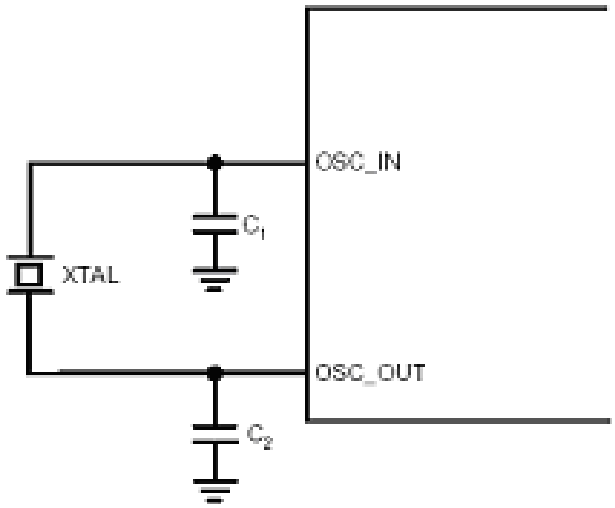


Figure 26. Typical Connection to a Crystal

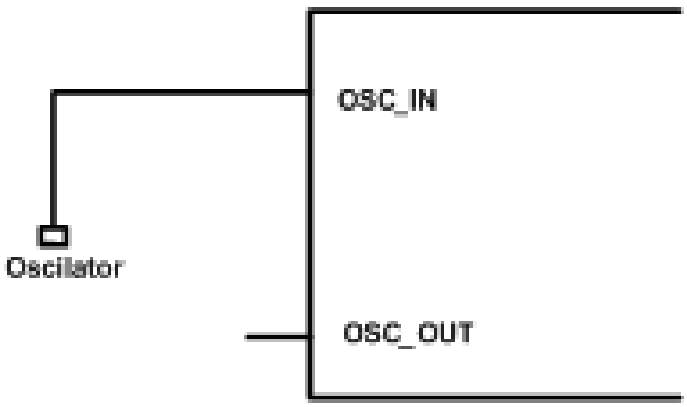


Figure 27. Typical Connection to a Oscillator

14.2. Power Supply DC Characteristics

Table 196. Power Supply DC Characteristics

Symbol	Parameter	Diff.	Min.	Typical	Max.	Units
VDD_REF_DDR	Voltage Reference 1.25V for DDR1 (VDDQ: 2.5V) Voltage Reference 0.9V for DDR2 (VDDQ: 1.8V)	+-2%	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V
VDD_REF_EPHY	Voltage Reference 0.6V for Ethernet PHY. 2.5K ohm 1% resister pull down	+-2.5%	0.609375	0.625	0.640625	V
VDD33_IO	Digital I/O Power Supply 3.3V.	+-5%	3.135	3.3	3.465	V
VDD25_18_DDRIO	Memory I/O Power Supply 2.5V, or 1.8V. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V	+-0.2	2.3 1.7	2.5(DDR1) 1.8(DDR2)	2.7 1.9	V
VDD33_25_MII	GMII/RGMII/MII Interface Power Supply 3.3V/2.5V .	+-5%	3.135 2.375	3.3 2.5	3.465 2.625	V
VDD33_SD30	SD Power supply 3.3V	+-5%	3.135	3.3	3.465	V
VDD33_18_SD30	SD IO Output Power 3.3V/1.8V	+0.1 / -0.05 +-5%	1.75 3.135	1.8 3.3	1.9 3.465	V
VDD1P05	Digital Core Power Supply 1.05V.	+0.8 / -0.7	1.05	1.12	1.20	V
AVDD33_EPHY	Ethernet Analog Power Supply 3.3V.	+-5%	3.135	3.3	3.465	V
AVDD1P05_EPHY	Ethernet Analog Power Supply 1.05V.	+0.8 / -0.7	1.05	1.12	1.20	V
AVDD33_BG	System Bandgap Power Supply 3.3V.	+-5%	3.135	3.3	3.465	V
AVDD1P05_PCIE	PCI Express Analog Power Supply 1.05V.	+0.8 / -0.7	1.05	1.12	1.20	V
AVDD1P05_PLL	PLL Power 1.05V.	+0.8 / -0.7	1.05	1.12	1.20	V
AVDD33_USB	USB 2.0 Analog Power 3.3V.	+-5%	3.135	3.3	3.465	V
AVDD1P05_USB	USB 2.0 Analog Power 1.05V.	+0.8 / -0.7	1.05	1.12	1.20	V
AVDD33_DDRPLL	DDR PLL Analog Power 3.3V	+-5%	3.135	3.3	3.465	V
AVDD1P05_DDRPLL	DDR PLL Analog Power 1.05V [1] Mode 1(NC): NC, using internal LDO (3.3V->1.05V) [2] Mode 2(AP): input power	[1] +-10% [2] +0.8 / -0.7	[1] 0.945 [2] 1.05	[1] 1.05 [2] 1.12	[1] 1.155 [2] 1.20	V
GND	System GND.	-	-	0	-	V
AGND_USB	USB GND.	-	-	0	-	V
AVDD33_SPS_DDR	SWR_DDR Power Supply 3.3V Input for DDR.	+-5%	3.135	3.3	3.465	V

AVDD25_18_SPS_DDR	SWR_DDR Output Power for DDR. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V	+-10% +-10%	2.25 1.62	2.5 1.8	2.75 1.98	V
AGND_SPS_DDR	SWR_DDR GND	-	-	0	-	V
AVDD33_SPS	SWR Power Supply 3.3V Input	+-5%	3.135	3.3	3.465	V
AGND_SPS	SWR GND	-	-	0	-	V
AVDD1P05_SPS	SWR Power Supply 1.05V Output	+-10%	0.945	1.05	1.155	V
AVDD1P05_AFE	Analog 1.05V power supply [1] Dedicated LDO for RF [2] Share with Digital Core [Note 6]	[1] +-5% [2] +0.8/-0.7	[1] 0.9975 [2] 1.05	[1] 1.05 [2] 1.12	[1] 1.1025 [2] 1.20	V
AVDD33_X	Analog 3.3V power supply	+-5%	3.135	3.3	3.465	V
VDD33_SYN	RF 3.3V power supply	+-5%	3.135	3.3	3.465	V
VDD1P05_SYN	RF 1.05V power supply [1] Dedicated LDO for RF [2] Share with Digital Core [Note 6]	[1] +-5% [2] +0.8/-0.7	[1] 0.9975 [2] 1.05	[1] 1.05 [2] 1.12	[1] 1.1025 [2] 1.20	V
AVDD33_RTX_S0	RF 3.3V power supply	+-5%	3.135	3.3	3.465	V
AVDD1P05_RTX_S1	RF 1.05V power supply [1] Dedicated LDO for RF [2] Share with Digital Core [Note 6]	[1] +-5% [2] +0.8/-0.7	[1] 0.9975 [2] 1.05	[1] 1.05 [2] 1.12	[1] 1.1025 [2] 1.20	V
AVDD1P05_RTX_S0	RF 1.05V power supply [1] Dedicated LDO for RF [2] Share with Digital Core [Note 6]	[1] +-5% [2] +0.8/-0.7	[1] 0.9975 [2] 1.05	[1] 1.05 [2] 1.12	[1] 1.1025 [2] 1.20	V
AVDD33_RTX_S1	RF 3.3V power supply	+-5%	3.135	3.3	3.465	V
ICC33	3.3V Current Consumption	-	30 [Note 1]	-	-	mA
ICC1P05	1.05V Current Consumption	-	10 [Note 2]	-	1200 [Note 3]	mA
ICC18_DDR2	DDR2 1.8V Current Consumption	-	[Note 4]	[Note 4]	450 [Note 5]	mA
ICC25_DDR1	DDR1 2.5V Current Consumption	-	[Note 4]	[Note 4]	450 [Note 5]	mA

Note 1: IC 3.3V leakage

Note 2: IC 1.05V leakage

Note 3: Max Output Current Capacity from internal Switching Regulator (Digital Core Power) (3.3V->1.05V)

Note 4: Depend on DRAM Vendor Spec

Note 5: Max Output Current Capacity from internal Switching Regulator / LDO (DDR Power) (DDR1: 3.3V->2.5V, DDR2: 3.3V->1.8V)

Note 6: Our preference is Option [1]: Dedicated LDO.

14.3. Digital IO Pin DC/AC Characteristics

14.3.1. Digital IO Pin Attribute (Not Share Pin)

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
MF_CK	3.3	8 or 16, Default: 16	Yes	125
MF_D0	3.3	8 or 16, Default: 16	Yes	125
MF_D1	3.3	8 or 16, Default: 16	Yes	125
MF_RSTN	3.3	8 or 16, Default: 16	No	125
MF_CS0N	3.3	8 or 16, Default: 16	No	125
MF_CS1N	3.3	8 or 16, Default: 16	No	125

Table 197. Digital IO Pin Attribute – SPI Nor Flash

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
P0_TXD3	3.3 or 2.5	Default: 8	No	125
P0_TXD2	3.3 or 2.5	Default: 8	No	125
P0_TXD1	3.3 or 2.5	Default: 8	No	125
P0_RXC	3.3 or 2.5	8 or 16, Default: 16	Yes	125
P0_RXD3	3.3 or 2.5	8 or 16, Default: 16	No	125
P0_RXD2	3.3 or 2.5	8 or 16, Default: 16	No	125
P0_RXD1	3.3 or 2.5	8 or 16, Default: 16	No	125
P0_RXD0	3.3 or 2.5	8 or 16, Default: 16	No	125
P0_TXD0	3.3 or 2.5	Default: 8	No	125
P0_TXC	3.3 or 2.5	Default: 8	No	125
P0_TXCTL	3.3 or 2.5	Default: 8	No	125
P0_RXCTL	3.3 or 2.5	8 or 16, Default: 16	No	125
P0_MDC	3.3 or 2.5	8 or 16, Default: 16	Yes	125
P0_MDIO	3.3 or 2.5	8 or 16, Default: 16	No	125

Table 198. Digital IO Pin Attribute – RGMII.

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
EMMC_RSTN	3.3	8 or 16, Default: 8	No	125
SD_WP	3.3	8 or 16, Default: 8	No	125
SD_CD	3.3	8 or 16, Default: 8	No	125

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
EMMC_CLK	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	No	125
EMMC_CMD	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	Yes	125
EMMC_DAT0	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	Yes	125
EMMC_DAT1	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	Yes	125
EMMC_DAT2	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	Yes	125
EMMC_DAT3	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	Yes	125
EMMC_DAT4	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	Yes	125
EMMC_DAT5	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	Yes	125
EMMC_DAT6	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	Yes	125
EMMC_DAT7	3.3/1.8	1.2 / 2.4 / 4.8 / 7.2 / 9.6 / 12 / 14.4 Default: 1.2	Yes	125

Table 199. Digital IO Pin Attribute – SD/eMMC.

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
WBB0	3.3	4 or 8, Defaut: 8	No	125
WBB1	3.3	4 or 8, Defaut: 8	No	125
WBB2	3.3	4 or 8, Defaut: 8	No	125
WBB3	3.3	4 or 8, Defaut: 8	No	125
WBB4	3.3	4 or 8, Defaut: 8	No	125
WBB5	3.3	4 or 8, Defaut: 8	No	125
WBB6	3.3	4 or 8, Defaut: 8	No	125
WBB7	3.3	4 or 8, Defaut: 8	No	125
WBB8	3.3	4 or 8, Defaut: 8	No	125
WBB9	3.3	4 or 8, Defaut: 8	No	125
WBB10	3.3	4 or 8, Defaut: 8	No	125
WBB11	3.3	4 or 8, Defaut: 8	No	125
WBB12	3.3	4 or 8, Defaut: 8	No	125

Table 200. Digital IO Pin Attribute – WiFi.

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
JTAG_TRSTN	3.3	4 or 8, Defaut: 8	Yes	125
JTAG_TCK	3.3	4 or 8, Defaut: 8	Yes	125
JTAG_TMS	3.3	4 or 8, Defaut: 8	No	125
JTAG_TDI	3.3	4 or 8, Defaut: 8	No	125
JTAG_TDO	3.3	8 or 16, Defaut: 16	No	125

Table 201. Digital IO Pin Attribute – JTAG.

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
GPIO_0	3.3	8 or 16, Default: 8	No	125
GPIO_1	3.3	8 or 16, Default: 8	No	125
GPIO_2	3.3	8 or 16, Default: 8	No	125

Table 202. Digital IO Pin Attribute – GPIO.

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
LED_PORT0	3.3	8 or 16, Defaut: 8	No	125
LED_PORT1	3.3	8 or 16, Defaut: 8	No	125
LED_PORT2	3.3	8 or 16, Defaut: 8	No	125
LED_PORT3	3.3	8 or 16, Defaut: 8	No	125
LED_PORT4	3.3	8 or 16, Defaut: 8	No	125

Table 203. Digital IO Pin Attribute – Switch LED.

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
U0_RX	3.3	4 or 8, Defaut: 8	No	125
U0_TX	3.3	4 or 8, Defaut: 8	No	125

Table 204. Digital IO Pin Attribute – Uart.

PIN NAME	Voltage (V)	Driving (mA)	Schmit Trigger Enable ?	Max Clock: MHz
PCIE_RSTN	3.3	4 or 8, Defaut: 8	No	125

Table 205. Digital IO Pin Attribute – PCIe.

14.3.2. Electrical Specifications – Digital IO Pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	DDR1 DC Operating Conditions (Source from: JESD79F Spec., Page 45) DDR1 AC Operating Conditions (Source from: JESD79F Spec., Page 46)				V
V_{IL}	Input-Low Voltage					V
VTT	I/O Termination Voltage					V
I_{IL}	Input-Leakage Current					uA
Ioz	Tri-State Output-Leakage Current					uA

Table 206. Typical Digital IO DC Operating Conditions (2.5V DDR1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	DDR2 DC Operating Conditions (Source from: JESD79-2F Spec., Page 62) DDR2 DC/AC Operating Conditions (Source from: JESD79-2F Spec., Page 64) DDR2 AC Operating Conditions (Source from: JESD79-2F Spec., Page 65)				V
V_{IL}	Input-Low Voltage					V
VTT	I/O Termination Voltage					V
I_{IL}	Input-Leakage Current					uA
Ioz	Tri-State Output-Leakage Current					uA

Table 207. Typical Digital IO DC Operating Conditions (1.8V DDR2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Vdd			**3.135**	**3.3**	**3.465**	**V**
V_{IH}	Input-High Voltage	LVTTL	2	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
V_{T+}	Schmitt-trigger High Level	Schmitt-trigger	1.78	1.87	1.97	V
V_{T-}	Schmitt-trigger Low Level	Schmitt-trigger	1.36	1.45	1.56	V
I_{IL}	Input-Leakage Current	VIN=3.3V or 0	-10	±1	10	uA

Table 208. Typical Digital IO DC Operating Conditions (3.3V GPIO/Flash/Uart/RGMII/WiFi digital/Jtag/LED/PCIe_RST)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Vdd			**2.375**	**2.5**	**2.625**	**V**
V_{IH}	Input-High Voltage	LVTTL	1.7	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.7	V
V_{OH}	Output-High Voltage	LVTTL	2	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.2	V
V_{T+}	Schmitt-trigger High Level	Schmitt-trigger	1.2	1.4	1.6	V
V_{T-}	Schmitt-trigger Low Level	Schmitt-trigger	1	1.2	1.4	V
I_I	Input-Leakage Current	VIN=2.5V or 0	-10	±1	10	uA

Table 209. Typical Digital IO DC Operating Conditions (2.5V RGMII)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Vdd			**2.7**	**3.3**	**3.6**	**V**
V_{IH}	Input-High Voltage		0.625 * VCCQ		VCCQ + 0.3	V
V_{IL}	Input-Low Voltage		VSS - 0.3		0.25 * VCCQ	V
V_{OH}	Output-High Voltage		0.75 * VCCQ			V
V_{OL}	Output-Low Voltage				0.125* VCCQ	V
V_{T+}	Schmitt-trigger High Level	Schmitt-trigger	1.99V	2.06V	2.11V	V
V_{T-}	Schmitt-trigger Low Level	Schmitt-trigger	1.3V	1.37V	1.46V	V
I_I	Input-Leakage Current	VIN=3.3V or 0	2.3	2.3	22.2	nA

Table 210. Typical Digital IO DC Operating Conditions (3.3V SD/eMMC)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Vdd			**1.7**	**1.8**	**1.95**	**V**
V_{IH}	Input-High Voltage		0.65 * VCCQ		VCCQ + 0.3	V
V_{IL}	Input-Low Voltage		VSS - 0.3		0.35 *VCCQ	V
V_{OH}	Output-High Voltage		VCCQ - 0.45V			V
V_{OL}	Output-Low Voltage				0.45V	V
V_{T+}	Schmitt-trigger High Level	Schmitt-trigger	1.09V	1.15V	1.19V	V
V_{T-}	Schmitt-trigger Low Level	Schmitt-trigger	0.66V	0.71V	0.77V	V
I_I	Input-Leakage Current	VIN=3.3V or 0	0.2	0.2	16.4	nA

Table 211. Typical Digital IO DC Operating Conditions (1.8V SD/eMMC)

14.3.3. Electrical Specifications - DDR

TABLE 6: ELECTRICAL CHARACTERISTICS AND DC OPERATING CONDITIONS

(Notes: 1-6, These characteristics are for DDR SDRAM only and obey SSTL_2 class II standard.)
(0°C ≤ TA ≤ 70°C; For DDR 200, 266, and 333, VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V for DDR400, VDDQ = +2.6 V ±0.1 V, VDD = +2.6 V ±0.1 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
Supply Voltage (for devices with a nominal VDD of 2.6 V)	VDD	2.5	2.7	V	
I/O Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDDQ	2.3	2.7	V	
I/O Supply Voltage (for devices with a nominal VDD of 2.6 V)	VDDQ	2.5	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	7
I/O Termination Voltage (system)	VTT	VREF-0.04	VREF+0.04	V	8
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.15	VDD+0.3	V	
Input Low (Logic 0) Voltage	VIL(DC)	-0.3	VREF-0.15	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	VIN(DC)	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(DC)	0.36	VDDQ+0.6	V	9
V-I Matching: Pullup to Pulldown Current Ratio	VI(Ratio)	0.71	1.4	-	e
INPUT LEAKAGE CURRENT, Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0 V)	IL	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	-5	5	µA	
OUTPUT LEVELS Output High Current (VOUT = 1.95 V) Output Low Current (VOUT = 0.35 V)	IOH IOL	-16.2 16.2		mA mA	

Table 212. DDR1 DC Operating Conditions (Source from: JESD79F Spec., Page 45)

TABLE 7: AC OPERATING CONDITIONS

(Notes: 1-6, These characteristics are for DDR SDRAM only and obey SSTL_2 class II standard.)
(0°C ≤ TA ≤ 70°C; For DDR 200, 266, and 333, VDDQ = +2.5 V ±0.2 V, Vdd = +3.3 V ±0.3 V or +2.5 V ±0.2 V; for DDR400, VDDQ = +2.6 V ±0.1 V, VDD = +2.6 V ±0.1 V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(ac)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(ac)		VREF - 0.31	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(ac)	0.7	VDDQ + 0.6	V	9
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	VIX(ac)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	10

Table 213. DDR1 AC Operating Conditions (Source from: JESD79F Spec., Page 46)

Table 17 — Recommended DC operating conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	mV	2. 3
VTT	Termination Voltage	VREF - 0.04	VREF	VREF + 0.04	V	4

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must be less than or equal to VDD.
NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2 % VREF(dc).
NOTE 4 VTT of transmitting device must track VREF of receiving device.
NOTE 5 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

Table 214. DDR2 DC Operating Conditions (Source from: JESD79-2F Spec., Page 62)

Measurement Definition for VM: Measure voltage (VM) at test pin (midpoint) with no load.

$$\Delta VM = \left(\frac{2 \times Vm}{VDDQ} - 1 \right) \times 100\%$$

Table 20 — Input DC logic level

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH}(dc)$	dc input logic HIGH	VREF + 0.125	VDDQ + 0.3	V	
$V_{IL}(dc)$	dc input logic LOW	- 0.3	VREF - 0.125	V	

Table 21 — Input AC logic level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min.	Max.	Min.	Max.		
V_{IH} (ac)	ac input logic HIGH	VREF + 0.250	VDDQ+Vpeak	VREF + 0.200	VDDQ+Vpeak	V	1
V_{IL} (ac)	ac input logic LOW	VSSQ-Vpeak	VREF - 0.250	VSSQ-Vpeak	VREF - 0.200	V	1

NOTE 1 Refer to Overshoot/undershoot specifications (Table 24 and Table 25) for Vpeak value: maximum peak amplitude allowed for overshoot adn undershoot.

Table 22 — AC input test conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 x V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE 1 Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL(AC)}$ level applied to the device under test.

NOTE 2 The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)}$ min for rising edges and the range from V_{REF} to $V_{IL(ac)}$ max for falling edges as shown in the below figure.

NOTE 3 AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

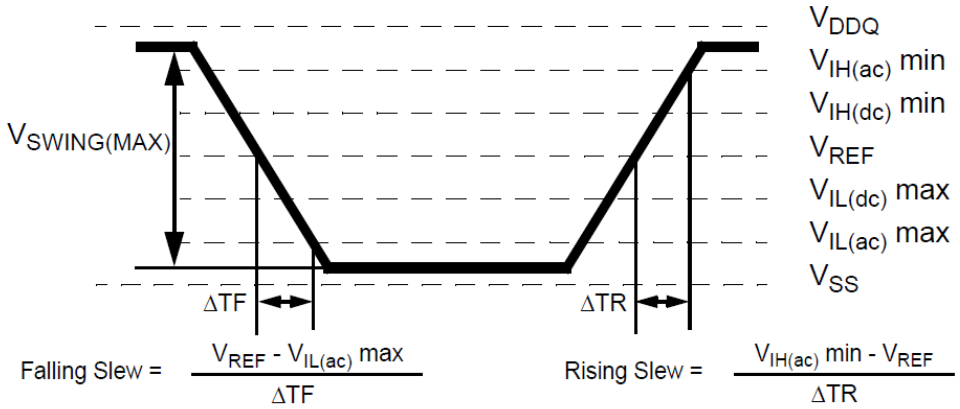


Figure 73 — AC input test signal waveform

Table 215. DDR2 DC/AC Operating Conditions (Source from: JESD79-2F Spec., Page 64)

Table 23 — Differential input AC logic level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID} (ac)	ac differential input voltage	0.5	VDDQ	V	1,3
V_{IX} (ac)	ac differential crosspoint voltage	0.5 x VDDQ - 0.175	0.5 x VDDQ + 0.175	V	2

NOTE 1 $V_{ID(AC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to $V_{IH(AC)} - V_{IL(AC)}$.

NOTE 2 The typical value of $V_{IX(AC)}$ is expected to be about 0.5 x VDDQ of the transmitting device and $V_{IX(AC)}$ is expected to track variations in VDDQ. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

NOTE 3 Refer to Overshoot/undershoot specifications (Table 24 and Table 25) for Vpeak value: maximum peak amplitude allowed for overshoot adn undershoot.

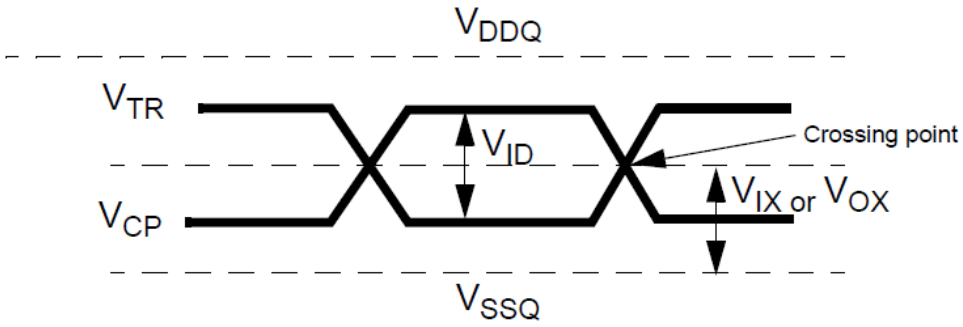


Figure 74 — Differential signal levels

Table 24 — Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Notes
V_{OX} (ac)	ac differential crosspoint voltage	0.5 x VDDQ - 0.125	0.5 x VDDQ + 0.125	V	1

NOTE 1 The typical value of $V_{OX(AC)}$ is expected to be about 0.5 x VDDQ of the transmitting device and $V_{OX(AC)}$ is expected to track variations in VDDQ . $V_{OX(AC)}$ indicates the voltage at which differential output signals must cross.

Table 216. DDR2 AC Operating Conditions (Source from: JESD79-2F Spec., Page 65)

14.3.4. Electrical Specification - RGMII

14.3.4.1 RGMII Clock Timing

Table 217. RGMII Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{PERIOD\_Gigabit}$	Clock Period for TX and RX Ethernet Clocks (125Mhz)	7.2	8	8.8	ns-	-
T_{PERIOD_100M}	Clock Period for TX and RX Ethernet Clocks (25Mhz)	36	40	44	ns	
T_{PERIOD_10M}	Clock Period for TX and RX Ethernet Clocks (2.5Mhz)	360	400	440	ns	
T_{DUTY}	Duty Cycle for TX and RX Ethernet Clocks	45	50	55	%	-
$T_{RISE/FALL}$	Rise And Fall Time Requirement for TX and RX Ethernet Clocks (20~80%)	-	-	0.75	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	-	-	ns	1

Note 1: For detailed information contact Realtek for the IBIS model.

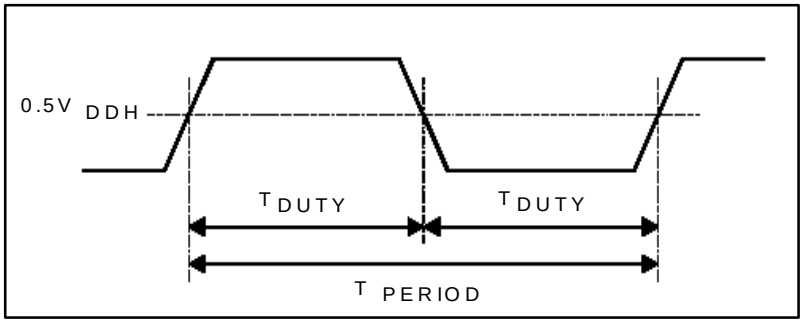


Figure 28. RGMII Clock Specifications-1

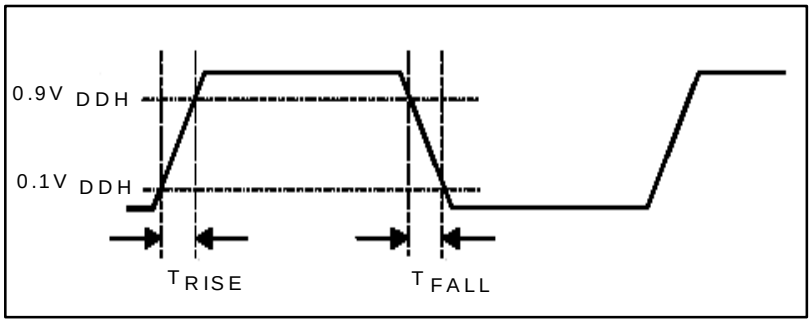


Figure 29. RGMII Clock Specifications-2

14.3.4.2 RGMII Timing Characteristics

Table 218. RGMII Timing Characteristics

SYM	Description/Condition	Min	Typ.	Max.	Units
T_{skewT}	Disable TXC Delay	-500	0	500	ps
T_{TX_SU}	Data to Clock Output Setup Time. Disable TXC Delay	-	400	-	ps
T_{TX_HO}	Data to Clock Output Hold Time. Disable TXC Delay	-	3.6	-	ns
T_{TX_SU}	Data to Clock Output Setup Time. Enable TXC Delay	-	1.6	-	ns
T_{TX_HO}	Data to Clock Output Hold Time. Enable TXC Delay	-	2.2	-	ns
T_{RX_SU}	Data to Clock Input Setup Time. Disable RXC Delay	1.0	-	-	ns
T_{RX_HO}	Data to Clock Input Hold Time. Disable RXC Delay	1.0	-	-	ns

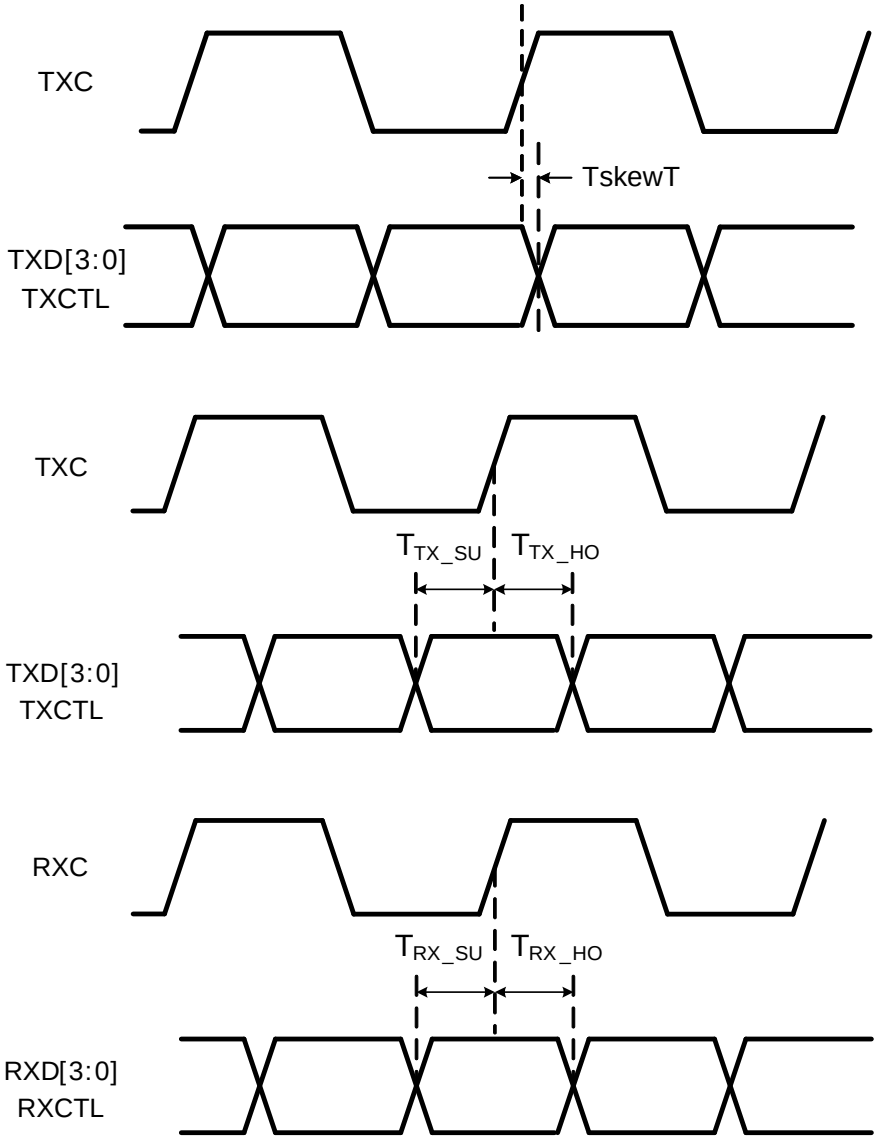
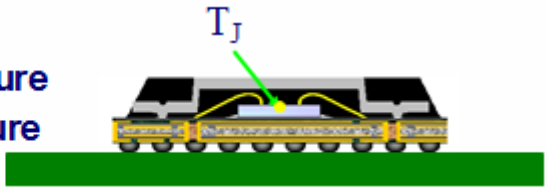


Figure 30. RGMII Timing Characteristics

15. Thermal Characteristics

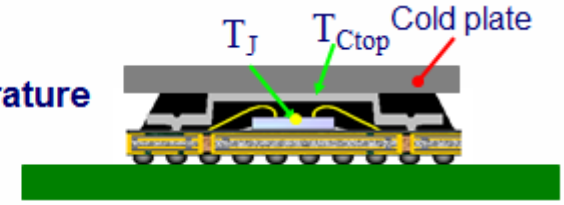
$$\theta_{JA} = \frac{T_J - T_A}{P_H}$$

Where T_J : Junction temperature
T_A : Ambient temperature
P_H : Power dissipation



$$\theta_{JCtop} = \frac{T_J - T_{Ctop}}{P_H}$$

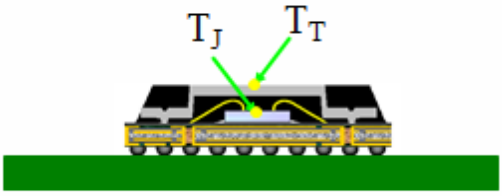
Where T_{Ctop} : Top case temperature



ψ_{JT} is defined as:

$\psi_{JT} = (T_J - T_T) / P_H$

Where T_T : Temperature at top-center of package



15.1. Temperature Limit Ratings

Table 219. Temperature Limit Ratings

Parameter	Minimum	Typical	Maximum	Units	Note
Storage Temperature	-55	-	125	°C	-
Ambient Operating Temperature	0	25	70	°C	1
Junction Temperature	0	-	125	°C	-

Note 1: It is necessary to satisfy this limitation of Junction Temperature.

15.2. Temperature Characteristics

HS: Heat Sink

Table 220. Thermal Properties – DR-QFN128: 8197FN

PCB (layer)	PCB Size	Theta ja (C/W)	Theta jc (C/W)	Psi jt (C/W)
2L	130x103mm2	28.6	8.8	2.3 [Note 1]

Table 221. Thermal Properties – DR-QFN128: 8197FS

PCB (layer)	PCB Size	Theta ja (C/W)	Theta jc (C/W)	Psi jt (C/W)
4L	135.5x126.7mm2	19.6	7.5	2 [Note 1]

Table 222. Thermal Properties – TF-BGA268: 8197FB

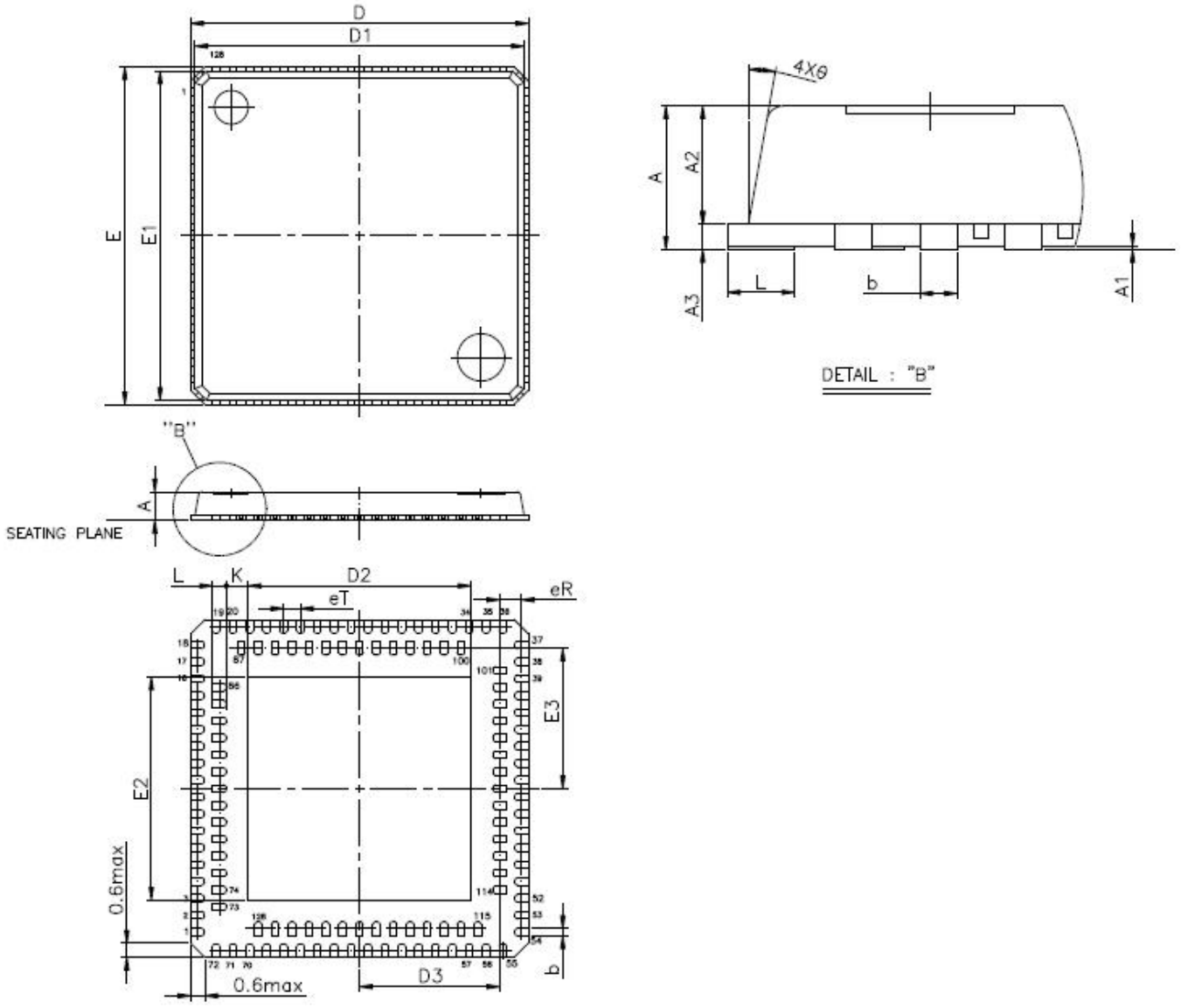
PCB (layer)	PCB Size	Theta ja (C/W)	Theta jc (C/W)	Psi jt (C/W)
4L	147 x 120mm2	21.7	9	2.6 [Note 1]

Note 1: **Psi JT data were estimated base on JEDEC PCB measurement results**

16. Mechanical Dimensions

16.1. DR-QFN128 (RTL8197FNT / RTL8197FN / RTL8197FH / RTL8197FS)

Thermally Enhanced Plastic Very Thin Fine Pitch Quad Flat No-Lead Package 128 Leads 10x10mm^2 Dual Row Outline

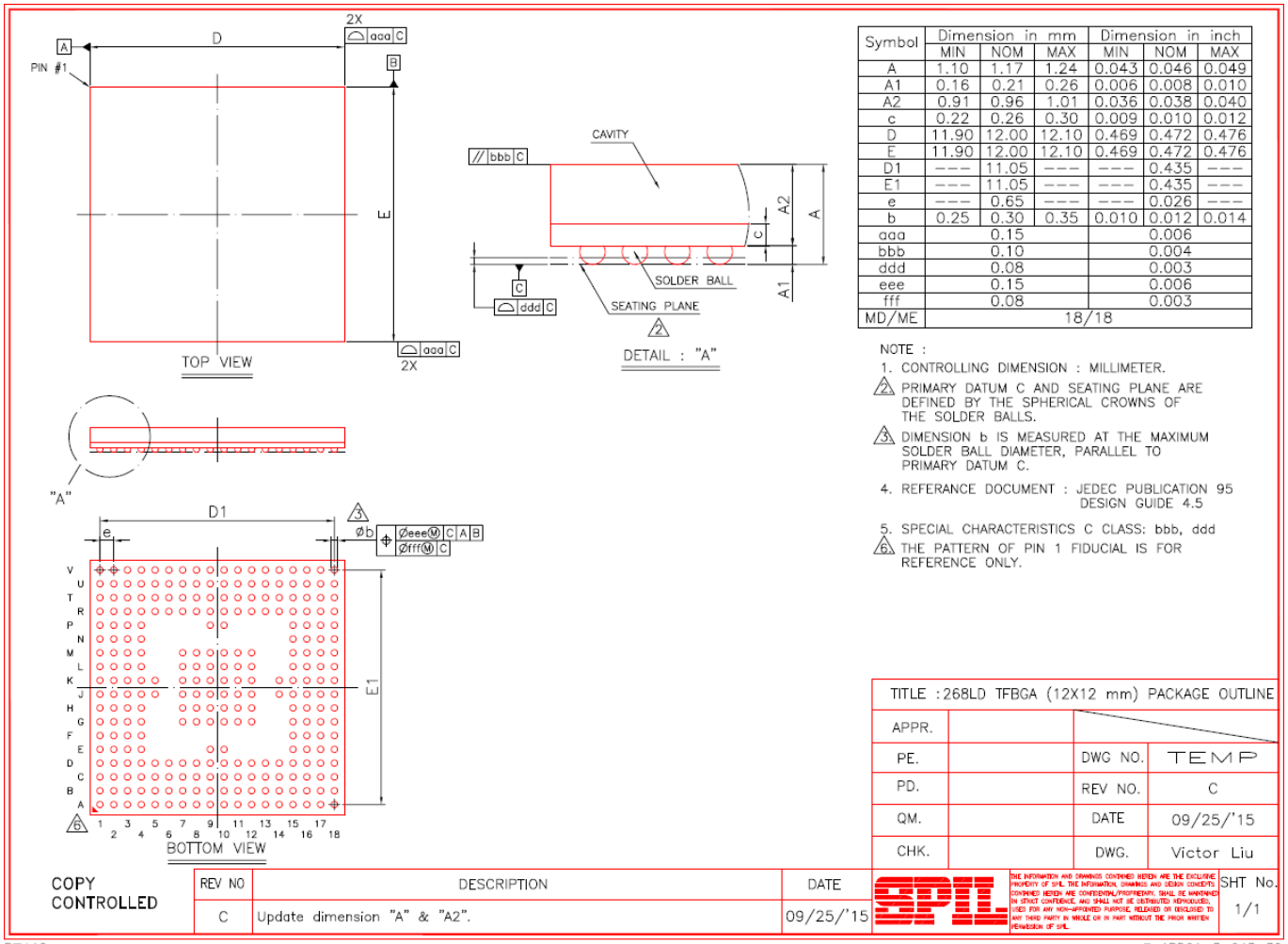


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	0.65	0.70	0.75	0.026	0.028	0.030
A_3		0.15 REF			0.006 REF	
b	0.18	0.22	0.30	0.007	0.009	0.012
D/E	9.90	10.00	10.10	0.390	0.394	0.398
D1/E1		9.75 BSC			0.384 BSC	
D2/E2	5.4	5.5	5.6	0.213	0.217	0.22
D3/E3		4.15 BSC			0.163 BSC	
eT		0.50 BSC			0.020 BSC	
eR		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	—	15°	0°	—	15°
K	0.20			0.008		

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENT：JEDEC MO-267.
3. REF / BSC TOLERANCE : +/- 0.2mm

16.2. TF-BGA268 (RTL8197FB)



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.17	1.24	0.043	0.046	0.049
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	---	11.05	---	---	0.435	---
E1	---	11.05	---	---	0.435	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		18/18				

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5
5. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

TITLE : 268LD TFBGA (12X12 mm) PACKAGE OUTLINE			
APPR.			
PE.		DWG NO.	TEMP
PD.		REV NO.	C
QM.		DATE	09/25/'15
CHK.		DWG.	Victor Liu

COPY CONTROLLED

REV NO	DESCRIPTION	DATE
C	Update dimension "A" & "A2".	09/25/'15

SPIL

SHT No. 1/1

REV.A2

T-APD01-3-043-32

17. Ordering Information

Table 223. Ordering Information

Part Number	Package	Status
RTL8197FNT-VEx-CG	DR-QFN128 MCM with: 1.) VE4: 64MB DDR2	
RTL8197FN-VEx-CG	DR-QFN128 MCM with: 1.) VE3 : 32MB DDR2 2.) VE4 : 64MB DDR2 3.) VE5 : 128MB DDR2	
RTL8197FH-VEx-CG	DR-QFN128 MCM with: 1.) VE4 : 64MB DDR2 2.) VE5 : 128MB DDR2	
RTL8197FS-VEx-CG	DR-QFN128 MCM with: 1.) VE3 : 32MB DDR2 2.) VE4 : 64MB DDR2 3.) VE5 : 128MB DDR2	
RTL8197FS-VSx-CG	DR-QFN128 MCM with: 1.) VS4 : 64MB DDR2 2.) VS5 : 128MB DDR2	
RTL8197FB-CG	TF-BGA268	

Note: Detail difference for part number, please check Chapter: Comparison between Part Number

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