MT7530 Giga Switch programming guide

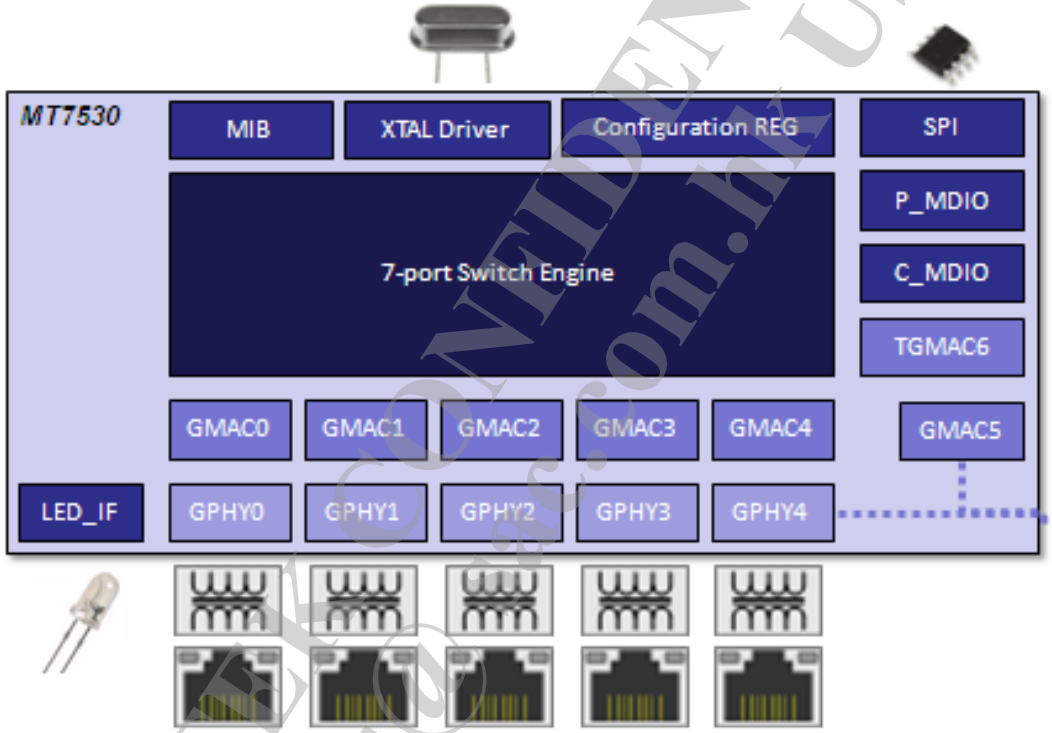
Version: 0.1
Release date: 2013-07-10

Document Revision History

Internal use only

Revision	Date	Author	Change Log
0.1	2013/07/10	JayYC	Initial release

MT7530 including 7-port Gigabit Ethernet MAC and 5-port Gigabit Ethernet PHY for several applications, such as xDSL , xPON and Wifi router. It complies with IEEE 802.3az for Energy Efficient Ethernet and cable-length /link down power saving mode. Please refer to the below figure to know the construct of MT7530.



Mode setting

The register 0x 7800 is hardware trap, it is made when power on (define by boot-strap resistance). You can change it by writing 0x7804. Finally, the system would active according ox7804 not 0x7800. Some registers of 0x7800 cannot be changed. For detail, please check the switch register map. You should check it bit by bit.

00007800 HWTRAP Hardware Trap Status Register 01007FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								bond_option								
Type								RO								
Reset								1								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ht_loopdet_dis	ht_p5_intf_sel	ht_smi_addr		ht_xtal_fsel		ht_p6_intf_dis	ht_p5_intf_mode	ht_p5_intf_dis	ht_c_mdio_bps_n	ht_eeprom_en	ht_chip_mode			
Type		RO	RO	RO		RO		RO	RO	RO	RO	RO	RO			
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

If you want to change 0x7804, you need to set bit 16 as 1 of 0x7804 first.

00007804 MHWTRAP Modified Hardware Trap Status Register 0100000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								bond_option				csr_p5_phy0_sel				csr_chg_trap
Type								RO				RW				RW
Reset								1				0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	csr_gsw_ck_sel	csr_loopdet_dis	csr_p5_intf_sel	csr_smi_addr		csr_xtal_fsel		csr_p6_intf_dis	csr_p5_intf_mode	csr_p5_intf_dis	csr_c_mdio_bps_n	csr_eeprom_en	csr_chip_mode			
Type	RW	RW	RW	RO		RO		RW	RW	RW	RW	RO	RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Please also check the detail trap of MT7530.

Pin name	Trap	Function	Description	Default
P0_LED_0	0x7800 bit [0]	Chip mode	Must as 4'b1111	4'b1111
P2_LED_0	0x7800 bit [3]			
P0_LED_1	0x7800 bit [6]			
P0_LED_2	0x7800 bit [1]			
P1_LED_1	0x7800 bit [2]	EEPROM_EN	1'b0: disable EEPROM 1'b1: external enable EEPROM	1'b1
P1_LED_2	0x7800 bit [4]	MDIO_Bypass	1'b0: Directly access 1'b1: indirectly access	1'b1
P2_LED_1	0x7800 bit [5]	P5_Disable	1'b0: Port 5 enable 1'b1: Port 5 disable	1'b1
P2_LED_2	0x7800 bit [7]	P5_Interface	1'b0: GMII/MII 1'b1: RGMII	1'b1
P3_LED_2	0x7800 bit [8]	P6_Disable	1'b0: Port 6 enable 1'b1: Port 6 disable	1'b1
P3_LED_0	0x7800 bit [9]	XTAL_SELECT	EXTERANL XTAL FEQ 1'b01: 20Mhz 1'b11: 40Mhz	2'b11
P4_LED_0	0x7800 bit [12]			

			1'b11: 25Mhz	
P3_LED_2	0x7800 bit [11]	SMI_ADDR	Chip SMI Address	2'b11
P3_LED_1	0x7800 bit [10]		Bit 4 and bit 3 of SMI address Bit [2:0] = 3'b111 *Note 1	
P4_LED_1	0x7800 bit [13]	Do not use	-	2'b1
P4_LED_2	0x7800 bit [14]	Loop detect	1'b0: loop detection enable 1'b1: loop detection disable	1'b1

*Note 1: We would suggest that SMI address of MT7530 is 5'b11111. If not, you need to change the driver of MT7530.

Link Status

You can find MAC control register put at 0x3000, 0x3100…0x3600. 0x3000 is for port 0 MAC control register. You can change MAC ability at this register.

00003000 PMCR_P0 PORT 0 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													IPG_CFG_P0		EXT_PHY_P0	MAC_MODE_P0
Type													RW		RW	RW
Reset													0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE_P0	MAC_TX_EN_P0	MAC_RX_EN_P0		MAC_PRE_P0	SFD_DET_MODE	BKOFF_EN_P0	BACKPR_EN_P0	FORCE_EEE1G_P0	FORCE_EEE100_P0	FORCE_RX_FC_P0	FORCE_TX_FC_P0	FORCE_SPD_P0		FORCE_DPX_P0	FORCE_LNK_P0
Type	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1		0	0	1	1	0	0	1	1	0	0	0	0

For every port, it has its own status to check register. 0x3008 is used for Port 0. 0x3108 is used for Port 1. Others please check the 0x3208, 0x3308, 0x3408, 0x3508 and 0x3608.
If you want to change port 0 status, you can use 0x3000 to change its ability.

00003008 PMSR_P0 PORT 0 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P0	EEE100_STS_P0	RX_FC_STS_P0	TX_FC_STS_P0	MAC_SPD_STS_P0		MAC_DPX_STS_P0	MAC_LNK_STS_P0
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Link Status change

You can find the 0x700c is a record if PHY status was changed. For example, if you plug into PHY 1, you can find the 0x700c become 00080002. Then drew the PHY 1, the 0x700c would still keep 00080002.You need to write "1" to the bit which you want clean at the register 0x700c. After that you can find it would become 00080000.

0000700C SYS_INT_STS System Interrupt Status 00000000

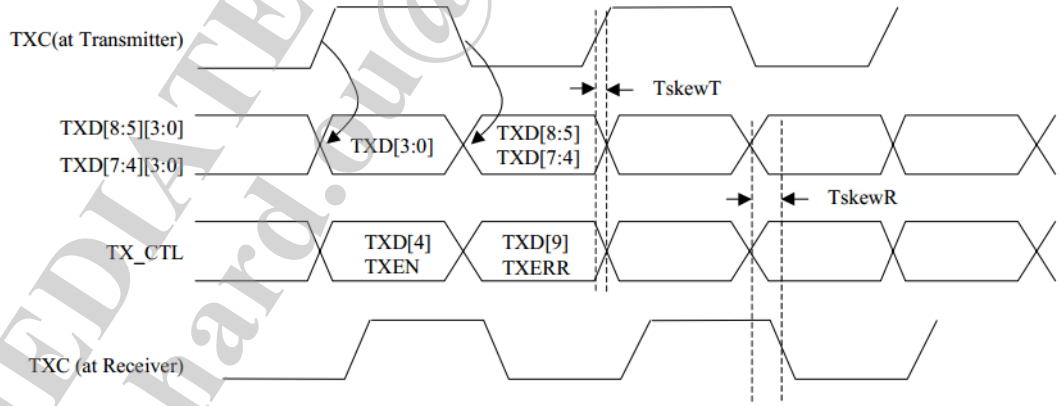
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_INT	ARL_SEC_TAG_INT	ARL_SEC_VLAN_INT	ARL_SEC_IG1X_INT	ARL_PKT_BC_INT	ARL_EQ_ERR_INT	ARL_PKT_QERR_INT	ARL_TBL_ERR_INT					PTP_INT	MIB_INT	BMU_INT	MAC_PC_INT
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C					W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PHY6_INT	PHY5_INT	PHY4_INT	PHY3_INT	PHY2_INT	PHY1_INT	PHY0_INT		PHY6_LC_INT	PHY5_LC_INT	PHY4_LC_INT	PHY3_LC_INT	PHY2_LC_INT	PHY1_LC_INT	PHY0_LC_INT
Type		W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

MAC 5 interface setup

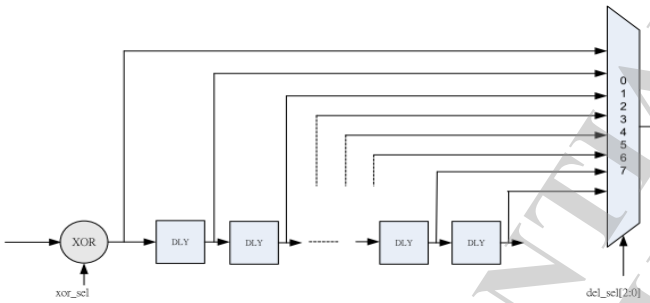
Usually, GMII of P5 does not need to do the delay. If you want to use as RGMII, you may modify the TX or RX delay timing. Please also notice that 10Mbps and 100Mbps mode also can do the delay. But, you know that their CLK timing is 400ns and 40ns. So, that also means the 2ns delay latency may not useful to them.

00007B04 P5RGMIITXCR P5 RGMII Wrapper TX Clock Control Register 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														csr_rgmii_txen_cfg		
Type														RW		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						csr_rgmii_txd_cfg						csr_rgmii_txc_cfg				
Type						RW						RW				
Reset						0	0	0				1	0	0	0	0



You can adjust 0x7b04 for P5 CLK, data and enable delay timing.
0x7b04: P5 RGMII Wrapper TX Clock Control Register
Bit 4 ([4] - Using 90-degree TXC (central align)) is used for adjusting align. You can change the bit if you got the short packet.
Bit 3 ([3] - Inverted RXC) is used for enable the XOR, like the below figure. It is usually for a large timing adjustment.



If you need to change the RX delay of P5, please modify 0x7b00. rxd_cfg and rctl_cfg .
Here is the sample when MT7530 link with Vitesse PHY.

(a) Change reg7B00[18:16] rxd_cfg[2:0] , from 3'b000 to 3'b010

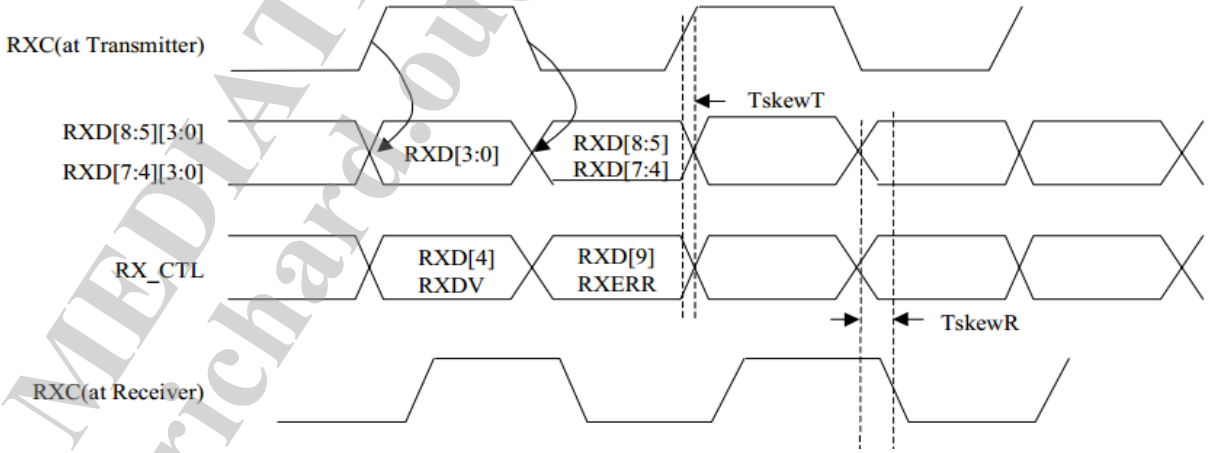
(b) Change reg7B00[26:24] rctl_cfg[2:0] , from3'b000 to 3'b010

You may also change the CLK align.

(a) Change reg7B04[4:0] GTXC setting , from 5'b10000 to 5'b01001

00007B00 P5RGMIIRXCR P5 RGMII Wrapper RX Clock Control Register 00000104

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						csr_rgmii_rctl_cfg								csr_rgmii_rxd_cfg		
Type						RW								RW		
Reset						0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								csr_rgmii_central_align					csr_rgmii_rxc_0deg_cfg			
Type								RW					RW			
Reset								1					0	1	0	0



Please notice the bit 8 of 7b00 is used for checking the enable delay or not. The delay chain would be no longer valid if the 8th bit set as 1.

csr_rgmii_central_align **1: RXC/RXD is central-aligned; RXC does not pass through the delay chain.**
0: RXC/RXD is not central-aligned (edge-aligned); RXC passes through the delay chain.

0x7810 is used for setting TXC driving. P5 CLK driving is 12mA as default value. Others, like TXD,MDC and TXEN are also locate at this register.

00007810 IO_DRV_CR IO Driving Strength Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							csr_normal_drv				csr_mdc_drv				csr_led_mdio_drv	
Type							RW				RW				RW	
Reset							0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			csr_p6_data_io_drv				csr_p6_clk_io_drv				csr_p5_io_data_drv				csr_p5_io_clk_drv	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

If P5 want to connect a PHY IC, you should check the below flow to make sure the PHY status:

1. Check 0x3508 : check the link up status
2. Check PHY is link up or not, use “tce miir 5 1”. If you get 796D, it means the PHY is link up.
3. Check 0x3500, 56300 is correct for its status.
4. Check 0x7018, it need to 7f7f8600 for enable polling mode.

00007018 PHY_POLL PHY Polling and SMI Master Control Register 007F8600

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		PHY_AP_EN								EEE_POLL_EN						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PHY_PRE_EN	RX_TA1_CHK_OFF		PHY_END_ADDR					PMDC_CFG			PHY_ST_ADDR				
Type	RW	RW		RW					RW			RW				
Reset	1	0		0	0	1	1	0	0	0		0	0	0	0	0

MAC 6 interface setup

MT7530 TX driving use full power as default setting. You can change the register to change it: 0x7a54, 0x7a5c, 0x7a64, 0x7a6c, 0x7a74.

All of them are used ff as default. You can change to 44 if you need.

00007A54 TRGMII_TD0_ODT TRGMII TD0 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD0_DM_DRVN_PRE		TD0_DM_DRVP_PRE		TD0_DM_TDSEL				TD0_ODTEN			TD0_DME_PRE	TD0_DM_DRVNT0	TD0_DM_DRVPT0	TD0_DM_DRVNTE	TD0_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD0_DM_ODTN				TD0_DM_ODTP			TD0_DM_DRVN				TD0_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A5C TRGMII_TD1_ODT TRGMII TD1 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD1_DM_DRVN_PRE		TD1_DM_DRVP_PRE		TD1_DM_TDSEL				TD1_ODTEN			TD1_DME_PRE	TD1_DM_DRVNT0	TD1_DM_DRVPT0	TD1_DM_DRVNTE	TD1_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD1_DM_ODTN				TD1_DM_ODTP			TD1_DM_DRVN				TD1_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A64 TRGMII_TD2_ODT TRGMII TD2 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD2_DM_DRVN_PRE		TD2_DM_DRVP_PRE		TD2_DM_TDSEL				TD2_ODTEN			TD2_DME_PRE	TD2_DM_DRVNT0	TD2_DM_DRVPT0	TD2_DM_DRVNTE	TD2_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD2_DM_ODTN				TD2_DM_ODTP			TD2_DM_DRVN				TD2_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A6C TRGMII_TD3_ODT TRGMII TD3 ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TD3_DM_DRVN_PRE		TD3_DM_DRVP_PRE		TD3_DM_TDSEL				TD3_ODTEN			TD3_DME_PRE	TD3_DM_DRVNT0	TD3_DM_DRVPT0	TD3_DM_DRVNTE	TD3_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TD3_DM_ODTN				TD3_DM_ODTP			TD3_DM_DRVN				TD3_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A74 TRGMII_TXCTL_ODT TRGMII TXCTL ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXCTL_DM_DRVN_PRE		TXCTL_DM_DRVP_PRE		TXCTL_DM_TDSEL				TXCTL_ODTEN			TXCTL_DME_PRE	TXCTL_DM_DRVNT0	TXCTL_DM_DRVPT0	TXCTL_DM_DRVNTE	TXCTL_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TXCTL_DM_ODTN				TXCTL_DM_ODTP			TXCTL_DM_DRVN				TXCTL_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

00007A7C TRGMII_TCK_ODT TRGMII TCK ODT REGISTER 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCK_DM_DRVN_PRE		TCK_DM_DRVP_PRE		TCK_DM_TDSEL				TCK_ODTEN			TCK_DME_PRE	TCK_DM_DRVNT0	TCK_DM_DRVPT0	TCK_DM_DRVNTE	TCK_DM_DRVPTE
Type	RW		RW		RW				RW			RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		TCK_DM_ODTN				TCK_DM_ODTP			TCK_DM_DRVN				TCK_DM_DRVP			
Type		RW				RW			RW				RW			
Reset		0	0	0		0	0	0	1	1	1	1	1	1	1	1

EEPROM:

Before use EEPROM, please read 0x7800 bit 4 is 1 or not. If you want to use it, it should be as 1. You need to use 0x7120 as the register for EEPROM programming. Here take the changing the port 0 register 4 for example.

Ethphxcmd gsww 7120 c0003075 // Must write the initial address of EEPROM as 7530
Ethphxcmd gsww 7120 c0021c70 // Use 0x701c to write PHY register, and write to address 2.
Ethphxcmd gsww 7120 c00405e1 // Write data 05e1 to address 4.
Ethphxcmd gsww 7120 c0068805
// Write data 8805 to address 6, the final data would be 880505e1

It means write 05E1 to register 4 of port 0.

00007120 EEPR_IND EEPROM INDIRECT ACCESS CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EP_IND_ACT	EP_IND_WR							EP_IND_ADDR							
Type	RW	RW							RW							
Reset	0	0							0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EP_IND_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0000701C PHY_IAC PHY Indirect Access Control 00090000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_ACS_ST		MDIO_REG_ADDR					MDIO_PHY_ADDR					MDIO_CMD		MDIO_ST	
Type	R/W/SC		RW					RW					RW		RW	
Reset	0		0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDIO_RW_DATA															
Type	R/W/RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Write command example:

command	switch reg	EEPROM ADD					
ethphxcmd gsww	7120	c000	3	0	7	5	*chip ID, only need write at EEPROM reg 0.
ethphxcmd gsww	7120	c002	1	c	7	0	*MDIO register
ethphxcmd gsww	7120	c004	0	1	8	1	* data
ethphxcmd gsww	7120	c006	8	8	0	5	*command line

Read command example:

command	switch reg	EEPROM ADD					
ethphxcmd gsww	7120	c000	3	0	7	5	*chip ID, only need write at EEPROM reg 0.
ethphxcmd gsww	7120	c002	1	c	7	0	*MDIO register
ethphxcmd gsww	7120	c004	0	0	0	0	*command line
ethphxcmd gswr	7120						

Output queue

Each port has 8 queues for different QoS services. Please know that QoS only active when traffic jam happen. It means that you should have flow control first for QoS. If not, you would only find the packet loss.
Free page: Read the 0x1fc0

For MT7530, if you want to check the queue, please use:
ethphxcmd gsww 7038 220
ethphxcmd gswr 7034

Here show the Q map:

	Q1 & Q0	Q3 & Q2	Q5 & Q4	Q7 & Q6
P0	220	221	222	223
P1	224	225	226	227
P2	228	229	22a	22b
P3	22c	22d	22e	22f
P4	230	231	232	233
P5	234	235	236	237
P6	238	239	23a	23b

00001FC0 FPLC Free Page Link Count Register 01EE01EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							MIN_FREE_PL_CNT									
Type							RO									
Reset							0	1	1	1	1	0	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FREE_PL_CNT									
Type							RO									
Reset							0	1	1	1	1	0	1	1	1	0

VLAN setting

You need use three registers to make 1 VLAN rule. Please follow the below information to do that:

0x94 104F0001 Port member 0~3+6 (4f =0100 1111)
0x98 00002000 Egress tag enable
0x90 80001010 VID member VID set as 10

00000090 VTCR VLAN Table Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSY	REV0														IDX_INVLD
Type	W1C	DC														RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FUNC				VID											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000094 VAWD1 VLAN and ACL Write Data I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000098 VAWD2 VLAN and ACL Write Data II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MAC forward control

0x0010 is used for MAC forwarding control rule. For different traffic, like broadcast, Unknown multicast...etc, you can set the forwarding port at this register.

00000010 MFC MAC Forward Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BC_FFP								UNM_FFP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNU_FFP								CPU_EN	CPU_PORT			MIRROR_EN	MIRROR_PORT		
Type	RW								RW	RW			RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MAC table aging time

Aging time is used for recording the MAC is exist or not and would be clean after 300 seconds if there is no traffic pass through again. For changing this, you can modify the 0x00A0.
The aging time would be depending on the switch core clock speed.

000000A0 AAC Address Age Control 00095001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0											AGE_DIS	AGE_CNT[7:4]			
Type	DC											RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AGE_CNT[3:0]				AGE_UNIT											
Type	RW				RW											
Reset	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1

MAC table

We have 2048 MAC entries exist in switch.
MT7530 build in the API command:
Ethphxcmd arl mactbl-disp
MAC AABBCCDDEEFF : TIMER:149, SA_PORT_FW:0, SA_MIR_EN:0, USER_PRI:0,
EG_TAG:0, LEAKY_EN:0, PORT:4, STATUS:1, TYPE:0
You can find that have an aging time, source port information over there.

For RT63368 or others platform, you can use the command flow to check the MAC table list:
Ethphxcmd gsww 80 8002 //clean
Ethphxcmd gsww 80 8004 //first MAC entry
Ethphxcmd gswr 84 // show the first entry
Ethphxcmd gswr 88 // show the firstentry
Ethphxcmd gsww 80 8005 //next MAC entry
Ethphxcmd gswr 84 // show the second entry
Ethphxcmd gswr 88 // show the second entry
For detail, you can check the register 0x0080,0x0084 and 0x0088.

00000080 ATC Address Table Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				ADDR											
Type	DC				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSY	SRCH_END	SRCH_HIT	ADDR_INVLD	AC_MAT				REV1		AC_SAT		REV2	AC_CMD		
Type	W1C	RO	RO	RO	RW				DC		RW		DC	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000084 TSRA1 Table Search Read Address I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

00000088 TSRA2 Table Search Read Address II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Flow control

You should set 0x1fe0 bit 31 as 1 for global flow control first.
We take Port 5 for example, if you want to disable TX and RX flow control, you should set the bit 5 and bit 4 of 0x3500 as 0. And read 4th and 5th bit of 0x3508 to check it works or not.

00001FE0 GFCCR0 Global Flow_Control Control Register 0 A0087858

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FC_EN		FC_OFF2ON_OPT	FC_ON2OFF_OPT					FC_PORT_BLK_THD							
Type	RW		RW	RW					RW							
Reset	1		1	0					0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FC_FREE_BLK_HITHD								FC_FREE_BLK_LOTHD							
Type	RW								RW							
Reset	0	1	1	1	1	0	0	0	0	1	0	1	1	0	0	0

0x3500

5	RW	FORCE_RX_FC_Pn	Port n Force Rx FC When (force_mode_pn = 1), this bit is used to control RX FC ability of port n 1'b1: Let MAC of port n to accept a pause frame when operates in full-duplex mode. 1'b0: Disable.	0x1
4	RW	FORCE_TX_FC_Pn	Port n Force Tx FC When (force_mode_pn = 1), this bit is used to control TX FC ability of port n 1'b1: Let MAC of port n to transmit a pause frame when operates in full-duplex mode and internal resouece is low. 1'b0: Disable.	0x1

00003508 PMSR_P5 PORT 5 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P5	EEE100_STS_P5	RX_FC_STS_P5	TX_FC_STS_P5	MAC_SPD_STS_P5		MAC_DPX_STS_P5	MAC_LNK_STS_P5
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Local port enable

This is used for debugging not for normal use. It means it would add the self port to the MAC table. So, the same packet would come out from the input port. Set 7th of 0x000c to enable it.

0000000C AGC ARL Global Control 00071819

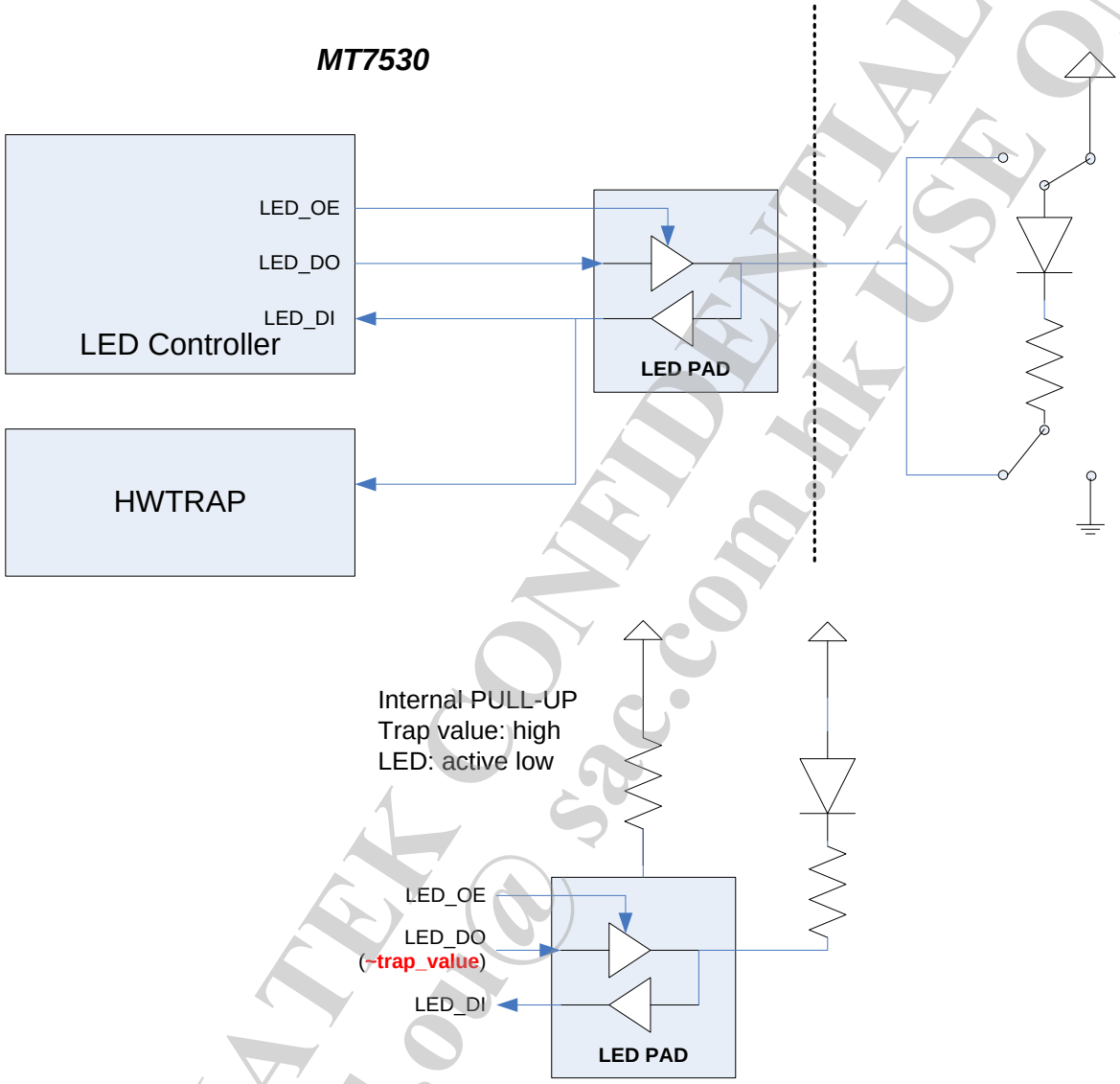
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MLDv2_int_en	REV0												ACL_INT	VLAN_INT	ADDR_INT
Type	RW	DC												RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RATE_COMP	COMP_BNUM							LOCAL_EN	ARL_P ADDING	ACL_MULTI	L2LEN_CHK	CTRL_DROP	VLAN4 CPU	ARL_PRI	ALR_RST_N
Type	RW	RW							RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1

LED controller

All hardware traps of MT7530 are weakly pull-up internally. The only way to pull-down these traps is using an external pull-down circuit. However, hardware traps and LEDs share the same pins in MT7530. To make LEDs work normally, the hardware configurations of LEDs will depend on its related values in the current design.
Every port has 3 LED to mean its behavior:

MT7530 Px_LED_0 is used for any ability linkup and traffic (10/100/1000).
MT7530 Px_LED_1 is used for 10/100 ability linkup and traffic (10/100).
MT7530 Px_LED_2 is used for Giga ability linkup and traffic (1000).

For trapping-high pins, the external LEDs should be active low. Its configuration is shown as below. OEs (output enables) of LED pads are controlled by the internal circuits, and LED_DO will always be LOW under this configuration. So the external LEDs should be active low.



MIB counter of port 0:

00004000	TDPC_P0	32	**TX Drop Packet Counter of Port 0**
00004004	TCRC_P0	32	**TX CRC Packet Counter of Port 0**
00004008	TUPC_P0	32	**TX Unicast Packet Counter of Port 0**
0000400C	TMPC_P0	32	**TX Multicast Packet Counter of Port 0**
00004010	TBPC_P0	32	**TX Broadcast Packet Counter of Port 0**
00004014	TCEC_P0	32	**TX Collision Event Counter of Port 0**
00004018	TSCEC_P0	32	**TX Single Collision Event Counter of Port 0**
0000401C	TMCEC_P0	32	**TX Multiple Collision Event Counter of Port 0**

00004020	TDEC_P0	32	**TX Deferred Event Counter of Port 0**
00004024	TLCEC_P0	32	**TX Late Collision Event Counter of Port 0**
00004028	TXCEC_P0	32	**TX excessive Collision Event Counter of Port 0**
0000402C	TPPC_P0	32	**TX Pause Packet Counter of Port 0**
00004030	TL64PC_P0	32	**TX packet Length in 64-byte slot Packet Counter of Port 0**
00004034	TL65PC_P0	32	**TX packet Length in 65-byte slot Packet Counter of Port 0**
00004038	TL128PC_P0	32	**TX packet Length in 128-byte slot Packet Counter of Port 0**
0000403C	TL256PC_P0	32	**TX packet Length in 256-byte slot Packet Counter of Port 0**
00004040	TL512PC_P0	32	**TX packet Length in 512-byte slot Packet Counter of Port 0**
00004044	TL1024PC_P0	32	**TX packet Length in 1024-byte slot Packet Counter of Port 0**
00004048	TOCL_P0	32	**TX Octet Counter Low double word of Port 0**
0000404C	TOCH_P0	32	**TX Octet Counter High double word of Port 0**
00004060	RDPC_P0	32	**RX Drop Packet Counter of Port 0**
00004064	RFPC_P0	32	**RX Filtering Packet Counter of Port 0**
00004068	RUPC_P0	32	**RX Unicast Packet Counter of Port 0**
0000406C	RMPC_P0	32	**RX Multicast Packet Counter of Port 0**
00004070	RBPC_P0	32	**RX Broadcast Packet Counter of Port 0**
00004074	RAEPC_P0	32	**RX Alignment Error Packet Counter of Port 0**
00004078	RCEPC_P0	32	**RX CRC(FCS) Error Packet Counter of Port 0**
0000407C	RUSPC_P0	32	**RX Undersize Packet Counter of Port 0**
00004080	RFEPC_P0	32	**RX Fragment Error Packet Counter of Port 0**
00004084	ROSPC_P0	32	**RX Oversize Packet Counter of Port 0**
00004088	RJEPC_P0	32	**RX Jabber Error Packet Counter of Port 0**
0000408C	RPPC_P0	32	**RX Pause Packet Counter of Port 0**
00004090	RL64PC_P0	32	**RX packet Length in 64-byte slot Packet Counter of Port 0**
00004094	RL65PC_P0	32	**RX packet Length in 65-byte slot Packet Counter of Port 0**
00004098	RL128PC_P0	32	**RX packet Length in 128-byte slot Packet Counter of Port 0**
0000409C	RL256PC_P0	32	**RX packet Length in 256-byte slot Packet Counter of Port 0**
000040A0	RL512PC_P0	32	**RX packet Length in 512-byte slot Packet Counter of Port 0**
000040A4	RL1024PC_P0	32	**RX packet Length in 1024-byte slot Packet Counter of Port 0**
000040A8	ROCL_P0	32	**RX Octet Counter Low double word of Port 0**
000040AC	ROCH_P0	32	**Rx Octet Counter High double word of Port 0**
000040B0	RDPC_CTRL_P0	32	**RX CTRL Drop Packet Counter of Port 0**
000040B4	RDPC_ING_P0	32	**RX Ingress Drop Packet Counter of Port 0**
000040B8	RDPC_ARL_P0	32	**RX ARL Drop Packet Counter of Port 0**
000040D0	TMIB_HF_STS_P0	32	**TX Port MIB Counter Half Full Status of Port 0**
000040D4	RMIB_HF_STS_P0	32	**RX Port MIB Counter Half Full Status of Port 0**

MIB counter of port 1:

00004100	TDPC_P1	32	**TX Drop Packet Counter of Port 1**
00004104	TCRC_P1	32	**TX CRC Packet Counter of Port 1**
00004108	TUPC_P1	32	**TX Unicast Packet Counter of Port 1**
0000410C	TMPC_P1	32	**TX Multicast Packet Counter of Port 1**
00004110	TBPC_P1	32	**TX Broadcast Packet Counter of Port 1**

00004114	TCEC_P1	32	TX Collision Event Counter of Port 1
00004118	TSCEC_P1	32	TX Single Collision Event Counter of Port 1
0000411C	TMCEC_P1	32	TX Multiple Collision Event Counter of Port 1
00004120	TDEC_P1	32	TX Deferred Event Counter of Port 1
00004124	TLCEC_P1	32	TX Late Collision Event Counter of Port 1
00004128	TXCEC_P1	32	TX excessive Collision Event Counter of Port 1
0000412C	TPPC_P1	32	TX Pause Packet Counter of Port 1
00004130	TL64PC_P1	32	TX packet Length in 64-byte slot Packet Counter of Port 1
00004134	TL65PC_P1	32	TX packet Length in 65-byte slot Packet Counter of Port 1
00004138	TL128PC_P1	32	TX packet Length in 128-byte slot Packet Counter of Port 1
0000413C	TL256PC_P1	32	TX packet Length in 256-byte slot Packet Counter of Port 1
00004140	TL512PC_P1	32	TX packet Length in 512-byte slot Packet Counter of Port 1
00004144	TL1024PC_P1	32	TX packet Length in 1024-byte slot Packet Counter of Port 1
00004148	TOCL_P1	32	TX Octet Counter Low double word of Port 1
0000414C	TOCH_P1	32	TX Octet Counter High double word of Port 1
00004160	RDPC_P1	32	RX Drop Packet Counter of Port 1
00004164	RFPC_P1	32	RX Filtering Packet Counter of Port 1
00004168	RUPC_P1	32	RX Unicast Packet Counter of Port 1
0000416C	RMPC_P1	32	RX Multicast Packet Counter of Port 1
00004170	RBPC_P1	32	RX Broadcast Packet Counter of Port 1
00004174	RAEPC_P1	32	RX Alignment Error Packet Counter of Port 1
00004178	RCEPC_P1	32	RX CRC(FCS) Error Packet Counter of Port 1
0000417C	RUSPC_P1	32	RX Undersize Packet Counter of Port 1
00004180	RFEPC_P1	32	RX Fragment Error Packet Counter of Port 1
00004184	ROSPC_P1	32	RX Oversize Packet Counter of Port 1
00004188	RJEPC_P1	32	RX Jabber Error Packet Counter of Port 1
0000418C	RPPC_P1	32	RX Pause Packet Counter of Port 1
00004190	RL64PC_P1	32	RX packet Length in 64-byte slot Packet Counter of Port 1
00004194	RL65PC_P1	32	RX packet Length in 65-byte slot Packet Counter of Port 1
00004198	RL128PC_P1	32	RX packet Length in 128-byte slot Packet Counter of Port 1
0000419C	RL256PC_P1	32	RX packet Length in 256-byte slot Packet Counter of Port 1
000041A0	RL512PC_P1	32	RX packet Length in 512-byte slot Packet Counter of Port 1
000041A4	RL1024PC_P1	32	RX packet Length in 1024-byte slot Packet Counter of Port 1
000041A8	ROCL_P1	32	RX Octet Counter Low double word of Port 1
000041AC	ROCH_P1	32	Rx Octet Counter High double word of Port 1
000041B0	RDPC_CTRL_P1	32	RX CTRL Drop Packet Counter of Port 1
000041B4	RDPC_ING_P1	32	RX Ingress Drop Packet Counter of Port 1
000041B8	RDPC_ARL_P1	32	RX ARL Drop Packet Counter of Port 1
000041D0	TMIB_HF_STS_P1	32	TX Port MIB Counter Half Full Status of Port 1
000041D4	RMIB_HF_STS_P1	32	RX Port MIB Counter Half Full Status of Port 1

MIB counter of port 2:

00004200	TDPC_P2	32	TX Drop Packet Counter of Port 2
00004204	TCRC_P2	32	TX CRC Packet Counter of Port 2

00004208	TUPC_P2	32	TX Unicast Packet Counter of Port 2
0000420C	TMPC_P2	32	TX Multicast Packet Counter of Port 2
00004210	TBPC_P2	32	TX Broadcast Packet Counter of Port 2
00004214	TCEC_P2	32	TX Collision Event Counter of Port 2
00004218	TSCEC_P2	32	TX Single Collision Event Counter of Port 2
0000421C	TMCEC_P2	32	TX Multiple Collision Event Counter of Port 2
00004220	TDEC_P2	32	TX Deferred Event Counter of Port 2
00004224	TLCEC_P2	32	TX Late Collision Event Counter of Port 2
00004228	TXCEC_P2	32	TX excessive Collision Event Counter of Port 2
0000422C	TPPC_P2	32	TX Pause Packet Counter of Port 2
00004230	TL64PC_P2	32	TX packet Length in 64-byte slot Packet Counter of Port 2
00004234	TL65PC_P2	32	TX packet Length in 65-byte slot Packet Counter of Port 2
00004238	TL128PC_P2	32	TX packet Length in 128-byte slot Packet Counter of Port 2
0000423C	TL256PC_P2	32	TX packet Length in 256-byte slot Packet Counter of Port 2
00004240	TL512PC_P2	32	TX packet Length in 512-byte slot Packet Counter of Port 2
00004244	TL1024PC_P2	32	TX packet Length in 1024-byte slot Packet Counter of Port 2
00004248	TOCL_P2	32	TX Octet Counter Low double word of Port 2
0000424C	TOCH_P2	32	TX Octet Counter High double word of Port 2
00004260	RDPC_P2	32	RX Drop Packet Counter of Port 2
00004264	RFPC_P2	32	RX Filtering Packet Counter of Port 2
00004268	RUPC_P2	32	RX Unicast Packet Counter of Port 2
0000426C	RMPC_P2	32	RX Multicast Packet Counter of Port 2
00004270	RBPC_P2	32	RX Broadcast Packet Counter of Port 2
00004274	RAEPC_P2	32	RX Alignment Error Packet Counter of Port 2
00004278	RCEPC_P2	32	RX CRC(FCS) Error Packet Counter of Port 2
0000427C	RUSPC_P2	32	RX Undersize Packet Counter of Port 2
00004280	RFEPC_P2	32	RX Fragment Error Packet Counter of Port 2
00004284	ROSPC_P2	32	RX Oversize Packet Counter of Port 2
00004288	RJEPC_P2	32	RX Jabber Error Packet Counter of Port 2
0000428C	RPPC_P2	32	RX Pause Packet Counter of Port 2
00004290	RL64PC_P2	32	RX packet Length in 64-byte slot Packet Counter of Port 2
00004294	RL65PC_P2	32	RX packet Length in 65-byte slot Packet Counter of Port 2
00004298	RL128PC_P2	32	RX packet Length in 128-byte slot Packet Counter of Port 2
0000429C	RL256PC_P2	32	RX packet Length in 256-byte slot Packet Counter of Port 2
000042A0	RL512PC_P2	32	RX packet Length in 512-byte slot Packet Counter of Port 2
000042A4	RL1024PC_P2	32	RX packet Length in 1024-byte slot Packet Counter of Port 2
000042A8	ROCL_P2	32	RX Octet Counter Low double word of Port 2
000042AC	ROCH_P2	32	Rx Octet Counter High double word of Port 2
000042B0	RDPC_CTRL_P2	32	RX CTRL Drop Packet Counter of Port 2
000042B4	RDPC_ING_P2	32	RX Ingress Drop Packet Counter of Port 2
000042B8	RDPC_ARL_P2	32	RX ARL Drop Packet Counter of Port 2
000042D0	TMIB_HF_STS_P2	32	TX Port MIB Counter Half Full Status of Port 2
000042D4	RMIB_HF_STS_P2	32	RX Port MIB Counter Half Full Status of Port 2

MIB counter of port 3:

00004300	TDPC_P3	32	**TX Drop Packet Counter of Port 3**
00004304	TCRC_P3	32	**TX CRC Packet Counter of Port 3**
00004308	TUPC_P3	32	**TX Unicast Packet Counter of Port 3**
0000430C	TMPC_P3	32	**TX Multicast Packet Counter of Port 3**
00004310	TBPC_P3	32	**TX Broadcast Packet Counter of Port 3**
00004314	TCEC_P3	32	**TX Collision Event Counter of Port 3**
00004318	TSCEC_P3	32	**TX Single Collision Event Counter of Port 3**
0000431C	TMCEC_P3	32	**TX Multiple Collision Event Counter of Port 3**
00004320	TDEC_P3	32	**TX Deferred Event Counter of Port 3**
00004324	TLCEC_P3	32	**TX Late Collision Event Counter of Port 3**
00004328	TXCEC_P3	32	**TX excessive Collision Event Counter of Port 3**
0000432C	TPPC_P3	32	**TX Pause Packet Counter of Port 3**
00004330	TL64PC_P3	32	**TX packet Length in 64-byte slot Packet Counter of Port 3**
00004334	TL65PC_P3	32	**TX packet Length in 65-byte slot Packet Counter of Port 3**
00004338	TL128PC_P3	32	**TX packet Length in 128-byte slot Packet Counter of Port 3**
0000433C	TL256PC_P3	32	**TX packet Length in 256-byte slot Packet Counter of Port 3**
00004340	TL512PC_P3	32	**TX packet Length in 512-byte slot Packet Counter of Port 3**
00004344	TL1024PC_P3	32	**TX packet Length in 1024-byte slot Packet Counter of Port 3**
00004348	TOCL_P3	32	**TX Octet Counter Low double word of Port 3**
0000434C	TOCH_P3	32	**TX Octet Counter High double word of Port 3**
00004360	RDPC_P3	32	**RX Drop Packet Counter of Port 3**
00004364	RFPC_P3	32	**RX Filtering Packet Counter of Port 3**
00004368	RUPC_P3	32	**RX Unicast Packet Counter of Port 3**
0000436C	RMPC_P3	32	**RX Multicast Packet Counter of Port 3**
00004370	RBPC_P3	32	**RX Broadcast Packet Counter of Port 3**
00004374	RAEPC_P3	32	**RX Alignment Error Packet Counter of Port 3**
00004378	RCEPC_P3	32	**RX CRC(FCS) Error Packet Counter of Port 3**
0000437C	RUSPC_P3	32	**RX Undersize Packet Counter of Port 3**
00004380	RFEPC_P3	32	**RX Fragment Error Packet Counter of Port 3**
00004384	ROSPC_P3	32	**RX Oversize Packet Counter of Port 3**
00004388	RJEPC_P3	32	**RX Jabber Error Packet Counter of Port 3**
0000438C	RPPC_P3	32	**RX Pause Packet Counter of Port 3**
00004390	RL64PC_P3	32	**RX packet Length in 64-byte slot Packet Counter of Port 3**
00004394	RL65PC_P3	32	**RX packet Length in 65-byte slot Packet Counter of Port 3**
00004398	RL128PC_P3	32	**RX packet Length in 128-byte slot Packet Counter of Port 3**
0000439C	RL256PC_P3	32	**RX packet Length in 256-byte slot Packet Counter of Port 3**
000043A0	RL512PC_P3	32	**RX packet Length in 512-byte slot Packet Counter of Port 3**
000043A4	RL1024PC_P3	32	**RX packet Length in 1024-byte slot Packet Counter of Port 3**
000043A8	ROCL_P3	32	**RX Octet Counter Low double word of Port 3**
000043AC	ROCH_P3	32	**Rx Octet Counter High double word of Port 3**
000043B0	RDPC_CTRL_P3	32	**RX CTRL Drop Packet Counter of Port 3**
000043B4	RDPC_ING_P3	32	**RX Ingress Drop Packet Counter of Port 3**
000043B8	RDPC_ARL_P3	32	**RX ARL Drop Packet Counter of Port 3**

000043D0	TMIB_HF_STS_P3	32	**TX Port MIB Counter Half Full Status of Port 3**
000043D4	RMIB_HF_STS_P3	32	**RX Port MIB Counter Half Full Status of Port 3**

MIB counter of port 4:

00004400	TDPC_P4	32	**TX Drop Packet Counter of Port 4**
00004404	TCRC_P4	32	**TX CRC Packet Counter of Port 4**
00004408	TUPC_P4	32	**TX Unicast Packet Counter of Port 4**
0000440C	TMPC_P4	32	**TX Multicast Packet Counter of Port 4**
00004410	TBPC_P4	32	**TX Broadcast Packet Counter of Port 4**
00004414	TCEC_P4	32	**TX Collision Event Counter of Port 4**
00004418	TSCEC_P4	32	**TX Single Collision Event Counter of Port 4**
0000441C	TMCEC_P4	32	**TX Multiple Collision Event Counter of Port 4**
00004420	TDEC_P4	32	**TX Deferred Event Counter of Port 4**
00004424	TLCEC_P4	32	**TX Late Collision Event Counter of Port 4**
00004428	TXCEC_P4	32	**TX excessive Collision Event Counter of Port 4**
0000442C	TPPC_P4	32	**TX Pause Packet Counter of Port 4**
00004430	TL64PC_P4	32	**TX packet Length in 64-byte slot Packet Counter of Port 4**
00004434	TL65PC_P4	32	**TX packet Length in 65-byte slot Packet Counter of Port 4**
00004438	TL128PC_P4	32	**TX packet Length in 128-byte slot Packet Counter of Port 4**
0000443C	TL256PC_P4	32	**TX packet Length in 256-byte slot Packet Counter of Port 4**
00004440	TL512PC_P4	32	**TX packet Length in 512-byte slot Packet Counter of Port 4**
00004444	TL1024PC_P4	32	**TX packet Length in 1024-byte slot Packet Counter of Port 4**
00004448	TOCL_P4	32	**TX Octet Counter Low double word of Port 4**
0000444C	TOCH_P4	32	**TX Octet Counter High double word of Port 4**
00004460	RDPC_P4	32	**RX Drop Packet Counter of Port 4**
00004464	RFPC_P4	32	**RX Filtering Packet Counter of Port 4**
00004468	RUPC_P4	32	**RX Unicast Packet Counter of Port 4**
0000446C	RMPC_P4	32	**RX Multicast Packet Counter of Port 4**
00004470	RBPC_P4	32	**RX Broadcast Packet Counter of Port 4**
00004474	RAEPC_P4	32	**RX Alignment Error Packet Counter of Port 4**
00004478	RCEPC_P4	32	**RX CRC(FCS) Error Packet Counter of Port 4**
0000447C	RUSPC_P4	32	**RX Undersize Packet Counter of Port 4**
00004480	RFEPC_P4	32	**RX Fragment Error Packet Counter of Port 4**
00004484	ROSPC_P4	32	**RX Oversize Packet Counter of Port 4**
00004488	RJEPC_P4	32	**RX Jabber Error Packet Counter of Port 4**
0000448C	RPPC_P4	32	**RX Pause Packet Counter of Port 4**
00004490	RL64PC_P4	32	**RX packet Length in 64-byte slot Packet Counter of Port 4**
00004494	RL65PC_P4	32	**RX packet Length in 65-byte slot Packet Counter of Port 4**
00004498	RL128PC_P4	32	**RX packet Length in 128-byte slot Packet Counter of Port 4**
0000449C	RL256PC_P4	32	**RX packet Length in 256-byte slot Packet Counter of Port 4**
000044A0	RL512PC_P4	32	**RX packet Length in 512-byte slot Packet Counter of Port 4**
000044A4	RL1024PC_P4	32	**RX packet Length in 1024-byte slot Packet Counter of Port 4**
000044A8	ROCL_P4	32	**RX Octet Counter Low double word of Port 4**
000044AC	ROCH_P4	32	**Rx Octet Counter High double word of Port 4**

000044B0	RDPC_CTRL_P4	32	**RX CTRL Drop Packet Counter of Port 4**
000044B4	RDPC_ING_P4	32	**RX Ingress Drop Packet Counter of Port 4**
000044B8	RDPC_ARL_P4	32	**RX ARL Drop Packet Counter of Port 4**
000044D0	TMIB_HF_STS_P4	32	**TX Port MIB Counter Half Full Status of Port 4**
000044D4	RMIB_HF_STS_P4	32	**RX Port MIB Counter Half Full Status of Port 4**

MIB counter of port 5:

00004500	TDPC_P5	32	**TX Drop Packet Counter of Port 5**
00004504	TCRC_P5	32	**TX CRC Packet Counter of Port 5**
00004508	TUPC_P5	32	**TX Unicast Packet Counter of Port 5**
0000450C	TMPC_P5	32	**TX Multicast Packet Counter of Port 5**
00004510	TBPC_P5	32	**TX Broadcast Packet Counter of Port 5**
00004514	TCEC_P5	32	**TX Collision Event Counter of Port 5**
00004518	TSCEC_P5	32	**TX Single Collision Event Counter of Port 5**
0000451C	TMCEC_P5	32	**TX Multiple Collision Event Counter of Port 5**
00004520	TDEC_P5	32	**TX Deferred Event Counter of Port 5**
00004524	TLCEC_P5	32	**TX Late Collision Event Counter of Port 5**
00004528	TXCEC_P5	32	**TX excessive Collision Event Counter of Port 5**
0000452C	TPPC_P5	32	**TX Pause Packet Counter of Port 5**
00004530	TL64PC_P5	32	**TX packet Length in 64-byte slot Packet Counter of Port 5**
00004534	TL65PC_P5	32	**TX packet Length in 65-byte slot Packet Counter of Port 5**
00004538	TL128PC_P5	32	**TX packet Length in 128-byte slot Packet Counter of Port 5**
0000453C	TL256PC_P5	32	**TX packet Length in 256-byte slot Packet Counter of Port 5**
00004540	TL512PC_P5	32	**TX packet Length in 512-byte slot Packet Counter of Port 5**
00004544	TL1024PC_P5	32	**TX packet Length in 1024-byte slot Packet Counter of Port 5**
00004548	TOCL_P5	32	**TX Octet Counter Low double word of Port 5**
0000454C	TOCH_P5	32	**TX Octet Counter High double word of Port 5**
00004560	RDPC_P5	32	**RX Drop Packet Counter of Port 5**
00004564	RFPC_P5	32	**RX Filtering Packet Counter of Port 5**
00004568	RUPC_P5	32	**RX Unicast Packet Counter of Port 5**
0000456C	RMPC_P5	32	**RX Multicast Packet Counter of Port 5**
00004570	RBPC_P5	32	**RX Broadcast Packet Counter of Port 5**
00004574	RAEPC_P5	32	**RX Alignment Error Packet Counter of Port 5**
00004578	RCEPC_P5	32	**RX CRC(FCS) Error Packet Counter of Port 5**
0000457C	RUSPC_P5	32	**RX Undersize Packet Counter of Port 5**
00004580	RFEPC_P5	32	**RX Fragment Error Packet Counter of Port 5**
00004584	ROSPC_P5	32	**RX Oversize Packet Counter of Port 5**
00004588	RJEPC_P5	32	**RX Jabber Error Packet Counter of Port 5**
0000458C	RPPC_P5	32	**RX Pause Packet Counter of Port 5**
00004590	RL64PC_P5	32	**RX packet Length in 64-byte slot Packet Counter of Port 5**
00004594	RL65PC_P5	32	**RX packet Length in 65-byte slot Packet Counter of Port 5**
00004598	RL128PC_P5	32	**RX packet Length in 128-byte slot Packet Counter of Port 5**
0000459C	RL256PC_P5	32	**RX packet Length in 256-byte slot Packet Counter of Port 5**
000045A0	RL512PC_P5	32	**RX packet Length in 512-byte slot Packet Counter of Port 5**

000045A4	RL1024PC_P5	32	**RX packet Length in 1024-byte slot Packet Counter of Port 5**
000045A8	ROCL_P5	32	**RX Octet Counter Low double word of Port 5**
000045AC	ROCH_P5	32	**Rx Octet Counter High double word of Port 5**
000045B0	RDPC_CTRL_P5	32	**RX CTRL Drop Packet Counter of Port 5**
000045B4	RDPC_ING_P5	32	**RX Ingress Drop Packet Counter of Port 5**
000045B8	RDPC_ARL_P5	32	**RX ARL Drop Packet Counter of Port 5**
000045D0	TMIB_HF_STS_P5	32	**TX Port MIB Counter Half Full Status of Port 5**
000045D4	RMIB_HF_STS_P5	32	**RX Port MIB Counter Half Full Status of Port 5**

MIB counter of port 6:

00004600	TDPC_P6	32	**TX Drop Packet Counter of Port 6**
00004604	TCRC_P6	32	**TX CRC Packet Counter of Port 6**
00004608	TUPC_P6	32	**TX Unicast Packet Counter of Port 6**
0000460C	TMPC_P6	32	**TX Multicast Packet Counter of Port 6**
00004610	TBPC_P6	32	**TX Broadcast Packet Counter of Port 6**
00004614	TCEC_P6	32	**TX Collision Event Counter of Port 6**
00004618	TSCEC_P6	32	**TX Single Collision Event Counter of Port 6**
0000461C	TMCEC_P6	32	**TX Multiple Collision Event Counter of Port 6**
00004620	TDEC_P6	32	**TX Deferred Event Counter of Port 6**
00004624	TLCEC_P6	32	**TX Late Collision Event Counter of Port 6**
00004628	TXCEC_P6	32	**TX excessive Collision Event Counter of Port 6**
0000462C	TPPC_P6	32	**TX Pause Packet Counter of Port 6**
00004630	TL64PC_P6	32	**TX packet Length in 64-byte slot Packet Counter of Port 6**
00004634	TL65PC_P6	32	**TX packet Length in 65-byte slot Packet Counter of Port 6**
00004638	TL128PC_P6	32	**TX packet Length in 128-byte slot Packet Counter of Port 6**
0000463C	TL256PC_P6	32	**TX packet Length in 256-byte slot Packet Counter of Port 6**
00004640	TL512PC_P6	32	**TX packet Length in 512-byte slot Packet Counter of Port 6**
00004644	TL1024PC_P6	32	**TX packet Length in 1024-byte slot Packet Counter of Port 6**
00004648	TOCL_P6	32	**TX Octet Counter Low double word of Port 6**
0000464C	TOCH_P6	32	**TX Octet Counter High double word of Port 6**
00004660	RDPC_P6	32	**RX Drop Packet Counter of Port 6**
00004664	RFPC_P6	32	**RX Filtering Packet Counter of Port 6**
00004668	RUPC_P6	32	**RX Unicast Packet Counter of Port 6**
0000466C	RMPC_P6	32	**RX Multicast Packet Counter of Port 6**
00004670	RBPC_P6	32	**RX Broadcast Packet Counter of Port 6**
00004674	RAEPC_P6	32	**RX Alignment Error Packet Counter of Port 6**
00004678	RCEPC_P6	32	**RX CRC(FCS) Error Packet Counter of Port 6**
0000467C	RUSPC_P6	32	**RX Undersize Packet Counter of Port 6**
00004680	RFEPC_P6	32	**RX Fragment Error Packet Counter of Port 6**
00004684	ROSPC_P6	32	**RX Oversize Packet Counter of Port 6**
00004688	RJEPC_P6	32	**RX Jabber Error Packet Counter of Port 6**
0000468C	RPPC_P6	32	**RX Pause Packet Counter of Port 6**
00004690	RL64PC_P6	32	**RX packet Length in 64-byte slot Packet Counter of Port 6**

00004694	RL65PC_P6	32	**RX packet Length in 65-byte slot Packet Counter of Port 6**
00004698	RL128PC_P6	32	**RX packet Length in 128-byte slot Packet Counter of Port 6**
0000469C	RL256PC_P6	32	**RX packet Length in 256-byte slot Packet Counter of Port 6**
000046A0	RL512PC_P6	32	**RX packet Length in 512-byte slot Packet Counter of Port 6**
000046A4	RL1024PC_P6	32	**RX packet Length in 1024-byte slot Packet Counter of Port 6**
000046A8	ROCL_P6	32	**RX Octet Counter Low double word of Port 6**
000046AC	ROCH_P6	32	**Rx Octet Counter High double word of Port 6**
000046B0	RDPC_CTRL_P6	32	**RX CTRL Drop Packet Counter of Port 6**
000046B4	RDPC_ING_P6	32	**RX Ingress Drop Packet Counter of Port 6**
000046B8	RDPC_ARL_P6	32	**RX ARL Drop Packet Counter of Port 6**
000046D0	TMIB_HF_STS_P6	32	**TX Port MIB Counter Half Full Status of Port 6**
000046D4	RMIB_HF_STS_P6	32	**RX Port MIB Counter Half Full Status of Port 6**