

Standard Cells

Open Source Tools

- yosys
- graywolf
- qrouter
- several FPGA routers

graywolf

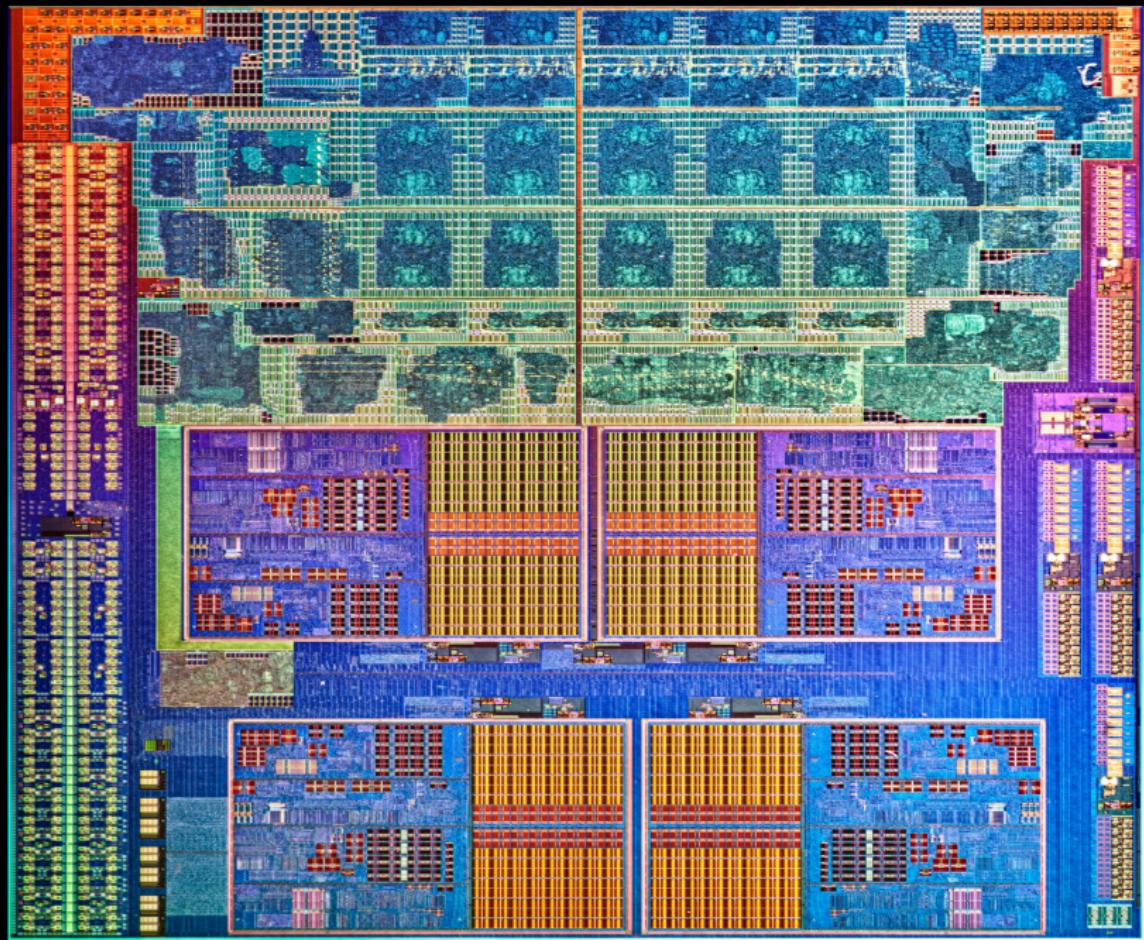
- Originates in Academia: TimberWolf
- Simulated annealing
 - Meta heuristic that is useful not only for placement
- Inline syscalls
 - This is just a bad idea

qrouter

- Started in 2011 by Tim Edwards
- Widely used for FPGA
 - Not ready for silicon
- Sequential routing
 - Parallelism not in scope
- Difficult to prove formal correctness
 - Prove that C implementation of Rip-up and Re-route is correct

Productive Tools

- Different tool sets like BonnRoute, Cadence Suite, Alliance tools, etc.
- Similar capabilities with respect to silicon
- Just throw man-power at VLSI — what is automation?



Routing: State of the Art

- Place components for a large chip
- Route wires roughly along a chessboard for a large chip
- Route detailed tracks and vias for a large chip
- Formal correctness: Rip-up and Re-route
- Formal style: Sequential/Imperative code

Routing: Proposed

- Decomposition for a large chip
- Place components and route for small chips in parallel
- Place abstract gates and route recursively
- Formal correctness: Reduction from SMT
- Formal style: Parallel/Declarative code

Divide and Conquer

Academia + Industry:

- Placement and Routing are different problems
- All components map to the same problem

LibreSilicon:

- Placement and Routing are the same problem
- Different components map to different problems

Routing Hierarchy

Academia + Industry:

- Geographical partitioning of a wafer → *cut tree*
- Based on preceding placement steps

LibreSilicon:

- Modular chip development → *subcell hierarchy*
- Subcells carry implicit and explicit subcells

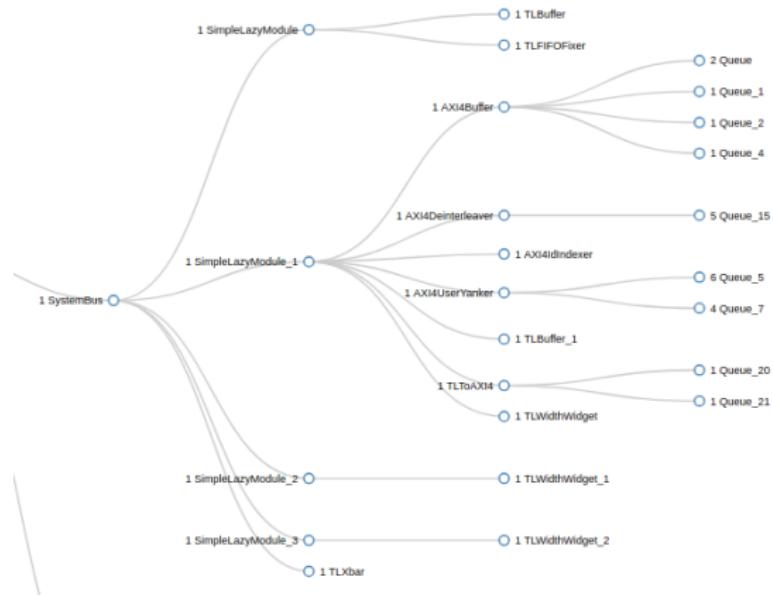
Frontier: Parallelism

- BonnRoute: concurrency + shared memory model
- qrouter: none
- lsc: map + reduce

Subcell hierarchies

- Explicit subcell hierarchies through high modularization
- Implicit subcell hierarchies through exlining
- Preserve hierarchy in compiler interfaces

High modularization



Exlining

- Proof of concept: picorv

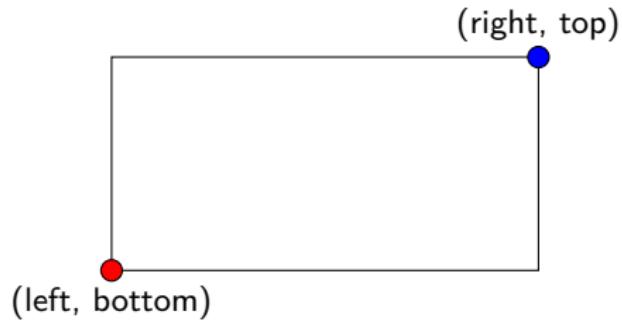
Unconstrained Small Unified Silicon Problem

- Components and nets → *rectilinear geometries*
- Components do not overlap
- Nets overlap with their pins on components

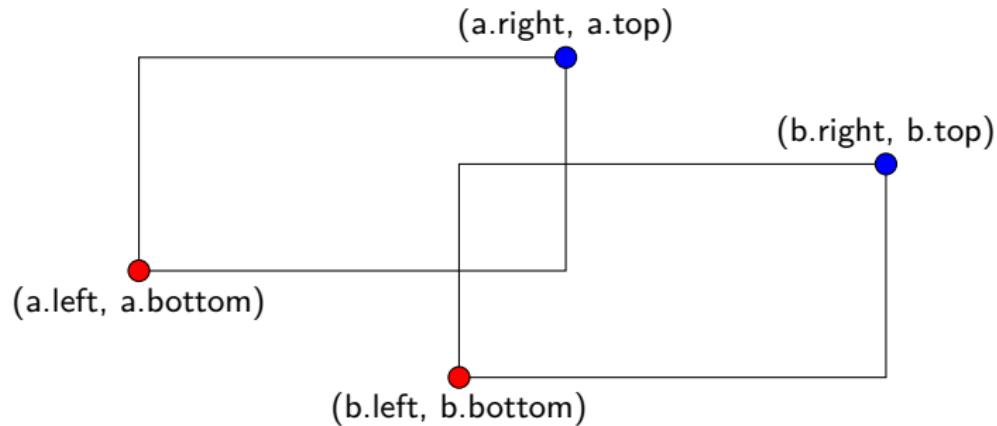
Minimizing Goals

- Layout area
- Maximum wire length
- Via count
- Crossing number (computational)
- Wire jogs (minor)

Defining rectangular components



Overlaps



Reduction from SMT

`b.left > a.right || a.bottom > b.top`

Combining in the LSC Semigroup

overlap + net connect + another constraint

Just stay here

non-critical EXP

Maximize yield

Compiler versus. process

Features

- MOSFETs
- LDMOSFETs (High voltage)
- BJTs
- Zener polysilicon diodes
- SONOS flash cells
- Polysilicon resistors
- Metal caps

Process design considerations

- Should be portable
- Robust
- Low amount of layers
- KISS (Keep it simple and stupid)
- Avoid expensive machines (can be manufactured in a home lab)

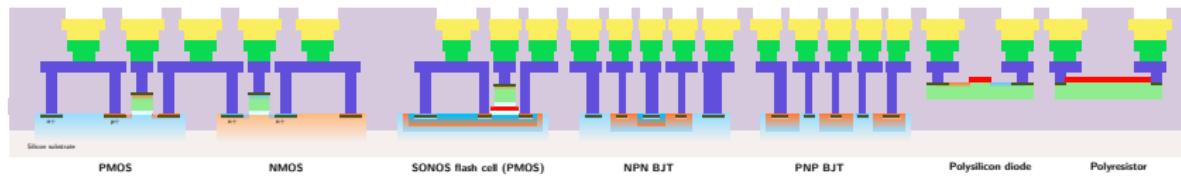
Process design considerations



Process design considerations



Cross section



PearlRiver (珠江芯片一号)

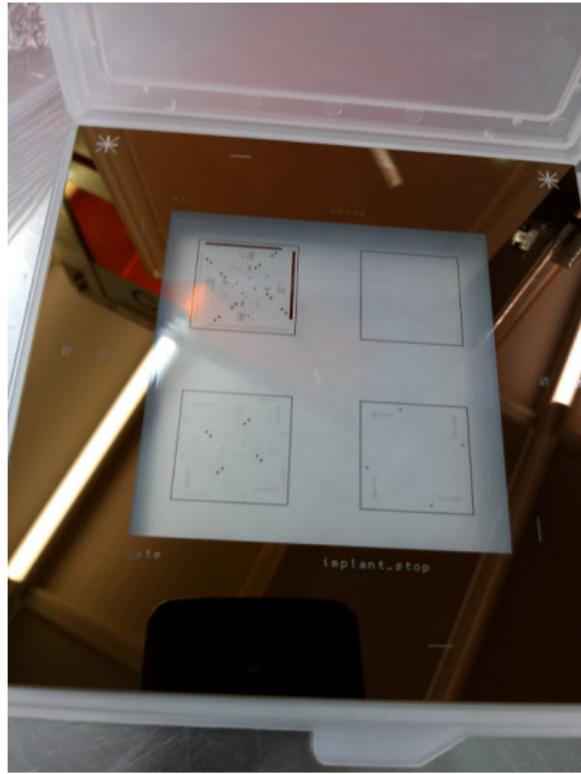


PearlRiver (珠江芯片一号)

Fulfils following functions:

- Debugging
- Calibration of new equipment to LibreSilicon
- Research of new features
- Syncing process features between fabs

Photomask



Photomask

- Is stepper/aligner brand specific
- ASML stepper masks contain 4 layers each
- The NFF stepper has a reduction value of 5:1
- A 5 micron gate on the mask is 1 micron on the wafer

Photo resist (HKUST)

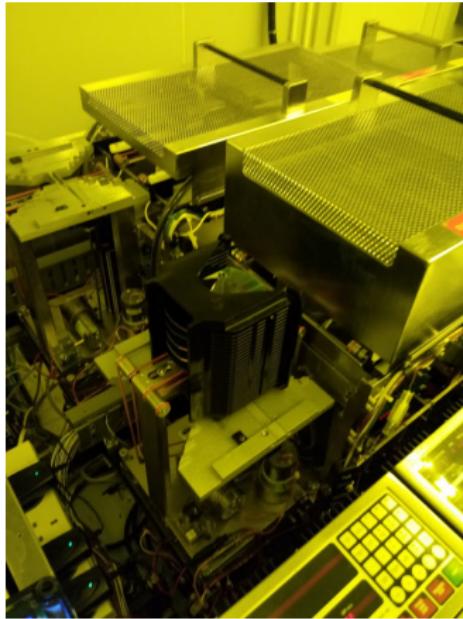


Photo resist (HKUST)

Two types of photo resist:

- FH 6400L (implantation)
- HPR 504 (normal etch)

Factors to consider:

- Thickness of FH 6400L and implantation energy are interlinked
- Thickness of HPR 504 and etching time are interlinked (selectivity)

After exposure



Alignment

