



>> **DATA SHEET**
(DOC No. HX8363-A-DS)

>> **HX8363-A**

480RGB x 864 dot, 16.7M color,
TFT Mobile Single Chip Driver
Preliminary version 03 July, 2011

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>> HX8363-A

480RGB x 864 dot, 16.7M color, TFT
Mobile Single Chip Driver



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Preliminary Version 03

July, 2011

1. General Description

This document describes Himax's HX8363-A is supports WVGA resolution driving controller. The HX8363-A is designed to provide a single-chip solution that combines a source driver, power supply circuit to drive a TFT dot matrix LCD with 480RGBx864 dots at maximum.

The HX8363-A can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8363-A also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8363-A also supports 16 / 18 / 24-bit RGB interface and 3-wire serial peripheral interface, MIPI DSI interface mode. Via serial peripheral interface or DSI interface, HX8363-A can receive the initialization settings for the display operation and for selecting the display functions. The initialization settings can be stored in the non-volatile memory and are loaded at display start.

The HX8363-A is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

2. Features

2.1 Display

- Resolution:
 - 480RGB x 864
 - 480RGB x 854
 - 480RGB x 800
 - 480RGB x 640
 - 360RGB x 640
- Display Color modes
 - Normal Display Mode On
 - 65,536 (R(5),G(6),B(5)) colors
 - 262,144 (R(6),G(6),B(6)) colors
 - 16,777,216 (R(8),G(8),B(8)) colors

2.2 Display Module

- Support 1440 source channel outputs
- Adjusted Source voltages (VinP0 ~ VinP16, VinN0 ~ VinN16)
- Output voltage level
 - VSP=4.7~5.5V
 - VSN=-5.5~-4.7V
 - Positive source output voltage level: VSPR to VSSA is 3.5V to 5V
 - Negative source output voltage level: VSNR to VSSA is -5V to -3.5V
 - Positive gate driver output voltage level: VGH to VSSA is 15V, 18V, 20V
 - Negative gate driver output voltage level: VGL to VSSA is -8V, -10V, -12V
 - VCOM= -2V ~ 0V, a step=16mV
- 1-dot inversion, 2-dot inversion, Column inversion

2.3 Display/Control Interface

- Display Interface types supported
 - Serial data transfer interface
 - 16-/18-/24- data lines parallel video (RGB) interface
 - ◆ Register control for display and function selection through SPI protocol
 - DSI (Display Serial Interface) interface
- Color modes
 - 16 bit/pixel: R(5), G(6), B(5)
 - 18 bit/pixel: R(6), G(6), B(6)
 - 24 bit/pixel: R(8), G(8), B(8)

2.4 Input power

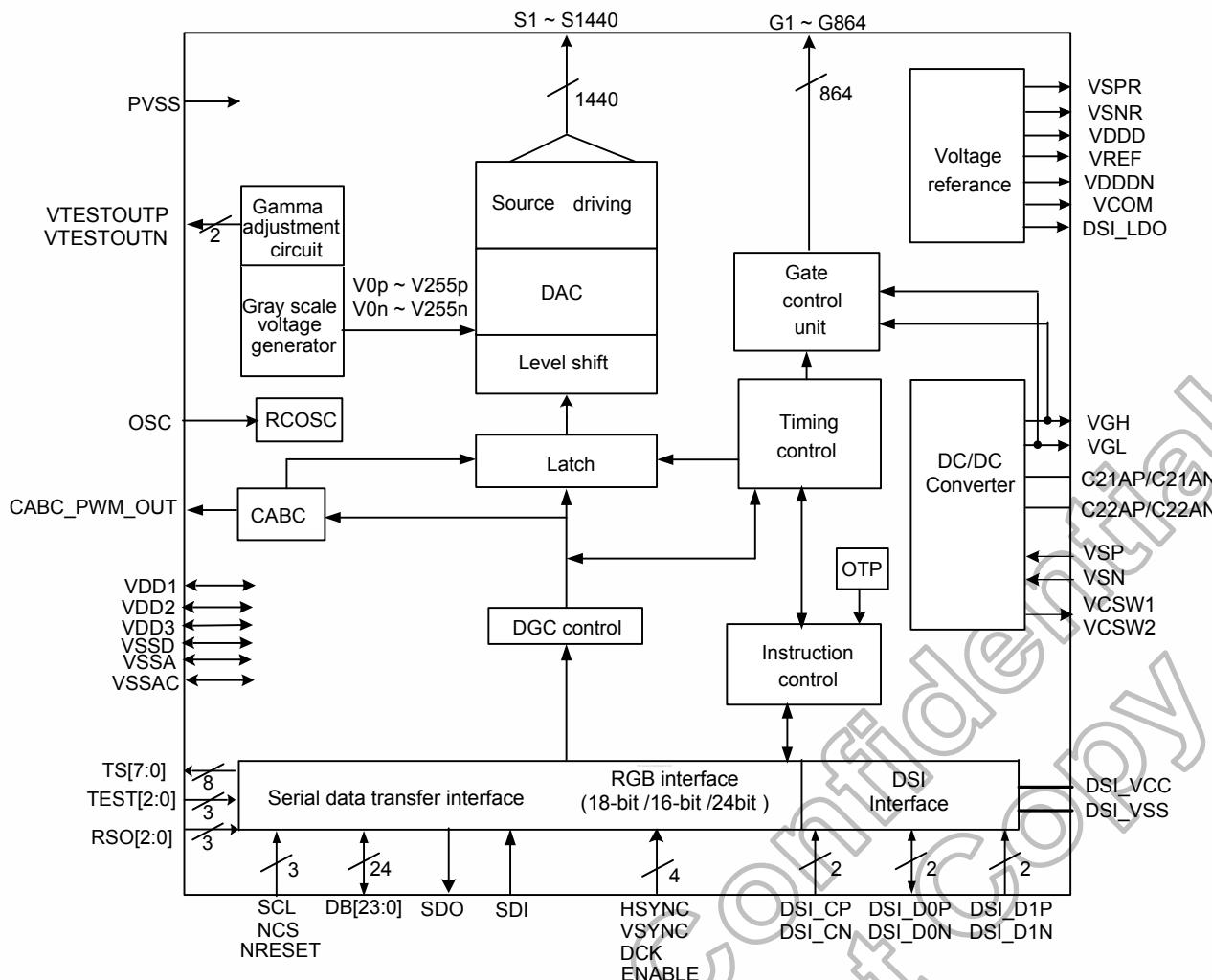
- I/O and interface power supply (VDD1): 1.65V ~ 3.3V
- Analog power supply (VDD2): 2.5V ~ 3.3V
- Logic power supply (VDD3): 2.5V ~ 3.3V
- DSI power supply (DSI_VCC): 1.65V ~ 3.3V
- OTP programming voltage (PVSS): 7.5V ± 0.2V

2.5 Miscellaneous

- Low power consumption, suitable for battery operated systems
- GAS function for preventing image sticking when abnormal power off
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -40 ~ +85 °C
- HBM ESD (Human Body Mode)>2KV, MM(Machine Mode)>±200V and Latch up >±200mA
- Proprietary multi phase driving for lower power consumption
- 4 selectable electro-optical transfer function (Gamma)
- Oscillator for display clock generation
- Support Inversion mode
- DC/DC converter for source
- Support DC COM driving
- VCOM voltage generator
- Support Equalize function
- Support 2 step gate signal
- Support normal black/normal white LCD
- OTP memory to store initialization register settings (3 times for VCOM setting , ID setting)
- Support Content Adaptive Brightness Control(CABC) function
- Support DGC(Digital Gamma Correction) Function

3. Device Overview

3.1 Block Diagram



3.2 Pin Description

Host Interface Pins						
Signals	I/O	Pin Number	Connected with	Description		
RSO0	I	1	MPU	Resolution selection pins. RSO[2:0] is used for selecting resolution. Must be connected to VSSD or VDD1.		
				RSO2	RSO1	RSO0 Resolution
				0	0	0 480RGBX864
				0	0	1 480RGBX854
				0	1	0 480RGBX800
				0	1	1 480RGBX640
				1	0	0 360 RGBX640
				1	0	1 Setting disable
				1	1	0 Setting disable
				1	1	1 Setting disable
BS0 ~ BS1	I	2	VSSD/VDD1	Select the MPU interface mode as listed below:		
				BS1	BS0	MPU interface mode
				0	0	3 wire serial + RGB interface (SCL Rising edge)
				0	1	DSI video mode
				1	0	Reserve
				1	1	Reserve
			Must be connected to VSSD or VDD1.			
NCS	I	1	MPU	Chip select signal. Low: chip can be accessed. High: chip cannot be accessed. If this pin is not used, please connect it to VSSD or VDD1.		
NRESET	I	3	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSSD or VDD1). (Latch type)		
SCL	I	1	MPU	Serves as a write signal and writes data at the rising edge. When operate in serial interface, it serves as SCL (Serial Clock) If not used, let it open or connected to VDD1.		
DB23~0	I/O	24	MPU	RGB interface		
				Data bus	Used	Unused
				16-bit bus	DB21~17, DB13~8, DB5~1	DB23~22, DB16~14, DB7~6, DB0
				18-bit bus	DB21~16, DB13~8, DB5~0	DB23~22, DB15~14, DB7~6
				24-bit bus	DB23~D0	--
			Let the unused pins open for each mode.			
SDO	O	3	MPU	Serial data output. Let it to open in MPU interface mode.		
SDI	I	1	MPU	Serial data input pin in serial interface operation.		
REGVDD	-	1	-	This pin is no function, please let it open.		
DSI_LDO_EN	-	1	-	This pin is no function, please let it open.		

Clock Input and RGB Interface				
Signals	I/O	Pin Number	Connected with	Description
H SYNC	I	1	-	Line synchronizing signal. Must be connected to VSSD or VDD1 if not used.
ENABLE	I	1	MPU	A data ENABLE signal in RGB I/F mode. Has to be fixed to VSSD level in MPU interface mode.
V SYNC	I	1	-	Frame synchronizing signal. Must be connected to VSSD or VDD1 if not used.
DCK	I	1	-	Dot clock signal. Must be connected to VSSD or VDD1 if not used.

Source and Gate Driver Output Pins														
Signals	I/O	Pin Number	Connected with	Description										
S1~S1440	O	1440	LCD	Output voltages applied to the liquid crystal. <table border="1"> <tr> <td>RGB resolution</td> <td>Source channels</td> </tr> <tr> <td>360RGB</td> <td>S1~S540, S901~S1440</td> </tr> <tr> <td>480RGB</td> <td>S1~S1440</td> </tr> </table>	RGB resolution	Source channels	360RGB	S1~S540, S901~S1440	480RGB	S1~S1440				
RGB resolution	Source channels													
360RGB	S1~S540, S901~S1440													
480RGB	S1~S1440													
G1 ~ G864	O	864	LCD	Gate driver output pins. These pins output VGH, VGL. (If not used, should be open) <table border="1"> <tr> <td>Gate resolution</td> <td>Gate channels</td> </tr> <tr> <td>640</td> <td>G1 ~ G640</td> </tr> <tr> <td>800</td> <td>G1 ~ G800</td> </tr> <tr> <td>854</td> <td>G1 ~ G854</td> </tr> <tr> <td>864</td> <td>G1 ~ G864</td> </tr> </table>	Gate resolution	Gate channels	640	G1 ~ G640	800	G1 ~ G800	854	G1 ~ G854	864	G1 ~ G864
Gate resolution	Gate channels													
640	G1 ~ G640													
800	G1 ~ G800													
854	G1 ~ G854													
864	G1 ~ G864													

Power Supply Pins																		
Signals	I/O	Pin Number	Connected with	Description														
PCCS0 ~ PCCS1	I	2	VSSD/ VDD3	Select the VSP/VSN bumping method as listed below: <table border="1"> <tr> <th>PCCS1</th> <th>PCCS0</th> <th>Driving mode</th> </tr> <tr> <td>0</td> <td>0</td> <td>One Inductor Mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>Two Inductor Mode</td> </tr> <tr> <td>1</td> <td>0</td> <td rowspan="2">Charge pump Mode (Use HX5186-A)</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </table> Must be connected to VSSD or VDD3.	PCCS1	PCCS0	Driving mode	0	0	One Inductor Mode	0	1	Two Inductor Mode	1	0	Charge pump Mode (Use HX5186-A)	1	1
PCCS1	PCCS0	Driving mode																
0	0	One Inductor Mode																
0	1	Two Inductor Mode																
1	0	Charge pump Mode (Use HX5186-A)																
1	1																	
VDD1	I	9	Power supply	A power supply for the I/O circuit. VDD1= 1.65 ~ 3.3V. VDD1 must less than VDD2 and VDD3.														
VDD2	I	3	Power supply	A power supply for the analog power. VDD2 = 2.5 ~ 3.3V. VDD2 input level should be same as VDD3 input level to avoid the level-mismatching at internal level shifter circuit.														
VDD3	I	9	Power supply	A power supply for the logic power, DC/DC converter VDD3 = 2.5 ~ 3.3V.														
VSSA	P	14	Power supply	Analog ground. VSSA = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.														
VSSAC	P	3	Power supply	Analog ground. Must connect to VSSA on the FPC.														
VSSD	P	26	Power supply	Ground for the internal logic. VSSD = 0V. When using the COG method, connect to VSSA on the FPC to prevent noise.														
PVSS	I	5	Power supply	External high voltage pin used in OTP mode and operates at 7.5V. If not used, let it open.														

Output Pins of Power and reference voltage				
Signals	I/O	Pin Number	Connected with	Description
VSP	I	6	Stabilizing capacitor	Input voltage from the set-up circuit (4.7V to 5.5V). It is generated from VDD3.
VSN	I	6	Stabilizing capacitor	Input voltage from the set-up circuit (-4.7V to -5.5V). It is generated from VDD3.
VSPC	I	1	VSP	Positive boosting reference voltage input.
VSNC	I	1	VSN	Negative boosting reference voltage input.
VSPR	O	2	Stabilizing capacitor	Positive regulated voltage output (3.5V ~ VSP - 0.5)
VSNR	O	2	Stabilizing capacitor	Positive regulated voltage output (-3.5V ~ VSN + 0.5)
VDDD	O	6	Stabilizing capacitor	Internal logic voltage output
VDDDN	O	4	Stabilizing capacitor	Internal logic voltage output (-2.5V fixed)
VREF	O	2	Stabilizing capacitor	Reference voltage from internal band gap circuit. The tolerance of VREF voltage is $\pm 3\%$ (1.8V fixed)
VGH	O	5	Stabilizing capacitor	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGH.
VGL	O	11	Stabilizing capacitor	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGL. Place a schottkey barrier diode between VGL and VSN.
VCOM	O	17	Stabilizing capacitor	The power supply of common voltage in DC com driving. The voltage range is set between -2V to 0V. It must be connected a stabilizing capacitor 2.2u to VSSD.
VCOMR	I	1	-	This pin is used for external VCOM input.
DSI_LDO	O	4	Capacitor	DSI regulator output pin. (1.2V ~ 1.3V) Connect to a stabilizing capacitor between DSI_VSS and DSI_LDO. If not used, please open these pins.

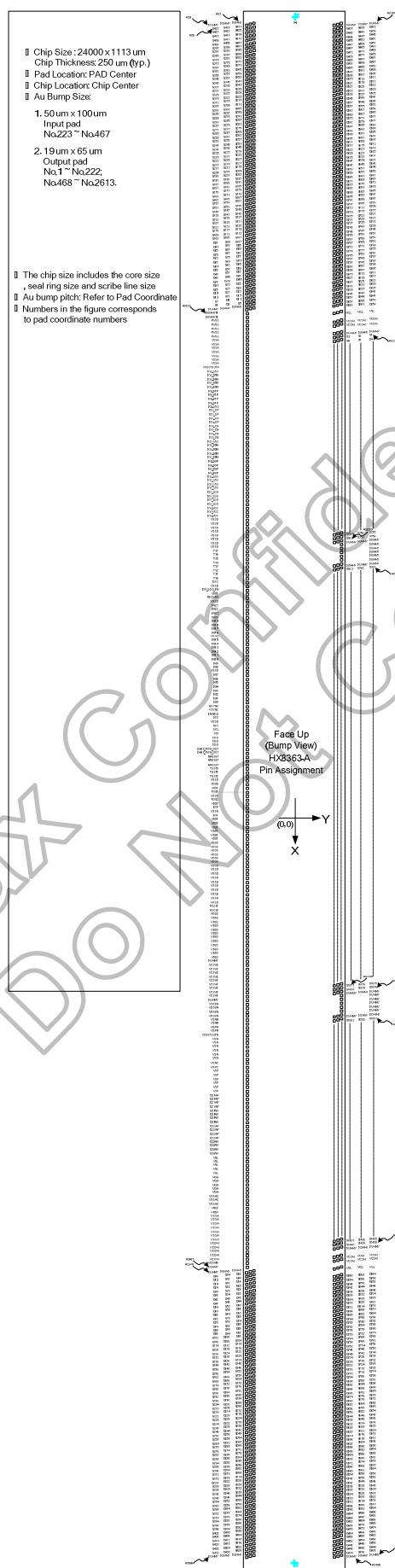
DC/DC pumping				
Signals	I/O	Pin Number	Connected with	Description
C21AP, C21AN	I/O	8	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH voltage.
C22AP, C22AN	I/O	8	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGL voltage.
VCSW1	O	5	-	Boosting control output1, it needs to connect to the gate pin of NMOS on external DC/DC converter circuit. (0~VDD3)
VCSW2	O	4	-	Boosting control output2, it needs to connect to the gate pin of PMOS on external DC/DC converter circuit. (0~VDD3)

CABC & ABC & Ambient light sensor				
Signals	I/O	Pin Number	Connected with	Description
CABC_PWM_OUT	O	2	-	Backlight On/Off control pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage range = 0~ VDD1.

Test Pins				
Signals	I/O	Pin Number	Connected with	Description
OSC	I	1	-	Oscillator input for test purpose. If not used, please let it open or connected to VSSD. (weak pull low)
TEST0	I	1	VSSD	A test pin. This pin is by internal logic function test. This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
TEST1	I	1	VSSD	A test pin. This pin is by internal logic function test. This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
TEST2	I	1	MPU	A test pin. This pin is by internal logic function test. This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
TS7~0	O	8	Open	A test pin. Disconnect it.
VTESTOUTP	O	1	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
VTESTOUTN	O	1	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
DUMMYR1 DUMMYR2	-	2	Open	Dummy pads. Available for measuring the COG contact resistance. They are short-circuited within the chip.
DUMMY	-	49	Open	Dummy pads. These pins are no function, please let them open.

MIPI-DSI Interface Parts				
Signals	I/O	Pin Number	Connected with	Description
DSI_D0P, DSI_D0N	I/O	8	DSI Host	MIPI-DSI Data differential signal input pins (Data lane 0). If not used, let it connected to DSI_VSS.
DSI_CP, DSI_CN	I	8	DSI Host	MIPI-DSI CLOCK differential signal input pins. If not used, let it connected to DSI_VSS.
DSI_D1P, DSI_D1N	I	8	DSI Host	MIPI-DSI Data differential signal input pins (Data lane 1). If not used, let it connected to DSI_VSS.
DSI_VCC	P	3	Power Supply	Power supply for the MIPI DSI analog power. DSI_VCC = 1.65V ~ 3.3V. If not used, let it open.
DSI_VSS	P	7	Ground	MIPI DSI analogy ground. DSI_VSS = 0V. When using the COG method, connect to VSSA on the FPC to prevent noise.

3.3 Pin Assignment



3.4 PAD Coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY	-11886	-285	61	G317	-11166	-285	121	G197	-10446	-285	181	G77	-9726	-285
2	DUMMY	-11874	-375	62	G315	-11154	-375	122	G195	-10434	-375	182	G75	-9714	-375
3	DUMMY	-11862	-465	63	G313	-11142	-465	123	G193	-10422	-465	183	G73	-9702	-465
4	G431	-11850	-285	64	G311	-11130	-285	124	G191	-10410	-285	184	G71	-9690	-285
5	G429	-11838	-375	65	G309	-11118	-375	125	G189	-10398	-375	185	G69	-9678	-375
6	G427	-11826	-465	66	G307	-11106	-465	126	G187	-10386	-465	186	G67	-9666	-465
7	G425	-11814	-285	67	G305	-11094	-285	127	G185	-10374	-285	187	G65	-9654	-285
8	G423	-11802	-375	68	G303	-11082	-375	128	G183	-10362	-375	188	G63	-9642	-375
9	G421	-11790	-465	69	G301	-11070	-465	129	G181	-10350	-465	189	G61	-9630	-465
10	G419	-11778	-285	70	G299	-11058	-285	130	G179	-10338	-285	190	G59	-9618	-285
11	G417	-11766	-375	71	G297	-11046	-375	131	G177	-10326	-375	191	G57	-9606	-375
12	G415	-11754	-465	72	G295	-11034	-465	132	G175	-10314	-465	192	G55	-9594	-465
13	G413	-11742	-285	73	G293	-11022	-285	133	G173	-10302	-285	193	G53	-9582	-285
14	G411	-11730	-375	74	G291	-11010	-375	134	G171	-10290	-375	194	G51	-9570	-375
15	G409	-11718	-465	75	G289	-10998	-465	135	G169	-10278	-465	195	G49	-9558	-465
16	G407	-11706	-285	76	G287	-10986	-285	136	G167	-10266	-285	196	G47	-9546	-285
17	G405	-11694	-375	77	G285	-10974	-375	137	G165	-10254	-375	197	G45	-9534	-375
18	G403	-11682	-465	78	G283	-10962	-465	138	G163	-10242	-465	198	G43	-9522	-465
19	G401	-11670	-285	79	G281	-10950	-285	139	G161	-10230	-285	199	G41	-9510	-285
20	G399	-11658	-375	80	G279	-10938	-375	140	G159	-10218	-375	200	G39	-9498	-375
21	G397	-11646	-465	81	G277	-10926	-465	141	G157	-10206	-465	201	G37	-9486	-465
22	G395	-11634	-285	82	G275	-10914	-285	142	G155	-10194	-285	202	G35	-9474	-285
23	G393	-11622	-375	83	G273	-10902	-375	143	G153	-10182	-375	203	G33	-9462	-375
24	G391	-11610	-465	84	G271	-10890	-465	144	G151	-10170	-465	204	G31	-9450	-465
25	G389	-11598	-285	85	G269	-10878	-285	145	G149	-10158	-285	205	G29	-9438	-285
26	G387	-11586	-375	86	G267	-10866	-375	146	G147	-10146	-375	206	G27	-9426	-375
27	G385	-11574	-465	87	G265	-10854	-465	147	G145	-10134	-465	207	G25	-9414	-465
28	G383	-11562	-285	88	G263	-10842	-285	148	G143	-10122	-285	208	G23	-9402	-285
29	G381	-11550	-375	89	G261	-10830	-375	149	G141	-10110	-375	209	G21	-9390	-375
30	G379	-11538	-465	90	G259	-10818	-465	150	G139	-10098	-465	210	G19	-9378	-465
31	G377	-11526	-285	91	G257	-10806	-285	151	G137	-10086	-285	211	G17	-9366	-285
32	G375	-11514	-375	92	G255	-10794	-375	152	G135	-10074	-375	212	G15	-9354	-375
33	G373	-11502	-465	93	G253	-10782	-465	153	G133	-10062	-465	213	G13	-9342	-465
34	G371	-11490	-285	94	G251	-10770	-285	154	G131	-10050	-285	214	G11	-9330	-285
35	G369	-11478	-375	95	G249	-10758	-375	155	G129	-10038	-375	215	G9	-9318	-375
36	G367	-11466	-465	96	G247	-10746	-465	156	G127	-10026	-465	216	G7	-9306	-465
37	G365	-11454	-285	97	G245	-10734	-285	157	G125	-10014	-285	217	G5	-9294	-285
38	G363	-11442	-375	98	G243	-10722	-375	158	G123	-10002	-375	218	G3	-9282	-375
39	G361	-11430	-465	99	G241	-10710	-465	159	G121	-9990	-465	219	G1	-9270	-465
40	G359	-11418	-285	100	G239	-10698	-285	160	G119	-9978	-285	220	DUMMY	-9258	-285
41	G357	-11406	-375	101	G237	-10686	-375	161	G117	-9966	-375	221	DUMMY	-9246	-375
42	G355	-11394	-465	102	G235	-10674	-465	162	G115	-9954	-465	222	DUMMY	-9234	-465
43	G353	-11382	-285	103	G233	-10662	-285	163	G113	-9942	-285	223	DUMMYR1	-9150	-447.5
44	G351	-11370	-375	104	G231	-10650	-375	164	G111	-9930	-375	224	DUMMYR2	-9075	-447.5
45	G349	-11358	-465	105	G229	-10638	-465	165	G109	-9918	-465	225	PVSS	-9000	-447.5
46	G347	-11346	-285	106	G227	-10626	-285	166	G107	-9906	-285	226	PVSS	-8925	-447.5
47	G345	-11334	-375	107	G225	-10614	-375	167	G105	-9894	-375	227	PVSS	-8850	-447.5
48	G343	-11322	-465	108	G223	-10602	-465	168	G103	-9882	-465	228	PVSS	-8775	-447.5
49	G341	-11310	-285	109	G221	-10590	-285	169	G101	-9870	-285	229	PVSS	-8700	-447.5
50	G339	-11298	-375	110	G219	-10578	-375	170	G99	-9858	-375	230	VSSA	-8625	-447.5
51	G337	-11286	-465	111	G217	-10566	-465	171	G97	-9846	-465	231	VSSA	-8550	-447.5
52	G335	-11274	-285	112	G215	-10554	-285	172	G95	-9834	-285	232	VSSA	-8475	-447.5
53	G333	-11262	-375	113	G213	-10542	-375	173	G93	-9822	-375	233	VSSA	-8400	-447.5
54	G331	-11250	-465	114	G211	-10530	-465	174	G91	-9810	-465	234	VSSA	-8325	-447.5
55	G329	-11238	-285	115	G209	-10518	-285	175	G89	-9798	-285	235	VSSA	-8250	-447.5
56	G327	-11226	-375	116	G207	-10506	-375	176	G87	-9786	-375	236	VSSA	-8175	-447.5
57	G325	-11214	-465	117	G205	-10494	-465	177	G85	-9774	-465	237	VTESTOUTP	-8100	-447.5
58	G323	-11202	-285	118	G203	-10482	-285	178	G83	-9762	-285	238	DSI_VSS	-8025	-447.5
59	G321	-11190	-375	119	G201	-10470	-375	179	G81	-9750	-375	239	DSI_D1N	-7950	-447.5
60	G319	-11178	-465	120	G199	-10458	-465	180	G79	-9738	-465	240	DSI_D1N	-7875	-447.5

No.	Name	X	Y
241	DSI_D1N	-7800	-447.5
242	DSI_D1N	-7725	-447.5
243	DSI_D1P	-7650	-447.5
244	DSI_D1P	-7575	-447.5
245	DSI_D1P	-7500	-447.5
246	DSI_D1P	-7425	-447.5
247	DSI_VSS	-7350	-447.5
248	DSI_CP	-7275	-447.5
249	DSI_CP	-7200	-447.5
250	DSI_CP	-7125	-447.5
251	DSI_CP	-7050	-447.5
252	DSI_CN	-6975	-447.5
253	DSI_CN	-6900	-447.5
254	DSI_CN	-6825	-447.5
255	DSI_CN	-6750	-447.5
256	DSI_VSS	-6675	-447.5
257	DSI_D0N	-6600	-447.5
258	DSI_D0N	-6525	-447.5
259	DSI_D0N	-6450	-447.5
260	DSI_D0N	-6375	-447.5
261	DSI_D0P	-6300	-447.5
262	DSI_D0P	-6225	-447.5
263	DSI_D0P	-6150	-447.5
264	DSI_D0P	-6075	-447.5
265	DSI_VSS	-6000	-447.5
266	DSI_VSS	-5925	-447.5
267	DSI_VSS	-5850	-447.5
268	DSI_VSS	-5775	-447.5
269	DSI_LDO	-5700	-447.5
270	DSI_LDO	-5625	-447.5
271	DSI_LDO	-5550	-447.5
272	DSI_LDO	-5475	-447.5
273	DSI_VCC	-5400	-447.5
274	DSI_VCC	-5325	-447.5
275	DSI_VCC	-5250	-447.5
276	VSSD	-5175	-447.5
277	VSSD	-5100	-447.5
278	VSSD	-5025	-447.5
279	VSSD	-4950	-447.5
280	VSSD	-4875	-447.5
281	VSSD	-4800	-447.5
282	VSSD	-4725	-447.5
283	VSSD	-4650	-447.5
284	TS7	-4575	-447.5
285	TS6	-4500	-447.5
286	TS5	-4425	-447.5
287	TS4	-4350	-447.5
288	TS3	-4275	-447.5
289	TS2	-4200	-447.5
290	TS1	-4125	-447.5
291	TS0	-4050	-447.5
292	OSC	-3975	-447.5
293	VSSD	-3900	-447.5
294	DSI_LDO_EN	-3825	-447.5
295	VDD1	-3750	-447.5
296	REGVDD	-3675	-447.5
297	VSSD	-3600	-447.5
298	DB23	-3525	-447.5
299	DB22	-3450	-447.5
300	DB21	-3375	-447.5
301	DB20	-3300	-447.5
302	DB19	-3225	-447.5
303	DB18	-3150	-447.5
304	DB17	-3075	-447.5
305	DB16	-3000	-447.5
306	VSSD	-2925	-447.5
307	DB15	-2850	-447.5
308	DB14	-2775	-447.5
309	DB13	-2700	-447.5
310	DB12	-2625	-447.5
311	DB11	-2550	-447.5
312	DB10	-2475	-447.5
313	DB9	-2400	-447.5
314	DB8	-2325	-447.5
315	VSSD	-2250	-447.5
316	DB7	-2175	-447.5
317	DB6	-2100	-447.5
318	DB5	-2025	-447.5
319	DB4	-1950	-447.5
320	DB3	-1875	-447.5
321	DB2	-1800	-447.5
322	DB1	-1725	-447.5
323	DB0	-1650	-447.5
324	H SYNC	-1575	-447.5
325	V SYNC	-1500	-447.5
326	ENABLE	-1425	-447.5
327	DCK	-1350	-447.5
328	VSSD	-1275	-447.5
329	NCS	-1200	-447.5
330	SCL	-1125	-447.5
331	SDI	-1050	-447.5
332	SDO	-975	-447.5
333	SDO	-900	-447.5
334	SDO	-825	-447.5
335	CABC_PWM_OUT	-750	-447.5
336	CABC_PWM_OUT	-675	-447.5
337	NRESET	-600	-447.5
338	NRESET	-525	-447.5
339	NRESET	-450	-447.5
340	TEST0	-375	-447.5
341	TEST1	-300	-447.5
342	TEST2	-225	-447.5
343	VSSD	-150	-447.5
344	RS00	-75	-447.5
345	VDD1	0	-447.5
346	RS01	75	-447.5
347	VSSD	150	-447.5
348	RS02	225	-447.5
349	VDD1	300	-447.5
350	BS0	375	-447.5
351	VSSD	450	-447.5
352	BS1	525	-447.5
353	VDD1	600	-447.5
354	VDD1	675	-447.5
355	VDD1	750	-447.5
356	VDD1	825	-447.5
357	VDD1	900	-447.5
358	VDD1	975	-447.5
359	VDDD	1050	-447.5
360	VDDD	1125	-447.5
361	VDDD	1200	-447.5
362	VDDD	1275	-447.5
363	VDDD	1350	-447.5
364	VDDD	1425	-447.5
365	VSSD	1500	-447.5
366	VSSD	1575	-447.5
367	VSSD	1650	-447.5
368	VSSD	1725	-447.5
369	VSSD	1800	-447.5
370	VSSD	1875	-447.5
371	VSSD	1950	-447.5
372	VSSD	2025	-447.5
373	VSSD	2100	-447.5
374	VSSD	2175	-447.5
375	PCCS1	2250	-447.5
376	PCCS0	2325	-447.5
377	VDD2	2400	-447.5
378	VDD2	2475	-447.5
379	VDD2	2550	-447.5
380	VDD3	2625	-447.5
381	VDD3	2700	-447.5
382	VDD3	2775	-447.5
383	VDD3	2850	-447.5
384	VDD3	2925	-447.5
385	VDD3	3000	-447.5
386	VDD3	3075	-447.5
387	VDD3	3150	-447.5
388	VDD3	3225	-447.5
389	DUMMY	3300	-447.5
390	VCSW2	3375	-447.5
391	VCSW2	3450	-447.5
392	VCSW2	3525	-447.5
393	VCSW2	3600	-447.5
394	VCSW1	3675	-447.5
395	VCSW1	3750	-447.5
396	VCSW1	3825	-447.5
397	VCSW1	3900	-447.5
398	VCSW1	3975	-447.5
399	DUMMY	4050	-447.5
400	VDDDN	4125	-447.5
401	VDDDN	4200	-447.5
402	VDDDN	4275	-447.5
403	VDDDN	4350	-447.5
404	VSNR	4425	-447.5
405	VSNR	4500	-447.5
406	VSPR	4575	-447.5
407	VSPR	4650	-447.5
408	VTESTOUTN	4725	-447.5
409	VSN	4800	-447.5
410	VSN	4875	-447.5
411	VSN	4950	-447.5
412	VSN	5025	-447.5
413	VSN	5100	-447.5
414	VSN	5175	-447.5
415	VSNC	5250	-447.5
416	VSPC	5325	-447.5
417	VSP	5400	-447.5
418	VSP	5475	-447.5
419	VSP	5550	-447.5
420	VSP	5625	-447.5
421	VSP	5700	-447.5
422	VSP	5775	-447.5
423	C21AP	5850	-447.5
424	C21AP	5925	-447.5
425	C21AP	6000	-447.5
426	C21AN	6075	-447.5
427	C21AN	6150	-447.5
428	C21AN	6225	-447.5
429	C21AN	6300	-447.5
430	C21AN	6375	-447.5
431	C22AP	6450	-447.5
432	C22AP	6525	-447.5
433	C22AP	6600	-447.5
434	C22AP	6675	-447.5
435	C22AN	6750	-447.5
436	C22AN	6825	-447.5
437	C22AN	6900	-447.5
438	C22AN	6975	-447.5
439	VGL	7050	-447.5
440	VGL	7125	-447.5
441	VGL	7200	-447.5
442	VGL	7275	-447.5
443	VGL	7350	-447.5
444	VGH	7425	-447.5
445	VGH	7500	-447.5
446	VGH	7575	-447.5
447	VGH	7650	-447.5
448	VGH	7725	-447.5
449	VSSAC	7800	-447.5
450	VSSAC	7875	-447.5
451	VSSAC	7950	-447.5
452	VREF	8025	-447.5
453	VREF	8100	-447.5
454	VSSA	8175	-447.5
455	VSSA	8250	-447.5
456	VSSA	8325	-447.5
457	VSSA	8400	-447.5
458	VSSA	8475	-447.5
459	VSSA	8550	-447.5
460	VSSA	8625	-447.5
461	VCOM	8700	-447.5
462	VCOM	8775	-447.5
463	VCOM	8850	-447.5
464	VCOM	8925	-447.5
465	VCOM	9000	-447.5
466	VCOMR	9075	-447.5
467	DUMMY	9150	-447.5
468	DUMMY	9234	-375
469	DUMMY	9246	-375
470	DUMMY	9258	-465
471	G2	9270	-285
472	G4	9282	-375
473	G6	9294	-465
474	G8	9306	-285
475	G10	9318	-375
476	G12	9330	-465
477	G14	9342	-285
478	G16	9354	-375
479	G18	9366	-465
480	G20	9378	-285

No.	Name	X	Y
481	G22	9390	-375
482	G24	9402	-465
483	G26	9414	-285
484	G28	9426	-375
485	G30	9438	-465
486	G32	9450	-285
487	G34	9462	-375
488	G36	9474	-465
489	G38	9486	-285
490	G40	9498	-375
491	G42	9510	-465
492	G44	9522	-285
493	G46	9534	-375
494	G48	9546	-465
495	G50	9558	-285
496	G52	9570	-375
497	G54	9582	-465
498	G56	9594	-285
499	G58	9606	-375
500	G60	9618	-465
501	G62	9630	-285
502	G64	9642	-375
503	G66	9654	-465
504	G68	9666	-285
505	G70	9678	-375
506	G72	9690	-465
507	G74	9702	-285
508	G76	9714	-375
509	G78	9726	-465
510	G80	9738	-285
511	G82	9750	-375
512	G84	9762	-465
513	G86	9774	-285
514	G88	9786	-375
515	G90	9798	-465
516	G92	9810	-285
517	G94	9822	-375
518	G96	9834	-465
519	G98	9846	-285
520	G100	9858	-375
521	G102	9870	-465
522	G104	9882	-285
523	G106	9894	-375
524	G108	9906	-465
525	G110	9918	-285
526	G112	9930	-375
527	G114	9942	-465
528	G116	9954	-285
529	G118	9966	-375
530	G120	9978	-465
531	G122	9990	-285
532	G124	10002	-375
533	G126	10014	-465
534	G128	10026	-285
535	G130	10038	-375
536	G132	10050	-465
537	G134	10062	-285
538	G136	10074	-375
539	G138	10086	-465
540	G140	10098	-285
541	G142	10110	-375
542	G144	10122	-465
543	G146	10134	-285
544	G148	10146	-375
545	G150	10158	-465
546	G152	10170	-285
547	G154	10182	-375
548	G156	10194	-465
549	G158	10206	-285
550	G160	10218	-375
551	G162	10230	-465
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559	G178	10326	-375
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562	G184	10362	-375
563	G186	10374	-465
564	G188	10386	-285
565	G190	10398	-375
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568	G196	10434	-375
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626	G312	11130	-465
627	G314	11142	-285
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648	G356	11394	-285
649	G358	11406	-375
650	G360	11418	-465
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652	G364	11442	-375
653	G366	11454	-465
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655	G370	11478	-375
656	G372	11490	-465
657	G374	11502	-285
658	G376	11514	-375
659	G378	11526	-465
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729	G506	11418	285
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731	G510	11394	465
732	G512	11382	285
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735	G518	11346	285
736	G520	11334	375
737	G522	11322	465
738	G524	11310	285
739	G526	11298	375
740	G528	11286	465
741	G530	11274	285
742	G532	11262	375
743	G534	11250	465
744	G536	11238	285
745	G538	11226	375
746	G540	11214	465
747	G542	11202	285
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749	G546	11178	465
750	G548	11166	285
751	G550	11154	375
752	G552	11142	465
753	G554	11130	285
754	G556	11118	375
755	G558	11106	465
756	G560	11094	285
757	G562	11082	375
758	G564	11070	465
759	G566	11058	285
760	G568	11046	375
761	G570	11034	465
762	G572	11022	285
763	G574	11010	375
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765	G578	10986	285
766	G580	10974	375
767	G582	10962	465
768	G584	10950	285
769	G586	10938	375
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771	G590	10914	285
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773	G594	10890	465
774	G596	10878	285
775	G598	10866	375
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969	S1392	8310	285
970	S1391	8298	375
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1125	S1236	6438	285
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1173	S1188	5862	285
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1176	S1185	5826	285
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1179	S1182	5790	285
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1209	S1152	5430	285
1210	S1151	5418	375
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1212	S1149	5394	285
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1218	S1143	5322	285
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1222	S1139	5274	375
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1224	S1137	5250	285
1225	S1136	5238	375
1226	S1135	5226	465
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1230	S1131	5178	285
1231	S1130	5166	375
1232	S1129	5154	465
1233	S1128	5142	285
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1236	S1125	5106	285
1237	S1124	5094	375
1238	S1123	5082	465
1239	S1122	5070	285
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1243	S1118	5022	375
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1245	S1116	4998	285
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1328	S1044	3882	375
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1340	S1032	3738	375
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1452	S920	2394	375
1453	S919	2382	465
1454	S918	2370	285
1455	S917	2358	375
1456	S916	2346	465
1457	S915	2334	285
1458	S914	2322	375
1459	S913	2310	465
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1461	S911	2286	375
1462	S910	2274	465
1463	S909	2262	285
1464	S908	2250	375
1465	S907	2238	465
1466	S906	2226	285
1467	S905	2214	375
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1469	S903	2190	285
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1472	S900	2154	285
1473	S899	2142	375
1474	S898	2130	465
1475	S897	2118	285
1476	S896	2106	375
1477	S895	2094	465
1478	S894	2082	285
1479	S893	2070	375
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1489	S883	1950	465
1490	S882	1938	285
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1492	S880	1914	465
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1581	S791	846	375
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1583	S789	822	285
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1586	S786	786	285
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1592	S780	714	285
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1607	S765	534	285
1608	S764	522	375
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1612	S760	474	465
1613	S759	462	285
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1713	S659	-738	375
1714	S658	-750	465
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1716	S656	-774	375
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1823	S549	-2058	285
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1825	S547	-2082	465
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1828	S544	-2118	465
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1835	S537	-2202	285
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1837	S535	-2226	465
1838	S534	-2238	285
1839	S533	-2250	375
1840	S532	-2262	465
1841	S531	-2274	285
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1844	S528	-2310	285
1845	S527	-2322	375
1846	S526	-2334	465
1847	S525	-2346	285
1848	S524	-2358	375
1849	S523	-2370	465
1850	S522	-2382	285
1851	S521	-2394	375
1852	S520	-2406	465
1853	S519	-2418	285
1854	S518	-2430	375
1855	S517	-2442	465
1856	S516	-2454	285
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1858	S514	-2478	465
1859	S513	-2490	285
1860	S512	-2502	375

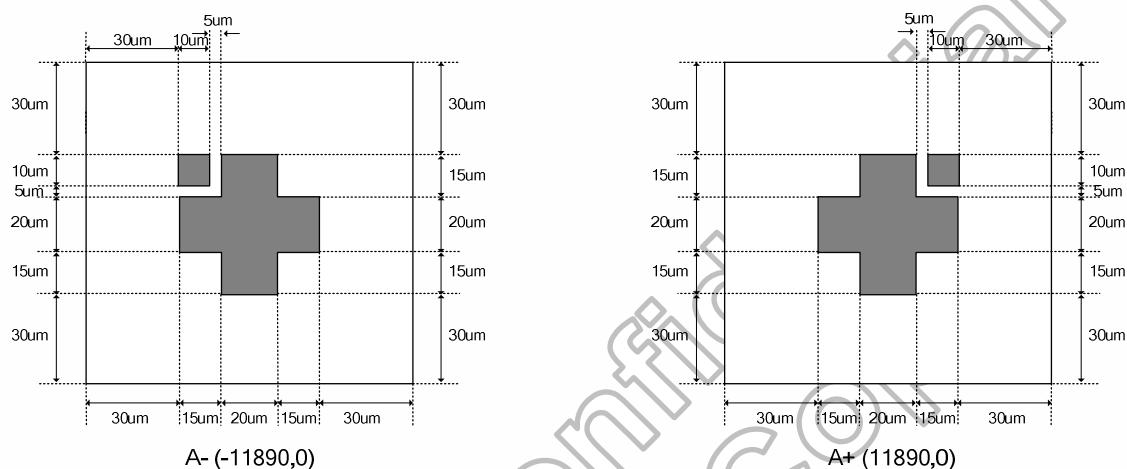
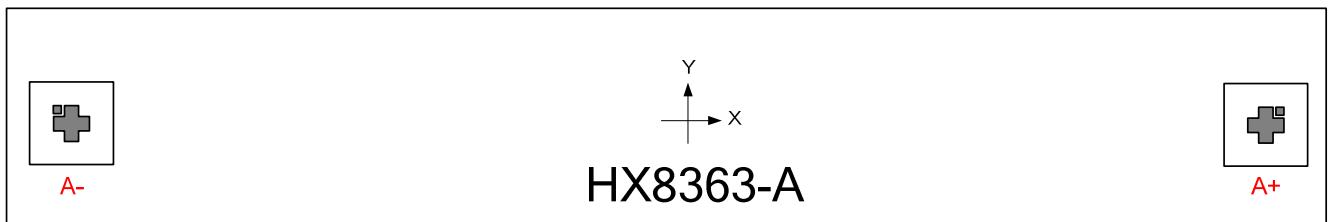
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1928	S444	-3318	285
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1932	S440	-3366	375
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1934	S438	-3390	285
1935	S437	-3402	375
1936	S436	-3414	465
1937	S435	-3426	285
1938	S434	-3438	375
1939	S433	-3450	465
1940	S432	-3462	285
1941	S431	-3474	375
1942	S430	-3486	465
1943	S429	-3498	285
1944	S428	-3510	375
1945	S427	-3522	465
1946	S426	-3534	285
1947	S425	-3546	375
1948	S424	-3558	465
1949	S423	-3570	285
1950	S422	-3582	375
1951	S421	-3594	465
1952	S420	-3606	285
1953	S419	-3618	375
1954	S418	-3630	465
1955	S417	-3642	285
1956	S416	-3654	375
1957	S415	-3666	465
1958	S414	-3678	285
1959	S413	-3690	375
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1967	S405	-3786	285
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1985	S387	-4002	285
1986	S386	-4014	375
1987	S385	-4026	465
1988	S384	-4038	285
1989	S383	-4050	375
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1991	S381	-4074	285
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1993	S379	-4098	465
1994	S378	-4110	285
1995	S377	-4122	375
1996	S376	-4134	465
1997	S375	-4146	285
1998	S374	-4158	375
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2000	S372	-4182	285
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2009	S363	-4290	285
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2012	DUMMY	-4326	285
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2142	S241	-6006	465
2143	S240	-6018	285
2144	S239	-6030	375
2145	S238	-6042	465
2146	S237	-6054	285
2147	S236	-6066	375
2148	S235	-6078	465
2149	S234	-6090	285
2150	S233	-6102	375
2151	S232	-6114	465
2152	S231	-6126	285
2153	S230	-6138	375
2154	S229	-6150	465
2155	S228	-6162	285
2156	S227	-6174	375
2157	S226	-6186	465
2158	S225	-6198	285
2159	S224	-6210	375
2160	S223	-6222	465

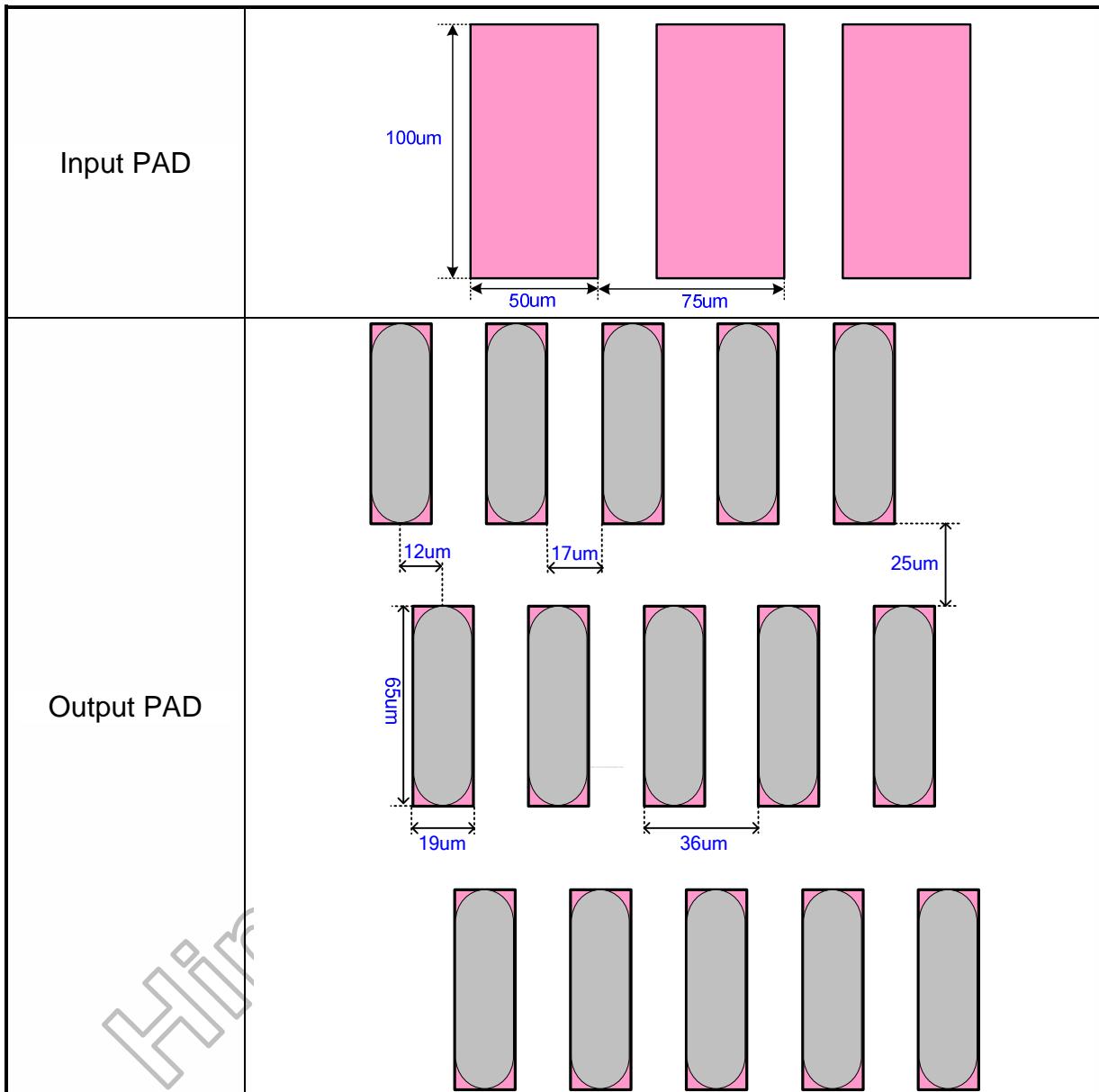
No.	Name	X	Y
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2163	S220	-6258	465
2164	S219	-6270	285
2165	S218	-6282	375
2166	S217	-6294	465
2167	S216	-6306	285
2168	S215	-6318	375
2169	S214	-6330	465
2170	S213	-6342	285
2171	S212	-6354	375
2172	S211	-6366	465
2173	S210	-6378	285
2174	S209	-6390	375
2175	S208	-6402	465
2176	S207	-6414	285
2177	S206	-6426	375
2178	S205	-6438	465
2179	S204	-6450	285
2180	S203	-6462	375
2181	S202	-6474	465
2182	S201	-6486	285
2183	S200	-6498	375
2184	S199	-6510	465
2185	S198	-6522	285
2186	S197	-6534	375
2187	S196	-6546	465
2188	S195	-6558	285
2189	S194	-6570	375
2190	S193	-6582	465
2191	S192	-6594	285
2192	S191	-6606	375
2193	S190	-6618	465
2194	S189	-6630	285
2195	S188	-6642	375
2196	S187	-6654	465
2197	S186	-6666	285
2198	S185	-6678	375
2199	S184	-6690	465
2200	S183	-6702	285
2201	S182	-6714	375
2202	S181	-6726	465
2203	S180	-6738	285
2204	S179	-6750	375
2205	S178	-6762	465
2206	S177	-6774	285
2207	S176	-6786	375
2208	S175	-6798	465
2209	S174	-6810	285
2210	S173	-6822	375
2211	S172	-6834	465
2212	S171	-6846	285
2213	S170	-6858	375
2214	S169	-6870	465
2215	S168	-6882	285
2216	S167	-6894	375
2217	S166	-6906	465
2218	S165	-6918	285
2219	S164	-6930	375
2220	S163	-6942	465
2221	S162	-6954	285
2222	S161	-6966	375
2223	S160	-6978	465
2224	S159	-6990	285
2225	S158	-7002	375
2226	S157	-7014	465
2227	S156	-7026	285
2228	S155	-7038	375
2229	S154	-7050	465
2230	S153	-7062	285
2231	S152	-7074	375
2232	S151	-7086	465
2233	S150	-7098	285
2234	S149	-7110	375
2235	S148	-7122	465
2236	S147	-7134	285
2237	S146	-7146	375
2238	S145	-7158	465
2239	S144	-7170	285
2240	S143	-7182	375
2241	S142	-7194	465
2242	S141	-7206	285
2243	S140	-7218	375
2244	S139	-7230	465
2245	S138	-7242	285
2246	S137	-7254	375
2247	S136	-7266	465
2248	S135	-7278	285
2249	S134	-7290	375
2250	S133	-7302	465
2251	S132	-7314	285
2252	S131	-7326	375
2253	S130	-7338	465
2254	S129	-7350	285
2255	S128	-7362	375
2256	S127	-7374	465
2257	S126	-7386	285
2258	S125	-7398	375
2259	S124	-7410	465
2260	S123	-7422	285
2261	S122	-7434	375
2262	S121	-7446	465
2263	S120	-7458	285
2264	S119	-7470	375
2265	S118	-7482	465
2266	S117	-7494	285
2267	S116	-7506	375
2268	S115	-7518	465
2269	S114	-7530	285
2270	S113	-7542	375
2271	S112	-7554	465
2272	S111	-7566	285
2273	S110	-7578	375
2274	S109	-7590	465
2275	S108	-7602	285
2276	S107	-7614	375
2277	S106	-7626	465
2278	S105	-7638	285
2279	S104	-7650	375
2280	S103	-7662	465
2281	S102	-7674	285
2282	S101	-7686	375
2283	S100	-7698	465
2284	S99	-7710	285
2285	S98	-7722	375
2286	S97	-7734	465
2287	S96	-7746	285
2288	S95	-7758	375
2289	S94	-7770	465
2290	S93	-7782	285
2291	S92	-7794	375
2292	S91	-7806	465
2293	S90	-7818	285
2294	S89	-7830	375
2295	S88	-7842	465
2296	S87	-7854	285
2297	S86	-7866	375
2298	S85	-7878	465
2299	S84	-7890	285
2300	S83	-7902	375
2301	S82	-7914	465
2302	S81	-7926	285
2303	S80	-7938	375
2304	S79	-7950	465
2305	S78	-7962	285
2306	S77	-7974	375
2307	S76	-7986	465
2308	S75	-7998	285
2309	S74	-8010	375
2310	S73	-8022	465
2311	S72	-8034	285
2312	S71	-8046	375
2313	S70	-8058	465
2314	S69	-8070	285
2315	S68	-8082	375
2316	S67	-8094	465
2317	S66	-8106	285
2318	S65	-8118	375
2319	S64	-8130	465
2320	S63	-8142	285
2321	S62	-8154	375
2322	S61	-8166	465
2323	S60	-8178	285
2324	S59	-8190	375
2325	S58	-8202	465
2326	S57	-8214	285
2327	S56	-8226	375
2328	S55	-8238	465
2329	S54	-8250	285
2330	S53	-8262	375
2331	S52	-8274	465
2332	S51	-8286	285
2333	S50	-8298	375
2334	S49	-8310	465
2335	S48	-8322	285
2336	S47	-8334	375
2337	S46	-8346	465
2338	S45	-8358	285
2339	S44	-8370	375
2340	S43	-8382	465
2341	S42	-8394	285
2342	S41	-8406	375
2343	S40	-8418	465
2344	S39	-8430	285
2345	S38	-8442	375
2346	S37	-8454	465
2347	S36	-8466	285
2348	S35	-8478	375
2349	S34	-8490	465
2350	S33	-8502	285
2351	S32	-8514	375
2352	S31	-8526	465
2353	S30	-8538	285
2354	S29	-8550	375
2355	S28	-8562	465
2356	S27	-8574	285
2357	S26	-8586	375
2358	S25	-8598	465
2359	S24	-8610	285
2360	S23	-8622	375
2361	S22	-8634	465
2362	S21	-8646	285
2363	S20	-8658	375
2364	S19	-8670	465
2365	S18	-8682	285
2366	S17	-8694	375
2367	S16	-8706	465
2368	S15	-8718	285
2369	S14	-8730	375
2370	S13	-8742	465
2371	S12	-8754	285
2372	S11	-8766	375
2373	S10	-8778	465
2374	S9	-8790	285
2375	S8	-8802	375
2376	S7	-8814	465
2377	S6	-8826	285
2378	S5	-8838	375
2379	S4	-8850	465
2380	S3	-8862	285
2381	S2	-8874	375
2382	S1	-8886	465
2383	DUMMY	-8898	285
2384	DUMMY	-8910	375
2385	DUMMY	-8922	465
2386	VCOM	-9090	285
2387	VCOM	-9102	375
2388	VCOM	-9114	465
2389	VCOM	-9126	285
2390	VCOM	-9138	375
2391	VCOM	-9150	465
2392	VGL	-9198	285
2393	VGL	-9210	375
2394	VGL	-9222	465
2395	G863	-9270	285
2396	G861	-9282	375
2397	G859	-9294	465
2398	G857	-9306	285
2399	G855	-9318	375
2400	G853	-9330	465

No.	Name	X	Y
2401	G851	-9342	285
2402	G849	-9354	375
2403	G847	-9366	465
2404	G845	-9378	285
2405	G843	-9390	375
2406	G841	-9402	465
2407	G839	-9414	285
2408	G837	-9426	375
2409	G835	-9438	465
2410	G833	-9450	285
2411	G831	-9462	375
2412	G829	-9474	465
2413	G827	-9486	285
2414	G825	-9498	375
2415	G823	-9510	465
2416	G821	-9522	285
2417	G819	-9534	375
2418	G817	-9546	465
2419	G815	-9558	285
2420	G813	-9570	375
2421	G811	-9582	465
2422	G809	-9594	285
2423	G807	-9606	375
2424	G805	-9618	465
2425	G803	-9630	285
2426	G801	-9642	375
2427	G799	-9654	465
2428	G797	-9666	285
2429	G795	-9678	375
2430	G793	-9690	465
2431	G791	-9702	285
2432	G789	-9714	375
2433	G787	-9726	465
2434	G785	-9738	285
2435	G783	-9750	375
2436	G781	-9762	465
2437	G779	-9774	285
2438	G777	-9786	375
2439	G775	-9798	465
2440	G773	-9810	285
2441	G771	-9822	375
2442	G769	-9834	465
2443	G767	-9846	285
2444	G765	-9858	375
2445	G763	-9870	465
2446	G761	-9882	285
2447	G759	-9894	375
2448	G757	-9906	465
2449	G755	-9918	285
2450	G753	-9930	375
2451	G751	-9942	465
2452	G749	-9954	285
2453	G747	-9966	375
2454	G745	-9978	465
2455	G743	-9990	285
2456	G741	-10002	375
2457	G739	-10014	465
2458	G737	-10026	285
2459	G735	-10038	375
2460	G733	-10050	465
2461	G731	-10062	285
2462	G729	-10074	375
2463	G727	-10086	465
2464	G725	-10098	285
2465	G723	-10110	375
2466	G721	-10122	465
2467	G719	-10134	285
2468	G717	-10146	375
2469	G715	-10158	465
2470	G713	-10170	285
2471	G711	-10182	375
2472	G709	-10194	465
2473	G707	-10206	285
2474	G705	-10218	375
2475	G703	-10230	465
2476	G701	-10242	285
2477	G699	-10254	375
2478	G697	-10266	465
2479	G695	-10278	285
2480	G693	-10290	375
2481	G691	-10302	465
2482	G689	-10314	285
2483	G687	-10326	375
2484	G685	-10338	465
2485	G683	-10350	285
2486	G681	-10362	375
2487	G679	-10374	465
2488	G677	-10386	285
2489	G675	-10398	375
2490	G673	-10410	465
2491	G671	-10422	285
2492	G669	-10434	375
2493	G667	-10446	465
2494	G665	-10458	285
2495	G663	-10470	375
2496	G661	-10482	465
2497	G659	-10494	285
2498	G657	-10506	375
2499	G655	-10518	465
2500	G653	-10530	285
2501	G651	-10542	375
2502	G649	-10554	465
2503	G647	-10566	285
2504	G645	-10578	375
2505	G643	-10590	465
2506	G641	-10602	285
2507	G639	-10614	375
2508	G637	-10626	465
2509	G635	-10638	285
2510	G633	-10650	375
2511	G631	-10662	465
2512	G629	-10674	285
2513	G627	-10686	375
2514	G625	-10698	465
2515	G623	-10710	285
2516	G621	-10722	375
2517	G619	-10734	465
2518	G617	-10746	285
2519	G615	-10758	375
2520	G613	-10770	465
2521	G611	-10782	285
2522	G609	-10794	375
2523	G607	-10806	465
2524	G605	-10818	285
2525	G603	-10830	375
2526	G601	-10842	465
2527	G599	-10854	285
2528	G597	-10866	375
2529	G595	-10878	465
2530	G593	-10890	285
2531	G591	-10902	375
2532	G589	-10914	465
2533	G587	-10926	285
2534	G585	-10938	375
2535	G583	-10950	465
2536	G581	-10962	285
2537	G579	-10974	375
2538	G577	-10986	465
2539	G575	-10998	285
2540	G573	-11010	375
2541	G571	-11022	465
2542	G569	-11034	285
2543	G567	-11046	375
2544	G565	-11058	465
2545	G563	-11070	285
2546	G561	-11082	375
2547	G559	-11094	465
2548	G557	-11106	285
2549	G555	-11118	375
2550	G553	-11130	465
2551	G551	-11142	285
2552	G549	-11154	375
2553	G547	-11166	465
2554	G545	-11178	285
2555	G543	-11190	375
2556	G541	-11202	465
2557	G539	-11214	285
2558	G537	-11226	375
2559	G535	-11238	465
2560	G533	-11250	285
2561	G531	-11262	375
2562	G529	-11274	465
2563	G527	-11286	285
2564	G525	-11298	375
2565	G523	-11310	465
2566	G521	-11322	285
2567	G519	-11334	375
2568	G517	-11346	465
2569	G515	-11358	285
2570	G513	-11370	375
2571	G511	-11382	465
2572	G509	-11394	285
2573	G507	-11406	375
2574	G505	-11418	465
2575	G503	-11430	285
2576	G501	-11442	375
2577	G499	-11454	465
2578	G497	-11466	285
2579	G495	-11478	375
2580	G493	-11490	465

Alignment mark	X	Y
A+	11890	0
A-	-11890	0

3.4.1 Bump Arrangement



Bump thickness: 12 +/- 3 μ m

4. Interface

4.1 System Interface

The HX8363-A supports 3-wire serial peripheral interface and RGB interface and MIPI DSI interface. Serial peripheral interface is always effective and it can be used to access internal command and parameter. The RGB interface is only used to access display data and display directly via source output. MIPI DSI can access both internal command and display data.

BS1	BS0	interface mode	DB pins
0	0	3 wire serial + RGB interface (SCL Rising edge)	RGB:16/18/24 bit
0	1	DSI command mode	DSI_CP, DSI_CN, DSI_D0P, DSI_D0N, DSI_D1P, DSI_D1N
1	0	Reserve	-
1	1	Reserve	-

Table 4.1: Interface selection

4.1.1 Serial Data Transfer Interface

The HX8363-A supports 3 wire serial data transfer interface. The 3 wire serial bus uses chip select line (NCS), serial input/output data SDI/SDO and the serial transfer clock line SCL).

Serial data write mode

The 3-Pin serial data packet contains a control bit DNC and a transmission byte. If DNC is low, the transmission byte is command byte. If DNC is high, the transmission byte is stored to command register. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, SCL clock pulse or SDI/SDO data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

3 wire Serial Data Stream Format

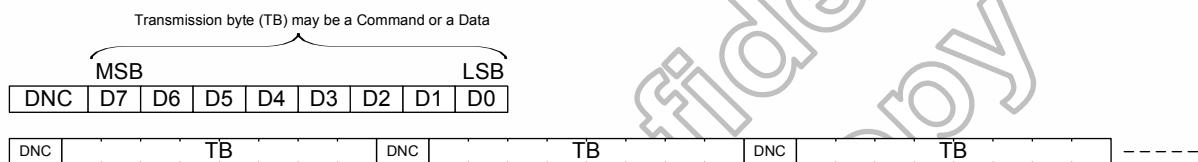
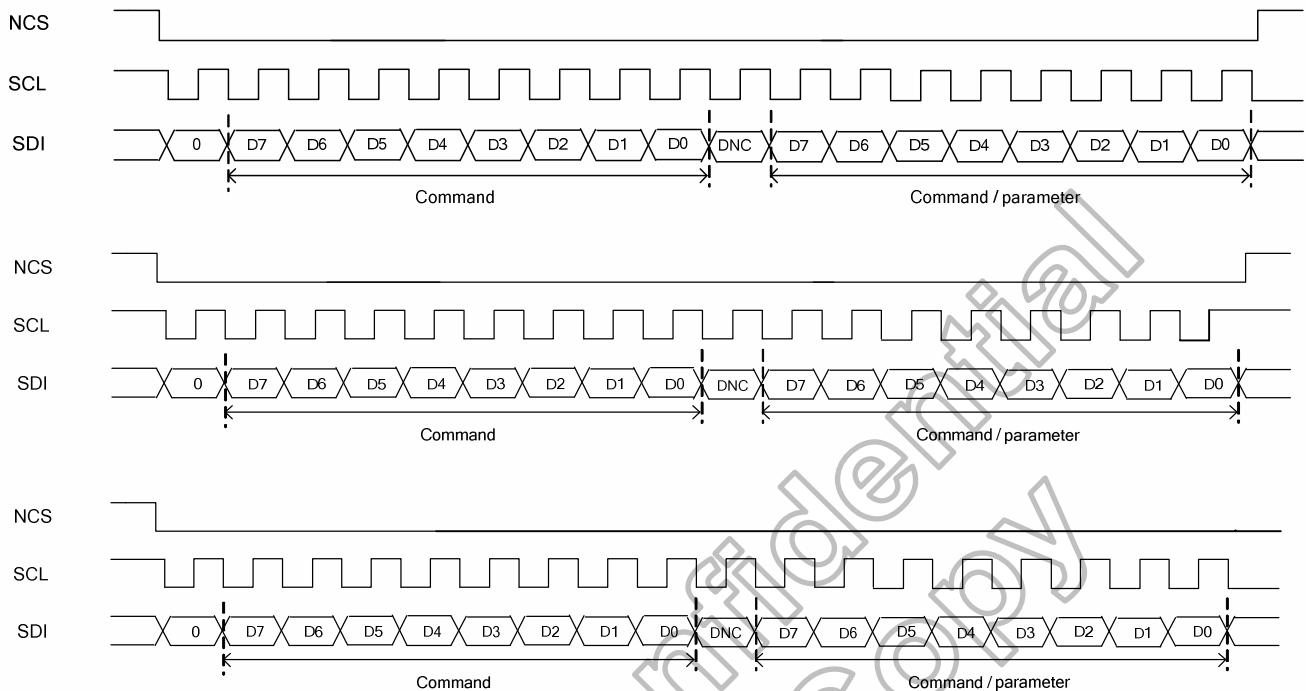


Figure 4.1: Serial Data stream, write mode

3 wire Serial Interface Protocol

**Figure 4.2: Serial Interface protocol 3 wire serial interface (write mode)**

Serial Data Read Mode

The micro controller firstly has to send a command and then the following byte is transmitted in the opposite direction. The read mode has three types of command data transmitted (8-/24-/32-bit) according command code.

3 wire Serial Interface Protocol

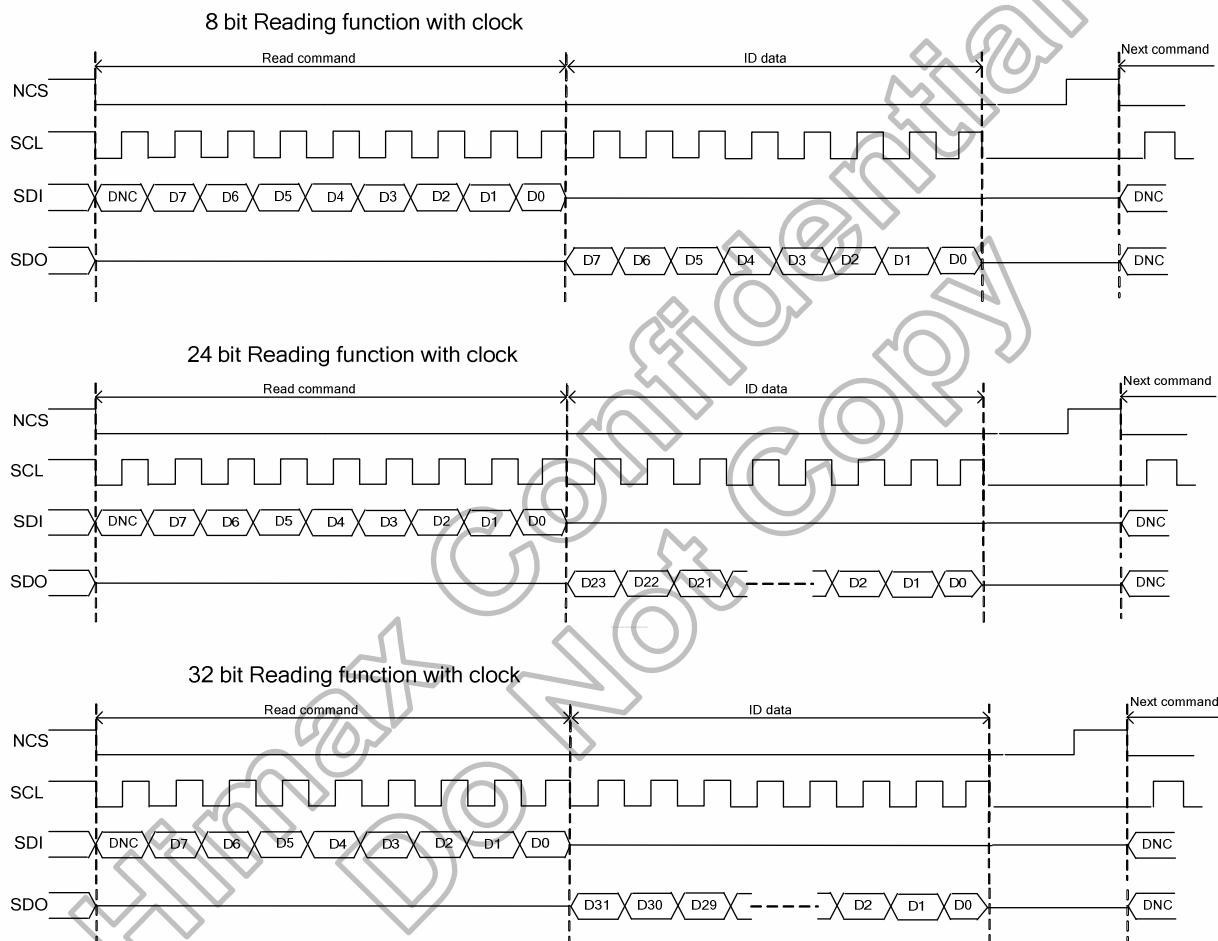
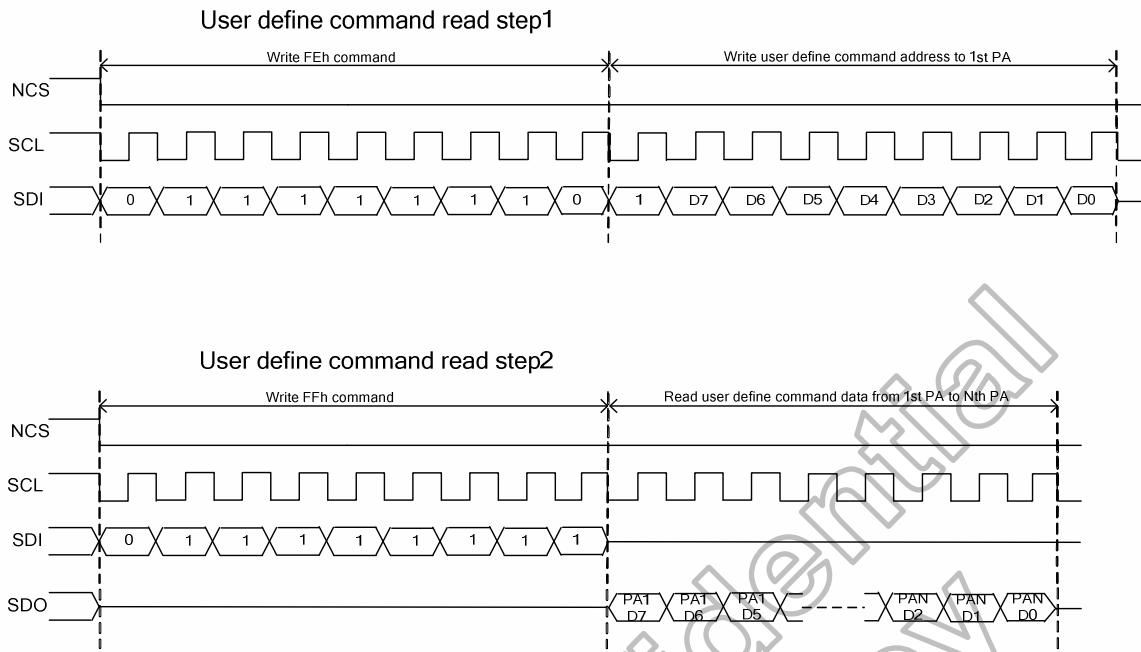
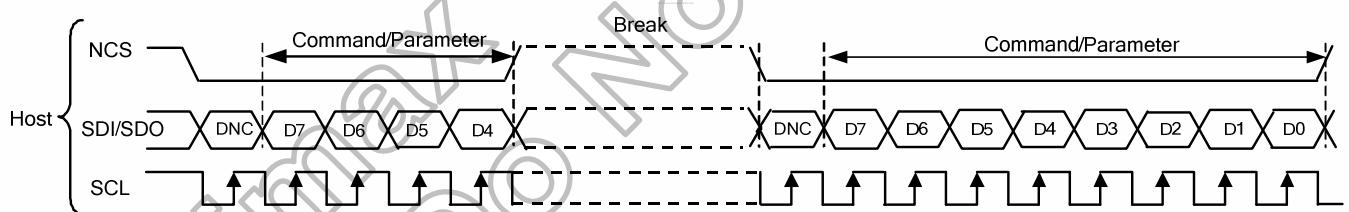


Figure 4.3 : 3 wire Serial Interface protocol, read mode

**Figure 4.4: 3 wire Serial Interface protocol, read mode for user define command**

If there is a break on data transmission when transmitting a command before a whole byte has been completed, then the display module will reset the interface so that it will be ready to receive the same byte re-transmitted when the chip select line (NCS) is next activated. See the following figure.

**Figure 4.5: Display Module Data Transfer Recovery**

4.2 RGB Interface

The HX8363-A supports RGB interface that is used 3 wire serial data transfer interface to transmit/receive command.

The HX8363-A uses 16, 18 or 24-bit parallel RGB interface which includes: HSYNC, VSYNC, ENABLE, DCK, DB[23...0] –lines. The interface is active after Power On sequence. Pixel clock (DCK) runs all the time without stopping and it is used to enter HSYNC, VSYNC, ENABLE and DB[23...0] –lines states when there is a rising edge of the DCK. The DCK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is negative ('-, '0', low) active and its state is read to the display module by a rising edge of the DCK-line. Horizontal synchronization (HSYNC) is used to tell when a new line of the frame is received. This is negative ('-, '0', low) active and its state is read to the display module by a rising edge of the DCK-line. Data enable (ENABLE) is used to tell when there is received RGB information that should be transferred on the display. This is positive ('+', '1', high) active and its state is read to the display module by a rising edge of the DCK-line. DB[23...0] (24 bit: R7-R0, G7-G0 and B7-B0; 18 bit: R5-R0, G5-G0 and B5-B0; 16 bit: R4- R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (when ENABLE =1 and there is a rising edge of DCK). DB[23...0] – lines can be set to "0" (low) or "1" (high). These lines are read by a rising edge of the DCK-line.

The pixel clock cycle is described in the following figure.

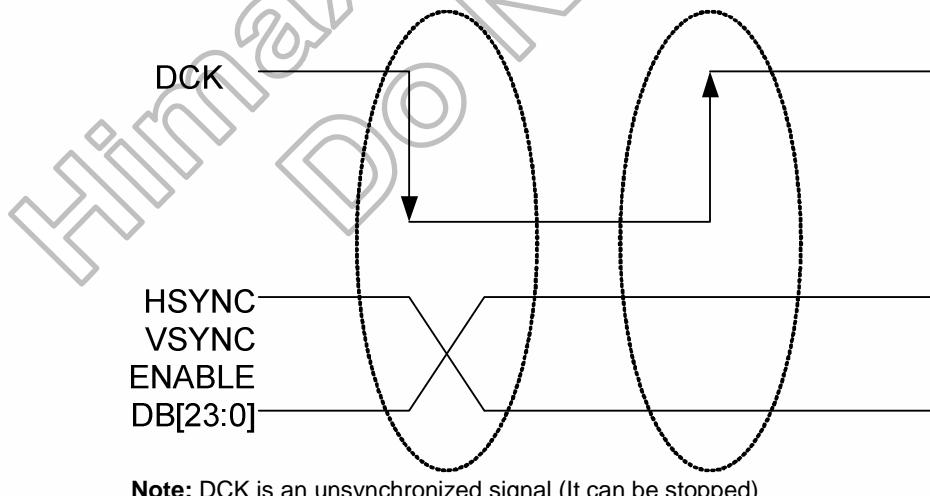
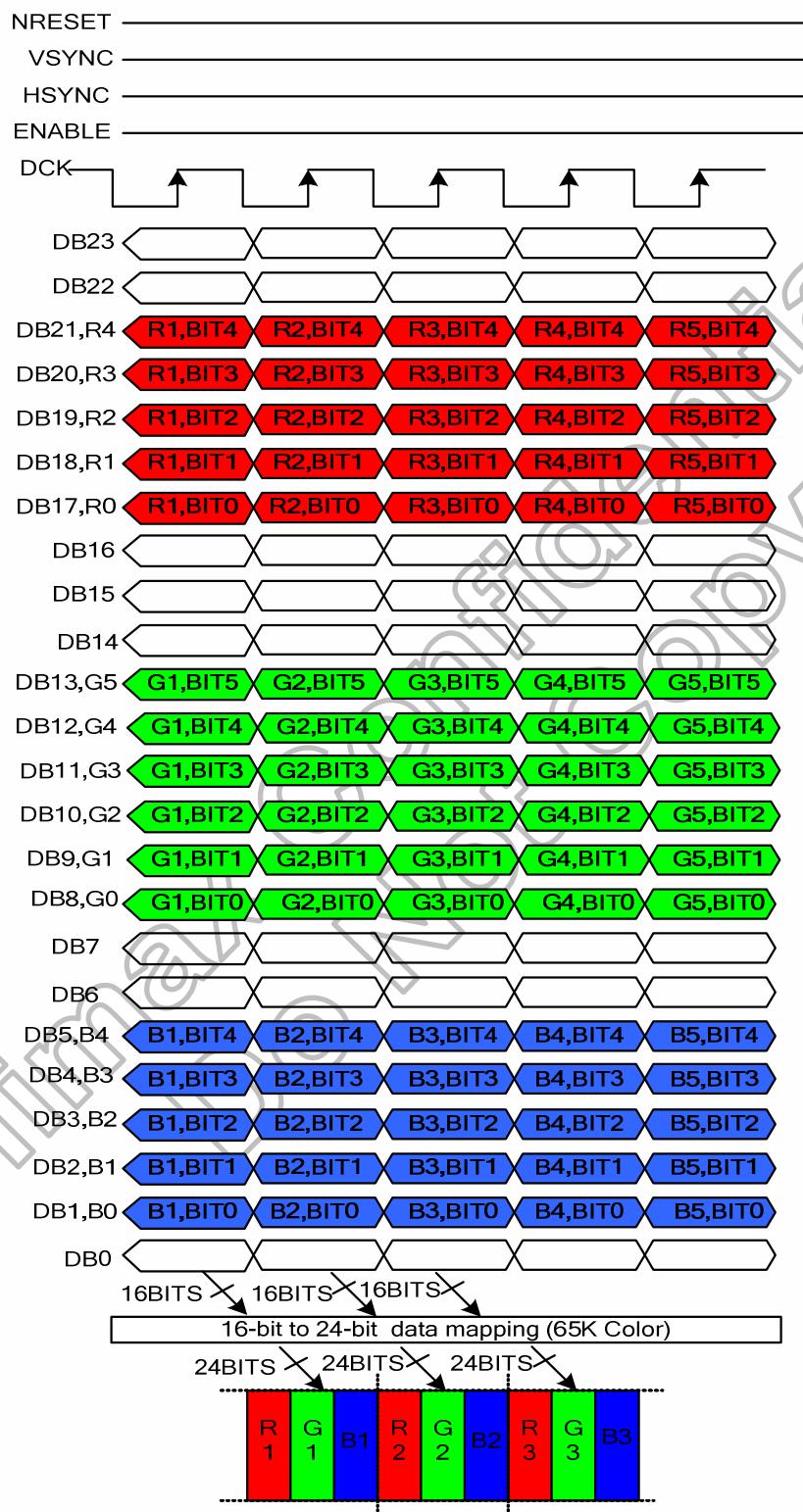


Figure 4.6: DCK cycle

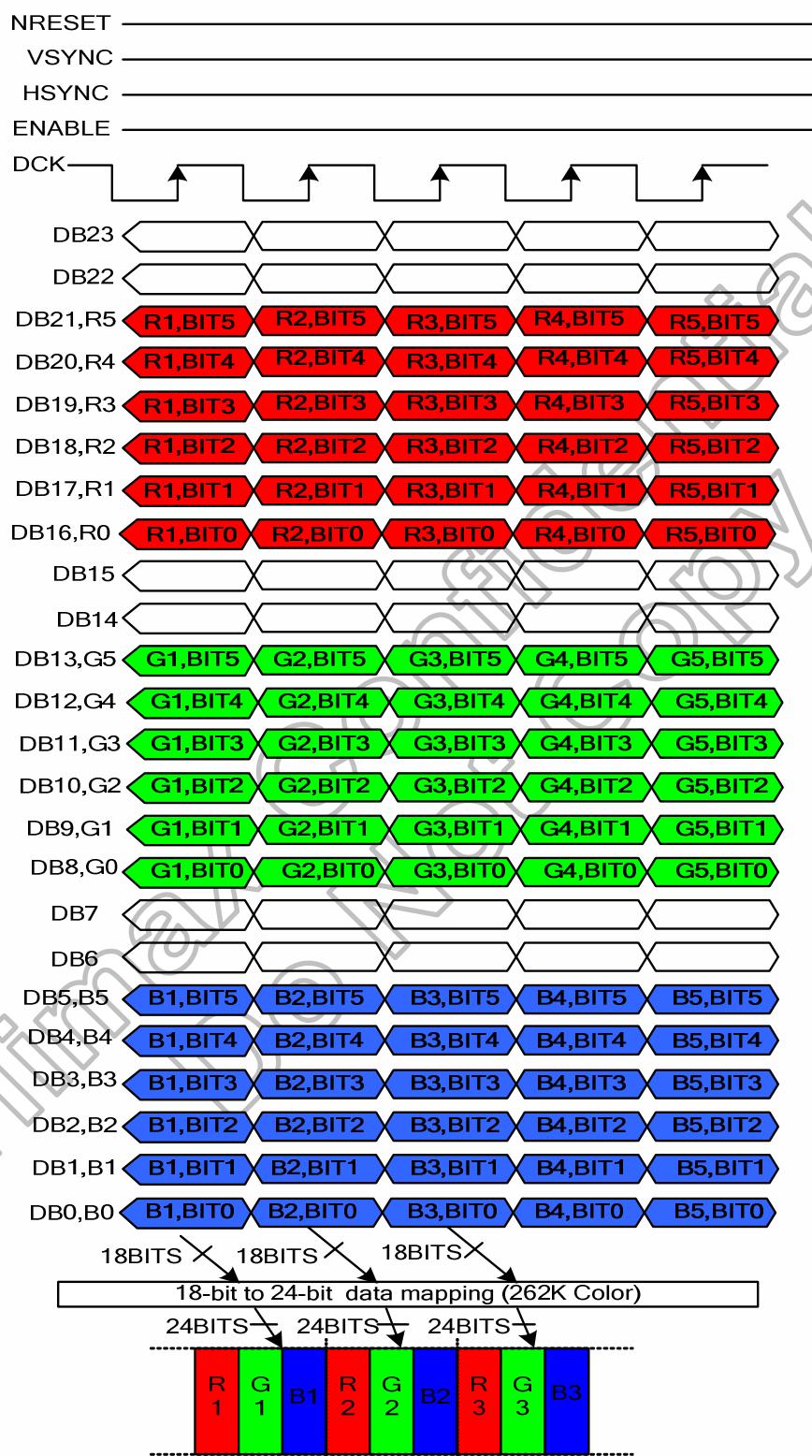
16 bit/pixel Color Order on the RGB I/F



Note: The Data order is shown as follows, MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit5, LSB = Bit0 for Green data and MSB = Bit4, LSB = Bit0 for Red and Blue data. DB23, DB22, DB16, DB14, DB7, DB6 and DB0 are opened.

Figure 4.7: 16 bit/pixel Color Order on the RGB I/F

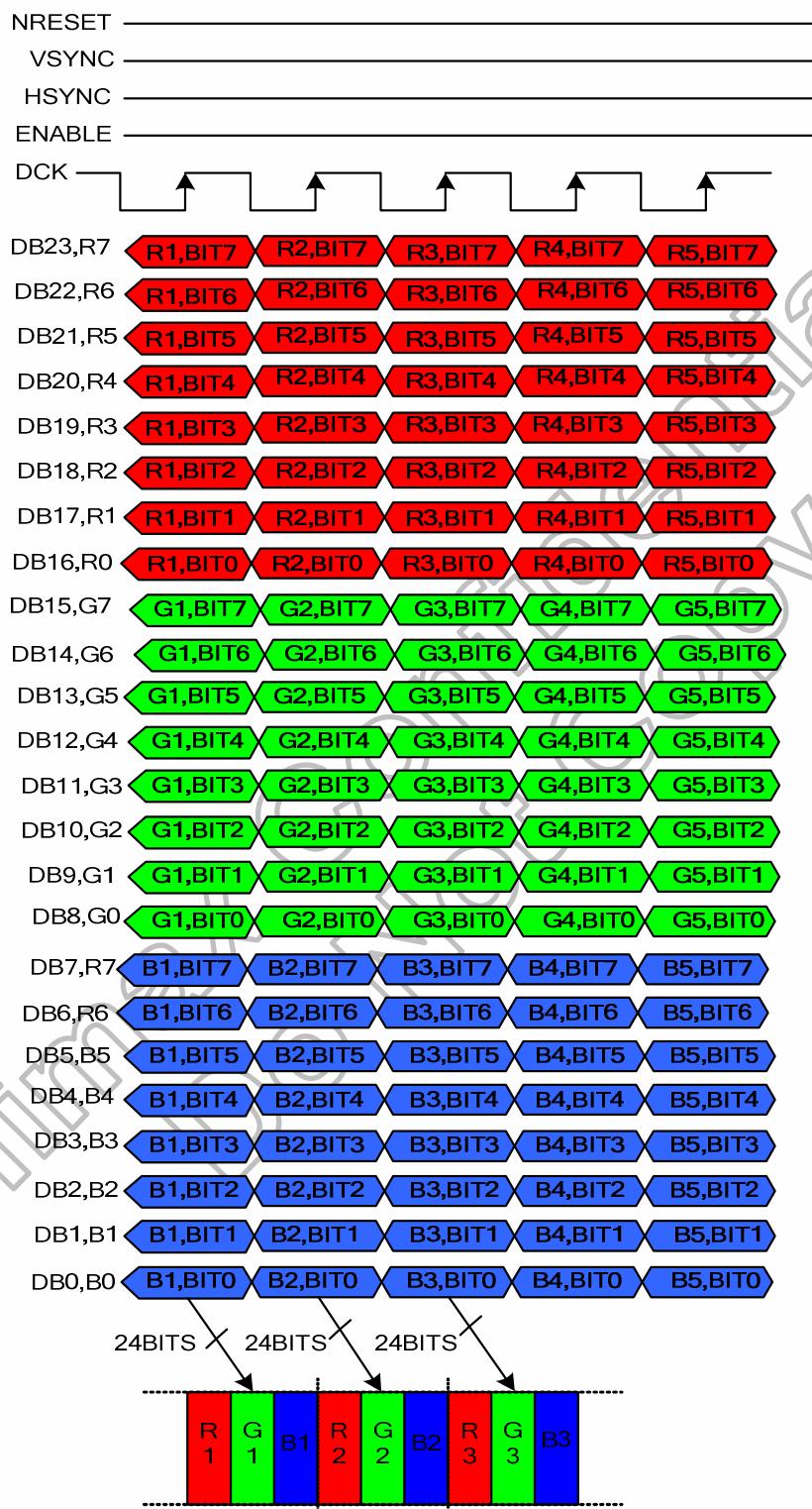
18 bit/pixel Color Order on the RGB I/F



Note: The Data order is shown as follows, MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data. DB23, DB22, DB15, DB14, DB7 and DB6 are opened.

Figure 4.8: 18 bit/pixel Color Order on the RGB I/F

24 bit/pixel Color Order on the RGB I/F



Note: The Data order is shown as follows, MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit7, LSB = Bit0 for Red, Green and Blue data.

Figure 4.9: 24bit/pixel Color Order on the RGB I/F

General Timing Diagram

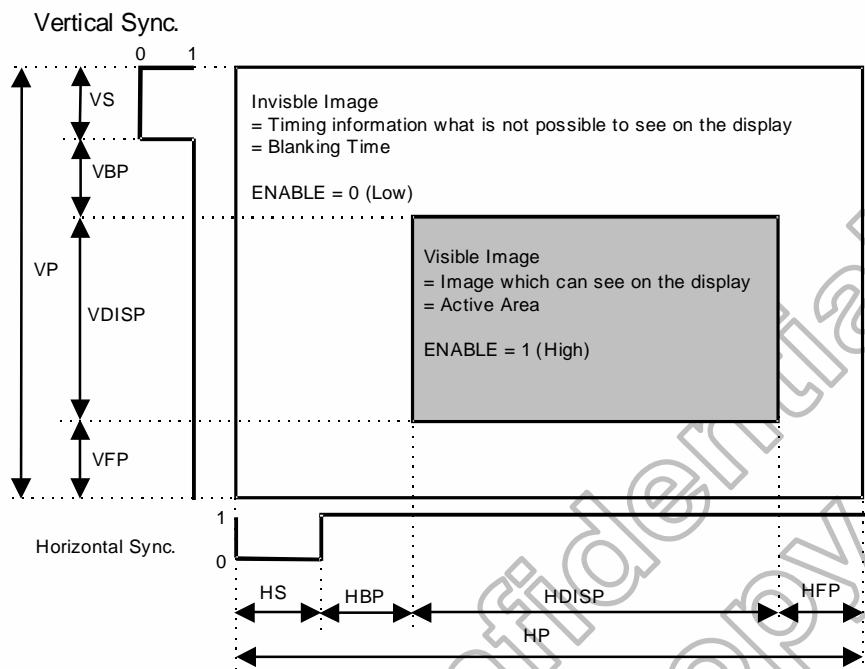


Figure 4.10: General Timing Diagram

The image information must be correct on the display, when the timings are in range on the interface. However, the image information might be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

4.3 DSI Protocol

The Protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data,

signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Figure 4.11 illustrates multiple HS Transmission packets.

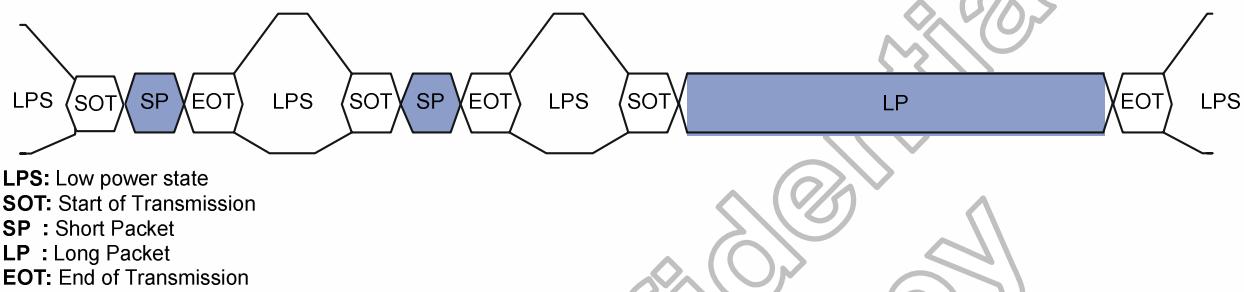
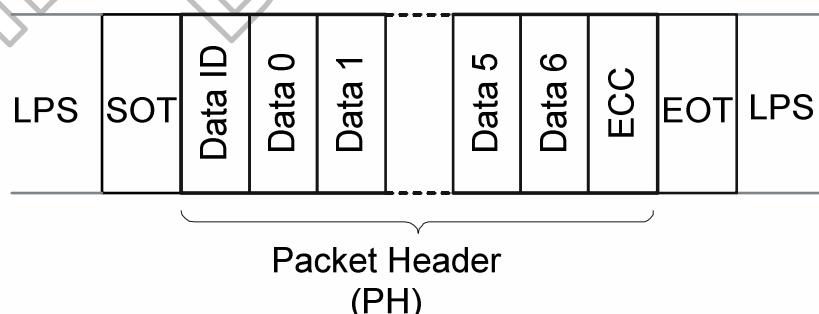


Figure 4.11: Multiple HS Transmission packets

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Short packets specify the payload length using the Data Type field and are from two to nine bytes in length. Short packet is used for most Command Mode commands and associated parameters.

Where short packets format include an 8-bit Data ID followed by zero to seven bytes and an 8-bit ECC. Figure 4.12 shows the structure of the Short packet.



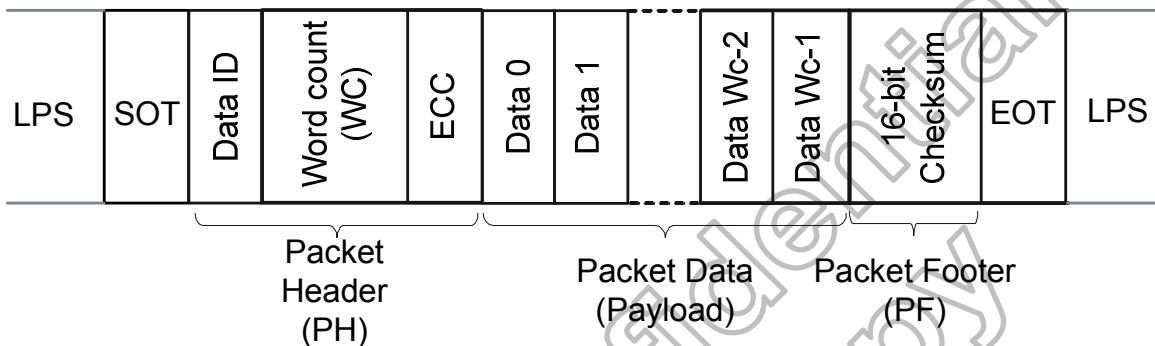
DI(Data ID): Contain Virtual Channel Identifier and Data Type.

ECC(Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet He

Figure 4.12: Structure of the Short packet

Long packets specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Figure 4.13 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where 65,541 bytes = $(2^{16}-1) + 4 \text{ bytes PH} + 2 \text{ bytes PF}$



DI (Data ID): Contain Virtual Channel Identifier and Data Type.

WC (Word Count): The receiver use WC to define packet end.

ECC (Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

PF(Packet Footer): Mean 16-bit Checksum.

Figure 4.13: Structure of the Long packet

According to packet form, basic elements include DI and ECC. Figure 5.34 the shows format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		DT (Data Type)					

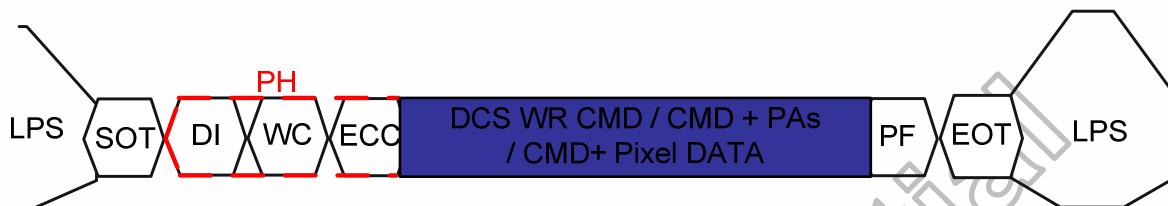
DI[7:6]: These two bits identify the data as directed to one of four virtual channels.

DI[5:0]: These six bits specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

Figure 4.14: The format of Data ID

Due to Data Type (DT) mean format of transmission type, Figure 4.15 show Short- / Long- packet transmission command sequence.

Long packet writes Command / Parameters / Pixel Data



DI: Write suitable Data type.

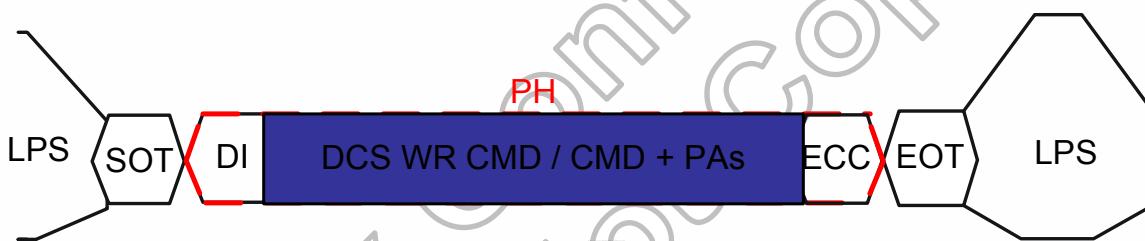
WC: Write number of Payload Data.

Ex: One CMD write, WC setting as 1.

CMD + PAs write, WC setting as number of (CMD+PAs).

CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

Short packet writes Command / Parameters



DI: Write suitable Data type.

Ex: One CMD write, DI + DCS WR CMD

CMD + PAs write, DI + DCS WR CMD + PAs

Figure 4.15: Short- / Long- packet transmission command sequence

4.3.1 Processor to peripheral Direction packets Data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 4.2 Data Types for Processor-sourced Packets.

Data Type, Hex	Data Type, Binary	Description Packet	Size
01h	00 0001	Sync Event, VSync Start	Short
11h	01 0001	Sync Event, VSync End	Short
21h	10 0001	Sync Event, HSync Start	Short
31h	11 0001	Sync Event, HSync End	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format <i>(This project is not use)</i>	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Table 4.2: Data Types for Processor-sourced Packets

Under tables list all detail function of all data types

Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)		
Data Type, Hex	Function Description	Number of bytes
01h	V Sync start, Start of VSA pulse.	2 bytes (DI + ECC)
11h	V Sync End, End of VSA pulse.	
21h	H Sync Start, Start of HSA pulse.	
31h	H Sync End, End of HSA pulse.	

Note: (1) VSync Start and VSync End event represents the start and end of the VSA, respectively. Similarly HSync Start and HSync End event represents the start and end of the HSA, respectively.

Display Status (Shutdown Command, Turn-On command)		
Data Type, Hex	Function Description	Number of bytes
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	2 bytes (DI + ECC)
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	

Note: (1) When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.

DCS Command Setting		
Data Type, Hex	Function Description	Number of bytes
06h	DCS Read command, the returned data may be of Short or Long packet format.	3 bytes (DI + DCS CMD. + ECC)
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

Note: (1) For write part, If DCS Short Write command, followed by BTA, the peripheral shall respond with **ACK** when without error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with **Acknowledge with Error Report**.

(2) When use DCS Read Command, the **Set Max Return Packet Size** command will limit the size of returning packets.

(3) The peripheral shall respond to DCS Read Command Request in one of the following ways:

- ◆ If an error was detected by the peripheral, it shall send **Acknowledge with Error Report**. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- ◆ If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.

(4) One byte <= Length of payload DATA <= $2^{WC}-1$

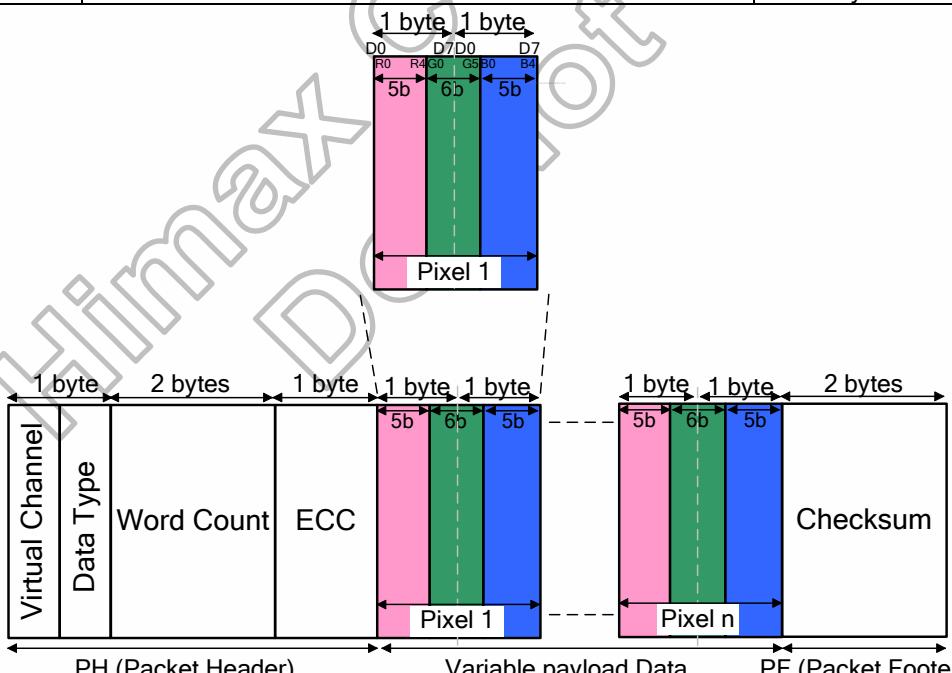
Return Packet Size setting		
Data Type, Hex	Function Description	Number of bytes
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes (DI + WC + ECC)

Note: (1) The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.

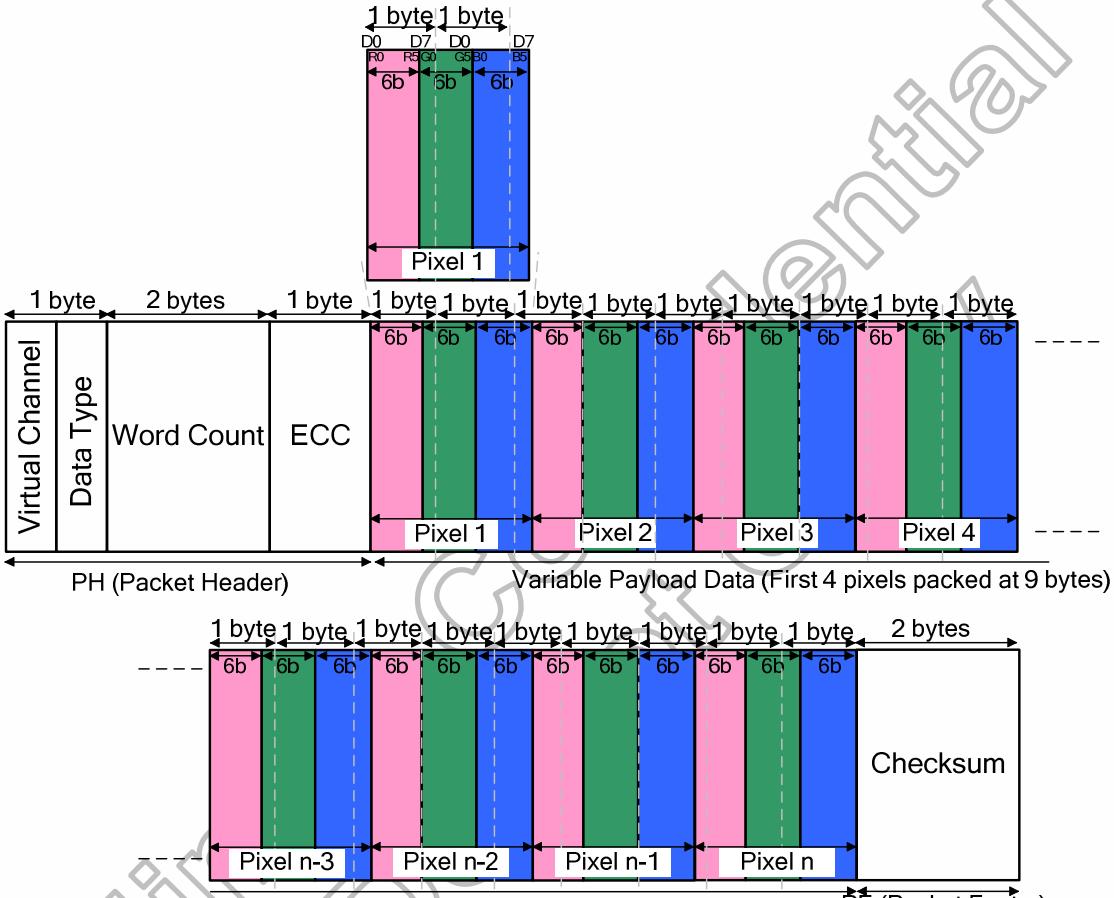
Variable Data Packet		
Data Type, Hex	Function Description	Number of bytes
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
19h	Blanking packet is used to convey blanking timing information in a Long packet.	

Note: (1) When **Null Packet**, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data.

(2) When **Blanking packet**, the packet represents a period between active scan lines of a Video Mode display.

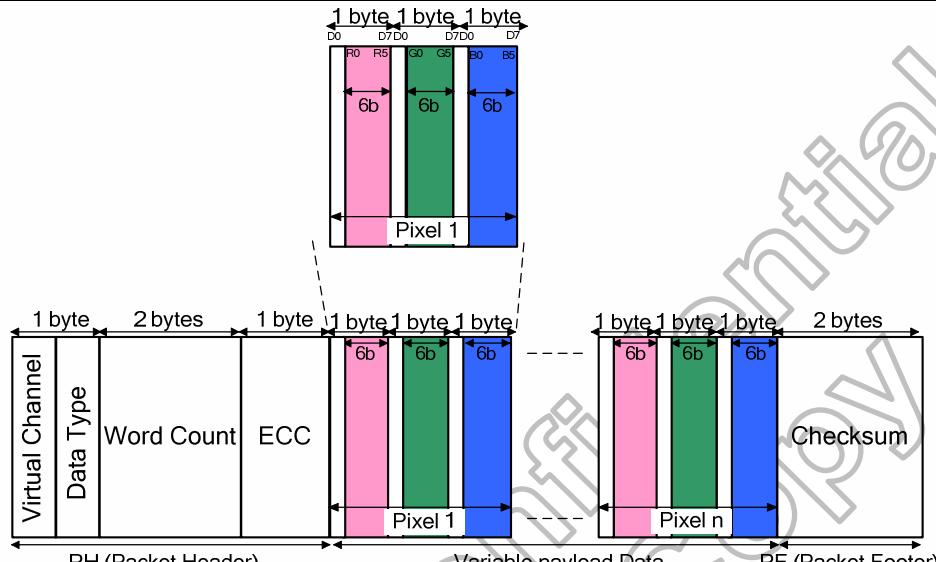
Data Stream Format		
Data Type, Hex	Function Description	Number of bytes
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "(5 bits) red, (6 bits) green and (5 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
		

Note: (1) Within a color component, the "LSB is sent first, the MSB last".

Data Stream Format		
Data Type, Hex	Function Description	Number of bytes
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is “(6 bits) red, (6 bits) green and (6 bits) blue”.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
		

Note: (1) Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a “clean start” for the next line.

Data Stream Format		
Data Type, Hex	Function Description	Number of bytes
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is "(6 bits) red, (6 bits) green and (6 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



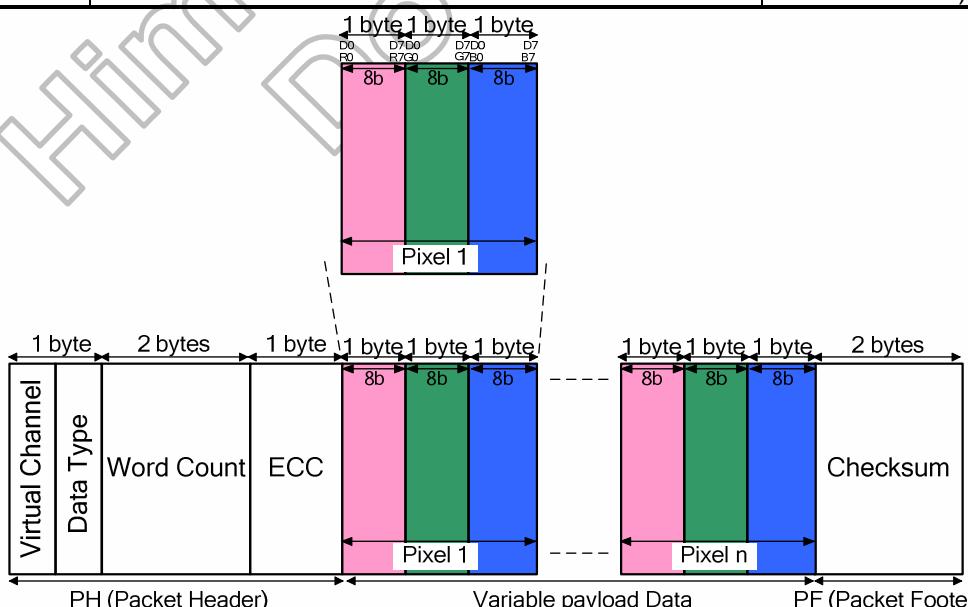
Pixel Structure: Shows a pixel divided into three 6-bit components: Red (R5 to R0), Green (G5 to G0), and Blue (B5 to B0). Bit ranges [7:2] are valid, while [1:0] are ignored.

Packet Structure:

- PH (Packet Header):** Contains Virtual Channel (1 byte), Data Type (2 bytes), Word Count (1 byte), and ECC (1 byte).
- Variable payload Data:** Contains multiple pixels. Each pixel is 18 bits long (3 bytes). It includes a "Pixel 1" example and a general "Pixel n" structure.
- PF (Packet Footer):** Contains a Checksum (2 bytes).

Note: (1) Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Packed Pixel Stream, 24bit Format		
Data Type, Hex	Function Description	Number of bytes
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



Pixel Structure: Shows a pixel divided into three 8-bit components: Red (R7 to R0), Green (G7 to G0), and Blue (B7 to B0).

Packet Structure:

- PH (Packet Header):** Contains Virtual Channel (1 byte), Data Type (2 bytes), Word Count (1 byte), and ECC (1 byte).
- Variable payload Data:** Contains multiple pixels. Each pixel is 24 bits long (3 bytes). It includes a "Pixel 1" example and a general "Pixel n" structure.
- PF (Packet Footer):** Contains a Checksum (2 bytes).

Note: (1) Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

4.3.2 Peripheral to Processor (Reverse Direction)

All Command Mode systems require bidirectional capability for returning READ data, ACK or error information to the host processor. Command Mode that use DCS shall have a bidirectional data path. Short packets and the header of Long packets may use ECC and Checksum to provide a higher level of data integrity. The Checksum feature enables detection of errors in the payload of Long packets. The packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction.

In general, if the host processor completes a transmission to the peripheral with **BTA** asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If **BTA** is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or other error information back to the host processor.

The processor-to-peripheral transactions with **BTA** asserted, can contain under form.

- A. Following a **non-Read command** in which no error was detected, the peripheral shall respond with Acknowledge.
- B. Following a **Read request** in which no error was detected, the peripheral shall send the requested READ data.
- C. Following a **Read request in which the ECC error** was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
- D. Following a **non-Read command in which the ECC error** was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report) packet, the Error Report shall have the ECC Error flag set.
- E. Following any command in which **SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid** was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

Which,

- A. "Acknowledge" includes 2 bytes which are DI (VC + Acknowledge Data Type) and ECC.
- B. "Acknowledge with Error Report" include 4 bytes which are DI, 2 bytes Error report and ECC.
- C. "Response to Read Request" contains 2 types which are Short packet and long packet.

An error report is comprised of two bytes following the DI byte, with an ECC byte following the error report bytes. Table 4.3 shows the Error Report Bit Definitions.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	reserved
3	Escape Mode Entry Command Error
4	reserved
5	reserved
6	reserved
7	reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	reserved
11	reserved
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

Table 4.3: Error Report Bit Definitions

Data Type, Hex	Data Type, Binary	Description Packet	Size
02h	00 0010	Acknowledge with Error Report	Short
1Ch	01 1100	DCS Long READ Response	Long

Table 4.4: The complete set of peripheral-to-processor Data Types

Acknowledge types		
Data Type, Hex	Function Description	Number of bytes
02	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes (DI + Error report + ECC)

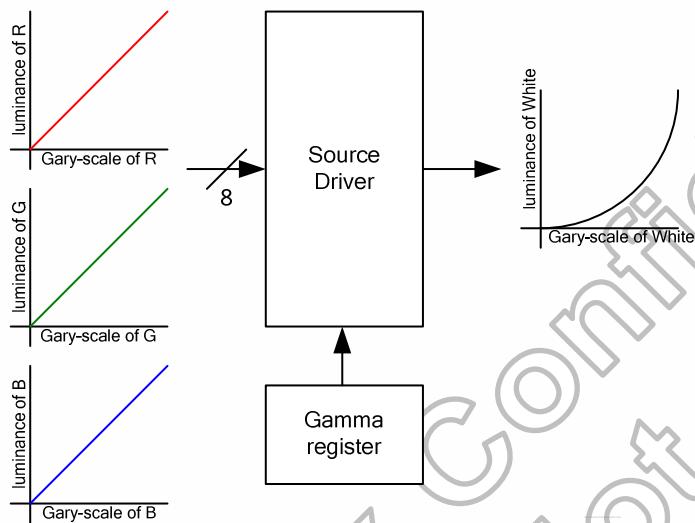
DCS Command Read types		
Data Type, Hex	Function Description	Number of bytes
1Ch	This is the long-packet response to DCS Read Request.	Up to 9 bytes (DI + Data0 ~ Data6 + ECC)

5. Function Description

5.1 Gamma characteristic correction function

The HX8363-A offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is select by internal register DGC_EN bit.

A) Gamma adjustment of Source Driver



B) Gamma adjustment of Digital Gamma Correction

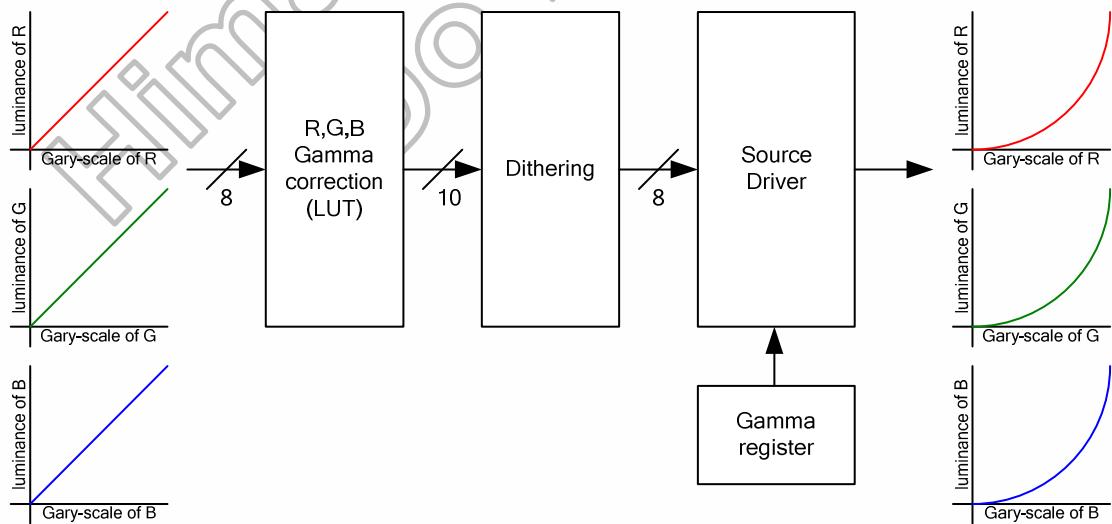
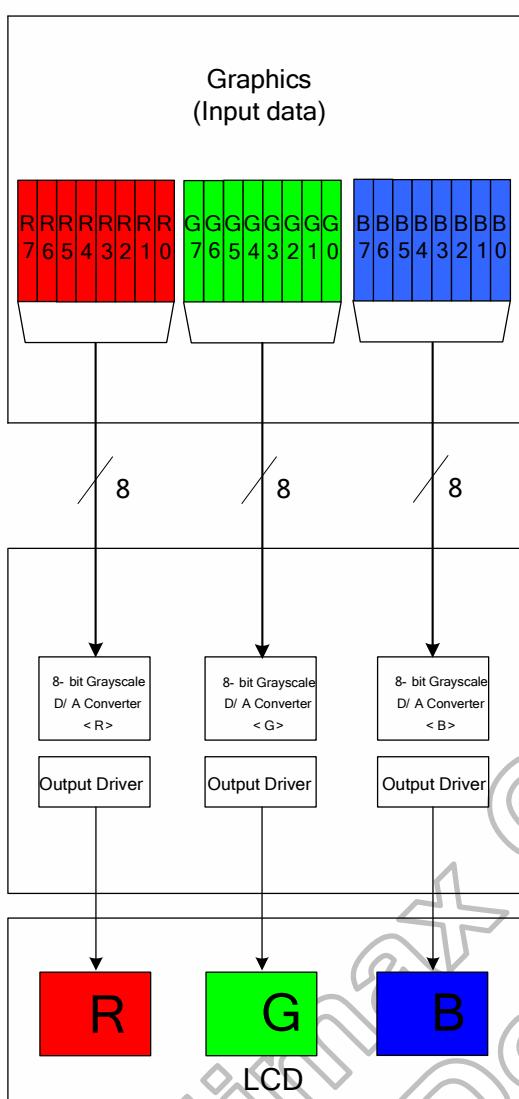


Figure 5.1: Gamma adjustments different of source driver with digital gamma correction

5.2 Gamma Characteristic Correction Function

The HX8363-A incorporates gamma adjustment function for the 16,777,216-color display. Gamma adjustment operation is implemented by deciding the 17 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 512 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

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Positive Polarity Register				
CGP5 ₀₀	CGP4 ₀₀	CGP3 ₀₁	CGP3 ₀₀	CGP2 ₀₁
VRP ₀₅	VRP ₀₄	VRP ₀₃	VRP ₀₂	VRP ₀₁
VRP ₁₅	VRP ₁₄	VRP ₁₃	VRP ₁₂	VRP ₁₁
VRP ₂₅	VRP ₂₄	VRP ₂₃	VRP ₂₂	VRP ₂₁
VRP ₃₅	VRP ₃₄	VRP ₃₃	VRP ₃₂	VRP ₃₁
VRP ₄₅	VRP ₄₄	VRP ₄₃	VRP ₄₂	VRP ₄₁
VRP ₅₅	VRP ₅₄	VRP ₅₃	VRP ₅₂	VRP ₅₁
PRP ₀₆	PRP ₀₅	PRP ₀₄	PRP ₀₃	PRP ₀₂
PRP ₁₆	PRP ₁₅	PRP ₁₄	PRP ₁₃	PRP ₁₂
PKP ₀₄	PKP ₀₃	PKP ₀₂	PKP ₀₁	PKP ₀₀
PKP ₁₄	PKP ₁₃	PKP ₁₂	PKP ₁₁	PKP ₁₀
PKP ₂₄	PKP ₂₃	PKP ₂₂	PKP ₂₁	PKP ₂₀
PKP ₃₄	PKP ₃₃	PKP ₃₂	PKP ₃₁	PKP ₃₀
PKP ₄₄	PKP ₄₃	PKP ₄₂	PKP ₄₁	PKP ₄₀
PKP ₅₄	PKP ₅₃	PKP ₅₂	PKP ₅₁	PKP ₅₀
PKP ₆₄	PKP ₆₃	PKP ₆₂	PKP ₆₁	PKP ₆₀
PKP ₇₄	PKP ₇₃	PKP ₇₂	PKP ₇₁	PKP ₇₀
PKP ₈₄	PKP ₈₃	PKP ₈₁	PKP ₈₁	PKP ₈₀

Negative Polarity Register				
CGN5 ₀₀	CGN4 ₀₀	CGN3 ₀₁	CGN3 ₀₀	CGN2 ₀₁
VRN ₀₅	VRN ₀₄	VRN ₀₃	VRN ₀₂	VRN ₀₁
VRN ₁₅	VRN ₁₄	VRN ₁₃	VRN ₁₂	VRN ₁₁
VRN ₂₅	VRN ₂₄	VRN ₂₃	VRN ₂₂	VRN ₂₁
VRN ₃₅	VRN ₃₄	VRN ₃₃	VRN ₃₂	VRN ₃₁
VRN ₄₅	VRN ₄₄	VRN ₄₃	VRN ₄₂	VRN ₄₁
VRN ₅₅	VRN ₅₄	VRN ₅₃	VRN ₅₂	VRN ₅₁
PRN ₀₆	PRN ₀₅	PRN ₀₄	PRN ₀₃	PRN ₀₂
PRN ₁₆	PRN ₁₅	PRN ₁₄	PRN ₁₃	PRN ₁₂
PKN ₀₄	PKN ₀₃	PKN ₀₂	PKN ₀₁	PKN ₀₀
PKN ₁₄	PKN ₁₃	PKN ₁₂	PKN ₁₁	PKN ₁₀
PKN ₂₄	PKN ₂₃	PKN ₂₂	PKN ₂₁	PKN ₂₀
PKN ₃₄	PKN ₃₃	PKN ₃₂	PKN ₃₁	PKN ₃₀
PKN ₄₄	PKN ₄₃	PKN ₄₂	PKN ₄₁	PKN ₄₀
PKN ₅₄	PKN ₅₃	PKN ₅₂	PKN ₅₁	PKN ₅₀
PKN ₆₄	PKN ₆₃	PKN ₆₂	PKN ₆₁	PKN ₆₀
PKN ₇₄	PKN ₇₃	PKN ₇₂	PKN ₇₁	PKN ₇₀
PKN ₈₄	PKN ₈₃	PKN ₈₁	PKN ₈₁	PKN ₈₀

Figure 5.2: Grayscale Control

Gamma-Characteristics Adjustment Register

This HX8363-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

(1) Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resistors in the top and bottom of the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(2) Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 88 to 1 selector in the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(3) Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output (Vg(P/N)3, 7, 19, 25, 32, 38, 44, 56, 60).

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor (PRP/N1) for center adjustment
	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)
	PKP7 4-0	PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)
Macro Adjustment	PKP8 4-0	PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)
	VRP0 5-0	VRN0 5-0	Variable resistor (VRP/N0) for offset adjustment
	VRP1 5-0	VRN1 5-0	Variable resistor (VRP/N1) for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor (VRP/N2) for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor (VRP/N3) for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor (VRP/N4) for offset adjustment
Offset Adjustment	VRP5 5-0	VRN5 5-0	Variable resistor (VRP/N5) for offset adjustment

Table 5.1: Gamma-Adjustment Registers

Gamma Register Stream and 8 to 1 Selector

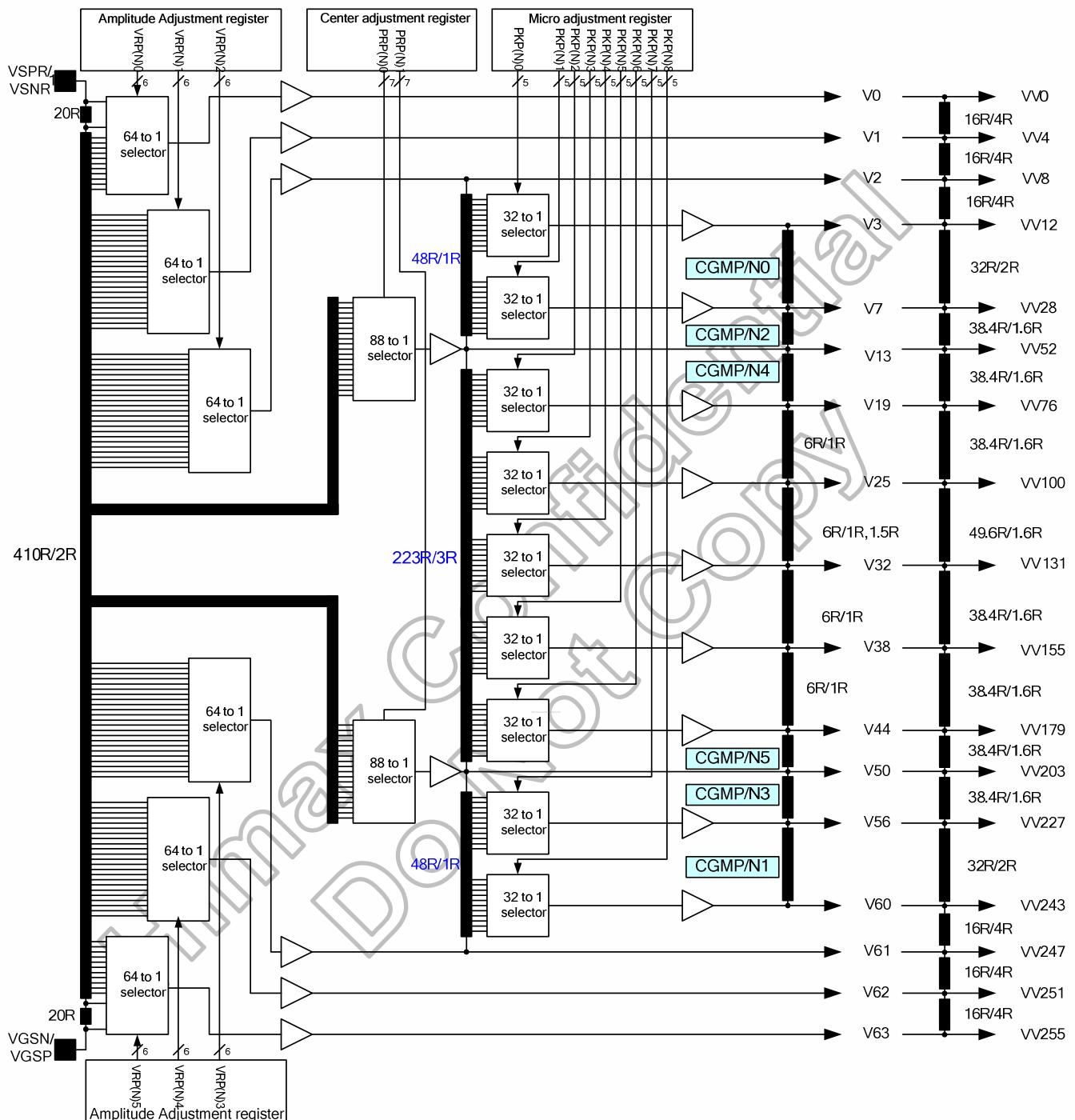
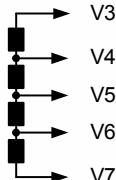
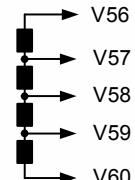


Figure 5.3: Gamma Resister Stream and Gamma Reference Voltage

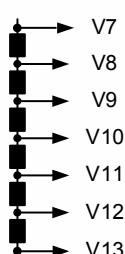
CGMP/N0	0	1	2	3
	1R	3R	3.5R	3.5R
	1R	2.5R	2.5R	2.5R
	1R	2R	1.8R	2R
	1R	2R	1.5R	2R



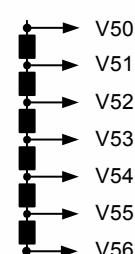
CGMP/N1	0	1	2	3
	1R	2R	1.5R	2R
	1R	2R	1.8R	2R
	1R	2.5R	2.5R	2.5R
	1R	3R	3.5R	3.5R



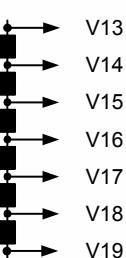
CGMP/N2	0	1	2	3
	1R	3R	4R	4.5R
	1R	3R	3R	4R
	1R	2.5R	3R	3R
	1R	2.5R	3R	3R
	1R	2.5R	2.5R	2.5R
	1R	2.5R	2.5R	2.5R



CGMP/N3	0	1	2	3
	1R	2.5R	2.5R	2.5R
	1R	2.5R	2.5R	2.5R
	1R	2.5R	3R	3R
	1R	2.5R	3R	3R
	1R	3R	3R	4R
	1R	3R	4R	4.5R



CGMP/N4	0	1
	1R	1.5R
	1R	1R



CGMP/N5	0	1
	1R	1R
	1R	1.5R

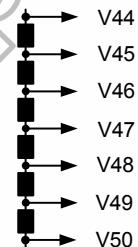


Figure 5.4: Gamma Resister Stream

Variable Resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0
000000	0R
000001	20R
000010	22R
000011	24R
•	•
•	•
011101	76R
011110	78R
011111	80R
100000	82R
100001	84R
100010	86R
•	•
•	•
111101	140R
111110	142R
111111	144R

Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1
000000	0R
000001	2R
000010	4R
000011	6R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
000011	6R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3
000000	0R
000001	2R
000010	4R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111100	120R
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4
000000	0R
000001	2R
000010	4R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111100	120R
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111100	120R
111101	122R
111110	124R
111111	144R

Table 5.2: Offset Adjustment 0 ~ 5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0
0000000	0R
0000001	2R
0000010	4R
•	•
•	•
1010101	170R
1010110	172R
1010111	174R

Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R
0000001	2R
0000010	4R
•	•
•	•
1010101	170R
1010110	172R
1010111	174R

Table 5.3: Center Adjustment

The grayscale levels are determined by the following formulas.

Reference Voltage	Macro Adjustment Value	VinP/N0 Formula
VinP0	VRP0 5-0 = 000000	VSPR
	VRP0 5-0 = 000001	((450R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000010	((450R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000011	((450R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000100	((450R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000101	((450R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000110	((450R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000111	((450R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001000	((450R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001001	((450R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001010	((450R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001011	((450R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001100	((450R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001101	((450R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001110	((450R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001111	((450R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010000	((450R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010001	((450R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010010	((450R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010011	((450R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010100	((450R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010101	((450R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010110	((450R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010111	((450R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011000	((450R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011001	((450R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011010	((450R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011011	((450R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011100	((450R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011101	((450R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011110	((450R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011111	((450R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100000	((450R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100001	((450R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100010	((450R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100011	((450R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100100	((450R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100101	((450R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100110	((450R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100111	((450R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101000	((450R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101001	((450R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101010	((450R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101011	((450R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101100	((450R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101101	((450R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101110	((450R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101111	((450R - 112R) / 450R) * (VSPR - VGSP) + VGSP
VRP0 5-0 = 110000	((450R - 114R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 110001	((450R - 116R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 110010	((450R - 118R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 110011	((450R - 120R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 110100	((450R - 122R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 110101	((450R - 124R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 110110	((450R - 126R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 110111	((450R - 128R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 111000	((450R - 130R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 111001	((450R - 132R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 111010	((450R - 134R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 111011	((450R - 136R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 111100	((450R - 138R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 111101	((450R - 140R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 111110	((450R - 142R) / 450R) * (VSPR - VGSP) + VGSP	
VRP0 5-0 = 111111	((450R - 144R) / 450R) * (VSPR - VGSP) + VGSP	

Table 5.4: VinP 0

Reference Voltage	Macro Adjustment Value	VinP/N1 Formula
VinP1	VRP1 5-0 = 000000	$(430R / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 000001	$((430R - 2R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 000010	$((430R - 4R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 000011	$((430R - 6R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 000100	$((430R - 8R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 000101	$((430R - 10R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 000110	$((430R - 12R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 000111	$((430R - 14R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 001000	$((430R - 16R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 001001	$((430R - 18R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 001010	$((430R - 20R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 001011	$((430R - 22R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 001100	$((430R - 24R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 001101	$((430R - 26R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 001110	$((430R - 28R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 001111	$((430R - 30R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 010000	$((430R - 32R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 010001	$((430R - 34R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 010010	$((430R - 36R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 010011	$((430R - 38R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 010100	$((430R - 40R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 010101	$((430R - 42R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 010110	$((430R - 44R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 010111	$((430R - 46R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 011000	$((430R - 48R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 011001	$((430R - 50R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 011010	$((430R - 52R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 011011	$((430R - 54R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 011100	$((430R - 56R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 011101	$((430R - 58R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 011110	$((430R - 60R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 011111	$((430R - 62R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 100000	$((430R - 64R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 100001	$((430R - 66R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 100010	$((430R - 68R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 100011	$((430R - 70R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 100100	$((430R - 72R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 100101	$((430R - 74R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 100110	$((430R - 76R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 100111	$((430R - 78R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 101000	$((430R - 80R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 101001	$((430R - 82R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 101010	$((430R - 84R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 101011	$((430R - 86R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 101100	$((430R - 88R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 101101	$((430R - 90R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 101110	$((430R - 92R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 101111	$((430R - 94R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 110000	$((430R - 96R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 110001	$((430R - 98R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 110010	$((430R - 100R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 110011	$((430R - 102R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 110100	$((430R - 104R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 110101	$((430R - 106R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 110110	$((430R - 108R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 110111	$((430R - 110R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 111000	$((430R - 112R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 111001	$((430R - 114R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 111010	$((430R - 116R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 111011	$((430R - 118R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 111100	$((430R - 120R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 111101	$((430R - 122R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 111110	$((430R - 124R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP1 5-0 = 111111	$((430R - 126R) / 450R) * (VSPR - VGSP) + VGSP$

Table 5.5: VinP 1

Reference Voltage	Macro Adjustment Value	VinP/N2 Formula
VinP2	VRP2 5-0 = 000000	((420R / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000001	((420R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000010	((420R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000011	((420R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000100	((420R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000101	((420R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000110	((420R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000111	((420R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001000	((420R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001001	((420R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001010	((420R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001011	((420R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001100	((420R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001101	((420R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001110	((420R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001111	((420R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010000	((420R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010001	((420R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010010	((420R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010011	((420R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010100	((420R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010101	((420R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010110	((420R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010111	((420R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011000	((420R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011001	((420R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011010	((420R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011011	((420R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011100	((420R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011101	((420R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011110	((420R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011111	((420R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100000	((420R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100001	((420R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100010	((420R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100011	((420R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100100	((420R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100101	((420R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100110	((420R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100111	((420R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101000	((420R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101001	((420R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101010	((420R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101011	((420R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101100	((420R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101101	((420R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101110	((420R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101111	((420R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110000	((420R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110001	((420R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110010	((420R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110011	((420R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110100	((420R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110101	((420R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110110	((420R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110111	((420R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111000	((420R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111001	((420R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111010	((420R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111011	((420R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111100	((420R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111101	((420R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111110	((420R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111111	((420R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.6: VinP 2

Reference Voltage	Macro Adjustment Value	VinP/N14 Formula
VinP14	VRP3 5-0 = 000000	$(156R / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000001	$((156R - 2R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000010	$((156R - 4R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000011	$((156R - 6R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000100	$((156R - 8R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000101	$((156R - 10R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000110	$((156R - 12R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000111	$((156R - 14R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001000	$((156R - 16R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001001	$((156R - 18R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001010	$((156R - 20R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001011	$((156R - 22R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001100	$((156R - 24R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001101	$((156R - 26R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001110	$((156R - 28R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001111	$((156R - 30R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010000	$((156R - 32R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010001	$((156R - 34R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010010	$((156R - 36R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010011	$((156R - 38R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010100	$((156R - 40R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010101	$((156R - 42R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010110	$((156R - 44R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010111	$((156R - 46R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011000	$((156R - 48R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011001	$((156R - 50R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011010	$((156R - 52R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011011	$((156R - 54R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011100	$((156R - 56R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011101	$((156R - 58R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011110	$((156R - 60R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011111	$((156R - 62R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100000	$((156R - 64R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100001	$((156R - 66R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100010	$((156R - 68R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100011	$((156R - 70R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100100	$((156R - 72R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100101	$((156R - 74R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100110	$((156R - 76R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100111	$((156R - 78R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101000	$((156R - 80R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101001	$((156R - 82R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101010	$((156R - 84R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101011	$((156R - 86R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101100	$((156R - 88R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101101	$((156R - 90R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101110	$((156R - 92R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101111	$((156R - 94R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110000	$((156R - 96R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110001	$((156R - 98R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110010	$((156R - 100R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110011	$((156R - 102R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110100	$((156R - 104R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110101	$((156R - 106R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110110	$((156R - 108R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110111	$((156R - 110R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111000	$((156R - 112R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111001	$((156R - 114R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111010	$((156R - 116R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111011	$((156R - 118R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111100	$((156R - 120R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111101	$((156R - 122R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111110	$((156R - 124R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111111	$((156R - 126R) / 450R) * (VSPR - VGSP) + VGSP$

Table 5.7: VinP 14

Reference Voltage	Macro Adjustment Value	VinP/N15Formula
VinP15	VRP4 5-0 = 000000	((146R / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000001	((146R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000010	((146R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000011	((146R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000100	((146R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000101	((146R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000110	((146R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000111	((146R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001000	((146R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001001	((146R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001010	((146R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001011	((146R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001100	((146R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001101	((146R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001110	((146R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001111	((146R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010000	((146R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010001	((146R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010010	((146R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010011	((146R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010100	((146R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010101	((146R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010110	((146R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010111	((146R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011000	((146R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011001	((146R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011010	((146R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011011	((146R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011100	((146R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011101	((146R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011110	((146R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011111	((146R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100000	((146R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100001	((146R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100010	((146R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100011	((146R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100100	((146R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100101	((146R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100110	((146R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100111	((146R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101000	((146R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101001	((146R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101010	((146R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101011	((146R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101100	((146R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101101	((146R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101110	((146R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101111	((146R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110000	((146R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110001	((146R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110010	((146R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110011	((146R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110100	((146R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110101	((146R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110110	((146R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110111	((146R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111000	((146R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111001	((146R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111010	((146R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111011	((146R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111100	((146R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111101	((146R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111110	((146R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111111	((146R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.8: VinP 15

Reference Voltage	Macro Adjustment Value	VinP/N16 Formula
VinP16	VRP5 5-0 = 000000	$((144R / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000001	$((144R - 2R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000010	$((144R - 4R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000011	$((144R - 6R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000100	$((144R - 8R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000101	$((144R - 10R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000110	$((144R - 12R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000111	$((144R - 14R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001000	$((144R - 16R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001001	$((144R - 18R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001010	$((144R - 20R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001011	$((144R - 22R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001100	$((144R - 24R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001101	$((144R - 26R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001110	$((144R - 28R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001111	$((144R - 30R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010000	$((144R - 32R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010001	$((144R - 34R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010010	$((144R - 36R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010011	$((144R - 38R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010100	$((144R - 40R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010101	$((144R - 42R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010110	$((144R - 44R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010111	$((144R - 46R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011000	$((144R - 48R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011001	$((144R - 50R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011010	$((144R - 52R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011011	$((144R - 54R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011100	$((144R - 56R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011101	$((144R - 58R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011110	$((144R - 60R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011111	$((144R - 62R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100000	$((144R - 64R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100001	$((144R - 66R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100010	$((144R - 68R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100011	$((144R - 70R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100100	$((144R - 72R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100101	$((144R - 74R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100110	$((144R - 76R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100111	$((144R - 78R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101000	$((144R - 80R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101001	$((144R - 82R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101010	$((144R - 84R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101011	$((144R - 86R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101100	$((144R - 88R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101101	$((144R - 90R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101110	$((144R - 92R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101111	$((144R - 94R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110000	$((144R - 96R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110001	$((144R - 98R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110010	$((144R - 100R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110011	$((144R - 102R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110100	$((144R - 104R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110101	$((144R - 106R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110110	$((144R - 108R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110111	$((144R - 110R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111000	$((144R - 112R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111001	$((144R - 114R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111010	$((144R - 116R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111011	$((144R - 118R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111100	$((144R - 120R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111101	$((144R - 122R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111110	$((144R - 124R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111111	VGSP

Table 5.9: VinP 16

Reference Voltage	Macro Adjustment Value	VinP/N5 Formula
VinP5	PRP0 6-0 = 0000000	(350R / 450R) (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000001	((350R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000010	((350R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000011	((350R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000100	((350R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000101	((350R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000110	((350R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000111	((350R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001000	((350R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001001	((350R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001010	((350R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001011	((350R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001100	((350R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001101	((350R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001110	((350R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001111	((350R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010000	((350R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010001	((350R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010010	((350R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010011	((350R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010100	((350R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010101	((350R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010110	((350R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010111	((350R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011000	((350R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011001	((350R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011010	((350R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011011	((350R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011100	((350R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011101	((350R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011110	((350R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011111	((350R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100000	((350R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100001	((350R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100010	((350R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100011	((350R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100100	((350R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100101	((350R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100110	((350R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100111	((350R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101000	((350R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101001	((350R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101010	((350R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101011	((350R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101100	((350R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101101	((350R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101110	((350R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101111	((350R - 94R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 0110000	((350R - 96R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110001	((350R - 98R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110010	((350R - 100R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110011	((350R - 102R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110100	((350R - 104R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110101	((350R - 106R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110110	((350R - 108R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110111	((350R - 110R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111000	((350R - 112R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111001	((350R - 114R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111010	((350R - 116R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111011	((350R - 118R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111100	((350R - 120R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111101	((350R - 122R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111110	((350R - 124R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111111	((350R - 126R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 1000000	((350R - 128R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 1000001	((350R - 130R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 1000010	((350R - 132R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 1000011	((350R - 134R) / 450R) * (VSPR - VGSP) + VGSP	

PRP0 6-0 = 1000100	((350R - 136R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1000101	((350R - 138R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1000110	((350R - 140R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1000111	((350R - 142R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1001000	((350R - 144R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1001001	((350R - 146R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1001010	((350R - 148R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1001011	((350R - 150R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1001100	((350R - 152R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1001101	((350R - 154R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1001110	((350R - 156R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1001111	((350R - 158R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1010000	((350R - 160R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1010001	((350R - 162R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1010010	((350R - 164R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1010011	((350R - 166R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1010100	((350R - 168R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1010101	((350R - 170R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1010110	((350R - 172R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1010111	((350R - 174R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 1011000	-
PRP0 6-0 = 1011001	-
PRP0 6-0 = 1011010	-
PRP0 6-0 = 1011011	-
PRP0 6-0 = 1011100	-
PRP0 6-0 = 1011101	-
PRP0 6-0 = 1011110	-
PRP0 6-0 = 1011111	-
PRP0 6-0 = 1100000	-
PRP0 6-0 = 1100001	-
PRP0 6-0 = 1100010	-
PRP0 6-0 = 1100011	-
PRP0 6-0 = 1100100	-
PRP0 6-0 = 1100101	-
PRP0 6-0 = 1100110	-
PRP0 6-0 = 1100111	-
PRP0 6-0 = 1101000	-
PRP0 6-0 = 1101001	-
PRP0 6-0 = 1101010	-
PRP0 6-0 = 1101011	-
PRP0 6-0 = 1101100	-
PRP0 6-0 = 1101101	-
PRP0 6-0 = 1101110	-
PRP0 6-0 = 1101111	-
PRP0 6-0 = 1110000	-
PRP0 6-0 = 1110001	-
PRP0 6-0 = 1110010	-
PRP0 6-0 = 1110011	-
PRP0 6-0 = 1110100	-
PRP0 6-0 = 1110101	-
PRP0 6-0 = 1110110	-
PRP0 6-0 = 1110111	-
PRP0 6-0 = 1111000	-
PRP0 6-0 = 1111001	-
PRP0 6-0 = 1111010	-
PRP0 6-0 = 1111011	-
PRP0 6-0 = 1111100	-
PRP0 6-0 = 1111101	-
PRP0 6-0 = 1111110	-
PRP0 6-0 = 1111111	-

Table 5.10: VinP5

Reference Voltage	Macro Adjustment Value	VinP/N11 Formula
VinP11	PRP1 6-0 = 0000000	(274R / 450R) (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000001	((274R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000010	((274R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000011	((274R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000100	((274R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000101	((274R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000110	((274R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000111	((274R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001000	((274R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001001	((274R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001010	((274R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001011	((274R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001100	((274R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001101	((274R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001110	((274R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001111	((274R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010000	((274R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010001	((274R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010010	((274R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010011	((274R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010100	((274R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010101	((274R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010110	((274R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010111	((274R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011000	((274R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011001	((274R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011010	((274R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011011	((274R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011100	((274R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011101	((274R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011110	((274R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011111	((274R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100000	((274R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100001	((274R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100010	((274R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100011	((274R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100100	((274R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100101	((274R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100110	((274R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100111	((274R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101000	((274R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101001	((274R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101010	((274R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101011	((274R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101100	((274R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101101	((274R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101110	((274R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101111	((274R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110000	((274R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110001	((274R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110010	((274R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110011	((274R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110100	((274R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110101	((274R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110110	((274R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110111	((274R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111000	((274R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111001	((274R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111010	((274R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111011	((274R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111100	((274R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111101	((274R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111110	((274R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111111	((274R - 126R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000000	((274R - 128R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000001	((274R - 130R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000010	((274R - 132R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000011	((274R - 134R) / 450R) * (VSPR - VGSP) + VGSP

PRP1 6-0 = 1000100	((274R - 136R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1000101	((274R - 138R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1000110	((274R - 140R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1000111	((274R - 142R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1001000	((274R - 144R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1001001	((274R - 146R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1001010	((274R - 148R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1001011	((274R - 150R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1001100	((274R - 152R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1001101	((274R - 154R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1001110	((274R - 156R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1001111	((274R - 158R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1010000	((274R - 160R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1010001	((274R - 162R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1010010	((274R - 164R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1010011	((274R - 166R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1010100	((274R - 168R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1010101	((274R - 170R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1010110	((274R - 172R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1010111	((274R - 174R) / 450R) * (VSPR - VGSP) + VGSP
PRP1 6-0 = 1011000	-
PRP1 6-0 = 1011001	-
PRP1 6-0 = 1011010	-
PRP1 6-0 = 1011011	-
PRP1 6-0 = 1011100	-
PRP1 6-0 = 1011101	-
PRP1 6-0 = 1011110	-
PRP1 6-0 = 1011111	-
PRP1 6-0 = 1100000	-
PRP1 6-0 = 1100001	-
PRP1 6-0 = 1100010	-
PRP1 6-0 = 1100011	-
PRP1 6-0 = 1100100	-
PRP1 6-0 = 1100101	-
PRP1 6-0 = 1100110	-
PRP1 6-0 = 1100111	-
PRP1 6-0 = 1101000	-
PRP1 6-0 = 1101001	-
PRP1 6-0 = 1101010	-
PRP1 6-0 = 1101011	-
PRP1 6-0 = 1101100	-
PRP1 6-0 = 1101101	-
PRP1 6-0 = 1101110	-
PRP1 6-0 = 1101111	-
PRP1 6-0 = 1110000	-
PRP1 6-0 = 1110001	-
PRP1 6-0 = 1110010	-
PRP1 6-0 = 1110011	-
PRP1 6-0 = 1110100	-
PRP1 6-0 = 1110101	-
PRP1 6-0 = 1110110	-
PRP1 6-0 = 1110111	-
PRP1 6-0 = 1111000	-
PRP1 6-0 = 1111001	-
PRP1 6-0 = 1111010	-
PRP1 6-0 = 1111011	-
PRP1 6-0 = 1111100	-
PRP1 6-0 = 1111101	-
PRP1 6-0 = 1111110	-
PRP1 6-0 = 1111111	-

Table 5.11: VinP 11

Reference Voltage	Macro Adjustment Value	VinP/N3 Formula
VinP3	PKP0 4-0 = 00000	$(47R / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00001	$((47R - 1R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00010	$((47R - 2R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00011	$((47R - 3R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00100	$((47R - 4R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00101	$((47R - 5R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00110	$((47R - 6R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00111	$((47R - 7R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01000	$((47R - 8R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01001	$((47R - 9R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01010	$((47R - 10R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01011	$((47R - 11R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01100	$((47R - 12R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01101	$((47R - 13R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01110	$((47R - 14R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01111	$((47R - 15R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10000	$((47R - 16R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10001	$((47R - 17R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10010	$((47R - 18R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10011	$((47R - 19R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10100	$((47R - 20R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10101	$((47R - 21R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10110	$((47R - 22R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10111	$((47R - 23R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11000	$((47R - 24R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11001	$((47R - 25R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11010	$((47R - 26R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11011	$((47R - 27R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11100	$((47R - 28R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11101	$((47R - 29R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11110	$((47R - 30R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11111	$((47R - 31R) / 48R) * (VinP2 - VinP5) + VinP5$

Table 5.12: VinP 3

Reference Voltage	Macro Adjustment Value	VinP4 Formula
VinP4	PKP1 4-0 = 00000	$(32R / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00001	$((32R - 1R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00010	$((32R - 2R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00011	$((32R - 3R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00100	$((32R - 4R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00101	$((32R - 5R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00110	$((32R - 6R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00111	$((32R - 7R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01000	$((32R - 8R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01001	$((32R - 9R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01010	$((32R - 10R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01011	$((32R - 11R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01100	$((32R - 12R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01101	$((32R - 13R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01110	$((32R - 14R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01111	$((32R - 15R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10000	$((32R - 16R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10001	$((32R - 17R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10010	$((32R - 18R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10011	$((32R - 19R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10100	$((32R - 20R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10101	$((32R - 21R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10110	$((32R - 22R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10111	$((32R - 23R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11000	$((32R - 24R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11001	$((32R - 25R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11010	$((32R - 26R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11011	$((32R - 27R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11100	$((32R - 28R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11101	$((32R - 29R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11110	$((32R - 30R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11111	$((32R - 31R) / 48R) * (VinP2 - VinP5) + VinP5$

Table 5.13: VinP 4

Reference Voltage	Macro Adjustment Value	VinP6 Formula
VinP6	PKP2 4-0 = 00000	$(220R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00001	$((220R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00010	$((220R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00011	$((220R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00100	$((220R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00101	$((220R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00110	$((220R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00111	$((220R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01000	$((220R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01001	$((220R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01010	$((220R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01011	$((220R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01100	$((220R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01101	$((220R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01110	$((220R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01111	$((220R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10000	$((220R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10001	$((220R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10010	$((220R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10011	$((220R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10100	$((220R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10101	$((220R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10110	$((220R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10111	$((220R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11000	$((220R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11001	$((220R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11010	$((220R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11011	$((220R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11100	$((220R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11101	$((220R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11110	$((220R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11111	$((220R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.14: VinP 6

Reference Voltage	Macro Adjustment Value	VinP7 Formula
VinP7	PKP3 4-0 = 00000	$(193R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00001	$((193R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00010	$((193R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00011	$((193R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00100	$((193R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00101	$((193R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00110	$((193R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00111	$((193R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01000	$((193R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01001	$((193R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01010	$((193R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01011	$((193R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01100	$((193R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01101	$((193R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01110	$((193R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01111	$((193R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10000	$((193R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10001	$((193R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10010	$((193R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10011	$((193R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10100	$((193R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10101	$((193R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10110	$((193R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10111	$((193R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11000	$((193R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11001	$((193R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11010	$((193R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11011	$((193R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11100	$((193R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11101	$((193R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11110	$((193R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11111	$((193R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.15: VinP 7

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Reference Voltage	Macro Adjustment Value	VinP8 Formula
VinP8	PKP4 4-0 = 00000	$(158R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00001	$((158R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00010	$((158R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00011	$((158R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00100	$((158R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00101	$((158R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00110	$((158R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00111	$((158R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01000	$((158R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01001	$((158R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01010	$((158R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01011	$((158R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01100	$((158R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01101	$((158R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01110	$((158R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01111	$((158R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10000	$((158R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10001	$((158R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10010	$((158R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10011	$((158R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10100	$((158R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10101	$((158R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10110	$((158R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10111	$((158R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11000	$((158R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11001	$((158R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11010	$((158R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11011	$((158R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11100	$((158R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11101	$((158R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11110	$((158R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11111	$((158R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.16: VinP 8

Reference Voltage	Macro Adjustment Value	VinP9 Formula
VinP9	PKP5 4-0 = 00000	$(123R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00001	$((123R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00010	$((123R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00011	$((123R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00100	$((123R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00101	$((123R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00110	$((123R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00111	$((123R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01000	$((123R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01001	$((123R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01010	$((123R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01011	$((123R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01100	$((123R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01101	$((123R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01110	$((123R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01111	$((123R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10000	$((123R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10001	$((123R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10010	$((123R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10011	$((123R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10100	$((123R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10101	$((123R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10110	$((123R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10111	$((123R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11000	$((123R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11001	$((123R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11010	$((123R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11011	$((123R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11100	$((123R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11101	$((123R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11110	$((123R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11111	$((123R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.17: VinP 9

Reference Voltage	Macro Adjustment Value	VinP10 Formula
VinP10	PKP6 4-0 = 00000	$(96R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00001	$((96R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00010	$((96R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00011	$((96R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00100	$((96R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00101	$((96R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00110	$((96R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00111	$((96R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01000	$((96R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01001	$((96R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01010	$((96R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01011	$((96R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01100	$((96R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01101	$((96R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01110	$((96R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01111	$((96R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10000	$((96R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10001	$((96R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10010	$((96R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10011	$((96R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10100	$((96R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10101	$((96R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10110	$((96R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10111	$((96R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11000	$((96R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11001	$((96R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11010	$((96R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11011	$((96R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11100	$((96R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11101	$((96R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11110	$((96R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11111	$((96R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.18: VinP 10

Reference Voltage	Macro Adjustment Value	VinP12 Formula
VinP12	PKP7 4-0 = 00000	$(47R / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00001	$((47R - 1R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00010	$((47R - 2R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00011	$((47R - 3R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00100	$((47R - 4R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00101	$((47R - 5R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00110	$((47R - 6R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00111	$((47R - 7R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01000	$((47R - 8R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01001	$((47R - 9R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01010	$((47R - 10R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01011	$((47R - 11R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01100	$((47R - 12R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01101	$((47R - 13R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01110	$((47R - 14R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01111	$((47R - 15R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10000	$((47R - 16R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10001	$((47R - 17R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10010	$((47R - 18R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10011	$((47R - 19R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10100	$((47R - 20R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10101	$((47R - 21R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10110	$((47R - 22R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10111	$((47R - 23R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11000	$((47R - 24R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11001	$((47R - 25R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11010	$((47R - 26R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11011	$((47R - 27R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11100	$((47R - 28R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11101	$((47R - 29R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11110	$((47R - 30R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11111	$((47R - 31R) / 48R) * (VinP11 - VinP14) + VinP14$

Table 5.19: VinP 12

Reference Voltage	Macro Adjustment Value	VinP13 Formula
VinP13	PKP8 4-0 = 00000	$(32R / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00001	$((32R - 1R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00010	$((32R - 2R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00011	$((32R - 3R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00100	$((32R - 4R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00101	$((32R - 5R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00110	$((32R - 6R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00111	$((32R - 7R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01000	$((32R - 8R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01001	$((32R - 9R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01010	$((32R - 10R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01011	$((32R - 11R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01100	$((32R - 12R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01101	$((32R - 13R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01110	$((32R - 14R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01111	$((32R - 15R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10000	$((32R - 16R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10001	$((32R - 17R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10010	$((32R - 18R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10011	$((32R - 19R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10100	$((32R - 20R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10101	$((32R - 21R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10110	$((32R - 22R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10111	$((32R - 23R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11000	$((32R - 24R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11001	$((32R - 25R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11010	$((32R - 26R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11011	$((32R - 27R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11100	$((32R - 28R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11101	$((32R - 29R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11110	$((32R - 30R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11111	$((32R - 31R) / 48R) * (VinP11 - VinP14) + VinP14$

Table 5.20: VinP 13

Reference Voltage	Macro Adjustment Value	VinN0 Formula
VinN0	VRN0 5-0 = 000000	VSNR
	VRN0 5-0 = 000001	((450R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000010	((450R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000011	((450R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000100	((450R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000101	((450R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000110	((450R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000111	((450R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001000	((450R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001001	((450R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001010	((450R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001011	((450R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001100	((450R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001101	((450R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001110	((450R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001111	((450R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010000	((450R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010001	((450R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010010	((450R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010011	((450R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010100	((450R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010101	((450R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010110	((450R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010111	((450R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011000	((450R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011001	((450R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011010	((450R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011011	((450R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011100	((450R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011101	((450R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011110	((450R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011111	((450R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100000	((450R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100001	((450R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100010	((450R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100011	((450R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100100	((450R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100101	((450R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100110	((450R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100111	((450R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101000	((450R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101001	((450R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101010	((450R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101011	((450R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101100	((450R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101101	((450R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101110	((450R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101111	((450R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110000	((450R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110001	((450R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110010	((450R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110011	((450R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110100	((450R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110101	((450R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110110	((450R - 126R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110111	((450R - 128R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111000	((450R - 130R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111001	((450R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111010	((450R - 134R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111011	((450R - 136R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111100	((450R - 138R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111101	((450R - 140R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111110	((450R - 142R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111111	((450R - 144R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.21: VinN 0

Reference Voltage	Macro Adjustment Value	VinN1 Formula
VinN1	VRN1 5-0 = 000000	$(430R / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 000001	$((430R - 2R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 000010	$((430R - 4R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 000011	$((430R - 6R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 000100	$((430R - 8R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 000101	$((430R - 10R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 000110	$((430R - 12R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 000111	$((430R - 14R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 001000	$((430R - 16R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 001001	$((430R - 18R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 001010	$((430R - 20R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 001011	$((430R - 22R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 001100	$((430R - 24R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 001101	$((430R - 26R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 001110	$((430R - 28R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 001111	$((430R - 30R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 010000	$((430R - 32R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 010001	$((430R - 34R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 010010	$((430R - 36R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 010011	$((430R - 38R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 010100	$((430R - 40R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 010101	$((430R - 42R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 010110	$((430R - 44R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 010111	$((430R - 46R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 011000	$((430R - 48R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 011001	$((430R - 50R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 011010	$((430R - 52R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 011011	$((430R - 54R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 011100	$((430R - 56R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 011101	$((430R - 58R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 011110	$((430R - 60R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 011111	$((430R - 62R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 100000	$((430R - 64R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 100001	$((430R - 66R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 100010	$((430R - 68R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 100011	$((430R - 70R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 100100	$((430R - 72R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 100101	$((430R - 74R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 100110	$((430R - 76R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 100111	$((430R - 78R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 101000	$((430R - 80R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 101001	$((430R - 82R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 101010	$((430R - 84R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 101011	$((430R - 86R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 101100	$((430R - 88R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 101101	$((430R - 90R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 101110	$((430R - 92R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 101111	$((430R - 94R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 110000	$((430R - 96R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 110001	$((430R - 98R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 110010	$((430R - 100R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 110011	$((430R - 102R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 110100	$((430R - 104R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 110101	$((430R - 106R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 110110	$((430R - 108R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 110111	$((430R - 110R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 111000	$((430R - 112R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 111001	$((430R - 114R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 111010	$((430R - 116R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 111011	$((430R - 118R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 111100	$((430R - 120R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 111101	$((430R - 122R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 111110	$((430R - 124R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN1 5-0 = 111111	$((430R - 126R) / 450R) * (VSNR - VGSN) + VGSN$

Table 5.22: VinN 1

Reference Voltage	Macro Adjustment Value	VinN2 Formula
VinN2	VRN2 5-0 = 000000	(420R / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000001	((420R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000010	((420R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000011	((420R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000100	((420R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000101	((420R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000110	((420R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000111	((420R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001000	((420R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001001	((420R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001010	((420R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001011	((420R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001100	((420R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001101	((420R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001110	((420R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001111	((420R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010000	((420R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010001	((420R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010010	((420R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010011	((420R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010100	((420R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010101	((420R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010110	((420R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010111	((420R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011000	((420R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011001	((420R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011010	((420R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011011	((420R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011100	((420R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011101	((420R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011110	((420R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011111	((420R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100000	((420R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100001	((420R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100010	((420R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100011	((420R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100100	((420R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100101	((420R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100110	((420R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100111	((420R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101000	((420R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101001	((420R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101010	((420R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101011	((420R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101100	((420R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101101	((420R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101110	((420R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101111	((420R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110000	((420R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110001	((420R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110010	((420R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110011	((420R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110100	((420R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110101	((420R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110110	((420R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110111	((420R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111000	((420R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111001	((420R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111010	((420R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111011	((420R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111100	((420R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111101	((420R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111110	((420R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111111	((420R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.23: VinN 2

Reference Voltage	Macro Adjustment Value	VinN14 Formula
VinN14	VRN3 5-0 = 000000	$(156R / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 000001	$((156R - 2R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 000010	$((156R - 4R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 000011	$((156R - 6R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 000100	$((156R - 8R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 000101	$((156R - 10R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 000110	$((156R - 12R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 000111	$((156R - 14R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 001000	$((156R - 16R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 001001	$((156R - 18R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 001010	$((156R - 20R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 001011	$((156R - 22R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 001100	$((156R - 24R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 001101	$((156R - 26R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 001110	$((156R - 28R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 001111	$((156R - 30R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 010000	$((156R - 32R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 010001	$((156R - 34R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 010010	$((156R - 36R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 010011	$((156R - 38R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 010100	$((156R - 40R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 010101	$((156R - 42R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 010110	$((156R - 44R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 010111	$((156R - 46R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 011000	$((156R - 48R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 011001	$((156R - 50R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 011010	$((156R - 52R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 011011	$((156R - 54R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 011100	$((156R - 56R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 011101	$((156R - 58R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 011110	$((156R - 60R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 011111	$((156R - 62R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 100000	$((156R - 64R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 100001	$((156R - 66R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 100010	$((156R - 68R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 100011	$((156R - 70R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 100100	$((156R - 72R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 100101	$((156R - 74R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 100110	$((156R - 76R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 100111	$((156R - 78R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 101000	$((156R - 80R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 101001	$((156R - 82R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 101010	$((156R - 84R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 101011	$((156R - 86R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 101100	$((156R - 88R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 101101	$((156R - 90R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 101110	$((156R - 92R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 101111	$((156R - 94R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 110000	$((156R - 96R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 110001	$((156R - 98R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 110010	$((156R - 100R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 110011	$((156R - 102R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 110100	$((156R - 104R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 110101	$((156R - 106R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 110110	$((156R - 108R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 110111	$((156R - 110R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 111000	$((156R - 112R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 111001	$((156R - 114R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 111010	$((156R - 116R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 111011	$((156R - 118R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 111100	$((156R - 120R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 111101	$((156R - 122R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 111110	$((156R - 124R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN3 5-0 = 111111	$((156R - 126R) / 450R) * (VSNR - VGSN) + VGSN$

Table 5.24: VinN 14

Reference Voltage	Macro Adjustment Value	VinN15Formula
VinN15	VRN4 5-0 = 000000	((146R / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000001	((146R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000010	((146R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000011	((146R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000100	((146R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000101	((146R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000110	((146R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000111	((146R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001000	((146R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001001	((146R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001010	((146R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001011	((146R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001100	((146R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001101	((146R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001110	((146R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001111	((146R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010000	((146R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010001	((146R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010010	((146R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010011	((146R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010100	((146R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010101	((146R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010110	((146R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010111	((146R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011000	((146R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011001	((146R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011010	((146R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011011	((146R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011100	((146R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011101	((146R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011110	((146R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011111	((146R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100000	((146R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100001	((146R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100010	((146R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100011	((146R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100100	((146R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100101	((146R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100110	((146R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100111	((146R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101000	((146R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101001	((146R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101010	((146R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101011	((146R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101100	((146R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101101	((146R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101110	((146R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101111	((146R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110000	((146R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110001	((146R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110010	((146R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110011	((146R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110100	((146R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110101	((146R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110110	((146R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110111	((146R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111000	((146R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111001	((146R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111010	((146R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111011	((146R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111100	((146R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111101	((146R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111110	((146R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111111	((146R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.25: VinN 15

Reference Voltage	Macro Adjustment Value	VinN16 Formula
VinN16	VRN5 5-0 = 000000	((144R / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000001	((144R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000010	((144R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000011	((144R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000100	((144R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000101	((144R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000110	((144R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000111	((144R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001000	((144R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001001	((144R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001010	((144R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001011	((144R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001100	((144R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001101	((144R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001110	((144R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001111	((144R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010000	((144R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010001	((144R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010010	((144R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010011	((144R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010100	((144R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010101	((144R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010110	((144R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010111	((144R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011000	((144R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011001	((144R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011010	((144R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011011	((144R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011100	((144R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011101	((144R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011110	((144R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011111	((144R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100000	((144R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100001	((144R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100010	((144R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100011	((144R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100100	((144R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100101	((144R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100110	((144R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100111	((144R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101000	((144R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101001	((144R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101010	((144R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101011	((144R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101100	((144R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101101	((144R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101110	((144R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101111	((144R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110000	((144R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110001	((144R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110010	((144R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110011	((144R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110100	((144R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110101	((144R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110110	((144R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110111	((144R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111000	((144R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111001	((144R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111010	((144R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111011	((144R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111100	((144R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111101	((144R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111110	((144R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111111	VGSN

Table 5.26: VinN 16

Reference Voltage	Macro Adjustment Value	VinN5 Formula
VinN5	PRNO 6-0 = 0000000	$(350R / 450R) (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0000001	$((350R - 2R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0000010	$((350R - 4R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0000011	$((350R - 6R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0000100	$((350R - 8R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0000101	$((350R - 10R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0000110	$((350R - 12R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0000111	$((350R - 14R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0001000	$((350R - 16R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0001001	$((350R - 18R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0001010	$((350R - 20R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0001011	$((350R - 22R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0001100	$((350R - 24R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0001101	$((350R - 26R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0001110	$((350R - 28R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0001111	$((350R - 30R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0010000	$((350R - 32R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0010001	$((350R - 34R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0010010	$((350R - 36R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0010011	$((350R - 38R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0010100	$((350R - 40R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0010101	$((350R - 42R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0010110	$((350R - 44R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0010111	$((350R - 46R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0011000	$((350R - 48R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0011001	$((350R - 50R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0011010	$((350R - 52R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0011011	$((350R - 54R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0011100	$((350R - 56R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0011101	$((350R - 58R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0011110	$((350R - 60R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0011111	$((350R - 62R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0100000	$((350R - 64R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0100001	$((350R - 66R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0100010	$((350R - 68R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0100011	$((350R - 70R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0100100	$((350R - 72R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0100101	$((350R - 74R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0100110	$((350R - 76R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0100111	$((350R - 78R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0101000	$((350R - 80R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0101001	$((350R - 82R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0101010	$((350R - 84R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0101011	$((350R - 86R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0101100	$((350R - 88R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0101101	$((350R - 90R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0101110	$((350R - 92R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0101111	$((350R - 94R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0110000	$((350R - 96R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0110001	$((350R - 98R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0110010	$((350R - 100R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0110011	$((350R - 102R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0110100	$((350R - 104R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0110101	$((350R - 106R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0110110	$((350R - 108R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0110111	$((350R - 110R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0111000	$((350R - 112R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0111001	$((350R - 114R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0111010	$((350R - 116R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 0111011	$((350R - 118R) / 450R) * (VSNR - VGSN) + VGSN$
PRNO 6-0 = 0111100	$((350R - 120R) / 450R) * (VSNR - VGSN) + VGSN$	
PRNO 6-0 = 0111101	$((350R - 122R) / 450R) * (VSNR - VGSN) + VGSN$	
PRNO 6-0 = 0111110	$((350R - 124R) / 450R) * (VSNR - VGSN) + VGSN$	
PRNO 6-0 = 0111111	$((350R - 126R) / 450R) * (VSNR - VGSN) + VGSN$	
PRNO 6-0 = 1000000	$((350R - 128R) / 450R) * (VSNR - VGSN) + VGSN$	
PRNO 6-0 = 1000001	$((350R - 130R) / 450R) * (VSNR - VGSN) + VGSN$	
PRNO 6-0 = 1000010	$((350R - 132R) / 450R) * (VSNR - VGSN) + VGSN$	
PRNO 6-0 = 1000011	$((350R - 134R) / 450R) * (VSNR - VGSN) + VGSN$	
PRNO 6-0 = 1000100	$((350R - 136R) / 450R) * (VSNR - VGSN) + VGSN$	
PRNO 6-0 = 1000101	$((350R - 138R) / 450R) * (VSNR - VGSN) + VGSN$	

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PRN0 6-0 = 1000110	((350R - 140R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1000111	((350R - 142R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1001000	((350R - 144R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1001001	((350R - 146R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1001010	((350R - 148R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1001011	((350R - 150R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1001100	((350R - 152R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1001101	((350R - 154R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1001110	((350R - 156R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1001111	((350R - 158R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1010000	((350R - 160R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1010001	((350R - 162R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1010010	((350R - 164R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1010011	((350R - 166R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1010100	((350R - 168R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1010101	((350R - 170R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1010110	((350R - 172R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1010111	((350R - 174R) / 450R) * (VSNR - VGSN) + VGSN
PRN0 6-0 = 1011000	-
PRN0 6-0 = 1011001	-
PRN0 6-0 = 1011010	-
PRN0 6-0 = 1011011	-
PRN0 6-0 = 1011100	-
PRN0 6-0 = 1011101	-
PRN0 6-0 = 1011110	-
PRN0 6-0 = 1011111	-
PRN0 6-0 = 1100000	-
PRN0 6-0 = 1100001	-
PRN0 6-0 = 1100010	-
PRN0 6-0 = 1100011	-
PRN0 6-0 = 1100100	-
PRN0 6-0 = 1100101	-
PRN0 6-0 = 1100110	-
PRN0 6-0 = 1100111	-
PRN0 6-0 = 1101000	-
PRN0 6-0 = 1101001	-
PRN0 6-0 = 1101010	-
PRN0 6-0 = 1101011	-
PRN0 6-0 = 1101100	-
PRN0 6-0 = 1101101	-
PRN0 6-0 = 1101110	-
PRN0 6-0 = 1101111	-
PRN0 6-0 = 1110000	-
PRN0 6-0 = 1110001	-
PRN0 6-0 = 1110010	-
PRN0 6-0 = 1110011	-
PRN0 6-0 = 1110100	-
PRN0 6-0 = 1110101	-
PRN0 6-0 = 1110110	-
PRN0 6-0 = 1110111	-
PRN0 6-0 = 1111000	-
PRN0 6-0 = 1111001	-
PRN0 6-0 = 1111010	-
PRN0 6-0 = 1111011	-
PRN0 6-0 = 1111100	-
PRN0 6-0 = 1111101	-
PRN0 6-0 = 1111110	-
PRN0 6-0 = 1111111	-

Table 5.27: VinN5

Reference Voltage	Macro Adjustment Value	VinN11 Formula
VinN11	PRN1 6-0 = 0000000	(274R / 450R) (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000001	((274R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000010	((274R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000011	((274R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 00000100	((274R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 00000101	((274R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 00000110	((274R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 00000111	((274R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001000	((274R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001001	((274R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001010	((274R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001011	((274R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001100	((274R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001101	((274R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001110	((274R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001111	((274R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010000	((274R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010001	((274R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010010	((274R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010011	((274R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010100	((274R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010101	((274R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010110	((274R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010111	((274R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011000	((274R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011001	((274R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011010	((274R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011011	((274R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011100	((274R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011101	((274R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011110	((274R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011111	((274R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100000	((274R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100001	((274R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100010	((274R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100011	((274R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100100	((274R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100101	((274R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100110	((274R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100111	((274R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101000	((274R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101001	((274R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101010	((274R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101011	((274R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101100	((274R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101101	((274R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101110	((274R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101111	((274R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110000	((274R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110001	((274R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110010	((274R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110011	((274R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110100	((274R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110101	((274R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110110	((274R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110111	((274R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111000	((274R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111001	((274R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111010	((274R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111011	((274R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111100	((274R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111101	((274R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111110	((274R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111111	((274R - 126R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000000	((274R - 128R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000001	((274R - 130R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000010	((274R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000011	((274R - 134R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000100	((274R - 136R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000101	((274R - 138R) / 450R) * (VSNR - VGSN) + VGSN

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PRN1 6-0 = 1000110	((274R - 140R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1000111	((274R - 142R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1001000	((274R - 144R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1001001	((274R - 146R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1001010	((274R - 148R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1001011	((274R - 150R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1001100	((274R - 152R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1001101	((274R - 154R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1001110	((274R - 156R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1001111	((274R - 158R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1010000	((274R - 160R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1010001	((274R - 162R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1010010	((274R - 164R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1010011	((274R - 166R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1010100	((274R - 168R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1010101	((274R - 170R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1010110	((274R - 172R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1010111	((274R - 174R) / 450R) * (VSNR - VGSN) + VGSN
PRN1 6-0 = 1011000	-
PRN1 6-0 = 1011001	-
PRN1 6-0 = 1011010	-
PRN1 6-0 = 1011011	-
PRN1 6-0 = 1011100	-
PRN1 6-0 = 1011101	-
PRN1 6-0 = 1011110	-
PRN1 6-0 = 1011111	-
PRN1 6-0 = 1100000	-
PRN1 6-0 = 1100001	-
PRN1 6-0 = 1100010	-
PRN1 6-0 = 1100011	-
PRN1 6-0 = 1100100	-
PRN1 6-0 = 1100101	-
PRN1 6-0 = 1100110	-
PRN1 6-0 = 1100111	-
PRN1 6-0 = 1101000	-
PRN1 6-0 = 1101001	-
PRN1 6-0 = 1101010	-
PRN1 6-0 = 1101011	-
PRN1 6-0 = 1101100	-
PRN1 6-0 = 1101101	-
PRN1 6-0 = 1101110	-
PRN1 6-0 = 1101111	-
PRN1 6-0 = 1110000	-
PRN1 6-0 = 1110001	-
PRN1 6-0 = 1110010	-
PRN1 6-0 = 1110011	-
PRN1 6-0 = 1110100	-
PRN1 6-0 = 1110101	-
PRN1 6-0 = 1110110	-
PRN1 6-0 = 1110111	-
PRN1 6-0 = 1111000	-
PRN1 6-0 = 1111001	-
PRN1 6-0 = 1111010	-
PRN1 6-0 = 1111011	-
PRN1 6-0 = 1111100	-
PRN1 6-0 = 1111101	-
PRN1 6-0 = 1111110	-
PRN1 6-0 = 1111111	-

Table 5.28: VinN 11

Reference Voltage	Macro Adjustment Value	VinN3 Formula
VinN3	PKNO 4-0 = 00000	$(47R / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00001	$((47R - 1R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00010	$((47R - 2R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00011	$((47R - 3R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00100	$((47R - 4R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00101	$((47R - 5R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00110	$((47R - 6R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00111	$((47R - 7R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01000	$((47R - 8R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01001	$((47R - 9R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01010	$((47R - 10R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01011	$((47R - 11R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01100	$((47R - 12R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01101	$((47R - 13R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01110	$((47R - 14R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01111	$((47R - 15R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10000	$((47R - 16R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10001	$((47R - 17R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10010	$((47R - 18R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10011	$((47R - 19R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10100	$((47R - 20R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10101	$((47R - 21R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10110	$((47R - 22R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10111	$((47R - 23R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11000	$((47R - 24R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11001	$((47R - 25R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11010	$((47R - 26R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11011	$((47R - 27R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11100	$((47R - 28R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11101	$((47R - 29R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11110	$((47R - 30R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11111	$((47R - 31R) / 48R) * (VinN2 - VinN5) + VinN5$

Table 5.29: VinN 3

Reference Voltage	Macro Adjustment Value	VinN4 Formula
VinN4	PKN1 4-0 = 00000	$(32R / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00001	$((32R - 1R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00010	$((32R - 2R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00011	$((32R - 3R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00100	$((32R - 4R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00101	$((32R - 5R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00110	$((32R - 6R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00111	$((32R - 7R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01000	$((32R - 8R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01001	$((32R - 9R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01010	$((32R - 10R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01011	$((32R - 11R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01100	$((32R - 12R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01101	$((32R - 13R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01110	$((32R - 14R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01111	$((32R - 15R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10000	$((32R - 16R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10001	$((32R - 17R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10010	$((32R - 18R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10011	$((32R - 19R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10100	$((32R - 20R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10101	$((32R - 21R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10110	$((32R - 22R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10111	$((32R - 23R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11000	$((32R - 24R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11001	$((32R - 25R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11010	$((32R - 26R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11011	$((32R - 27R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11100	$((32R - 28R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11101	$((32R - 29R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11110	$((32R - 30R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11111	$((32R - 31R) / 48R) * (VinN2 - VinN5) + VinN5$

Table 5.30: VinN 4

Reference Voltage	Macro Adjustment Value	VinN6 Formula
VinN6	PKN2 4-0 = 00000	$(220R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00001	$((220R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00010	$((220R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00011	$((220R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00100	$((220R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00101	$((220R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00110	$((220R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00111	$((220R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01000	$((220R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01001	$((220R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01010	$((220R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01011	$((220R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01100	$((220R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01101	$((220R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01110	$((220R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01111	$((220R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10000	$((220R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10001	$((220R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10010	$((220R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10011	$((220R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10100	$((220R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10101	$((220R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10110	$((220R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10111	$((220R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11000	$((220R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11001	$((220R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11010	$((220R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11011	$((220R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11100	$((220R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11101	$((220R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11110	$((220R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11111	$((220R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.31: VinN 6

Reference Voltage	Macro Adjustment Value	VinN7 Formula
VinN7	PKN3 4-0 = 00000	$(193R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00001	$((193R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00010	$((193R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00011	$((193R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00100	$((193R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00101	$((193R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00110	$((193R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00111	$((193R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01000	$((193R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01001	$((193R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01010	$((193R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01011	$((193R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01100	$((193R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01101	$((193R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01110	$((193R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01111	$((193R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10000	$((193R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10001	$((193R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10010	$((193R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10011	$((193R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10100	$((193R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10101	$((193R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10110	$((193R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10111	$((193R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11000	$((193R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11001	$((193R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11010	$((193R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11011	$((193R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11100	$((193R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11101	$((193R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11110	$((193R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11111	$((193R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.32: VinN 7

Reference Voltage	Macro Adjustment Value	VinN8 Formula
VinN8	PKN4 4-0 = 00000	$(158R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00001	$((158R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00010	$((158R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00011	$((158R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00100	$((158R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00101	$((158R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00110	$((158R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00111	$((158R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01000	$((158R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01001	$((158R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01010	$((158R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01011	$((158R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01100	$((158R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01101	$((158R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01110	$((158R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01111	$((158R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10000	$((158R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10001	$((158R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10010	$((158R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10011	$((158R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10100	$((158R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10101	$((158R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10110	$((158R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10111	$((158R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11000	$((158R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11001	$((158R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11010	$((158R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11011	$((158R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11100	$((158R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11101	$((158R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11110	$((158R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11111	$((158R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.33: VinN 8

Reference Voltage	Macro Adjustment Value	VinN9 Formula
VinN9	PKN5 4-0 = 00000	$(123R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00001	$((123R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00010	$((123R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00011	$((123R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00100	$((123R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00101	$((123R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00110	$((123R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00111	$((123R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01000	$((123R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01001	$((123R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01010	$((123R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01011	$((123R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01100	$((123R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01101	$((123R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01110	$((123R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01111	$((123R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10000	$((123R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10001	$((123R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10010	$((123R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10011	$((123R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10100	$((123R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10101	$((123R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10110	$((123R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10111	$((123R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11000	$((123R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11001	$((123R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11010	$((123R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11011	$((123R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11100	$((123R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11101	$((123R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11110	$((123R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11111	$((123R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.34: VinN 9

Reference Voltage	Macro Adjustment Value	VinN10 Formula
VinN10	PKN6 4-0 = 00000	$(96R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00001	$((96R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00010	$((96R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00011	$((96R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00100	$((96R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00101	$((96R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00110	$((96R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00111	$((96R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01000	$((96R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01001	$((96R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01010	$((96R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01011	$((96R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01100	$((96R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01101	$((96R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01110	$((96R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01111	$((96R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10000	$((96R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10001	$((96R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10010	$((96R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10011	$((96R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10100	$((96R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10101	$((96R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10110	$((96R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10111	$((96R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11000	$((96R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11001	$((96R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11010	$((96R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11011	$((96R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11100	$((96R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11101	$((96R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11110	$((96R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11111	$((96R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.35: VinN 10

Reference Voltage	Macro Adjustment Value	VinN12 Formula
VinN12	PKN7 4-0 = 00000	$(47R / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00001	$((47R - 1R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00010	$((47R - 2R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00011	$((47R - 3R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00100	$((47R - 4R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00101	$((47R - 5R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00110	$((47R - 6R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00111	$((47R - 7R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01000	$((47R - 8R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01001	$((47R - 9R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01010	$((47R - 10R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01011	$((47R - 11R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01100	$((47R - 12R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01101	$((47R - 13R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01110	$((47R - 14R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01111	$((47R - 15R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10000	$((47R - 16R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10001	$((47R - 17R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10010	$((47R - 18R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10011	$((47R - 19R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10100	$((47R - 20R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10101	$((47R - 21R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10110	$((47R - 22R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10111	$((47R - 23R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11000	$((47R - 24R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11001	$((47R - 25R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11010	$((47R - 26R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11011	$((47R - 27R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11100	$((47R - 28R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11101	$((47R - 29R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11110	$((47R - 30R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11111	$((47R - 31R) / 48R) * (VinN11 - VinN14) + VinN14$

Table 5.36: VinN 12

Reference Voltage	Macro Adjustment Value	VinN13 Formula
VinN13	PKN8 4-0 = 00000	$(32R / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00001	$((32R - 1R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00010	$((32R - 2R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00011	$((32R - 3R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00100	$((32R - 4R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00101	$((32R - 5R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00110	$((32R - 6R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00111	$((32R - 7R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01000	$((32R - 8R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01001	$((32R - 9R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01010	$((32R - 10R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01011	$((32R - 11R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01100	$((32R - 12R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01101	$((32R - 13R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01110	$((32R - 14R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01111	$((32R - 15R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10000	$((32R - 16R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10001	$((32R - 17R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10010	$((32R - 18R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10011	$((32R - 19R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10100	$((32R - 20R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10101	$((32R - 21R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10110	$((32R - 22R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10111	$((32R - 23R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11000	$((32R - 24R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11001	$((32R - 25R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11010	$((32R - 26R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11011	$((32R - 27R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11100	$((32R - 28R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11101	$((32R - 29R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11110	$((32R - 30R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11111	$((32R - 31R) / 48R) * (VinN11 - VinN14) + VinN14$

Table 5.37: VinP/N 13

Grayscale Voltage	Formula
V0	VinP0
V1	VinP1
V2	VinP2
V3	VinP3
V4	$CGMP0=0 = VinP3 - (VinP3 - VinP4)*(1R/4R)$ $CGMP0=1 = VinP3 - (VinP3 - VinP4)*(3R/9.5R)$ $CGMP0=2 = VinP3 - (VinP3 - VinP4)*(3.5R/9.3R)$ $CGMP0=3 = VinP3 - (VinP3 - VinP4)*(3.5R/10R)$
V5	$CGMP0=0 = VinP3 - (VinP3 - VinP4)*(2R/4R)$ $CGMP0=1 = VinP3 - (VinP3 - VinP4)*(5.5R/9.5R)$ $CGMP0=2 = VinP3 - (VinP3 - VinP4)*(6R/9.3R)$ $CGMP0=3 = VinP3 - (VinP3 - VinP4)*(6R/10R)$
V6	$CGMP0=0 = VinP3 - (VinP3 - VinP4)*(3R/4R)$ $CGMP0=1 = VinP3 - (VinP3 - VinP4)*(7.5R/9.5R)$ $CGMP0=2 = VinP3 - (VinP3 - VinP4)*(7.8R/9.3R)$ $CGMP0=3 = VinP3 - (VinP3 - VinP4)*(8R/10R)$
V7	VinP4
V8	$CGMP2=0 = VinP4 - (VinP4 - VinP5)*(1R/6R)$ $CGMP2=1 = VinP4 - (VinP4 - VinP5)*(3R/16R)$ $CGMP2=2 = VinP4 - (VinP4 - VinP5)*(4R/18R)$ $CGMP2=3 = VinP4 - (VinP4 - VinP5)*(4.5R/19.5R)$
V9	$CGMP2=0 = VinP4 - (VinP4 - VinP5)*(2R/6R)$ $CGMP2=1 = VinP4 - (VinP4 - VinP5)*(6R/16R)$ $CGMP2=2 = VinP4 - (VinP4 - VinP5)*(7R/18R)$ $CGMP2=3 = VinP4 - (VinP4 - VinP5)*(8.5R/19.5R)$
V10	$CGMP2=0 = VinP4 - (VinP4 - VinP5)*(3R/6R)$ $CGMP2=1 = VinP4 - (VinP4 - VinP5)*(8.5R/16R)$ $CGMP2=2 = VinP4 - (VinP4 - VinP5)*(10R/18R)$ $CGMP2=3 = VinP4 - (VinP4 - VinP5)*(11.5R/19.5R)$
V11	$CGMP2=0 = VinP4 - (VinP4 - VinP5)*(4R/6R)$ $CGMP2=1 = VinP4 - (VinP4 - VinP5)*(11R/16R)$ $CGMP2=2 = VinP4 - (VinP4 - VinP5)*(13R/18R)$ $CGMP2=3 = VinP4 - (VinP4 - VinP5)*(14.5R/19.5R)$
V12	$CGMP2=0 = VinP4 - (VinP4 - VinP5)*(5R/6R)$ $CGMP2=1 = VinP4 - (VinP4 - VinP5)*(13.5R/16R)$ $CGMP2=2 = VinP4 - (VinP4 - VinP5)*(15.5R/18R)$ $CGMP2=3 = VinP4 - (VinP4 - VinP5)*(17R/19.5R)$
V13	VinP5
V14	$CGMP4=0 = VinP5 - (VinP5 - VinP6)*(1R/6R)$ $CGMP4=1 = VinP5 - (VinP5 - VinP6)*(1.5R/6.5R)$
V15	$CGMP4=0 = VinP5 - (VinP5 - VinP6)*(2R/6R)$ $CGMP4=1 = VinP5 - (VinP5 - VinP6)*(2.5R/6.5R)$

Grayscale Voltage	Formula
V16	$CGMP4=0 = VinP5 - (VinP5 - VinP6)*(3R/6R)$ $CGMP4=1 = VinP5 - (VinP5 - VinP6)*(3.5R/6.5R)$
V17	$CGMP4=0 = VinP5 - (VinP5 - VinP6)*(4R/6R)$ $CGMP4=1 = VinP5 - (VinP5 - VinP6)*(4.5R/6.5R)$
V18	$CGMP4=0 = VinP5 - (VinP5 - VinP6)*(5R/6R)$ $CGMP4=1 = VinP5 - (VinP5 - VinP6)*(5.5R/6.5R)$
V19	VinP6
V20	$VinP6 - (VinP6 - VinP7)*(1R/6R)$
V21	$VinP6 - (VinP6 - VinP7)*(2R/6R)$
V22	$VinP6 - (VinP6 - VinP7)*(3R/6R)$
V23	$VinP6 - (VinP6 - VinP7)*(4R/6R)$ $VinP6 - (VinP6 - VinP7)*(5R/6R)$
V24	VinP7
V25	VinP7
V26	$VinP7 - (VinP7 - VinP8)*(1R/7.5R)$
V27	$VinP7 - (VinP7 - VinP8)*(2R/7.5R)$
V28	$VinP7 - (VinP7 - VinP8)*(3R/7.5R)$
V29	$VinP7 - (VinP7 - VinP8)*(4R/7.5R)$
V30	$VinP7 - (VinP7 - VinP8)*(5R/7.5R)$
V31	$VinP7 - (VinP7 - VinP8)*(6R/7.5R)$
V32	VinP8
V33	$VinP8 - (VinP8 - VinP9)*(1R/6R)$
V34	$VinP8 - (VinP8 - VinP9)*(2R/6R)$
V35	$VinP8 - (VinP8 - VinP9)*(3R/6R)$
V36	$VinP8 - (VinP8 - VinP9)*(4R/6R)$
V37	$VinP8 - (VinP8 - VinP9)*(5R/6R)$
V38	VinP9
V39	$VinP9 - (VinP9 - VinP10)*(1R/6R)$
V40	$VinP9 - (VinP9 - VinP10)*(2R/6R)$
V41	$VinP9 - (VinP9 - VinP10)*(3R/6R)$
V42	$VinP9 - (VinP9 - VinP10)*(4R/6R)$
V43	$VinP9 - (VinP9 - VinP10)*(5R/6R)$
V44	VinP10
V45	$CGMP5=0 = VinP10 - (VinP10 - VinP11)*(1R/6R)$ $CGMP5=1 = VinP10 - (VinP10 - VinP11)*(1R/6.5R)$
V46	$CGMP5=0 = VinP10 - (VinP10 - VinP11)*(2R/6R)$ $CGMP5=1 = VinP10 - (VinP10 - VinP11)*(2R/6.5R)$
V47	$CGMP5=0 = VinP10 - (VinP10 - VinP11)*(3R/6R)$ $CGMP5=1 = VinP10 - (VinP10 - VinP11)*(3R/6.5R)$
V48	$CGMP5=0 = VinP10 - (VinP10 - VinP11)*(4R/6R)$ $CGMP5=1 = VinP10 - (VinP10 - VinP11)*(4R/6.5R)$
V49	$CGMP5=0 = VinP10 - (VinP10 - VinP11)*(5R/6R)$ $CGMP5=1 = VinP10 - (VinP10 - VinP11)*(5R/6.5R)$

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V50	VinP11	V56	VinP12
V51	$CGMP3=0 = VinP11 - (VinP11 - VinP12) * (1R/6R)$ $CGMP3=1 = VinP11 - (VinP11 - VinP12) * (2.5R/16R)$ $CGMP3=2 = VinP11 - (VinP11 - VinP12) * (2.5R/18R)$ $CGMP3=3 = VinP11 - (VinP11 - VinP12) * (2.5R/19.5R)$	V57	$CGMP1=0 = VinP12 - (VinP12 - VinP13) * (1R/4R)$ $CGMP1=1 = VinP12 - (VinP12 - VinP13) * (2R/9.5R)$ $CGMP1=2 = VinP12 - (VinP12 - VinP13) * (1.5R/9.3R)$ $CGMP1=3 = VinP12 - (VinP12 - VinP13) * (2R/10R)$
V52	$CGMP3=0 = VinP11 - (VinP11 - VinP12) * (2R/6R)$ $CGMP3=1 = VinP11 - (VinP11 - VinP12) * (5R/16R)$ $CGMP3=2 = VinP11 - (VinP11 - VinP12) * (5R/18R)$ $CGMP3=3 = VinP11 - (VinP11 - VinP12) * (5R/19.5R)$	V58	$CGMP1=0 = VinP12 - (VinP12 - VinP13) * (2R/4R)$ $CGMP1=1 = VinP12 - (VinP12 - VinP13) * (4R/9.5R)$ $CGMP1=2 = VinP12 - (VinP12 - VinP13) * (3.3R/9.3R)$ $CGMP1=3 = VinP12 - (VinP12 - VinP13) * (4R/10R)$
V53	$CGMP3=0 = VinP11 - (VinP11 - VinP12) * (3R/6R)$ $CGMP3=1 = VinP11 - (VinP11 - VinP12) * (7.5R/16R)$ $CGMP3=2 = VinP11 - (VinP11 - VinP12) * (8R/18R)$ $CGMP3=3 = VinP11 - (VinP11 - VinP12) * (8R/19.5R)$	V59	$CGMP1=0 = VinP12 - (VinP12 - VinP13) * (3R/4R)$ $CGMP1=1 = VinP12 - (VinP12 - VinP13) * (6.5R/9.5R)$ $CGMP1=2 = VinP12 - (VinP12 - VinP13) * (5.8R/9.3R)$ $CGMP1=3 = VinP12 - (VinP12 - VinP13) * (6.5R/10R)$
V54	$CGMP3=0 = VinP11 - (VinP11 - VinP12) * (4R/6R)$ $CGMP3=1 = VinP11 - (VinP11 - VinP12) * (10R/16R)$ $CGMP3=2 = VinP11 - (VinP11 - VinP12) * (11R/18R)$ $CGMP3=3 = VinP11 - (VinP11 - VinP12) * (11R/19.5R)$	V60	VinP13
V55	$CGMP3=0 = VinP11 - (VinP11 - VinP12) * (5R/6R)$ $CGMP3=1 = VinP11 - (VinP11 - VinP12) * (13R/16R)$ $CGMP3=2 = VinP11 - (VinP11 - VinP12) * (14R/18R)$ $CGMP3=3 = VinP11 - (VinP11 - VinP12) * (15R/19.5R)$	V61	VinP14
		V62	VinP15
		V63	VinP16

Table 5.38: Voltage Calculation Formula of 64-Grayscale Voltage (Positive Polarity)

Grayscale Voltage	Formula
V0	VinN0
V1	VinN1
V2	VinN2
V3	VinN3
V4	$CGMN0=0 = VinN3 - (VinN3 - VinN4)*(1R/4R)$ $CGMN0=1 = VinN3 - (VinN3 - VinN4)*(3R/9.5R)$ $CGMN0=2 = VinN3 - (VinN3 - VinN4)*(3.5R/9.3R)$ $CGMN0=3 = VinN3 - (VinN3 - VinN4)*(3.5R/10R)$
V5	$CGMN0=0 = VinN3 - (VinN3 - VinN4)*(2R/4R)$ $CGMN0=1 = VinN3 - (VinN3 - VinN4)*(5.5R/9.5R)$ $CGMN0=2 = VinN3 - (VinN3 - VinN4)*(6R/9.3R)$ $CGMN0=3 = VinN3 - (VinN3 - VinN4)*(6R/10R)$
V6	$CGMN0=0 = VinN3 - (VinN3 - VinN4)*(3R/4R)$ $CGMN0=1 = VinN3 - (VinN3 - VinN4)*(7.5R/9.5R)$ $CGMN0=2 = VinN3 - (VinN3 - VinN4)*(7.8R/9.3R)$ $CGMN0=3 = VinN3 - (VinN3 - VinN4)*(8R/10R)$
V7	VinN4
V8	$CGMN2=0 = VinN4 - (VinN4 - VinN5)*(1R/6R)$ $CGMN2=1 = VinN4 - (VinN4 - VinN5)*(3R/16R)$ $CGMN2=2 = VinN4 - (VinN4 - VinN5)*(4R/18R)$ $CGMN2=3 = VinN4 - (VinN4 - VinN5)*(4.5R/19.5R)$
V9	$CGMN2=0 = VinN4 - (VinN4 - VinN5)*(2R/6R)$ $CGMN2=1 = VinN4 - (VinN4 - VinN5)*(6R/16R)$ $CGMN2=2 = VinN4 - (VinN4 - VinN5)*(7R/18R)$ $CGMN2=3 = VinN4 - (VinN4 - VinN5)*(8.5R/19.5R)$
V10	$CGMN2=0 = VinN4 - (VinN4 - VinN5)*(3R/6R)$ $CGMN2=1 = VinN4 - (VinN4 - VinN5)*(8.5R/16R)$ $CGMN2=2 = VinN4 - (VinN4 - VinN5)*(10R/18R)$ $CGMN2=3 = VinN4 - (VinN4 - VinN5)*(11.5R/19.5R)$
V11	$CGMN2=0 = VinN4 - (VinN4 - VinN5)*(4R/6R)$ $CGMN2=1 = VinN4 - (VinN4 - VinN5)*(11R/16R)$ $CGMN2=2 = VinN4 - (VinN4 - VinN5)*(13R/18R)$ $CGMN2=3 = VinN4 - (VinN4 - VinN5)*(14.5R/19.5R)$
V12	$CGMN2=0 = VinN4 - (VinN4 - VinN5)*(5R/6R)$ $CGMN2=1 = VinN4 - (VinN4 - VinN5)*(13.5R/16R)$ $CGMN2=2 = VinN4 - (VinN4 - VinN5)*(15.5R/18R)$ $CGMN2=3 = VinN4 - (VinN4 - VinN5)*(17R/19.5R)$
V13	VinN5
V14	$CGMN4=0 = VinN5 - (VinN5 - VinN6)*(1R/6R)$ $CGMN4=1 = VinN5 - (VinN5 - VinN6)*(1.5R/6.5R)$
V15	$CGMN4=0 = VinN5 - (VinN5 - VinN6)*(2R/6R)$ $CGMN4=1 = VinN5 - (VinN5 - VinN6)*(2.5R/6.5R)$

Grayscale Voltage	Formula
V16	$CGMN4=0 = VinN5 - (VinN5 - VinN6)*(3R/6R)$ $CGMN4=1 = VinN5 - (VinN5 - VinN6)*(3.5R/6.5R)$
V17	$CGMN4=0 = VinN5 - (VinN5 - VinN6)*(4R/6R)$ $CGMN4=1 = VinN5 - (VinN5 - VinN6)*(4.5R/6.5R)$
V18	$CGMN4=0 = VinN5 - (VinN5 - VinN6)*(5R/6R)$ $CGMN4=1 = VinN5 - (VinN5 - VinN6)*(5.5R/6.5R)$
V19	VinN6
V20	$VinN6 - (VinN6 - VinN7)*(1R/6R)$
V21	$VinN6 - (VinN6 - VinN7)*(2R/6R)$
V22	$VinN6 - (VinN6 - VinN7)*(3R/6R)$
V23	$VinN6 - (VinN6 - VinN7)*(4R/6R)$
V24	$VinN6 - (VinN6 - VinN7)*(5R/6R)$
V25	VinN7
V26	$VinN7 - (VinN7 - VinN8)*(1R/7.5R)$
V27	$VinN7 - (VinN7 - VinN8)*(2R/7.5R)$
V28	$VinN7 - (VinN7 - VinN8)*(3R/7.5R)$
V29	$VinN7 - (VinN7 - VinN8)*(4R/7.5R)$
V30	$VinN7 - (VinN7 - VinN8)*(5R/7.5R)$
V31	$VinN7 - (VinN7 - VinN8)*(6R/7.5R)$
V32	VinN8
V33	$VinN8 - (VinN8 - VinN9)*(1R/6R)$
V34	$VinN8 - (VinN8 - VinN9)*(2R/6R)$
V35	$VinN8 - (VinN8 - VinN9)*(3R/6R)$
V36	$VinN8 - (VinN8 - VinN9)*(4R/6R)$
V37	$VinN8 - (VinN8 - VinN9)*(5R/6R)$
V38	VinN9
V39	$VinN9 - (VinN9 - VinN10)*(1R/6R)$
V40	$VinN9 - (VinN9 - VinN10)*(2R/6R)$
V41	$VinN9 - (VinN9 - VinN10)*(3R/6R)$
V42	$VinN9 - (VinN9 - VinN10)*(4R/6R)$
V43	$VinN9 - (VinN9 - VinN10)*(5R/6R)$
V44	VinN10
V45	$CGMN5=0 = VinN10 - (VinN10 - VinN11)*(1R/6R)$ $CGMN5=1 = VinN10 - (VinN10 - VinN11)*(1R/6.5R)$
V46	$CGMN5=0 = VinN10 - (VinN10 - VinN11)*(2R/6R)$ $CGMN5=1 = VinN10 - (VinN10 - VinN11)*(2R/6.5R)$
V47	$CGMN5=0 = VinN10 - (VinN10 - VinN11)*(3R/6R)$ $CGMN5=1 = VinN10 - (VinN10 - VinN11)*(3R/6.5R)$
V48	$CGMN5=0 = VinN10 - (VinN10 - VinN11)*(4R/6R)$ $CGMN5=1 = VinN10 - (VinN10 - VinN11)*(4R/6.5R)$
V49	$CGMN5=0 = VinN10 - (VinN10 - VinN11)*(5R/6R)$ $CGMN5=1 = VinN10 - (VinN10 - VinN11)*(5R/6.5R)$

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V50	VinN11	V56	VinN12
V51	$CGMN3=0 = VinN11 - (VinN11 - VinN12) * (1R/6R)$ $CGMN3=1 = VinN11 - (VinN11 - VinN12) * (2.5R/16R)$ $CGMN3=2 = VinN11 - (VinN11 - VinN12) * (2.5R/18R)$ $CGMN3=3 = VinN11 - (VinN11 - VinN12) * (2.5R/19.5R)$	V57	$CGMN1=0 = VinN12 - (VinN12 - VinN13) * (1R/4R)$ $CGMN1=1 = VinN12 - (VinN12 - VinN13) * (2R/9.5R)$ $CGMN1=2 = VinN12 - (VinN12 - VinN13) * (1.5R/9.3R)$ $CGMN1=3 = VinN12 - (VinN12 - VinN13) * (2R/10R)$
V52	$CGMN3=0 = VinN11 - (VinN11 - VinN12) * (2R/6R)$ $CGMN3=1 = VinN11 - (VinN11 - VinN12) * (5R/16R)$ $CGMN3=2 = VinN11 - (VinN11 - VinN12) * (5R/18R)$ $CGMN3=3 = VinN11 - (VinN11 - VinN12) * (5R/19.5R)$	V58	$CGMN1=0 = VinN12 - (VinN12 - VinN13) * (2R/4R)$ $CGMN1=1 = VinN12 - (VinN12 - VinN13) * (4R/9.5R)$ $CGMN1=2 = VinN12 - (VinN12 - VinN13) * (3.3R/9.3R)$ $CGMN1=3 = VinN12 - (VinN12 - VinN13) * (4R/10R)$
V53	$CGMN3=0 = VinN11 - (VinN11 - VinN12) * (3R/6R)$ $CGMN3=1 = VinN11 - (VinN11 - VinN12) * (7.5R/16R)$ $CGMN3=2 = VinN11 - (VinN11 - VinN12) * (8R/18R)$ $CGMN3=3 = VinN11 - (VinN11 - VinN12) * (8R/19.5R)$	V59	$CGMN1=0 = VinN12 - (VinN12 - VinN13) * (3R/4R)$ $CGMN1=1 = VinN12 - (VinN12 - VinN13) * (6.5R/9.5R)$ $CGMN1=2 = VinN12 - (VinN12 - VinN13) * (5.8R/9.3R)$ $CGMN1=3 = VinN12 - (VinN12 - VinN13) * (6.5R/10R)$
V54	$CGMN3=0 = VinN11 - (VinN11 - VinN12) * (4R/6R)$ $CGMN3=1 = VinN11 - (VinN11 - VinN12) * (10R/16R)$ $CGMN3=2 = VinN11 - (VinN11 - VinN12) * (11R/18R)$ $CGMN3=3 = VinN11 - (VinN11 - VinN12) * (11R/19.5R)$	V60	VinN13
V55	$CGMN3=0 = VinN11 - (VinN11 - VinN12) * (5R/6R)$ $CGMN3=1 = VinN11 - (VinN11 - VinN12) * (13R/16R)$ $CGMN3=2 = VinN11 - (VinN11 - VinN12) * (14R/18R)$ $CGMN3=3 = VinN11 - (VinN11 - VinN12) * (15R/19.5R)$	V61	VinN14
		V62	VinN15
		V63	VinN16

Table 5.39: Voltage Calculation Formula of 64-Grayscale Voltage (Negative Polarity)

Grayscale Voltage	Formula
VV0	V0
VV1	V0 - (V0 - V1)*(4R/16R)
VV2	V0 - (V0 - V1)*(8R/16R)
VV3	V0 - (V0 - V1)*(12R/16R)
VV4	V1
VV5	V1 - (V1 - V2)*(4R/16R)
VV6	V1 - (V1 - V2)*(8R/16R)
VV7	V1 - (V1 - V2)*(12R/16R)
VV8	V2
VV9	V2 - (V2 - V3)*(4R/16R)
VV10	V2 - (V2 - V3)*(8R/16R)
VV11	V2 - (V2 - V3)*(12R/16R)
VV12	V3
VV13	V3 - (V3 - V4)*(2R/8R)
VV14	V3 - (V3 - V4)*(4R/8R)
VV15	V3 - (V3 - V4)*(6R/8R)
VV16	V4
VV17	V4 - (V4 - V5)*(2R/8R)
VV18	V4 - (V4 - V5)*(4R/8R)
VV19	V4 - (V4 - V5)*(6R/8R)
VV20	V5
VV21	V5 - (V5 - V6)*(2R/8R)
VV22	V5 - (V5 - V6)*(4R/8R)
VV23	V5 - (V5 - V6)*(6R/8R)
VV24	V6
VV25	V6 - (V6 - V7)*(2R/8R)
VV26	V6 - (V6 - V7)*(4R/8R)
VV27	V6 - (V6 - V7)*(6R/8R)
VV28	V7
VV29	V7 - (V7 - V8)*(1.6R/6.4R)
VV30	V7 - (V7 - V8)*(3.2R/6.4R)
VV31	V7 - (V7 - V8)*(4.8R/6.4R)
VV32	V8
VV33	V8 - (V8 - V9)*(1.6R/6.4R)
VV34	V8 - (V8 - V9)*(3.2R/6.4R)
VV35	V8 - (V8 - V9)*(4.8R/6.4R)
VV36	V9
VV37	V9 - (V9 - V10)*(1.6R/6.4R)
VV38	V9 - (V9 - V10)*(3.2R/6.4R)
VV39	V9 - (V9 - V10)*(4.8R/6.4R)
VV40	V10
VV41	V10 - (V10 - V11)*(1.6R/6.4R)
VV42	V10 - (V10 - V11)*(3.2R/6.4R)
VV43	V10 - (V10 - V11)*(4.8R/6.4R)

Grayscale Voltage	Formula
VV44	V11
VV45	V11 - (V11 - V12)*(1.6R/6.4R)
VV46	V11 - (V11 - V12)*(3.2R/6.4R)
VV47	V11 - (V11 - V12)*(4.8R/6.4R)
VV48	V12
VV49	V12 - (V12 - V13)*(1.6R/6.4R)
VV50	V12 - (V12 - V13)*(3.2R/6.4R)
VV51	V12 - (V12 - V13)*(4.8R/6.4R)
VV52	V13
VV53	V13 - (V13 - V14)*(1.6R/6.4R)
VV54	V13 - (V13 - V14)*(3.2R/6.4R)
VV55	V13 - (V13 - V14)*(4.8R/6.4R)
VV56	V14
VV57	V14 - (V14 - V15)*(1.6R/6.4R)
VV58	V14 - (V14 - V15)*(3.2R/6.4R)
VV59	V14 - (V14 - V15)*(4.8R/6.4R)
VV60	V15
VV61	V15 - (V15 - V16)*(1.6R/6.4R)
VV62	V15 - (V15 - V16)*(3.2R/6.4R)
VV63	V15 - (V15 - V16)*(4.8R/6.4R)
VV64	V16
VV65	V16 - (V16 - V17)*(1.6R/6.4R)
VV66	V16 - (V16 - V17)*(3.2R/6.4R)
VV67	V16 - (V16 - V17)*(4.8R/6.4R)
VV68	V17
VV69	V17 - (V17 - V18)*(1.6R/6.4R)
VV70	V17 - (V17 - V18)*(3.2R/6.4R)
VV71	V17 - (V17 - V18)*(4.8R/6.4R)
VV72	V18
VV73	V18 - (V18 - V19)*(1.6R/6.4R)
VV74	V18 - (V18 - V19)*(3.2R/6.4R)
VV75	V18 - (V18 - V19)*(4.8R/6.4R)
VV76	V19
VV77	V19 - (V19 - V20)*(1.6R/6.4R)
VV78	V19 - (V19 - V20)*(3.2R/6.4R)
VV79	V19 - (V19 - V20)*(4.8R/6.4R)
VV80	V20
VV81	V20 - (V20 - V21)*(1.6R/6.4R)
VV82	V20 - (V20 - V21)*(3.2R/6.4R)
VV83	V20 - (V20 - V21)*(4.8R/6.4R)
VV84	V21
VV85	V21 - (V21 - V22)*(1.6R/6.4R)
VV86	V21 - (V21 - V22)*(3.2R/6.4R)
VV87	V21 - (V21 - V22)*(4.8R/6.4R)

Grayscale Voltage	Formula
VV88	V22
VV89	V22 - (V22 - V23)*(1.6R/6.4R)
VV90	V22 - (V22 - V23)*(3.2R/6.4R)
VV91	V22 - (V22 - V23)*(4.8R/6.4R)
VV92	V23
VV93	V23 - (V23 - V24)*(1.6R/6.4R)
VV94	V23 - (V23 - V24)*(3.2R/6.4R)
VV95	V23 - (V23 - V24)*(4.8R/6.4R)
VV96	V24
VV97	V24 - (V24 - V25)*(1.6R/6.4R)
VV98	V24 - (V24 - V25)*(3.2R/6.4R)
VV99	V24 - (V24 - V25)*(4.8R/6.4R)
VV100	V25
VV101	V25 - (V25 - V26)*(1.6R/6.4R)
VV102	V25 - (V25 - V26)*(3.2R/6.4R)
VV103	V25 - (V25 - V26)*(4.8R/6.4R)
VV104	V26
VV105	V26 - (V26 - V27)*(1.6R/6.4R)
VV106	V26 - (V26 - V27)*(3.2R/6.4R)
VV107	V26 - (V26 - V27)*(4.8R/6.4R)
VV108	V27
VV109	V27 - (V27 - V28)*(1.6R/6.4R)
VV110	V27 - (V27 - V28)*(3.2R/6.4R)
VV111	V27 - (V27 - V28)*(4.8R/6.4R)
VV112	V28
VV113	V28 - (V28 - V29)*(1.6R/6.4R)
VV114	V28 - (V28 - V29)*(3.2R/6.4R)
VV115	V28 - (V28 - V29)*(4.8R/6.4R)
VV116	V29
VV117	V29 - (V29 - V30)*(1.6R/6.4R)
VV118	V29 - (V29 - V30)*(3.2R/6.4R)
VV119	V29 - (V29 - V30)*(4.8R/6.4R)
VV120	V30
VV121	V30 - (V30 - V31)*(1.6R/6.4R)
VV122	V30 - (V30 - V31)*(3.2R/6.4R)
VV123	V30 - (V30 - V31)*(4.8R/6.4R)
VV124	V31
VV125	V31 - (V31 - V32)*(1.6R/11.2R)
VV126	V31 - (V31 - V32)*(3.2R/11.2R)
VV127	V31 - (V31 - V32)*(4.8R/11.2R)
VV128	V31 - (V31 - V32)*(6.4R/11.2R)
VV129	V31 - (V31 - V32)*(8R/11.2R)
VV130	V31 - (V31 - V32)*(9.6R/11.2R)
VV131	V32

Grayscale Voltage	Formula
VV132	V32 - (V32 - V33)*(1.6R/6.4R)
VV133	V32 - (V32 - V33)*(3.2R/6.4R)
VV134	V32 - (V32 - V33)*(4.8R/6.4R)
VV135	V33
VV136	V33 - (V33 - V34)*(1.6R/6.4R)
VV137	V33 - (V33 - V34)*(3.2R/6.4R)
VV138	V33 - (V33 - V34)*(4.8R/6.4R)
VV139	V34
VV140	V34 - (V34 - V35)*(1.6R/6.4R)
VV141	V34 - (V34 - V35)*(3.2R/6.4R)
VV142	V34 - (V34 - V35)*(4.8R/6.4R)
VV143	V35
VV144	V35 - (V35 - V36)*(1.6R/6.4R)
VV145	V35 - (V35 - V36)*(3.2R/6.4R)
VV146	V35 - (V35 - V36)*(4.8R/6.4R)
VV147	V36
VV148	V36 - (V36 - V37)*(1.6R/6.4R)
VV149	V36 - (V36 - V37)*(3.2R/6.4R)
VV150	V36 - (V36 - V37)*(4.8R/6.4R)
VV151	V37
VV152	V37 - (V37 - V38)*(1.6R/6.4R)
VV153	V37 - (V37 - V38)*(3.2R/6.4R)
VV154	V37 - (V37 - V38)*(4.8R/6.4R)
VV155	V38
VV156	V38 - (V38 - V39)*(1.6R/6.4R)
VV157	V38 - (V38 - V39)*(3.2R/6.4R)
VV158	V38 - (V38 - V39)*(4.8R/6.4R)
VV159	V39
VV160	V39 - (V39 - V40)*(1.6R/6.4R)
VV161	V39 - (V39 - V40)*(3.2R/6.4R)
VV162	V39 - (V39 - V40)*(4.8R/6.4R)
VV163	V40
VV164	V40 - (V40 - V41)*(1.6R/6.4R)
VV165	V40 - (V40 - V41)*(3.2R/6.4R)
VV166	V40 - (V40 - V41)*(4.8R/6.4R)
VV167	V41
VV168	V41 - (V41 - V42)*(1.6R/6.4R)
VV169	V41 - (V41 - V42)*(3.2R/6.4R)
VV170	V41 - (V41 - V42)*(4.8R/6.4R)
VV171	V42
VV172	V42 - (V42 - V43)*(1.6R/6.4R)
VV173	V42 - (V42 - V43)*(3.2R/6.4R)
VV174	V42 - (V42 - V43)*(4.8R/6.4R)
VV175	V43

Grayscale Voltage	Formula
VV176	$V43 - (V43 - V44) * (1.6R/6.4R)$
VV177	$V43 - (V43 - V44) * (3.2R/6.4R)$
VV178	$V43 - (V43 - V44) * (4.8R/6.4R)$
VV179	$V44$
VV180	$V44 - (V44 - V45) * (1.6R/6.4R)$
VV181	$V44 - (V44 - V45) * (3.2R/6.4R)$
VV182	$V44 - (V44 - V45) * (4.8R/6.4R)$
VV183	$V45$
VV184	$V45 - (V45 - V46) * (1.6R/6.4R)$
VV185	$V45 - (V45 - V46) * (3.2R/6.4R)$
VV186	$V45 - (V45 - V46) * (4.8R/6.4R)$
VV187	$V46$
VV188	$V46 - (V46 - V47) * (1.6R/6.4R)$
VV189	$V46 - (V46 - V47) * (3.2R/6.4R)$
VV190	$V46 - (V46 - V47) * (4.8R/6.4R)$
VV191	$V47$
VV192	$V47 - (V47 - V48) * (1.6R/6.4R)$
VV193	$V47 - (V47 - V48) * (3.2R/6.4R)$
VV194	$V47 - (V47 - V48) * (4.8R/6.4R)$
VV195	$V48$
VV196	$V48 - (V48 - V49) * (1.6R/6.4R)$
VV197	$V48 - (V48 - V49) * (3.2R/6.4R)$
VV198	$V48 - (V48 - V49) * (4.8R/6.4R)$
VV199	$V49$
VV200	$V49 - (V49 - V50) * (1.6R/6.4R)$
VV201	$V49 - (V49 - V50) * (3.2R/6.4R)$
VV202	$V49 - (V49 - V50) * (4.8R/6.4R)$
VV203	$V50$
VV204	$V50 - (V50 - V51) * (1.6R/6.4R)$
VV205	$V50 - (V50 - V51) * (3.2R/6.4R)$
VV206	$V50 - (V50 - V51) * (4.8R/6.4R)$
VV207	$V51$
VV208	$V51 - (V51 - V52) * (1.6R/6.4R)$
VV209	$V51 - (V51 - V52) * (3.2R/6.4R)$
VV210	$V51 - (V51 - V52) * (4.8R/6.4R)$
VV211	$V52$
VV212	$V52 - (V52 - V53) * (1.6R/6.4R)$
VV213	$V52 - (V52 - V53) * (3.2R/6.4R)$
VV214	$V52 - (V52 - V53) * (4.8R/6.4R)$
VV215	$V53$

Grayscale Voltage	Formula
VV216	$V53 - (V53 - V54) * (1.6R/6.4R)$
VV217	$V53 - (V53 - V54) * (3.2R/6.4R)$
VV218	$V53 - (V53 - V54) * (4.8R/6.4R)$
VV219	$V54$
VV220	$V54 - (V54 - V55) * (1.6R/6.4R)$
VV221	$V54 - (V54 - V55) * (3.2R/6.4R)$
VV222	$V54 - (V54 - V55) * (4.8R/6.4R)$
VV223	$V55$
VV224	$V55 - (V55 - V56) * (1.6R/6.4R)$
VV225	$V55 - (V55 - V56) * (3.2R/6.4R)$
VV226	$V55 - (V55 - V56) * (4.8R/6.4R)$
VV227	$V56$
VV228	$V56 - (V56 - V57) * (2R/8R)$
VV229	$V56 - (V56 - V57) * (4R/8R)$
VV230	$V56 - (V56 - V57) * (6R/8R)$
VV231	$V57$
VV232	$V57 - (V57 - V58) * (2R/8R)$
VV233	$V57 - (V57 - V58) * (4R/8R)$
VV234	$V57 - (V57 - V58) * (6R/8R)$
VV235	$V58$
VV236	$V58 - (V58 - V59) * (2R/8R)$
VV237	$V58 - (V58 - V59) * (4R/8R)$
VV238	$V58 - (V58 - V59) * (6R/8R)$
VV239	$V59$
VV240	$V59 - (V59 - V60) * (2R/8R)$
VV241	$V59 - (V59 - V60) * (4R/8R)$
VV242	$V59 - (V59 - V60) * (6R/8R)$
VV243	$V60$
VV244	$V60 - (V60 - V61) * (4R/16R)$
VV245	$V60 - (V60 - V61) * (8R/16R)$
VV246	$V60 - (V60 - V61) * (12R/16R)$
VV247	$V61$
VV248	$V61 - (V61 - V62) * (4R/16R)$
VV249	$V61 - (V61 - V62) * (8R/16R)$
VV250	$V61 - (V61 - V62) * (12R/16R)$
VV251	$V62$
VV252	$V62 - (V62 - V63) * (4R/16R)$
VV253	$V62 - (V62 - V63) * (8R/16R)$
VV254	$V62 - (V62 - V63) * (12R/16R)$
VV255	$V63$

Table 5.40: Voltage Calculation Formula of 256-Grayscale Voltage (Positive/Negative Polarity)

5.3 Gamma curve

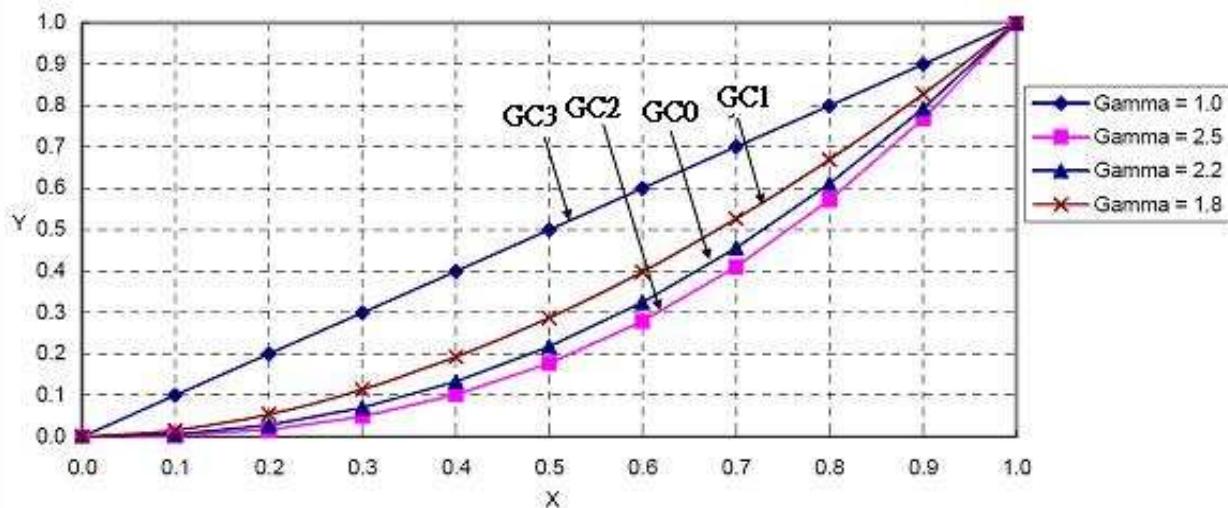


Figure 5.5: Gamma Curve according to the GC0 to GC3 Bit

5.4 Oscillator

The HX8363-A can oscillate an internal R-C oscillator with an internal oscillation resistor (R_f).

The oscillation frequency is changed according to the internal register. The default frequency is 5.5 MHz. The tolerance of internal oscillator frequency is $\pm 10\%$.

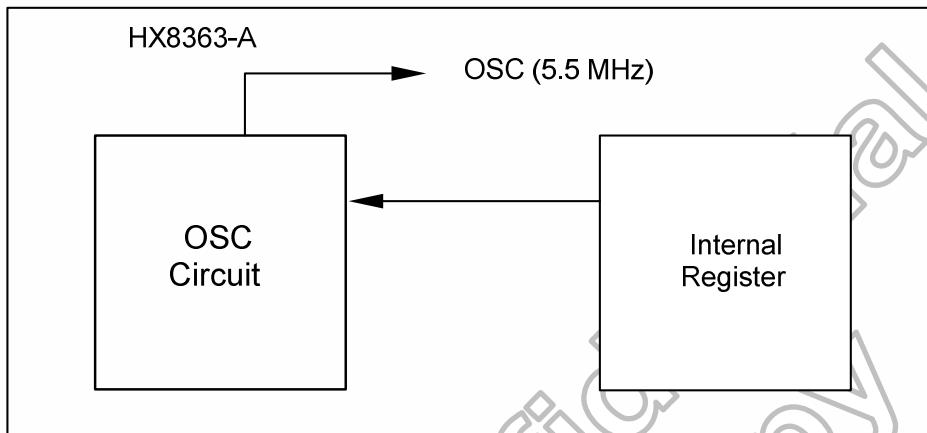


Figure 5.6: Oscillation Circuit

5.5 LCD Power Generation Scheme

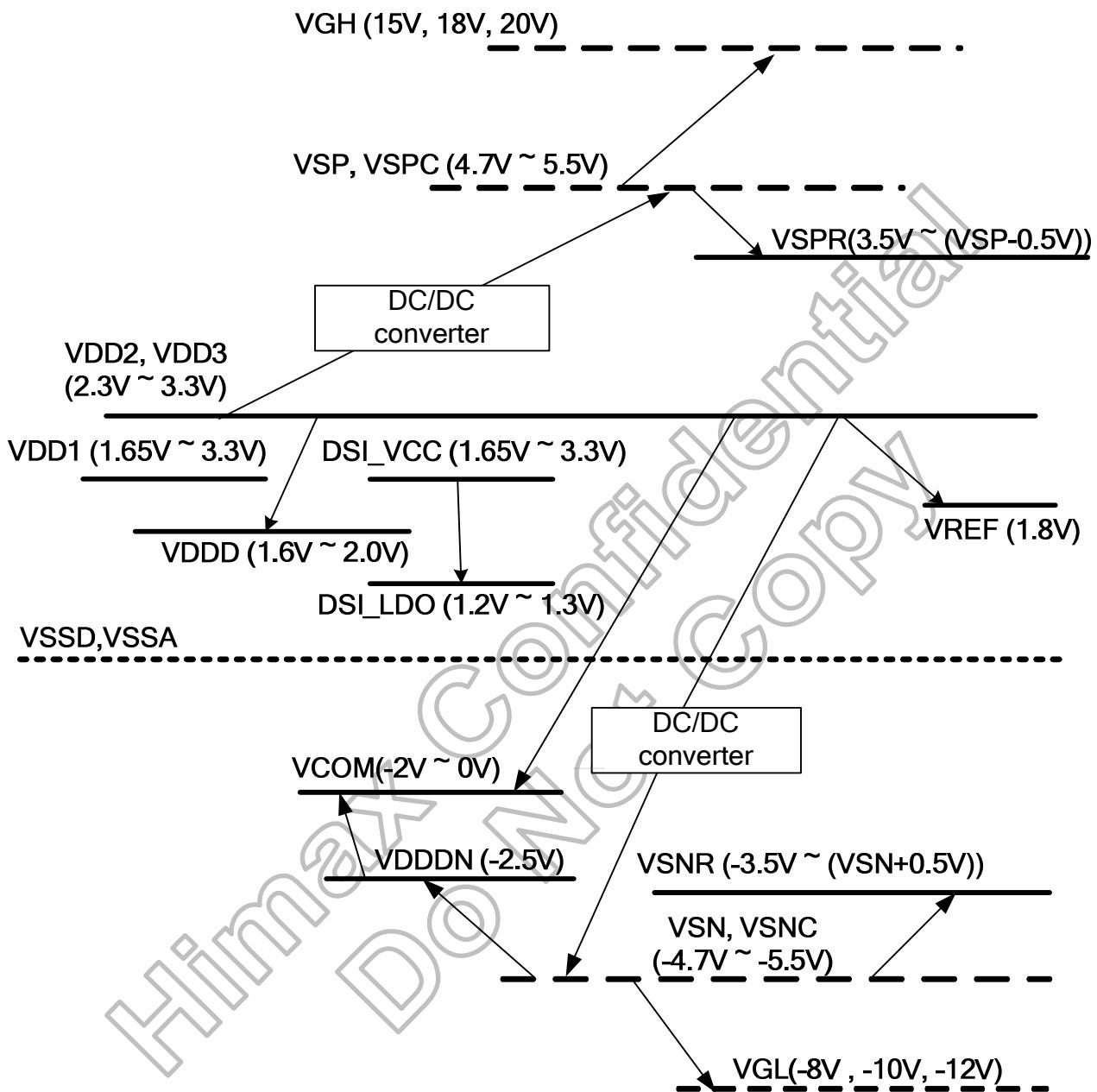


Figure 5.7: LCD Power Generation Scheme

5.6 DC/DC Converter Circuit

5.6.1 Use PFM DC/DC Converter

The PFM DC-DC converter generates the high voltage level VSP/VSN required for source drivers. HX8363-A contains sub-circuits of the PFM boost converter, including a precision 1.8V reference voltage, comparator, PFM controlling logic, and the output buffer. The boost converter uses an external power transistor to provide maximum efficiency and to minimize the number of external components. The output voltage of the boost converter can be set from 4.7 to 5.5 (VSP) and -4.7 to -5.5V (VSN).

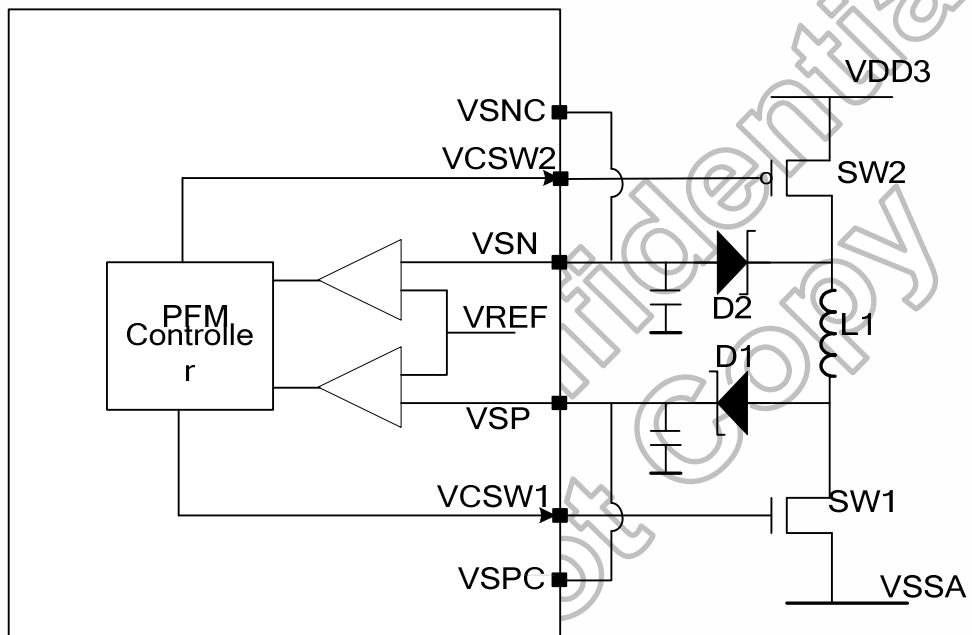


Figure 5.8: DC/DC Converter Circuit (PFM)

5.6.2 Use HX5186-A

The HX5186-A is highly efficient switching voltage generator circuits that generate the high voltage level VSP/VSN required for source drivers. HX8363-A contains Charge Pump Controller for HX5186-A, including a comparator for VSP/VSN feedback control. HX5186-A can provide maximum efficiency and use minimum number of external components. The output voltage of the boost converter can be set from 4.7 to 5.5 (VSP) and -4.7 to -5.5V (VSN)

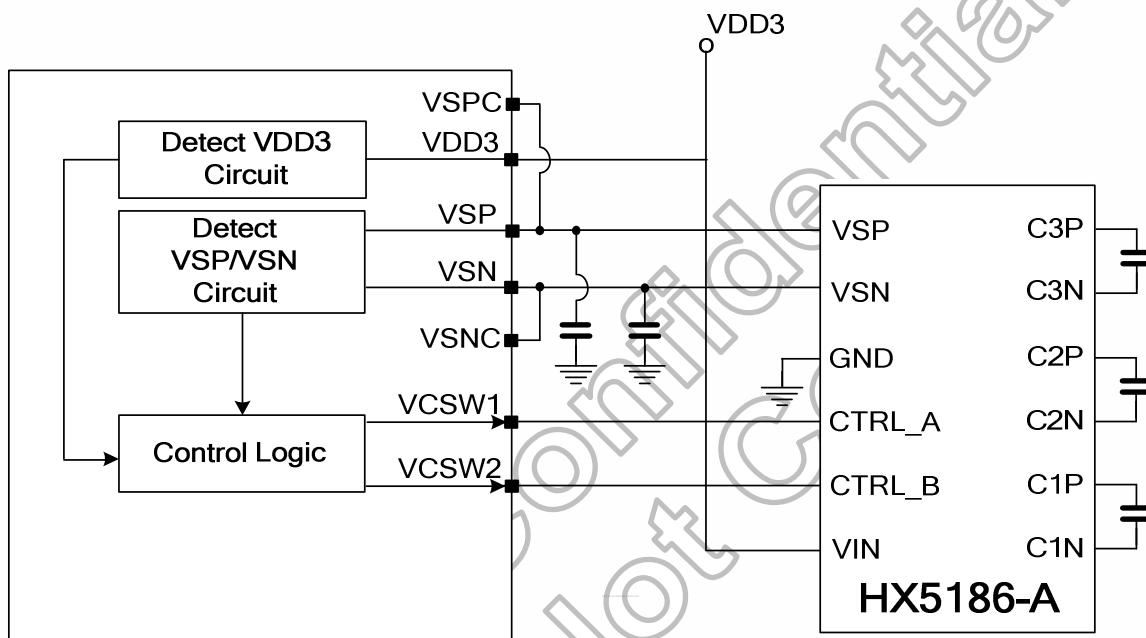


Figure 5.9: DC/DC Converter Circuit (HX5186-A)

5.7 Characteristics of I/O

5.7.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
DB23 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from DB[23...0] during Power On/Off sequences, Hardware Reset and Software Reset.

Table 5.41: Characteristics of Output or Bi-directional (I/O) Pins

5.7.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
NRESET	Section 5.18	Input valid	Input valid	Input valid	Section 5.18
NCS	Input valid	Input valid	Input valid	Input valid	Input valid
DB23 to DB0	Input valid	Input valid	Input valid	Input valid	Input valid
OSC	Input valid	Input valid	Input valid	Input valid	Input valid
TEST2-0	Low	Low	Low	TEST1	Low
HSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
VSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
ENABLE	Input valid	Input valid	Input valid	Input valid	Input valid
DCK	Input valid	Input valid	Input valid	Input valid	Input valid
SDI, SCL	Input valid	Input valid	Input valid	Input valid	Input valid

Table 5.42: Characteristics of Input Pins

5.8 Sleep Out –Command and Self-Diagnostic functions of The Display Module

5.8.1 Register Loading Detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OPT and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:

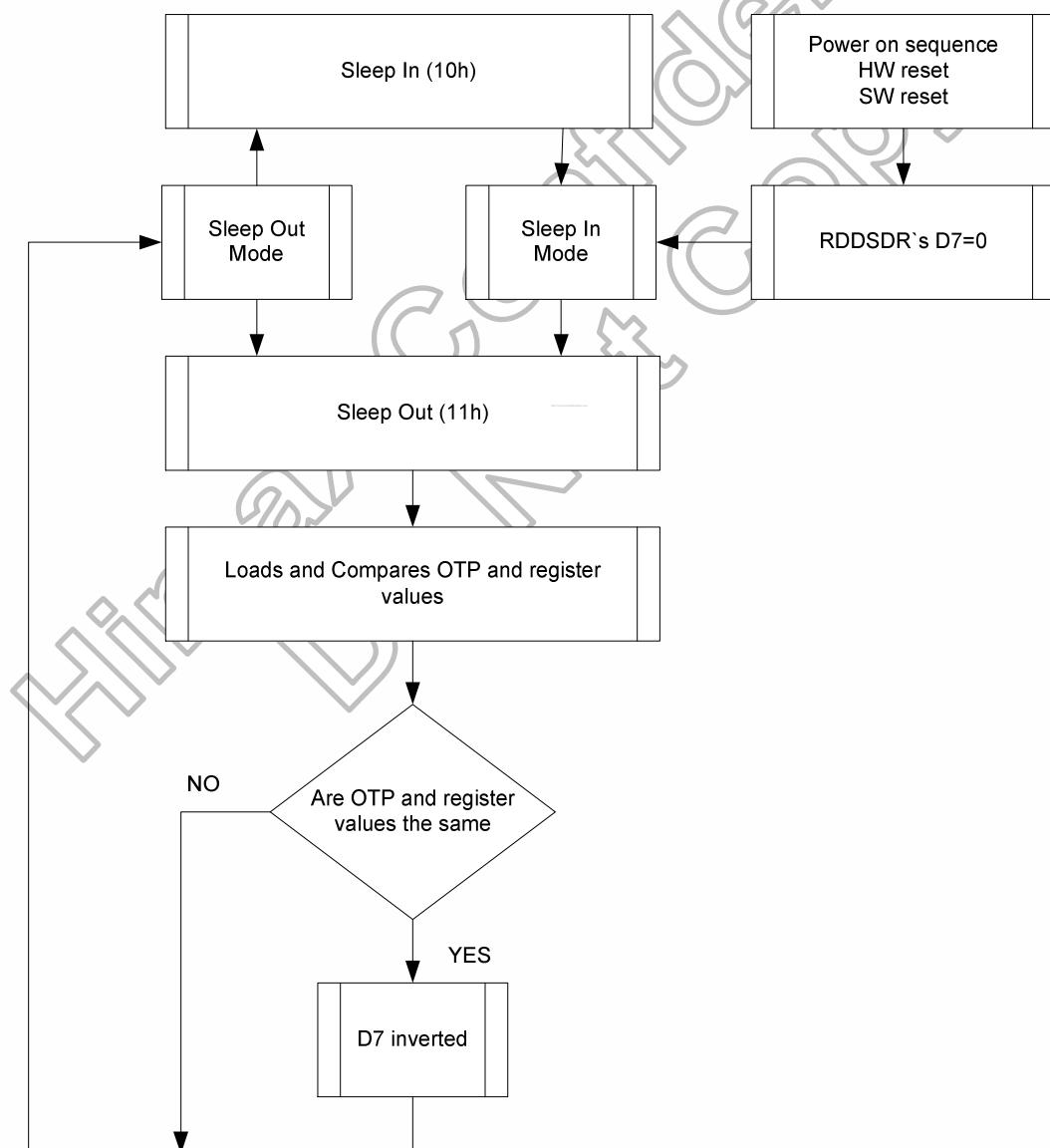
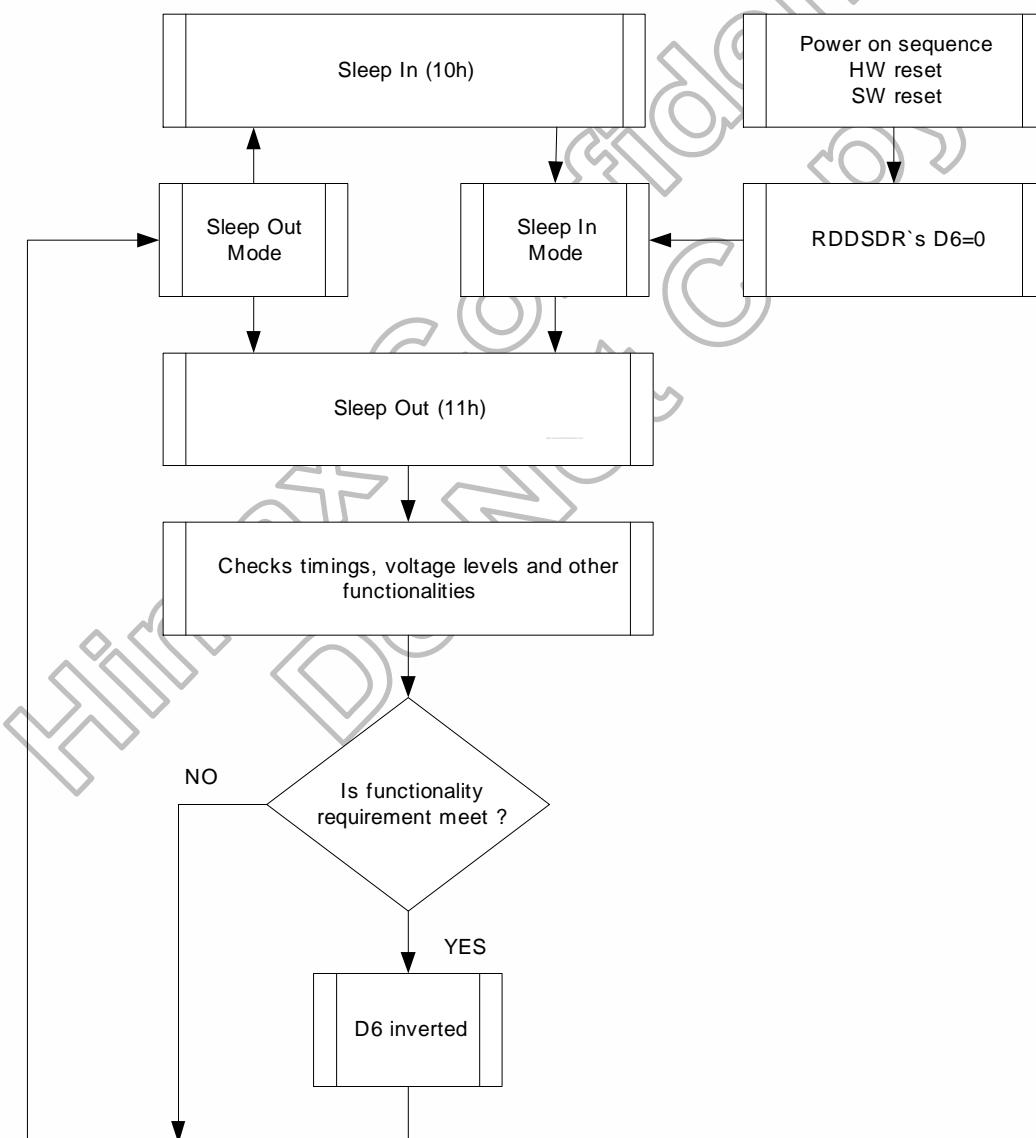


Figure 5.10: Sleep Out Flow Chart – Command and Self-Diagnostic Functions

5.8.2 Functionality Detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (= increased by 1), which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if Customer's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 5.11: Sleep Out Flow Chart Internal Function Detection

5.9 Power On/Off Sequence

VDD1, VDD2 and VDD3 can be applied in any order. VDD1, VDD2 and VDD3 can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VDD1 and VDD2 must be powered down minimum 120msec after NRESET has been released. During power off, if LCD is in the Sleep In mode, VDD1, VDD2 and VDD3 can be powered down minimum 0msec after NRESET has been released. NCS can be applied at any timing. NRESET has priority over NCS. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. If NRESET line is not held stable by host during Power On Sequence as defined in Sections 5.9.1 and 5.9.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below.

5.9.1 Case 1 – NRESET line is held High or Unstable by Host at Power On

If NRESET line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

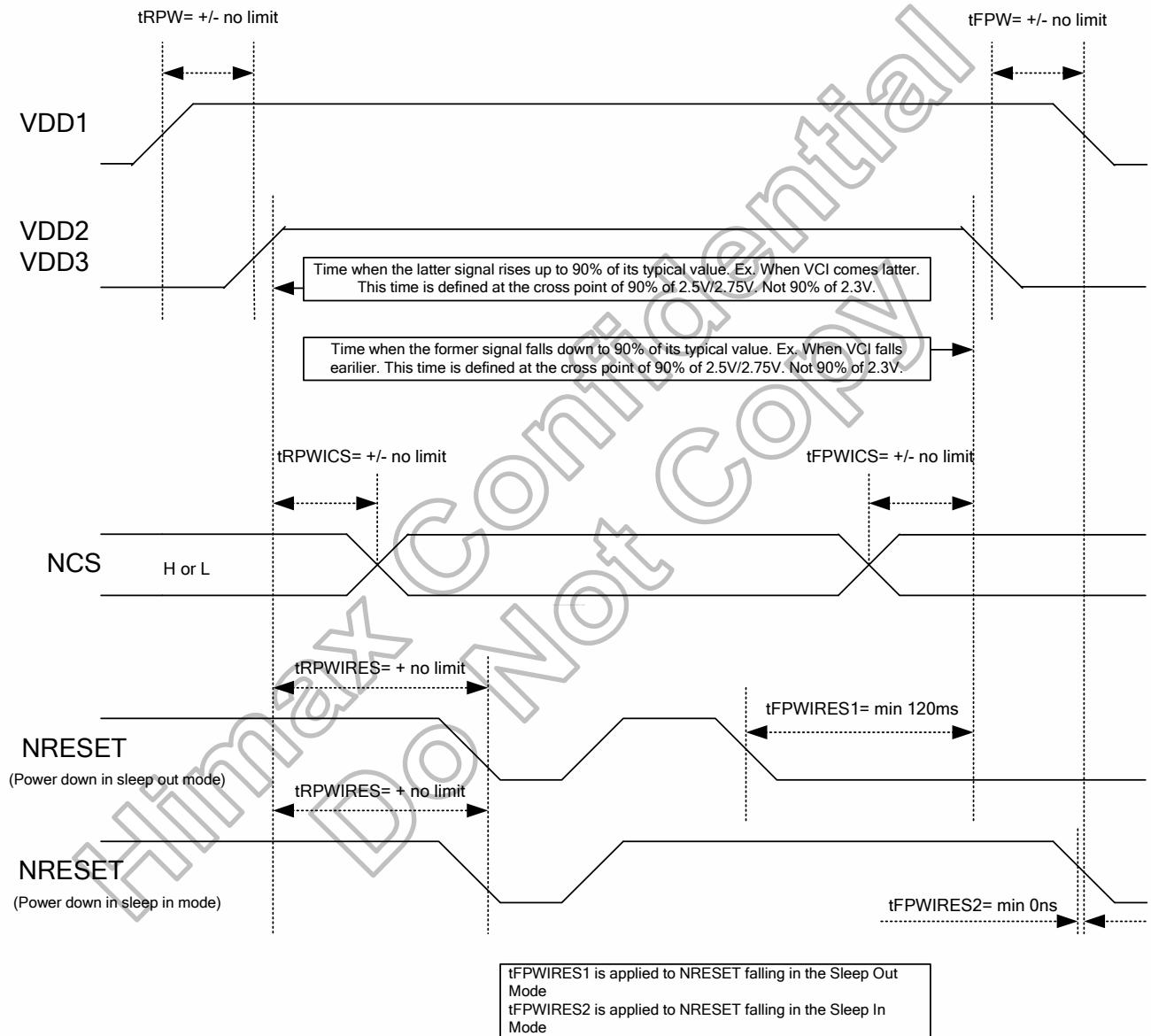


Figure 5.12: Case 1 – NRESET line is held High or Unstable by Host at Power On

5.9.2 Case 2 – NRESET line is held Low by Host at Power On

If NRESET line is held Low (and stable) by the host during Power On, then the NRESET must be held low for minimum 10 μ sec after both VDD1, VDD2 and VDD3 have been applied.

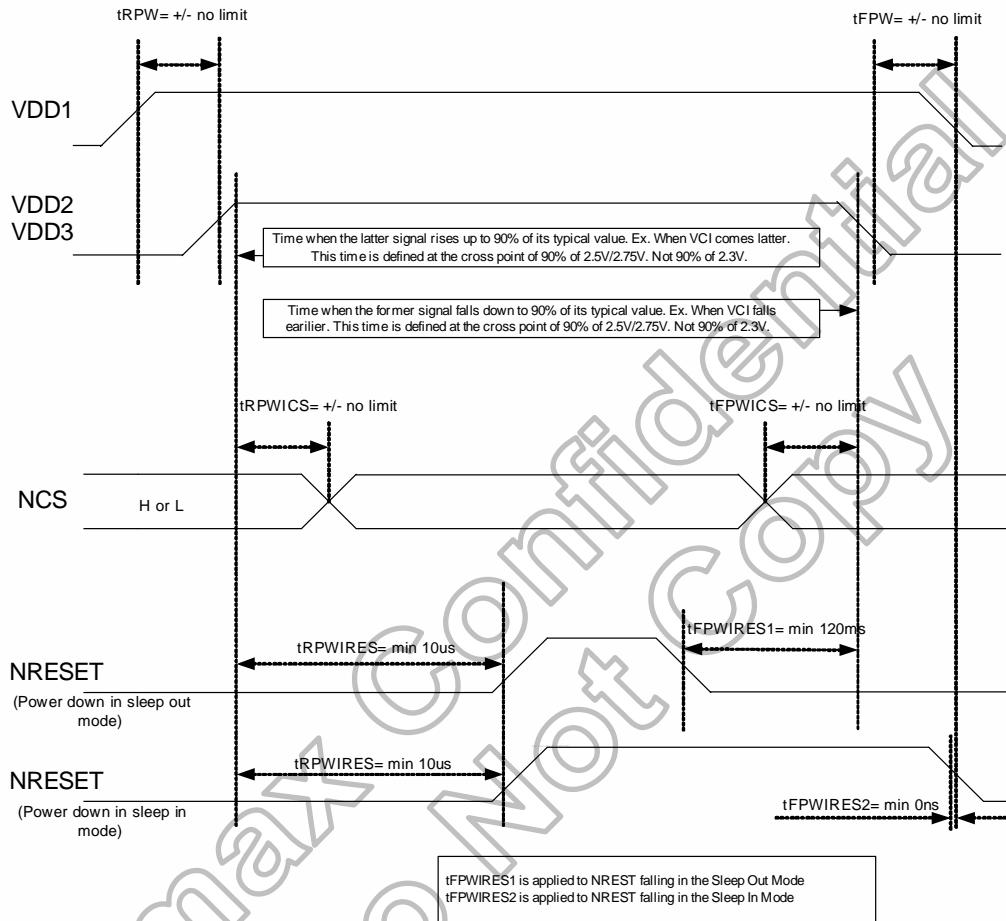
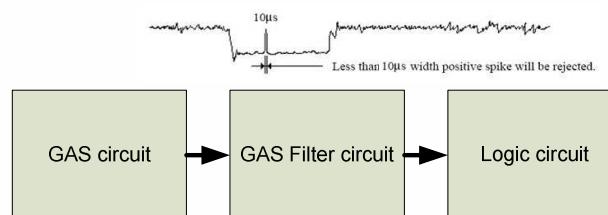


Figure 5.13: Case 2 – NRESET line is held Low by Host at Power On

5.10 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.



Note: HX8363-A is support the noise reject filter (10 μ s) to reject spike or noise.

5.11 Content Adaptive Brightness Control (CABC) Function

The general block diagram of the CABC and the brightness control is illustrated below:

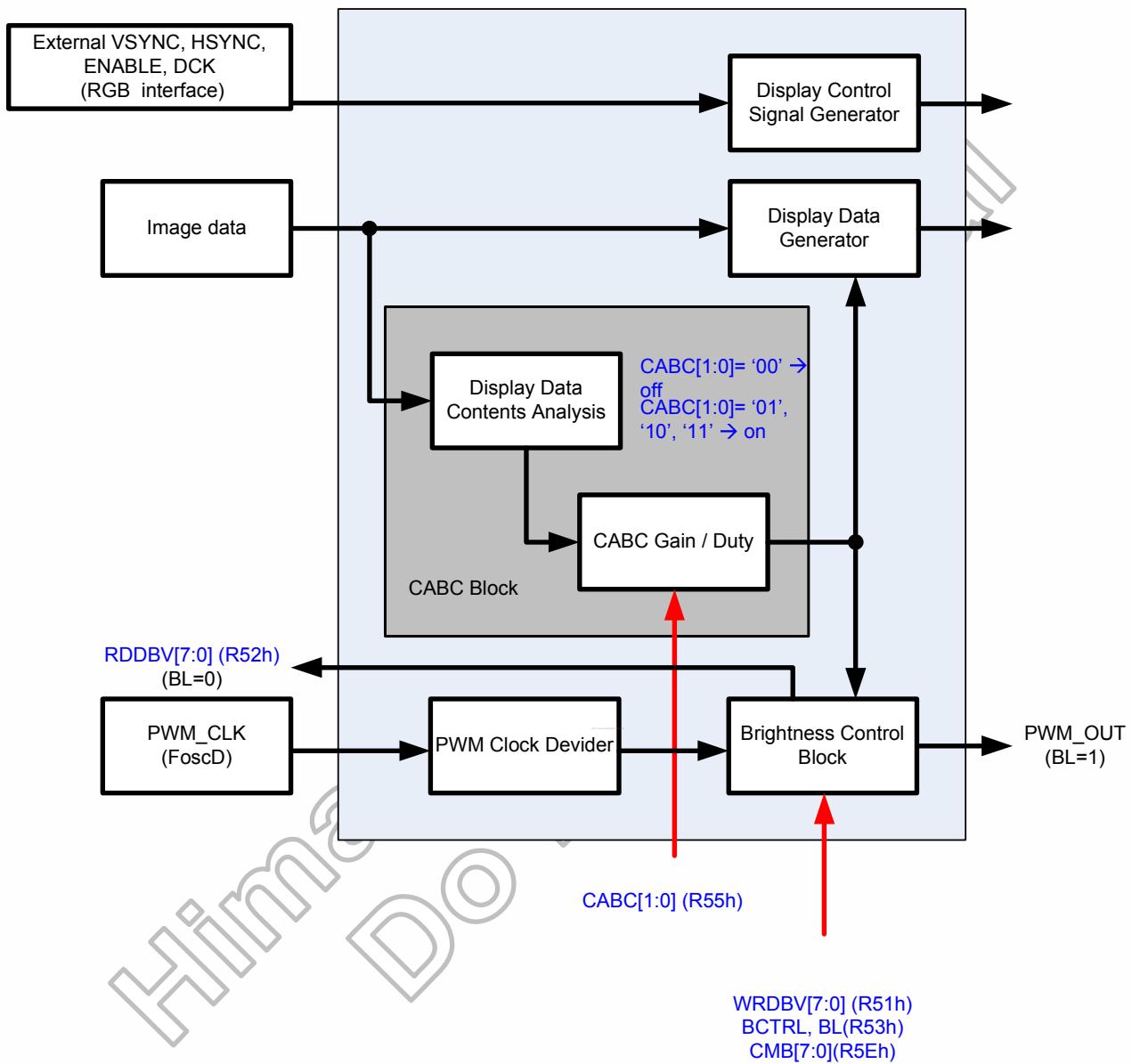
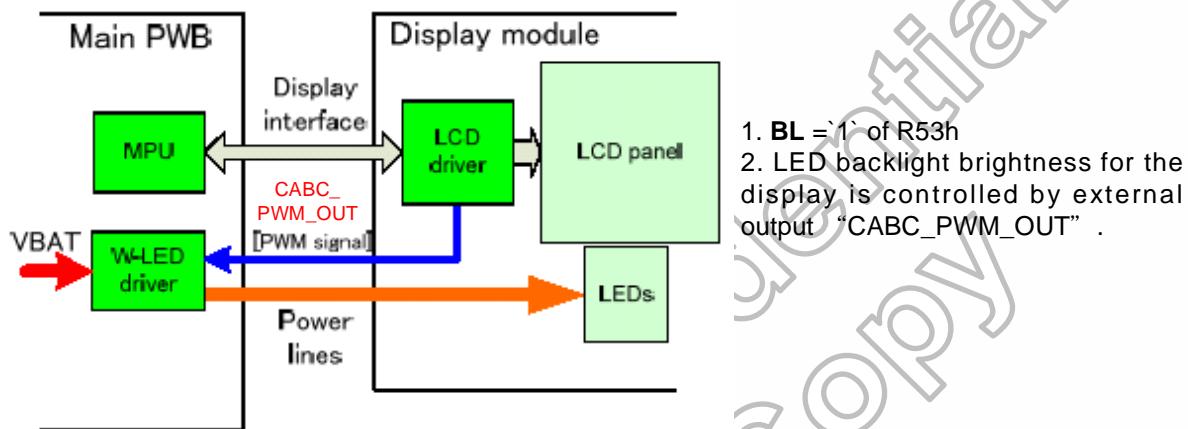


Figure 5.14: CABC Block Diagram

5.11.1 Module Architectures

HX8363-A can support two module architectures for CABC operation. The **BL** bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- Architecture I



- Architecture II

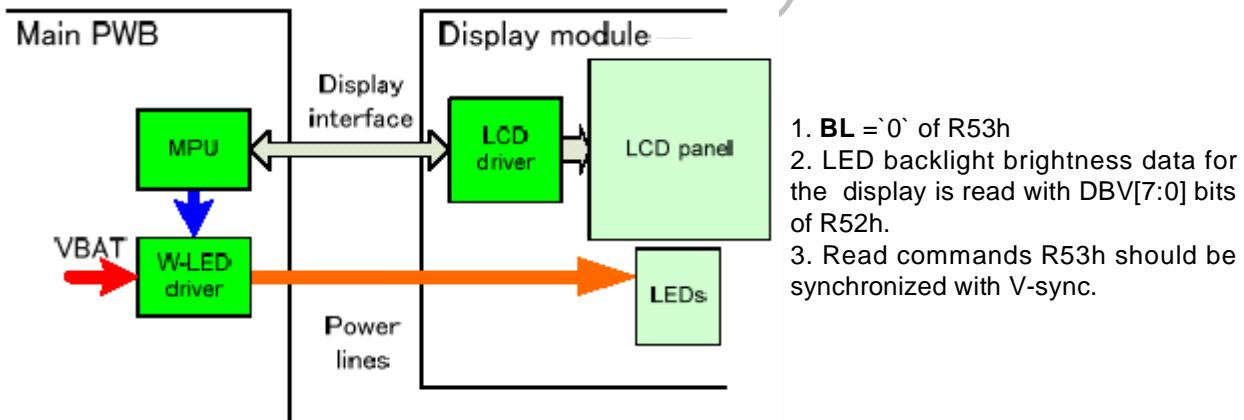


Figure 5.15: Module architecture

5.11.2 Brightness Control Block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness.

There are register bits, WRDBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as $(WRDBV[7:0])/255 \times \text{CABC duty}$ (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period = 2.95 ms, and WRDBV[7:0](R51h) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM_OUT duty = $(228) / 255 \times 74.42\% \equiv 66.54\%$. Correspond to the CABC_PWM_OUT period = 2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.96ms, and the low-level of CABC_PWM_OUT = 0.99ms.

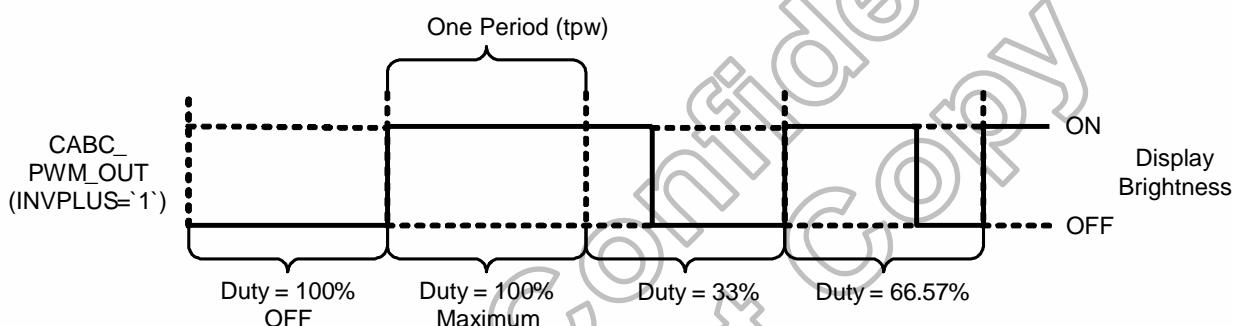


Figure 5.16: CABC_PWM_OUT Output Duty

Symbol	Parameter	Min.	Max.	unit	description
tpw	Pulse width	0.0333	8.33	ms	

Note: (1) The signal rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.

(2) The pulse width range by setting CABC related registers is located between 0.0333ms to 8.33ms.

Table 5.43: CABC timing table

When Architecture II module is used ($BL=0$) with the example below, the CABC_PWM_OUT is always output low and the WRDBV[7:0](R51h) will be read a value as 169_{DEC} ($(169)/255 \equiv 66.27\%$).

5.11.3 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (**CMB[7:0]** bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (**BCTRL='0'** of R53h), CABC minimum brightness setting is ignored. “**CMB[7:0]**, Read CABC minimum brightness (R5Fh) “always read the setting value of “**CMB[7:0]**, Write CABC minimum brightness (R5Eh)”

6. Command

6.1 Command List

6.1.1 Standard Command

(Hex)	Operation Code	DNC	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (HEX)
00	NOP	0	0	0	0	0	0	0	0	0	No operation	
01	SWRESET	0	0	0	0	0	0	0	0	1	Software reset	
06	RDRED	0	0	0	0	0	0	1	1	0	Read Red Color	
		1				R[7:0]						
07	RDGREEN	0	0	0	0	0	1	1	1	1	Read Green Color	
		1				G[7:0]						
08	RDBLUE	0	0	0	0	1	0	0	0	0	Read Blue Color	
		1				B[7:0]						
0A	RDDPM	0	0	0	0	1	0	1	0	0	Read display power mode	
		1				D[7:0]						
0B	RDDMADCTL	0	0	0	0	1	0	1	1	1	Read display MADCTL	
		1				D[7:0]						
0C	RDDCOLMOD	0	0	0	0	1	1	0	0	0	Read display pixel format	
		1				D[7:0]						
0D	RDDIM	0	0	0	0	1	1	0	1	1	Read display image mode	
		1				D[7:0]						
0E	RDDSM	0	0	0	0	1	1	1	0	0	Read Display Signal Mode	
		1				D[7:0]						
0F	RDDSDR	0	0	0	0	1	1	1	1	1	Read display self-diagnostic result	
		1				D[7:0]						
10	SLPIN	0	0	0	0	1	0	0	0	0	Sleep in and charge-pump off	
11	SLPOUT	0	0	0	0	1	0	0	0	1	Sleep out and charge-pump on	
20	INVOFF	0	0	0	1	0	0	0	0	0	Display inversion off	
21	INVON	0	0	0	1	0	0	0	0	1	Display inversion on	
26	GAMSET	0	0	0	1	0	0	1	1	0	Gamma set	
		1				GC[7:0]						
28	DISPOFF	0	0	0	1	0	1	0	0	0	Display off	
29	DISPON	0	0	0	1	0	1	0	0	1	Display on	

(Hex)	Operation Code	DNC	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (HEX)
36	MADCTL	0	0	0	1	1	0	1	1	0	Memory access control	
		1	xx	xx	xx	xx	BGR	xx	SS	GS		
3A	COLMOD	0	0	0	1	1	1	0	1	0	Interface Pixel Format	
		1	xx	CSEL_RGB[2:0](110)	xx	xx	xx	xx	xx	xx		
A1	Read_DDB_start	0	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	
		1										
		1										
		1										
		1										
		1										
A8	Read_DDB_continue	0	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	
		1										
		1										
		1										
DA	RDID1	0	1	1	0	1	1	0	1	0	Read ID1	
		1										
DB	RDID2	0	1	1	0	1	1	0	1	1	Read ID2	
		1	1									
DC	RDID3	0	1	1	0	1	1	1	0	0	Read ID3	
		1										

(Hex)	Operation Code	DNC	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (HEX)
51	WRDISBV	0	0	1	0	1	0	0	0	1	Write Display Brightness	
		1	WRDBV[7:0](00)									
52	RDDISBV	0	0	1	0	1	0	0	1	0	Read Display Brightness Value	
		1	RDDBV[7:0]									
53	WRCTRLD	0	0	1	0	1	0	0	1	1	Write CTRL Display	
		1	0	0	BCT RL	0	DD	BL	xx	xx		
54	RDCTRLD	0	0	1	0	1	0	1	0	0	Read Control Value Display	
		1	xx	xx	BCT RL	xx	DD	BL	xx	xx		
55	WRCABC	0	0	1	0	1	0	1	0	1	Write Content Adaptive Brightness Control	
		1	xx	xx	xx	xx	xx	xx	CABC[1:0](00)			
56	RDCABC	0	0	1	0	1	0	1	1	0	Read Content Adaptive Brightness Control	
		1	xx	xx	xx	xx	xx	xx	CABC[1:0]			
5E	WRCABCMB	0	0	1	0	1	1	1	1	0	Write CABC minimum brightness	
		1	CMB 7	CMB 6	CMB 5	CMB 4	CMB 3	CMB 2	CMB 1	CMB 0		
5F	RDCABCMB	0	0	1	0	1	1	1	1	1	Read CABC minimum brightness	
		1	CMB[7:0]									

Note: (1) Undefined commands are treated as NOP (00BHB) command.

(2) B0BHB to D9BHB and DEBHB to FFBHB are for factory use of display supplier. Customer can decide if these commands are available or they are treated as NOP (00BHB) commands before shipping to customer. Default value is NOP (00BHB).

6.1.2 User Define Command List Table

User define command list is available only set “SETEXC” command.

(Hex)	Operation Code	DNC	D7	D6	D5	D4	D3	D2	D1	D0	Function
B1	SETPOWER	0	1	0	1	1	0	0	0	1	Set power related setting
		1	-	VSN_EN	VSP_EN	VGL_EN	VGH_EN	-	VDDDN_HZ	SLP	
		1	-	FS12	FS11	FS10	-	AP2	AP1	AP0	
		1	-	-	-	-	BT3	BT2	BT1	BT0	
		1	DT1	DT0	DC1	DC0	DC_DIV1 V3	DC_DIV2	DC_DIV1	DC_DIV0	
		1	-	DTPS2	DTPS1	DTPS0	-	DTP2	DTP1	DTP0	
		1	-	DTNS2	DTNS1	DTNS0	-	DTN2	DTN1	DTN0	
		1	-	-	-	BTP4	BTP3	BTP2	BTP1	BTP0	
		1	-	-	-	BTN4	BTN3	BTN2	BTN1	BTN0	
		1	VRHP7	VRHP6	VRHP5	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0	
		1	VRHN7	VRHN6	VRHN5	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0	
		1	-	-	VRMP5	VRMP4	VRMP3	VRMP2	VRMP1	VRMP0	
		1	-	-	VRMN5	VRMN4	VRMN3	VRMN2	VRMN1	VRMN0	
B3	SETRGBIF	0	1	0	1	1	0	0	1	1	Set RGB interface related register)
		1	-	-	-	-	DPL(0)	HSPL(0)	VSPL(0)	EPL(1)	
B4	SETCYC	0	1	0	1	1	0	1	0	0	Set Display waveform cycles
		1	-	-	-	-	NW[1:0]	-	-	-	
		1					SON[7:0]				
		1					SOFF[7:0]				
		1					EQS[7:0]				
		1					EQON[7:0]				
		1					GDON[7:0]				
		1					GDOFF[7:0]				
		1					GVSSP1[7:0]				
		1					GVSSP2[7:0]				
B6	SETVCOM (OTPx3)	0	1	0	1	1	0	1	1	0	Set VCOM Voltage
B9	SETEXTC	1	VCMC7	VCMC 6	VCMC 5	VCMC 4	VCMC3	VCMC 2	VCMC 1	VCMC 0	Set extended command set
		0	1	0	1	1	1	0	0	1	
		1					EXTC1[7:0](00)				
		1					EXTC2[7:0](00)				
BB	SETOPT	1					EXTC3[7:0](00)				Set OTP Related Setting
		0	1	0	1	1	1	0	1	1	
		1	OTP_LO AD_DISABL E (0)	-	OTP_PC E	OTP_P WE (0)		OTP_PT M[2:0]		OTP_PR OG	
		1					OTP_MASK[7:0] (8'b0)				
		1					OTP_INDEX[7:0] (8'b1111_1111)				
		1					OTP_DATA_READ				
		1									
C1	SETDGCLUT	0	1	1	0	0	0	0	0	1	Set DGC LUT
		1	-	-	-	-	-	-	-	DGC_E N	
		1					D1[7:0]				
		1					Dn[7:0]				
C3	SETID	1					D126[7:0]				Set ID
		0	1	1	0	0	0	0	1	1	
		1					ID1[7:0](8'b0)				
		1					ID2[6:0](7'b0)				
C4	SETDDB	1					ID3[7:0](8'b0)				Set DDB
		0	1	1	0	0	0	1	0	0	
		1					DDB1[7:0](8'b0)				
		1					DDB2[7:0](8'b0)				
		1					DDB3[7:0](8'b0)				
		1					DDB4[7:0](8'b0)				

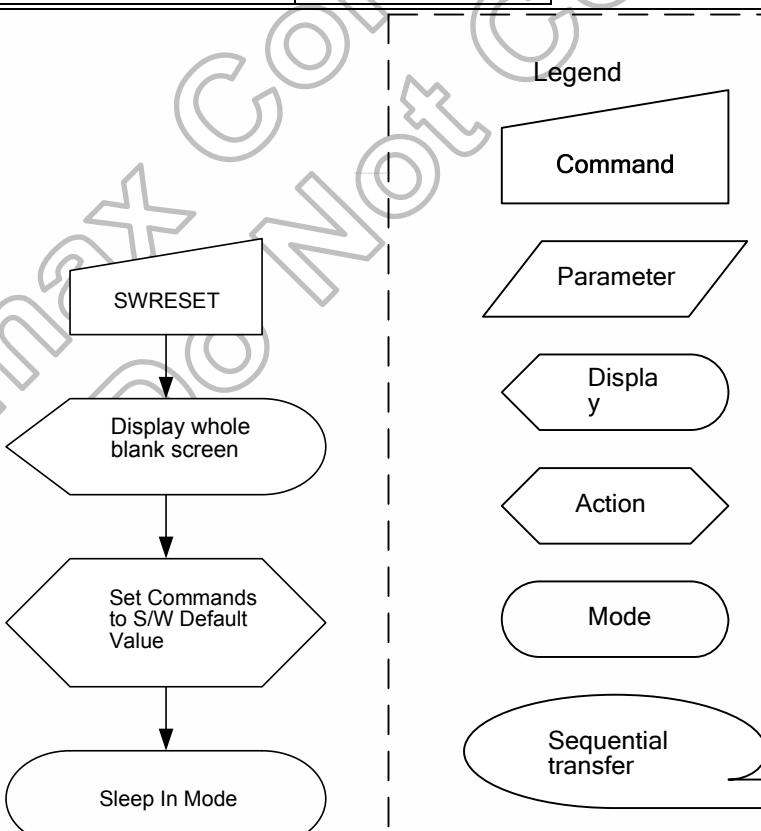
(Hex)	Operation Code	DNC	D7	D6	D5	D4	D3	D2	D1	D0	Function	
CC	SETPANEL	0	1	1	0	0	1	1	0	0	Get panel related register	
		1	-	-	-	SM_PA_NEL(0)	SS_PAN_EL(0)	GS_PAN_EL(0)	REV_PA_NEL(1)	BGR_PANE_L(0)		
FE	SET SPI READ INDEX	0	1	1	1	1	1	1	1	0	SET SPI READ Command Address	
		1	CMD_ADD[7:0]									
FF	SPIREAD	0	1	1	1	1	1	1	1	1	Read SPI Command Data	
		1	CMD_DATA1[7:0]									
		1	:									
		1	CMD_DATAN[7:0]									
E0	SETGAMMA (OTPx4)	0	1	1	1	0	0	0	0	0	Set Gamma Curve Related Setting	
		1	-	-	G1_VRP0[5:0]							
		1	G1_CGMP0[1:0]	G1_VRP1[5:0]								
		1	G1_CGMP1[1:0]	G1_VRP2[5:0]								
		1	G1_CGMP2[1:0]	G1_VRP3[5:0]								
		1	G1_CGMP3[1:0]	G1_VRP4[5:0]								
		1	G1_CGMP5	G1_CGMP4	G1_VRP5[5:0]							
		1	G1_PRP0[6]	-	G1_PKP0[4:0]							
		1			G1_PKP1[4:0]							
		1	G1_PRP0[3:2]	-	G1_PKP2[4:0]							
		1	G1_PRP0[1:0]	-	G1_PKP3[4:0]							
		1	G1_PRP1[6]	-	G1_PKP4[4:0]							
		1			G1_PKP5[4:0]							
		1	G1_PRP1[3:2]	-	G1_PKP6[4:0]							
		1	G1_PRP1[1:0]	-	G1_PKP7[4:0]							
		1			G1_PKP8[4:0]							
		1			G1_VRN0[5:0]							
		1	G1_CGMN0[1:0]	G1_VRN1[5:0]								
		1	G1_CGMN1[1:0]	G1_VRN2[5:0]								
		1	G1_CGMN2[1:0]	G1_VRN3[5:0]								
		1	G1_CGMN3[1:0]	G1_VRN4[5:0]								
		1	G1_CGMN5	G1_CGMN4	G1_VRN5[5:0]							
		1	G1_PRN0[6]	-	G1_PKN0[4:0]							
		1			G1_PKN1[4:0]							
		1	G1_PRN0[3:2]	-	G1_PKN2[4:0]							
		1	G1_PRN0[1:0]	-	G1_PKN3[4:0]							
		1	G1_PRN1[6]	-	G1_PKN4[4:0]							
		1			G1_PKN5[4:0]							
		1	G1_PRN1[3:2]	-	G1_PKN6[4:0]							
		1	G1_PRN1[1:0]	-	G1_PKN7[4:0]							
		1	-	-	G1_PKN8[4:0]							

6.2 Command Description

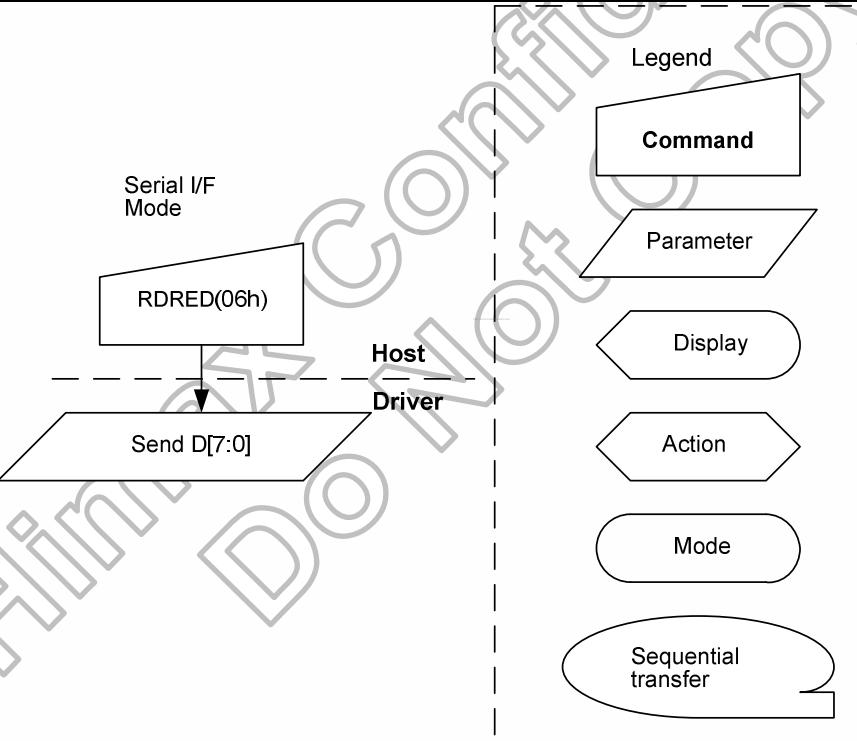
6.2.1 NOP

00 H	NOP (No Operation)									
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	0	0	0	00
Parameter	No Parameter									
Description	This command is an empty command; it does not have any effect on the display module.									
Restriction										
Register Availability	Status		Availability							
	Sleep Out		Yes							
	Sleep In		Yes							
Default	Status		Default Value							
	Power On Sequence		N/A							
	S/W Reset		N/A							
	H/W Reset		N/A							
Flow Chart										

6.2.2 Software Reset (01h)

01 H	SWRESET (Software Reset)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	0	0	0	0	1	01								
Parameter	No Parameter																	
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)																	
Restriction	<p>It will be necessary to wait 5msec before sending new command following software reset.</p> <p>The display module loads all display suppliers' factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.</p> <p>The host processor continues to send DCK, HSYNC, and VSYNC and ENABLE signals to HX8363-A for two frames after this command is sent.</p>																	
Register Availability	<table border="1"> <tr> <td>Status</td> <td>Availability</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>										Status	Availability	Sleep Out	Yes	Sleep In	Yes		
Status	Availability																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <tr> <td>Status</td> <td>Default Value</td> </tr> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </table>										Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A
Status	Default Value																	
Power On Sequence	N/A																	
S/W Reset	N/A																	
H/W Reset	N/A																	
Flow Chart	 <pre> graph TD SWRESET[SWRESET] --> Display[Display whole blank screen] Display --> Set[Set Commands to S/W Default Value] Set --> SleepIn[Sleep In Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																	

6.2.3 Read Red Color (06h)

RDRED (Read Red Colour)										
06 H	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	1	1	0	06
1 st parameter	1	R7	R6	R5	R4	R3	R2	R1	R0	xx
Description	The first parameter is telling red colour value of the first pixel of the frame when there is used RGB I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'. 24 bit format: R7 is MSB and R0 is LSB.									
Restriction										
Register Availability	Status	Availability								
	Sleep Out	Yes								
	Sleep In	Yes								
Default	Status	Default Value								
	Power On Sequence	00h								
	S/W Reset	00h								
	H/W Reset	00h								
Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 									

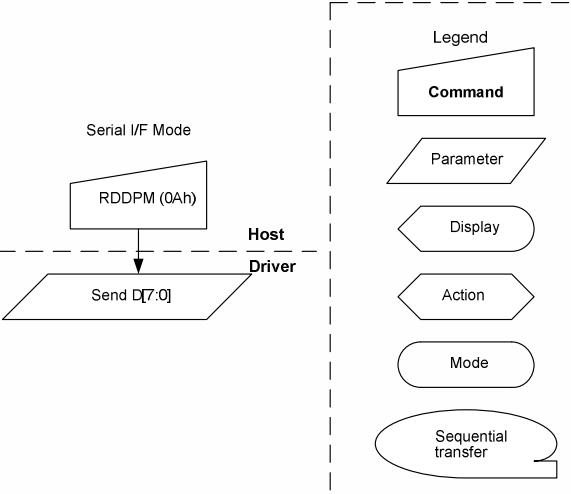
6.2.4 Read Green Color (07h)

07 H	RDGREEN (Read Green Colour)									
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	1	1	1	07
1 st parameter	1	G7	G6	G5	G4	G3	G2	G1	G0	xx
Description	The first parameter is telling green colour value of the first pixel of the frame when there is used RGB I/F. 16 and 18 bit formats: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'. 24 bit format: G7 is MSB and G0 is LSB.									
Restriction										
Register Availability	Status	Availability								
	Sleep Out	Yes								
	Sleep In	Yes								
Default	Status	Default Value								
	Power On Sequence	00h								
	S/W Reset	00h								
	H/W Reset	00h								
Flow Chart	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 									

6.2.5 Read Blue Color (08h)

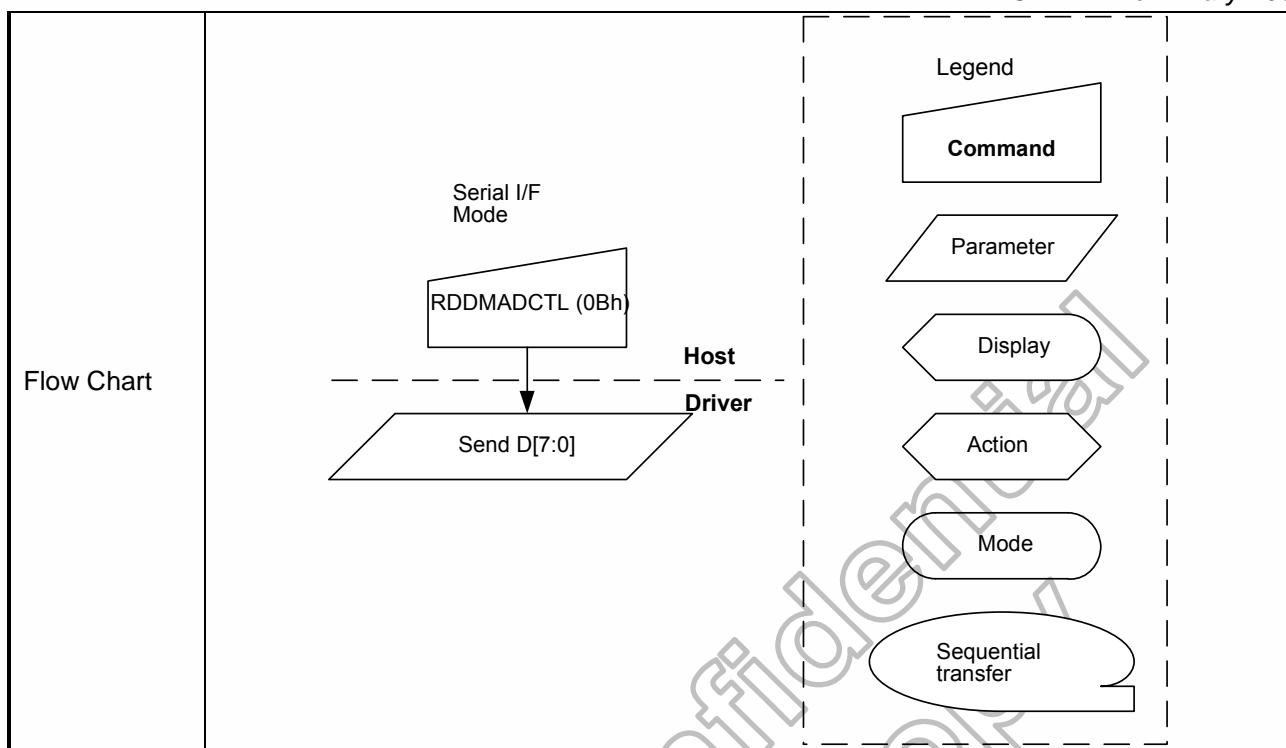
RDBLUE (Read Blue Colour)										
08 H	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	1	0	0	0	08
1 st parameter	1	B7	B6	B5	B4	B3	B2	B1	B0	xx
Description	The first parameter is telling blue colour value of the first pixel of the frame when there is used RGB I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'. 24 bit format: B7 is MSB and B0 is LSB.									
Restriction										
Register Availability	Status	Availability								
	Sleep Out	Yes								
	Sleep In	Yes								
Default	Status	Default Value								
	Power On Sequence	00h								
	S/W Reset	00h								
	H/W Reset	00h								
Flow Chart	<pre> graph TD Host[Host] -- "Send D[7:0]" --> Driver[Driver] subgraph Legend [Legend] Command[Command] Parameter[Parameter] Display[Display] Action[Action] Mode[Mode] Sequential[Sequential transfer] end subgraph Flow [Flow] RDBLUE[RDBLUE(08h)] RDBLUE -- "Serial I/F Mode" --> SendD[Send D[7:0]] SendD --> Sequential Sequential --> Mode Mode --> Action Action --> Display Display --> Parameter Parameter --> Command Command --> RDBLUE end </pre>									

6.2.6 Read Display Power Mode (0Ah)

0A H	RDDPM (Read Display Power Mode)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	0	1	0	1	0	0A								
1 st parameter	1	D[7:0]							xx									
This command indicates the current status of the display as described in the table below:																		
Description	Bit	Description		Comment														
	D7	Booster Voltage Status																
	D6	Idle Mode On/Off		Set to '0'														
	D5	Partial Mode On/Off		Set to '0'														
	D4	Sleep In/Out																
	D3	Display Normal Mode On/Off																
	D2	Display On/Off																
	D1	Not Defined		Set to '0'														
	D0	Not Defined		Set to '0'														
Description	Bit D7 – Booster Voltage Status '0' = Booster Off or has a fault. '1' = Booster On and working OK (Meets display supplier's optical requirements).																	
	Bit D6 – Idle Mode On/Off This bit is not applicable for this project, so it is set to "0".																	
	Bit D5 – Partial Mode On/Off This bit is not applicable for this project, so it is set to "0".																	
	Bit D4 – Sleep In/Out '0' = Sleep In Mode. '1' = Sleep Out Mode.																	
	Bit D3 – Display Normal Mode On/Off '0' = Display Normal Mode Off. '1' = Display Normal Mode On.																	
	Bit D2 – Display On/Off '0' = Display is Off. '1' = Display is On.																	
	Restrictions																	
	Register Availability	Status		Availability														
		Sleep Out		Yes														
Flow Chart	Default	Sleep In or Booster Off		Yes														
		Status		Default Value														
		Power On Sequence		08HEX														
		S/W Reset		08HEX														
		H/W Reset		08HEX														
 <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																		

6.2.7 Read Display MADCTL (0Bh)

RDDMADCTL (Read Display MADCTL)														
0B H	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX				
Command	0	0	0	0	0	1	0	1	1	0B				
1 st parameter	1	D[7:0]								xx				
This command indicates the current status of the display as described in the table below:														
Description	Bit	Description					Comment							
	D7	Page Address Order					Set to '0'							
	D6	Column Address Order					Set to '0'							
	D5	Page/Column Order					Set to '0'							
	D4	Line Address Order					Set to '0'							
	D3	RGB/BGR Order												
	D2	Display Data Latch Order					Set to '0'							
	D1	Source scan sequence												
	D0	Gate scan sequence												
	Bit D7 – Page Address Order													
	This bit is not applicable for this project, so it is set to "0".													
	Bit D6 – Column Address Order													
	This bit is not applicable for this project, so it is set to "0".													
	Bit D5 – Page/Column Order													
	This bit is not applicable for this project, so it is set to "0".													
	Bit D4 – Line Address Order													
	This bit is not applicable for this project, so it is set to "0".													
	Bit D3 – RGB/BGR Order													
	'0' = RGB (When MADCTL B3='0').													
	'1' = BGR (When MADCTL B3='1').													
	Bit D2 – Display Data Latch Data Order													
	This bit is not applicable for this project, so it is set to "0".													
	Bit D1 – Source scan sequence													
	'0' = Normal (When MADCTL B1='0').													
	'1' = Flipped (When MADCTL B1='1').													
	Bit D0 – Gate scan sequence													
	'0' = Normal (When MADCTL B0='0').													
Restrictions														
Register Availability	Status	Availability												
	Sleep Out	Yes												
Default	Sleep In or Booster Off	Yes												
	Status	Default Value												
	Power On Sequence	00HEX												
	S/W Reset	00HEX												
	H/W Reset	00HEX												



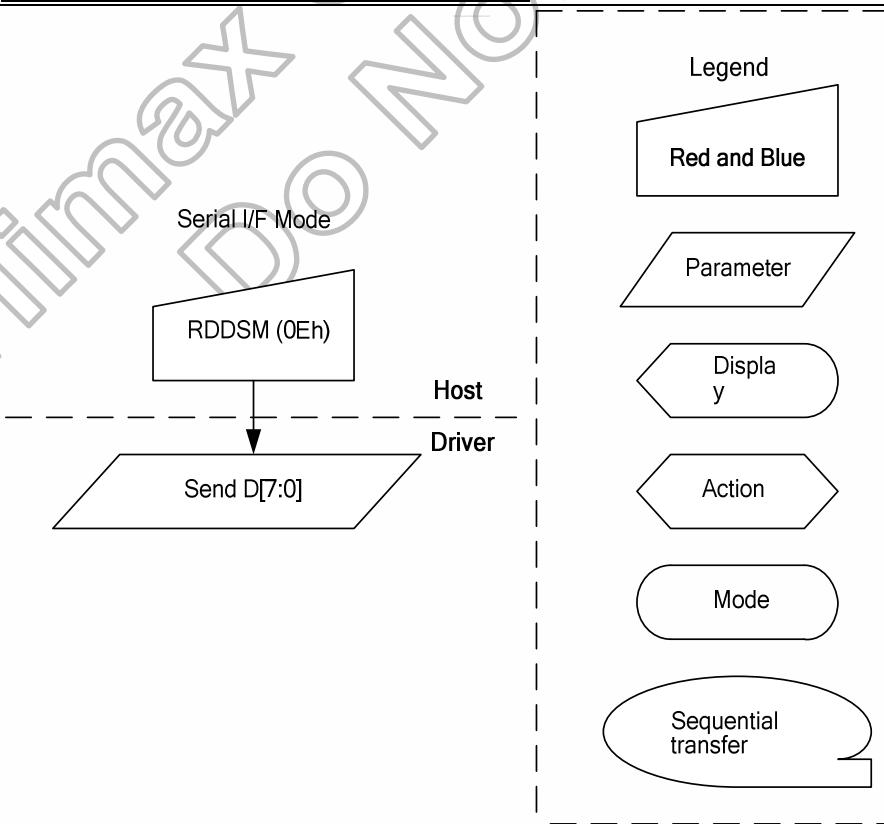
6.2.8 Read Display Pixel Format (0Ch)

0C H	RDDCOLMOD (Read Display COLMOD)																																						
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX																													
Command	0	0	0	0	0	1	1	0	0	0C																													
1 st parameter	1	D[7:0]								xx																													
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th> <th colspan="2">Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td colspan="2" rowspan="4">DPI Interface Pixel format</td> <td>Set to '0'</td> </tr> <tr> <td>D6</td> <td></td> <td></td> </tr> <tr> <td>D5</td> <td></td> <td></td> </tr> <tr> <td>D4</td> <td></td> <td></td> </tr> <tr> <td>D3</td> <td colspan="2" rowspan="4">DBI Interface Pixel format</td> <td>Set to '0'</td> </tr> <tr> <td>D2</td> <td></td> <td>Set to '0'</td> </tr> <tr> <td>D1</td> <td></td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td></td> <td>Set to '0'</td> </tr> </tbody> </table> Bits D7, D3 – Reserved Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition Bits D2, D1, D0 – DBI Interface Colour Pixel Format Definition. This bit is not applicable for this project, so it is set to "0".									Bit	Description		Comment	D7	DPI Interface Pixel format		Set to '0'	D6			D5			D4			D3	DBI Interface Pixel format		Set to '0'	D2		Set to '0'	D1		Set to '0'	D0		Set to '0'
Bit	Description		Comment																																				
D7	DPI Interface Pixel format		Set to '0'																																				
D6																																							
D5																																							
D4																																							
D3	DBI Interface Pixel format		Set to '0'																																				
D2				Set to '0'																																			
D1				Set to '0'																																			
D0				Set to '0'																																			
Restrictions																																							
Register Availability	Status		Availability																																				
	Sleep Out		Yes																																				
Default	Status		Default Value																																				
	Power On Sequence		'70'h																																				
	S/W Reset		'70'h																																				
	H/W Reset		'70'h																																				
Flow Chart																																							

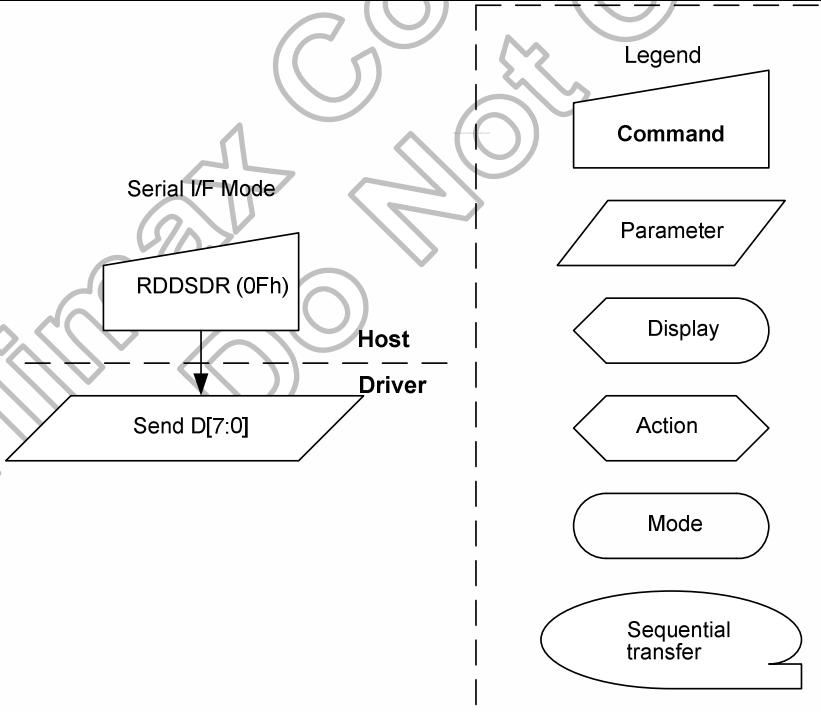
6.2.9 Read Display Image Mode (0Dh)

0D H	RDDIM (Read Display Image Mode)																																																						
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																													
Command	0	0	0	0	0	1	1	0	1	0D																																													
1 st parameter	1	D[7:0]								xx																																													
	This command indicates the current status of the display as described in the table below: Bit D7 – Vertical Scrolling On/Off This bit is not applicable for this project, so it is set to '0' Bit D6 – Reserved set to '0' Bit D5 – Inversion On/Off '0' = Inversion is Off. '1' = Inversion is On. Bits D4, D3 – Reserved set to '0' Bits D2, D1, D0 – Gamma Curve Selection																																																						
Description	<table border="1"> <thead> <tr> <th>Gamma Curve Selected</th><th>D2</th><th>D1</th><th>D0</th><th>Gamma Set (26h) Parameter</th></tr> </thead> <tbody> <tr> <td>Gamma Curve 1</td><td>0</td><td>0</td><td>0</td><td>GC0</td></tr> <tr> <td>Gamma Curve 2</td><td>0</td><td>0</td><td>1</td><td>GC1</td></tr> <tr> <td>Gamma Curve 3</td><td>0</td><td>1</td><td>0</td><td>GC2</td></tr> <tr> <td>Gamma Curve 4</td><td>0</td><td>1</td><td>1</td><td>GC3</td></tr> <tr> <td>Not Defined</td><td>1</td><td>0</td><td>0</td><td>Not Defined</td></tr> <tr> <td>Not Defined</td><td>1</td><td>0</td><td>1</td><td>Not Defined</td></tr> <tr> <td>Not Defined</td><td>1</td><td>1</td><td>0</td><td>Not Defined</td></tr> <tr> <td>Not Defined</td><td>1</td><td>1</td><td>1</td><td>Not Defined</td></tr> </tbody> </table>										Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter	Gamma Curve 1	0	0	0	GC0	Gamma Curve 2	0	0	1	GC1	Gamma Curve 3	0	1	0	GC2	Gamma Curve 4	0	1	1	GC3	Not Defined	1	0	0	Not Defined	Not Defined	1	0	1	Not Defined	Not Defined	1	1	0	Not Defined	Not Defined	1	1	1	Not Defined
Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter																																																			
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Gamma Curve 2	0	0	1	GC1																																																			
Gamma Curve 3	0	1	0	GC2																																																			
Gamma Curve 4	0	1	1	GC3																																																			
Not Defined	1	0	0	Not Defined																																																			
Not Defined	1	0	1	Not Defined																																																			
Not Defined	1	1	0	Not Defined																																																			
Not Defined	1	1	1	Not Defined																																																			
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Status	Default Value																																																						
Power On Sequence	00HEX																																																						
S/W Reset	00HEX																																																						
H/W Reset	00HEX																																																						
Flow Chart	<pre> graph TD Host[Host] -- "Send D[7:0]" --> Driver[Driver] subgraph "Serial I/F Mode" RDDIM[RDDIM (0Dh)] RDDIM --> D[7:0] end RDDIM --- Host RDDIM --- D[7:0] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																																						

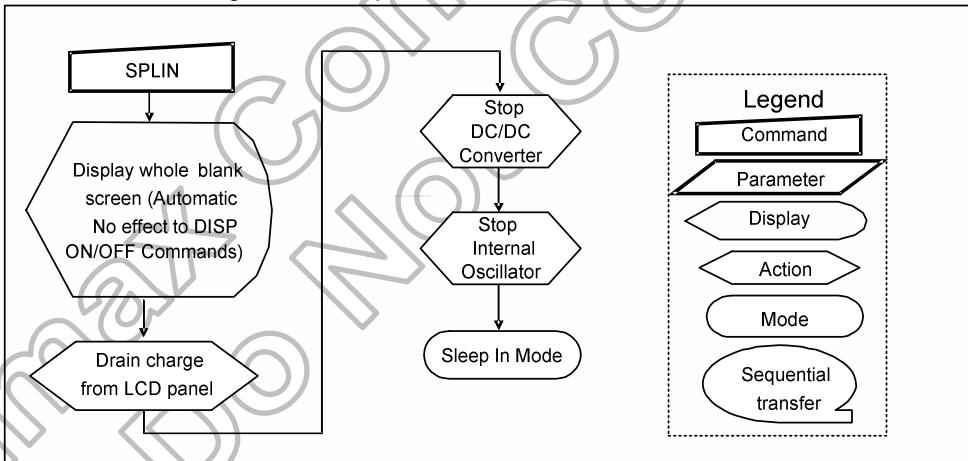
6.2.10 Read Display Signal Mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)																		
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	0	0	0	0	1	1	1	0	0E									
1 st parameter	1	D[7:0]							xx										
Description	<p>This command indicates the status of the display self-diagnostic results after Sleep Out –command as described in the table below:</p> <ul style="list-style-type: none"> • Bit D5 – Horizontal Sync. (RGB I/F) On/Off. ‘0’ = Horizontal Sync. Line is Off (“Low”). ‘1’ = Horizontal Sync. Line is On (“High”). • Bit D4 – Vertical Sync. (RGB I/F) On/Off. ‘0’ = Vertical Sync. Line is Off (“Low”). ‘1’ = Vertical Sync. Line is On (“High”). • Bit D3 – Pixel Clock (PCLK, RGB I/F) On/Off. ‘0’ = PCLK line is Off (“Low”). ‘1’ = PCLK line is On (“High”). • Bit D2 – Data Enable (DE, RGB I/F) On/Off. ‘0’ = DE line is Off (“Low”). ‘1’ = DE line is On (“High”). • Bit D7, D6, D1 are D0 – are for future use and are set to ‘0’. 																		
Restrictions																			
Register Availability	<table border="1"> <tr> <td>Status</td> <td>Availability</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes											
Status	Availability																		
Sleep Out	Yes																		
Sleep In or Booster Off	Yes																		
Default	<table border="1"> <tr> <td>Status</td> <td>Default Value</td> </tr> <tr> <td>Power On Sequence</td> <td>NA</td> </tr> <tr> <td>S/W Reset</td> <td>NA</td> </tr> <tr> <td>H/W Reset</td> <td>NA</td> </tr> </table>		Status	Default Value	Power On Sequence	NA	S/W Reset	NA	H/W Reset	NA									
Status	Default Value																		
Power On Sequence	NA																		
S/W Reset	NA																		
H/W Reset	NA																		
Flow Chart	 <pre> graph TD Host[Host] -- "Send D[7:0]" --> Driver[Driver] Driver -- "RDDSM (0Eh)" --> Host </pre> <p>Legend:</p> <ul style="list-style-type: none"> Red and Blue (parallelogram) Parameter (trapezoid) Display (diamond) Action (hexagon) Mode (oval) Sequential transfer (oval) 																		

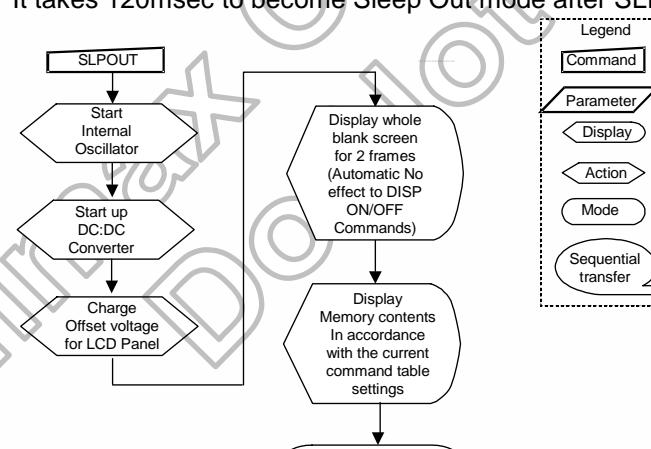
6.2.11 Read Display Self-Diagnostic Result (0Fh)

0F H	RDDSDR (Read Display Self-Diagnostic Result)																		
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	0	0	0	0	1	1	1	1	0F									
1 st parameter	1	D[7:0]							xx										
Description	This command indicates the status of the display self-diagnostic results after Sleep Out –command as described in the table below: Bit D7 – Register Loading Detection Bit D6 – Functionality Detection Bit D5 – Chip Attachment Detection Set to '0' if feature unimplemented. Bit D4 – Display Glass Break Detection Set to '0' if feature unimplemented. Bits D[3:0] – Reserved Set to '0'.																		
Restrictions																			
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes											
Status	Availability																		
Sleep Out	Yes																		
Sleep In or Booster Off	Yes																		
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>00HEX</td> </tr> <tr> <td>S/W Reset</td> <td>00HEX</td> </tr> <tr> <td>H/W Reset</td> <td>00HEX</td> </tr> </table>		Status	Default Value	Power On Sequence	00HEX	S/W Reset	00HEX	H/W Reset	00HEX									
Status	Default Value																		
Power On Sequence	00HEX																		
S/W Reset	00HEX																		
H/W Reset	00HEX																		
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <pre> graph TD Host[Host] -- "RDDSDR (0Fh)" --> Driver[Driver] Driver -- "Send D[7:0]" --> Host </pre>																		

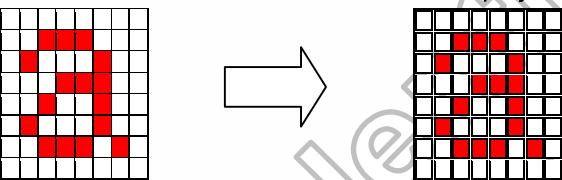
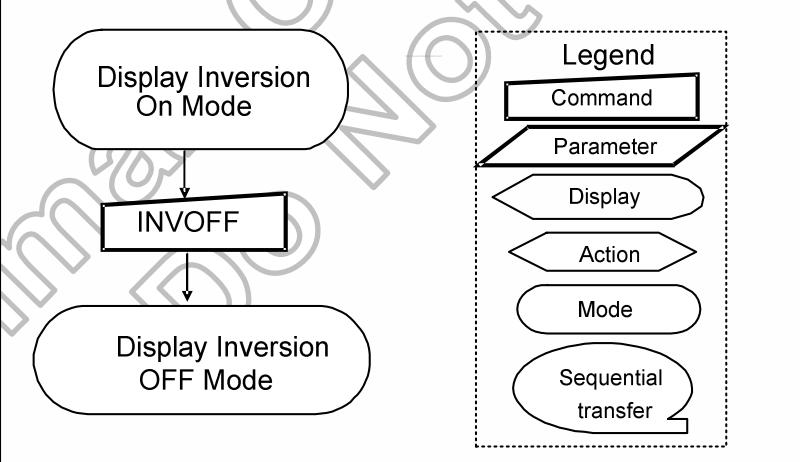
6.2.12 Sleep In (10h)

10 H	SLPIN (Sleep In)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	0	1	0	0	0	0	10								
Parameter	No Parameter																	
Description	This command is used to enter the Sleep in mode.																	
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).</p> <p>It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p> <p>The host processor continues to send DCK, HSYNC, and VSYNC and ENABLE signals to HX8363-A for two frames after this command is sent.</p>																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Sleep Out	Yes	Sleep In	Yes		
Status	Availability																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode
Status	Default Value																	
Power On Sequence	Sleep in mode																	
S/W Reset	Sleep in mode																	
H/W Reset	Sleep in mode																	
Flow Chart	<p>It takes 120msec to get into Sleep In mode after SLPIN command issued.</p>  <pre> graph TD SLPIN[SLPIN] --> Blank[Display whole blank screen Automatic No effect to DISP ON/OFF Commands] Blank --> Drain[Drain charge from LCD panel] Drain --> StopDC[Stop DC/DC Converter] StopDC --> StopIO[Stop Internal Oscillator] StopIO --> SleepInMode[Sleep In Mode] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																	

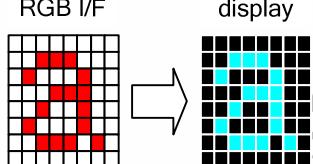
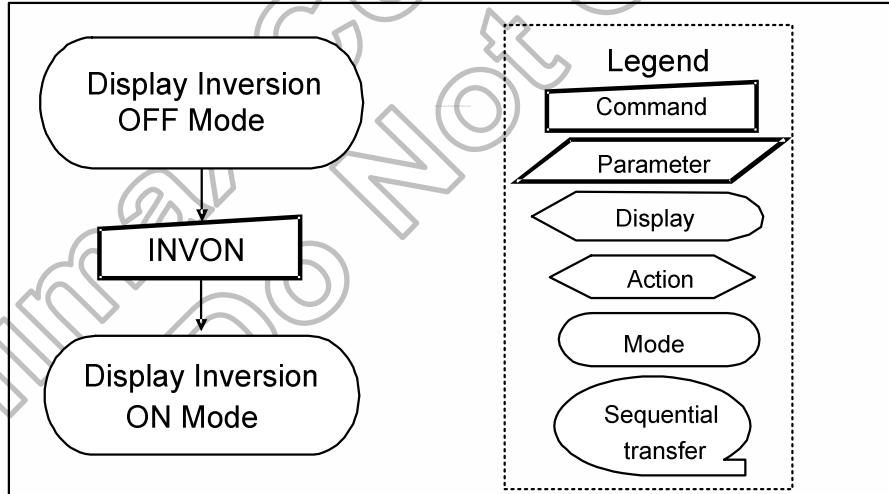
6.2.13 Sleep Out (11h)

11 H	SLPOUT (Sleep Out)															
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
Command	0	0	0	0	1	0	0	0	1	11						
Parameter	No Parameter															
Description	This command turns off sleep mode.															
Restriction	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).</p> <p>It will be necessary to wait 5msec before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out -mode.</p> <p>The display module is doing self-diagnostic functions during this 5msec.</p> <p>It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p> <p>The host processor sends DCK, HSYNC, and VSYNC and ENABLE signals to HX8363-A for two frames before this command is sent.</p>															
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>										Status	Availability	Sleep Out	Yes	Sleep In	Yes
Status	Availability															
Sleep Out	Yes															
Sleep In	Yes															
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> </table>										Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode
Status	Default Value															
Power On Sequence	Sleep In Mode															
S/W Reset	Sleep In Mode															
Flow Chart	<p>It takes 120msec to become Sleep Out mode after SLPOUT command issued.</p>  <pre> graph TD SLPOUT[SLPOUT] --> StartOsc[Start Internal Oscillator] StartOsc --> StartDCDC[Start up DC:DC Converter] StartDCDC --> ChargeOffset[Charge Offset voltage for LCD Panel] ChargeOffset --> BlankScreen{Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)} BlankScreen --> MemoryContent{Display Memory contents In accordance with the current command table settings} MemoryContent --> SleepOutMode(Sleep Out mode) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 															

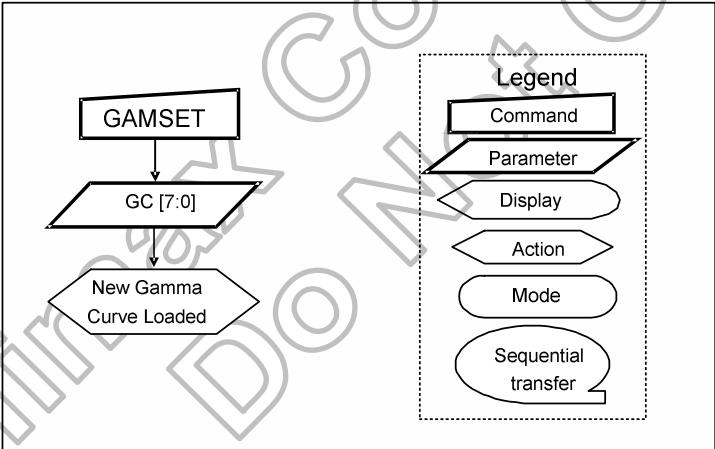
6.2.14 Display Inversion Off (20h)

20 H	INVOFF (Display Inversion Off)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	0	0	0	0	20								
Parameter	No Parameter																	
Description	<p>This command is used to recover from display inversion mode. This command makes no change of contents of image data. This command does not change any other status.</p> <p style="text-align: center;">(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> RGB I/F (Example) Display </div> 																	
Restriction	This command has no effect when module is already in inversion off mode.																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In or Booster Off</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes		
Status	Availability																	
Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Display Inversion off</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Display Inversion off</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Display Inversion off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off
Status	Default Value																	
Power On Sequence	Display Inversion off																	
S/W Reset	Display Inversion off																	
H/W Reset	Display Inversion off																	
Flow Chart	 <pre> graph TD A([Display Inversion On Mode]) --> B[INVOFF] B --> C([Display Inversion OFF Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																	

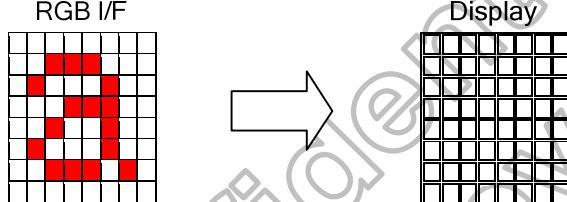
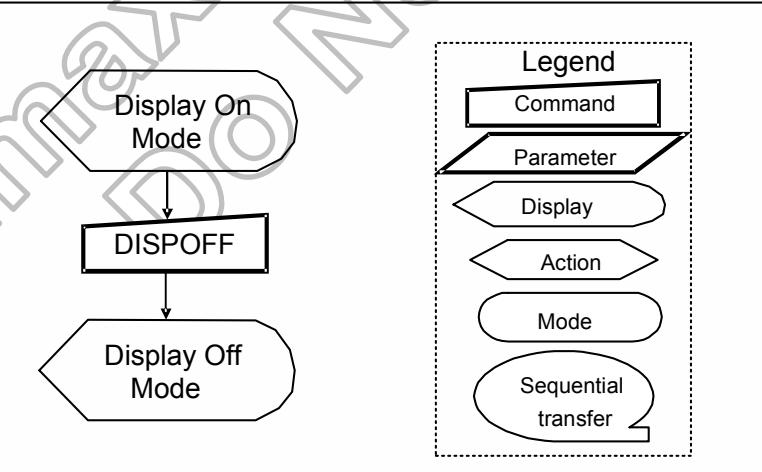
6.2.15 Display Inversion On (21h)

21 H	INVON (Display Inversion On)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	0	0	0	1	21								
Parameter	No Parameter																	
Description	<p>This command is used to enter into display inversion mode. This command makes no change of contents of image data. Every bit is inverted from the RGB I/F to the display. This command does not change any other status.</p> <p>(Example)</p> 																	
Restriction	This command has no effect when module is already in inversion on mode.																	
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>										Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes		
Status	Availability																	
Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion off</td> </tr> </table>										Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off
Status	Default Value																	
Power On Sequence	Display Inversion off																	
S/W Reset	Display Inversion off																	
H/W Reset	Display Inversion off																	
Flow Chart	 <pre> graph TD A([Display Inversion OFF Mode]) --> B[INVON] B --> C([Display Inversion ON Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																	

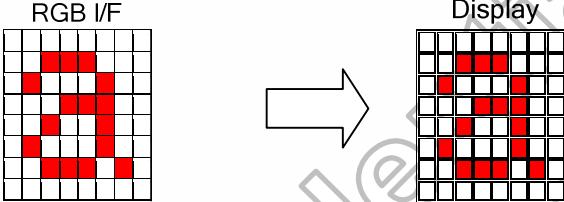
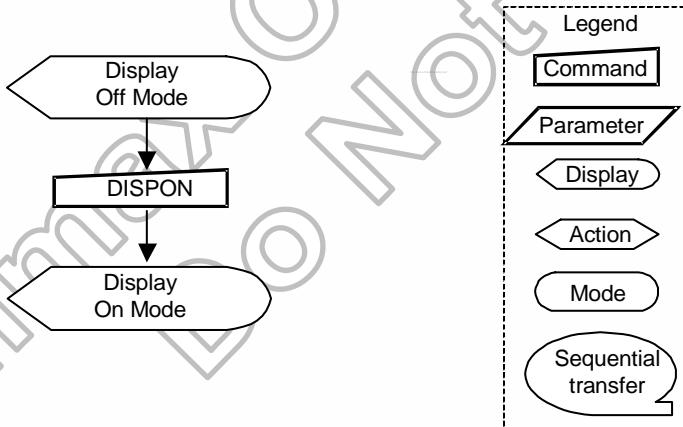
6.2.16 Gamma Set (26h)

26 H	GAMSET (Gamma Set)																								
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	0	0	1	0	0	1	1	0	26															
Parameter	1	GC[7:0]								1..08															
Description	<p>This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Section Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:</p> <table border="1"> <tr> <th>GC[7..0]</th><th>Parameter</th><th>Curve Selected</th></tr> <tr> <td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr> <tr> <td>02h</td><td>GC1</td><td>Gamma Curve 2</td></tr> <tr> <td>04h</td><td>GC2</td><td>Gamma Curve 3</td></tr> <tr> <td>08h</td><td>GC3</td><td>Gamma Curve 4</td></tr> </table> <p>Note: All other values are undefined.</p>										GC[7..0]	Parameter	Curve Selected	01h	GC0	Gamma Curve 1	02h	GC1	Gamma Curve 2	04h	GC2	Gamma Curve 3	08h	GC3	Gamma Curve 4
GC[7..0]	Parameter	Curve Selected																							
01h	GC0	Gamma Curve 1																							
02h	GC1	Gamma Curve 2																							
04h	GC2	Gamma Curve 3																							
08h	GC3	Gamma Curve 4																							
Restriction	Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.																								
Register Availability	<table border="1"> <tr> <th>Status</th><th>Availability</th></tr> <tr> <td>Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In or Booster Off</td><td>Yes</td></tr> </table>										Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes									
Status	Availability																								
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Default	<table border="1"> <tr> <th>Status</th><th>Default Value</th></tr> <tr> <td>Power On Sequence</td><td>01HEX</td></tr> <tr> <td>S/W Reset</td><td>01HEX</td></tr> <tr> <td>H/W Reset</td><td>01HEX</td></tr> </table>										Status	Default Value	Power On Sequence	01HEX	S/W Reset	01HEX	H/W Reset	01HEX							
Status	Default Value																								
Power On Sequence	01HEX																								
S/W Reset	01HEX																								
H/W Reset	01HEX																								
Flow Chart	 <pre> graph TD GAMSET[GAMSET] --> GC[GC[7:0]] GC --> NewGamma[New Gamma Curve Loaded] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

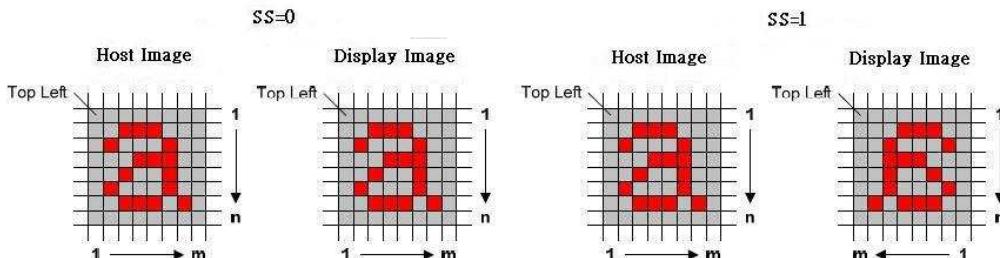
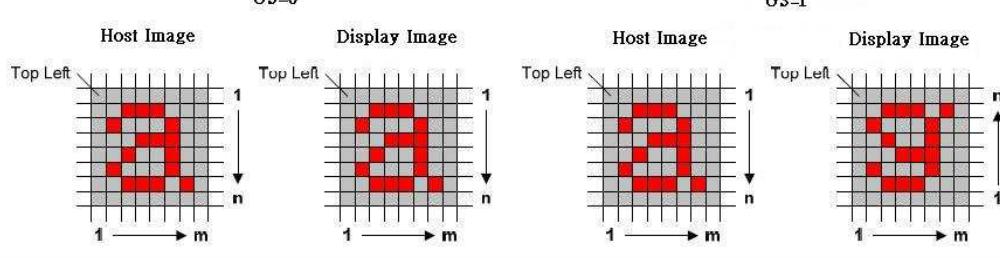
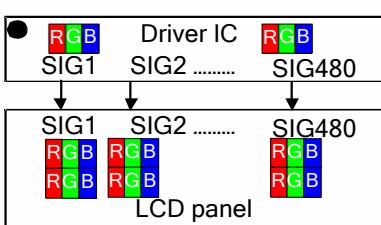
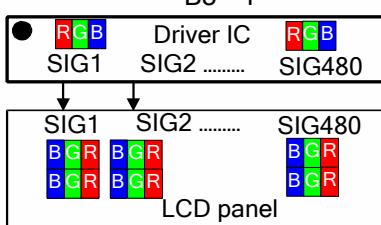
6.2.17 Display Off (28h)

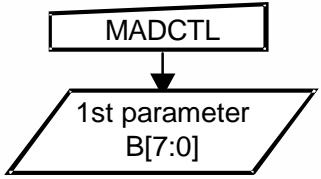
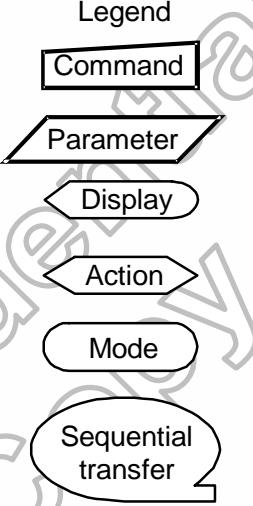
28 H	DISPOFF (Display Off)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	1	0	0	0	28								
Parameter	No Parameter																	
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from RGB I/F is disabled and blank page inserted.</p> <p>This command makes no change of contents of RGB I/F.</p> <p>This command does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p> <p style="text-align: center;">Example</p> 																	
Restriction	This command has no effect when module is already in display off mode.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes		
Status	Availability																	
Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value																	
Power On Sequence	Display off																	
S/W Reset	Display off																	
H/W Reset	Display off																	
Flow Chart	 <pre> graph TD A([Display On Mode]) --> B[DISPOFF] B --> C([Display Off Mode]) </pre>																	

6.2.18 Display On (29h)

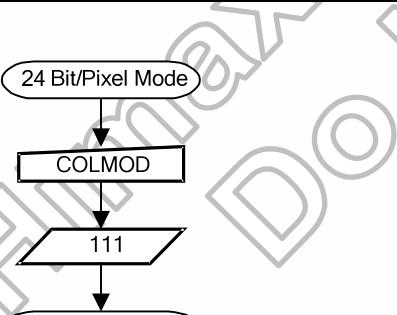
29 H	DISPON (Display On)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	0	1	0	1	0	0	1	29								
Parameter	NO PARAMETER																	
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from the RGB I/F is enabled.</p> <p>This command makes no change of contents of image data</p> <p>This command does not change any other status.</p> <p>(Example)</p> 																	
Restriction	This command has no effect when module is already in display on mode.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes		
Status	Availability																	
Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value																	
Power On Sequence	Display off																	
S/W Reset	Display off																	
H/W Reset	Display off																	
Flow Chart	 <pre> graph TD A([Display Off Mode]) --> B[DISPON] B --> C([Display On Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																	

6.2.19 Memory Access Control (36h)

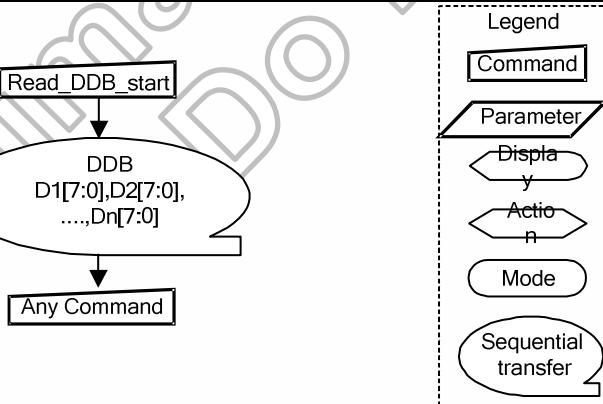
36 H	MADCTL (Memory Access Control)																																				
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	0	0	1	1	0	1	1	0	36																											
1 st parameter	1	xx	xx	xx	xx	BGR	xx	SS	GS	XX																											
	This command defines write scanning direction of LCD. Bit Assignment <table border="1"> <thead> <tr> <th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr> </thead> <tbody> <tr> <td>B7</td><td>PAGE ADDRESS ORDER</td><td>This bit is not applicable for this project, so it is set to "0".</td></tr> <tr> <td>B6</td><td>COLUMN ADDRESS ORDER</td><td>This bit is not applicable for this project, so it is set to "0".</td></tr> <tr> <td>B5</td><td>PAGE/COLUMN SELECTION</td><td>This bit is not applicable for this project, so it is set to "0".</td></tr> <tr> <td>B4</td><td>Display Device Line Refresh Order</td><td>This bit is not applicable for this project, so it is set to "0".</td></tr> <tr> <td>B3</td><td>RGB-BGR ORDER (BGR)</td><td>Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)</td></tr> <tr> <td>B2</td><td>Display Data Latch Data Order</td><td>This bit is not applicable for this project, so it is set to "0".</td></tr> <tr> <td>B1</td><td>Flip Horizontal (Source scan sequence)</td><td>Select the Source driver scan direction on panel module</td></tr> <tr> <td>B0</td><td>Flip Vertical (Gate scan sequence)</td><td>Select the Gate driver scan direction on panel module</td></tr> </tbody> </table>										BIT	NAME	DESCRIPTION	B7	PAGE ADDRESS ORDER	This bit is not applicable for this project, so it is set to "0".	B6	COLUMN ADDRESS ORDER	This bit is not applicable for this project, so it is set to "0".	B5	PAGE/COLUMN SELECTION	This bit is not applicable for this project, so it is set to "0".	B4	Display Device Line Refresh Order	This bit is not applicable for this project, so it is set to "0".	B3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)	B2	Display Data Latch Data Order	This bit is not applicable for this project, so it is set to "0".	B1	Flip Horizontal (Source scan sequence)	Select the Source driver scan direction on panel module	B0	Flip Vertical (Gate scan sequence)	Select the Gate driver scan direction on panel module
BIT	NAME	DESCRIPTION																																			
B7	PAGE ADDRESS ORDER	This bit is not applicable for this project, so it is set to "0".																																			
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B4	Display Device Line Refresh Order	This bit is not applicable for this project, so it is set to "0".																																			
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B1	Flip Horizontal (Source scan sequence)	Select the Source driver scan direction on panel module																																			
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Description	Source scan sequence (SS)																																				
																																					
																																					
	Gate scan sequence (GS)																																				
																																					
																																					
	RGB-BGR Order																																				
	B3="0"					B3="1"																															
																																					
																																					
	LCD panel																																				

Restriction	D7, D6, D5, D4, and D2 of the 1st parameter are set to '0' internally.	
Register Availability	Status	Availability
	Sleep Out	Yes
Default	Status	Default Value
	Power On Sequence	B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0
	S/W Reset	B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0
Flow Chart	 <pre> graph TD MADCTL[MADCTL] --> Parameter[/1st parameter B[7:0]/] </pre>	
	 <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 	

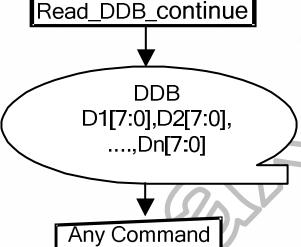
6.2.20 Interface Pixel Format (3Ah)

3A H		COLMOD (Interface Pixel Format)																																													
		DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command		0	0	0	1	1	1	0	1	0	3A																																				
1 st parameter		1	xx	CSEL_RGB[2:0]			xx	xx	xx	xx	011,10 1,110,1 11																																				
Description	<p>This command is used to define the format of RGB picture data. The formats are shown in the following table:</p> <p>D6~D4 : DPI Pixel format Definition. D2~D0 : DBI Pixel format Definition.</p> <p>This bit is not applicable for this project, so it is set to "0".</p> <table border="1"> <thead> <tr> <th>RGB Interface Format</th> <th>D6</th> <th>D5</th> <th>D4</th> </tr> </thead> <tbody> <tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>Not Defined</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>Not Defined</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>16 bit/pixel</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>18 bit/pixel</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>24 bit/pixel</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>											RGB Interface Format	D6	D5	D4	Not Defined	0	0	0	Not Defined	0	0	1	Not Defined	0	1	0	Not Defined	0	1	1	Not Defined	1	0	0	16 bit/pixel	1	0	1	18 bit/pixel	1	1	0	24 bit/pixel	1	1	1
RGB Interface Format	D6	D5	D4																																												
Not Defined	0	0	0																																												
Not Defined	0	0	1																																												
Not Defined	0	1	0																																												
Not Defined	0	1	1																																												
Not Defined	1	0	0																																												
16 bit/pixel	1	0	1																																												
18 bit/pixel	1	1	0																																												
24 bit/pixel	1	1	1																																												
Restriction	There is no visible effect until the image data is written to.																																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In or Booster Off</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes																														
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>'70'h</td></tr> <tr><td>S/W Reset</td><td>'70'h</td></tr> <tr><td>H/W Reset</td><td>'70'h</td></tr> </tbody> </table>											Status	Default Value	Power On Sequence	'70'h	S/W Reset	'70'h	H/W Reset	'70'h																												
Status	Default Value																																														
Power On Sequence	'70'h																																														
S/W Reset	'70'h																																														
H/W Reset	'70'h																																														
Flow Chart	 <pre> graph TD A([24 Bit/Pixel Mode]) --> B[COLMOD] B --> C[/111/] C --> D([24 Bit/Pixel Mode]) </pre> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>																																														

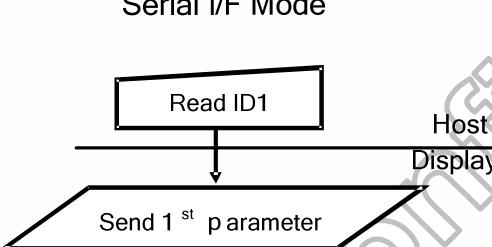
6.2.21 Read_DDB_start (A1h)

A1 H		Read_DDB_start																		
		DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command		0	1	0	1	0	0	0	0	1	A1									
1 st parameter	1					ID1[7:0]					xx									
2 nd parameter	1					ID2[7:0]					xx									
3 rd parameter	1					ID3[7:0]					xx									
4 th parameter	1					ID4[7:0]					xx									
5 th parameter	1	1	1	1	1	1	1	1	1	1	xx									
Description	<p>This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data.</p> <p>The format of returned data is as follows:</p> <p>Parameter 1: MS (most significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.</p> <p>Parameter 2: LS (least significant) byte of Supplier ID.</p> <p>Parameter 3: MS (most significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.</p> <p>Parameter 4: LS (least significant) byte of Supplier Elective Data</p> <p>Parameter 5: single-byte <i>Escape or Exit Code</i> (EEC). The code is interpreted as follows:</p> <ul style="list-style-type: none"> - FFh - Exit code – there is no more data in the Descriptor Block 																			
Restriction																				
Register Availability	<table border="1"> <tr> <td>Status</td> <td>Availability</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes												
Status	Availability																			
Sleep Out	Yes																			
Sleep In or Booster Off	Yes																			
Default	<table border="1"> <tr> <td>Status</td> <td>Default Value</td> </tr> <tr> <td>Power On Sequence</td> <td>PA1st~4th is OTP value, PA5th is FFh</td> </tr> <tr> <td>S/W Reset</td> <td>PA1st~4th is OTP value, PA5th is FFh</td> </tr> <tr> <td>H/W Reset</td> <td>PA1st~4th is OTP value, PA5th is FFh</td> </tr> </table>		Status	Default Value	Power On Sequence	PA1st~4th is OTP value, PA5th is FFh	S/W Reset	PA1st~4th is OTP value, PA5th is FFh	H/W Reset	PA1st~4th is OTP value, PA5th is FFh										
Status	Default Value																			
Power On Sequence	PA1st~4th is OTP value, PA5th is FFh																			
S/W Reset	PA1st~4th is OTP value, PA5th is FFh																			
H/W Reset	PA1st~4th is OTP value, PA5th is FFh																			
Flow Chart	 <pre> graph TD A[Read_DDB_start] --> B{DDB D1[7:0], D2[7:0], ..., Dn[7:0]} B --> C[Any Command] style B fill:none,stroke:none style C fill:none,stroke:none %% Legend subgraph Legend direction TB L1[Command] --- R1[] L2[Parameter] --- R2[] L3[Display] --- R3[] L4[Action] --- R4[] L5[Mode] --- R5[] L6[Sequential transfer] --- R6[] end </pre>																			

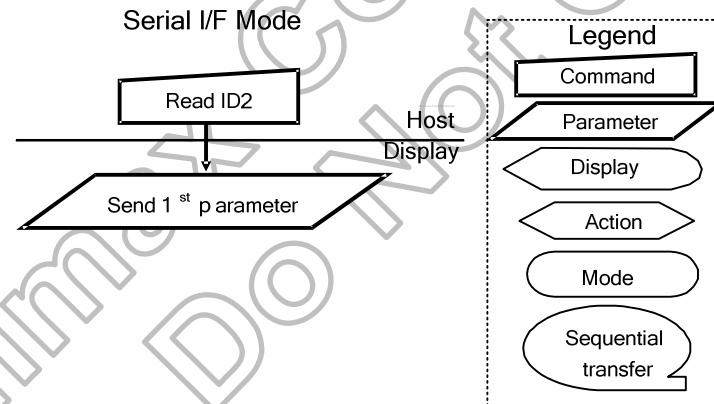
6.2.22 Read_DDB_continue (A8h)

A8 H	Read_DDB_continue																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	0	1	0	1	0	0	0	A8								
1 st parameter	1	DDB_DATA								xx								
Description	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.																	
Restriction	There is no visible effect until the image data is written to.																	
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>										Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes		
Status	Availability																	
Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>Without A1h read, 1st~4th read is the same as A8h 1st~4th OTP value, after 5th read is FFh.</td> </tr> <tr> <td>S/W Reset</td> <td>Without A1h read, 1st~4th read is the same as A8h 1st~4th OTP value, after 5th read is FFh.</td> </tr> <tr> <td>H/W Reset</td> <td>Without A1h read, 1st~4th read is the same as A8h 1st~4th OTP value, after 5th read is FFh.</td> </tr> </table>										Status	Default Value	Power On Sequence	Without A1h read, 1st~4th read is the same as A8h 1st~4th OTP value, after 5th read is FFh.	S/W Reset	Without A1h read, 1st~4th read is the same as A8h 1st~4th OTP value, after 5th read is FFh.	H/W Reset	Without A1h read, 1st~4th read is the same as A8h 1st~4th OTP value, after 5th read is FFh.
Status	Default Value																	
Power On Sequence	Without A1h read, 1st~4th read is the same as A8h 1st~4th OTP value, after 5th read is FFh.																	
S/W Reset	Without A1h read, 1st~4th read is the same as A8h 1st~4th OTP value, after 5th read is FFh.																	
H/W Reset	Without A1h read, 1st~4th read is the same as A8h 1st~4th OTP value, after 5th read is FFh.																	
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																	

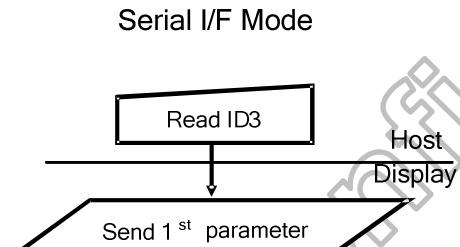
6.2.23 Read ID1 (DAh)

DA H	RDID1 (Read ID1)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	1	1	0	1	0	DA								
1 st parameter	1	module's manufacturer[7:0]								xx								
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.																	
Restriction																		
Register Availability	Status		Availability															
	Sleep Out		Yes															
	Sleep In or Booster Off		Yes															
Default	Status		Default Value															
	Power On Sequence		OTP value															
	S/W Reset		OTP value															
	H/W Reset		OTP value															
Flow Chart	<p>Serial I/F Mode</p>  <pre> graph TD Host[Host] --> Read[Read ID1] Read --> Send[Send 1st parameter] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																	

6.2.24 Read ID2 (DBh)

DB H	RDID2 (Read ID2)																														
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	0	1	1	0	1	1	0	1	1	DB																					
1 st parameter	1	1	LCD module/driver version [6:0]							-																					
Description	<p>This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:</p> <table border="1"> <thead> <tr> <th>ID Byte Value V[7:0]</th> <th>Version</th> <th>Changes</th> </tr> </thead> <tbody> <tr> <td>80h</td> <td></td> <td></td> </tr> <tr> <td>81h</td> <td></td> <td></td> </tr> <tr> <td>82h</td> <td></td> <td></td> </tr> <tr> <td>83h</td> <td></td> <td></td> </tr> <tr> <td>84h</td> <td></td> <td></td> </tr> <tr> <td>85h</td> <td></td> <td></td> </tr> </tbody> </table>										ID Byte Value V[7:0]	Version	Changes	80h			81h			82h			83h			84h			85h		
ID Byte Value V[7:0]	Version	Changes																													
80h																															
81h																															
82h																															
83h																															
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Restrictions																															
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Status	Default Value																														
Power On Sequence	OTP value																														
S/W Reset	OTP value																														
H/W Reset	OTP value																														
Flow Chart	<p>Serial I/F Mode</p>  <pre> graph TD Host[Host] -- "Read ID2" --> Display[Display] Display -- "Send 1 st p parameter" --> Host </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																														

6.2.25 Read ID3 (DCh)

DC H	RDID3 (Read ID3)																		
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	1	0	1	1	1	0	0	DC									
1 st parameter	1	LCD module/driver ID[7:0]							xx										
Description	This read byte identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.																		
Restrictions																			
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes											
Status	Availability																		
Sleep Out	Yes																		
Sleep In or Booster Off	Yes																		
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>OTP value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP value</td> </tr> </table>		Status	Default Value	Power On Sequence	OTP value	S/W Reset	OTP value	H/W Reset	OTP value									
Status	Default Value																		
Power On Sequence	OTP value																		
S/W Reset	OTP value																		
H/W Reset	OTP value																		
Flow Chart	<p style="text-align: center;">Serial I/F Mode</p>  <p>The flowchart illustrates the process for reading the ID3 register. It starts with a rectangular box labeled "Read ID3". An arrow points from this box down to a trapezoidal box labeled "Send 1st parameter". To the right of the flowchart is a legend box titled "Legend" containing six items: "Command" (represented by a rectangle), "Parameter" (represented by a parallelogram), "Display" (represented by a diamond), "Action" (represented by a trapezoid), "Mode" (represented by an oval), and "Sequential transfer" (represented by an ellipse).</p>																		

6.2.26 Write Display Brightness (51h)

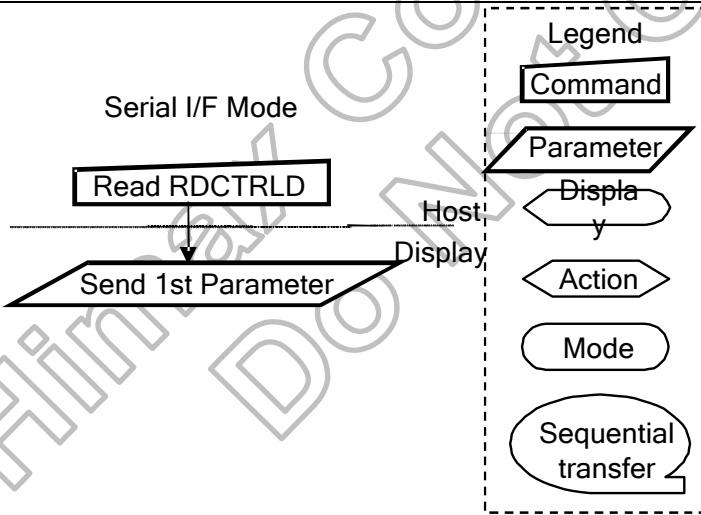
6.2.27 Read Display Brightness Value (52h)

52 H	RDDISBV (Read Display Brightness Value)																		
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	0	1	0	1	0	0	1	0	52									
1 st parameter	1	RDDBV[7:0]							xx										
Description	<p>This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>See chapters: "Brightness Control BlockX", "Display configuration" and "XWrite Display Brightness (51h)X" This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode. See chapter "Write CTRL Display (53h)" bit DB = '1'.</p> <p>DBV[7:0] is reset when display is in sleep-in mode.</p> <p>DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (53h)" command is '0'. DBV[7:0] is manual set brightness specified with "Write CTRL Display (53h)" command when bit BCTRL is '1' and bit A of "Write CTRL Display (53h)" command is '0'.</p>																		
Restriction																			
Register Availability	<table border="1"> <tr> <td>Status</td><td>Availability</td></tr> <tr> <td>Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </table>										Status	Availability	Sleep Out	Yes	Sleep In	Yes			
Status	Availability																		
Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <tr> <td>Status</td><td>Default Value</td></tr> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h	
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	<p>The flowchart illustrates the communication sequence between the Host and the Display. It starts with a rectangular box labeled "Read RDDISBV" with an arrow pointing down to a trapezoidal box labeled "Send 1st Parameter". The "Read RDDISBV" box is associated with the "Host" and the "Send 1st Parameter" box is associated with the "Display". To the right of the flowchart is a legend enclosed in a dashed box:</p> <ul style="list-style-type: none"> Command (rectangle) Parameter (rectangle) Display (trapezoid) Action (diamond) Mode (oval) Sequential transfer (oval) 																		

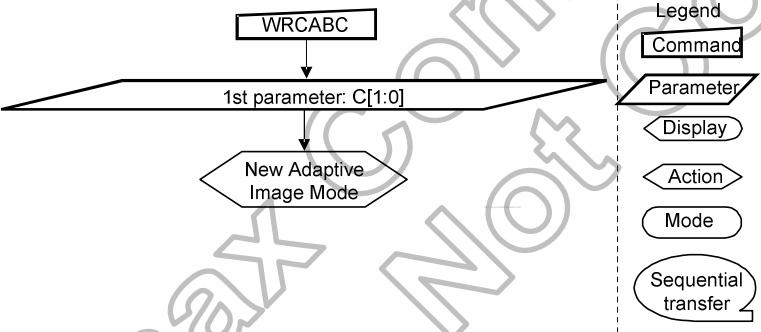
6.2.28 Write CTRL Display (53h)

WRCTRLD (Write Control Display)																		
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	0	1	0	0	1	1	53								
1 st parameter	1	0	0	BCTRL	0	DD	BL	0	0	00.. FF								
Description	<p>This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. (Refer to "Turn Off Display Brightness".) When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.</p>																	
Restriction																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Sleep Out	Yes	Sleep In	Yes		
Status	Availability																	
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Sleep In	Yes																	
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	<pre> graph TD WRCTRLD[WRCTRLD] --> BCTRL[BCTRL, DD, BL] BCTRL --> NewValue{New Control Value Loaded} </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																	

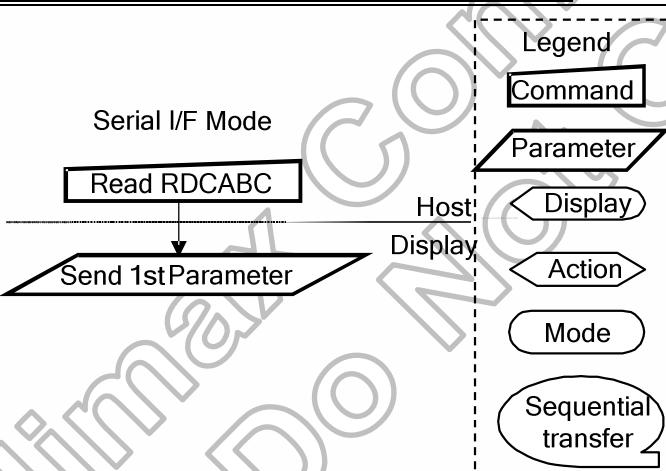
6.2.29 Read CTRL Value Display (54h)

54 H	RDCTRLD (Read Control Value Display)																		
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	0	1	0	1	0	1	0	0	54									
1 st parameter	1	0	0	BCTRL	0	DD	BL	0	0	xx									
Description	This command returns ambient light and brightness control values BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On																		
Restriction																			
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Sleep Out	Yes	Sleep In	Yes											
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Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h									
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	 <pre> graph TD Host[Host] -- "Read RDCTRLD" --> Display[Display] Display -- "Send 1st Parameter" --> Host </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																		

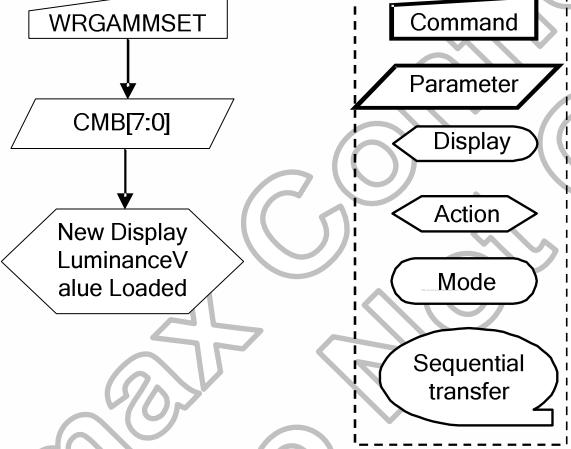
6.2.30 Write Content Adaptive Brightness Control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)																								
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	0	1	0	1	0	1	0	1	55															
1 st parameter	1	xx	xx	xx	xx	xx	xx	CABC[1:0](00)	xx																
Description	This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, Which are defined on a table below. <table border="1" style="margin-left: 20px;"> <tr> <th>C1</th><th>C0</th><th>Function</th></tr> <tr> <td>0</td><td>0</td><td>Off</td></tr> <tr> <td>0</td><td>1</td><td>User Interface Image</td></tr> <tr> <td>1</td><td>0</td><td>Still Picture</td></tr> <tr> <td>1</td><td>1</td><td>Moving Image</td></tr> </table>										C1	C0	Function	0	0	Off	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image
C1	C0	Function																							
0	0	Off																							
0	1	User Interface Image																							
1	0	Still Picture																							
1	1	Moving Image																							
Restriction																									
Register Availability	Status		Availability																						
	Sleep Out		Yes																						
	Sleep In		Yes																						
Default	Status		Default Value																						
	Power On Sequence		00h																						
	S/W Reset		00h																						
	H/W Reset		00h																						
Flow Chart	 <pre> graph TD A[WRCABC] --> B{1st parameter: C[1:0]} B --> C{New Adaptive Image Mode} </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

6.2.31 Read Content Adaptive Brightness Control (56h)

56 H	RDCABC (Read Content Adaptive Brightness Control)																								
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	0	1	0	1	0	1	1	0	56															
1 st parameter	1	0	0	0	0	0	0	CABC[1:0]	xx																
Description	<p>This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.</p> <table border="1"> <thead> <tr> <th>C1</th><th>C0</th><th>Function</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Off</td></tr> <tr> <td>0</td><td>1</td><td>User Interface Image</td></tr> <tr> <td>1</td><td>0</td><td>Still Picture</td></tr> <tr> <td>1</td><td>1</td><td>Moving Image</td></tr> </tbody> </table>										C1	C0	Function	0	0	Off	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image
C1	C0	Function																							
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0	1	User Interface Image																							
1	0	Still Picture																							
1	1	Moving Image																							
Restriction																									
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Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	 <pre> graph TD Host[Host] -- "Read RDCABC" --> Display[Display] Display -- "Send 1st Parameter" --> Host </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

6.2.32 Write CABC minimum brightness (5Eh)

5E H	RDMFFSVM (Read Median Filtered FS Value MSBs)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	0	1	1	1	1	0	5E								
1 st parameter	1	CMB 7	CMB 6	CMB 5	CMB 4	CMB 3	CMB 2	CMB 1	CMB 0	00.. FF								
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. See chapter "Minimum brightness setting of CABC function".																	
Restriction	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).																	
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>										Status	Availability	Sleep Out	Yes	Sleep In	Yes		
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	
Flow Chart	 <pre> graph TD WRGAMMSET[WRGAMMSET] --> CMB[CMB[7:0]] CMB --> NewDisplay[New Display Luminance Value Loaded] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																	

6.2.33 Read CABC minimum brightness (5Fh)

5F H	RDCABCMB (Read CABC minimum brightness)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	0	1	0	1	1	1	1	1	5F								
1 st parameter	1	CMB[7:0]								XX								
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter "Minimum brightness setting of CABC function". CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command.																	
Restriction																		
Register Availability	Status		Availability															
	Sleep Out		Sleep In															
	Sleep Out	Yes	Sleep In	Yes														
Default	Status		Default Value															
	Power On Sequence		S/W Reset		H/W Reset		00h	00h	00h									
Flow Chart	<pre> graph TD Host[Host] -- "Read RDCABCMB" --> Display[Display] Display -- "Send 1st Parameter" --> Host subgraph Legend [Legend] Command[Command] Parameter[Parameter] DisplayL[Display] Action[Action] Mode[Mode] Sequential[Sequential transfer] end </pre>																	

6.2.34 SETPOWER: Set Power (B1h)

RB1 H	SETPOWER(Set power related setting)																																																																																																														
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																					
Command	0	1	0	1	1	0	0	0	1	B1																																																																																																					
1 st Parameter	1	-	VSN_EN	VSP_EN	VGL_EN	VGH_EN	-	VDDDN_HZ	SLP																																																																																																						
2 nd Parameter	1	-	FS12	FS11	FS10	-	AP2	AP1	AP0																																																																																																						
3 rd Parameter	1	-	-	-	-	BT3	BT2	BT1	BT0																																																																																																						
4 th Parameter	1	DT1	DT0	DC1	DC0	DC_DIV3	DC_DIV2	DC_DIV1	DC_DIV0																																																																																																						
5 th Parameter	1	-	DTPS2	DTPS1	DTPS0	-	DTP2	DTP1	DTP0																																																																																																						
6 th Parameter	1	-	DTNS2	DTNS1	DTNS0	-	DTN2	DTN1	DTN0																																																																																																						
7 th Parameter	1	-	-	-	BTP4	BTP3	BTP2	BTP1	BTP0																																																																																																						
8 th Parameter	1	-	-	-	BTN4	BTN3	BTN2	BTN1	BTN0																																																																																																						
9 th Parameter	1	VRHP7	VRHP6	VRHP5	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0																																																																																																						
10 th Parameter	1	VRHN7	VRHN6	VRHN5	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0																																																																																																						
11 th Parameter	1	-	-	VRMP5	VRMP4	VRMP3	VRMP2	VRMP1	VRMP0																																																																																																						
12 th Parameter	1	-	-	VRMN5	VRMN4	VRMN3	VRMN2	VRMN1	VRMN0																																																																																																						
Description	This command is used to set related setting of power.																																																																																																														
	VSP_EN: ON/OFF the operation of VSP circuit.																																																																																																														
	<table border="1"> <tr> <td>VSP_EN</td> <td>Operation of VSP DC/DC circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table>										VSP_EN	Operation of VSP DC/DC circuit	0	OFF	1	ON																																																																																															
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VSN_EN: ON/OFF the operation of VSN circuit.																																																																																																															
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VGH_EN: ON/OFF the operation of VGH charge bump circuit.																																																																																																															
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BT3	BT2	BT1	BT0	VGH	VGL																																																																																																										
0	0	0	0	2*(VSP-VSN)	VDDDN-1*(VSP-VSN)																																																																																																										
0	0	0	1	2*(VSP-VSN)	-1*(VSP-VSN)																																																																																																										
0	0	1	0	2*(VSP-VSN)	VDD3-1*(VSP-VSN)																																																																																																										
0	0	1	1	1*(VSP-VSN)+(VDD3-VSN)	VDDDN-1*(VSP-VSN)																																																																																																										
0	1	0	0	1*(VSP-VSN)+(VDD3-VSN)	-1*(VSP-VSN)																																																																																																										
0	1	0	1	1*(VSP-VSN)+(VDD3-VSN)	VDD3-1*(VSP-VSN)																																																																																																										
0	1	1	0	1*(VSP-VSN)+(VSSD-VSN)	VDDDN-1*(VSP-VSN)																																																																																																										
0	1	1	1	1*(VSP-VSN)+(VSSD-VSN)	-1*(VSP-VSN)																																																																																																										
1	0	0	0	1*(VSP-VSN)+(VSSD-VSN)	VDD3-1*(VSP-VSN)																																																																																																										
1	0	0	1	Inhibited	Inhibited																																																																																																										
1	0	1	0	Inhibited	Inhibited																																																																																																										
1	0	1	1	Inhibited	Inhibited																																																																																																										
1	1	0	0	Inhibited	Inhibited																																																																																																										
1	1	0	1	Inhibited	Inhibited																																																																																																										
1	1	1	0	Inhibited	Inhibited																																																																																																										
1	1	1	1	Inhibited	Inhibited																																																																																																										

FS1[2:0]: Set the operating frequency of the step-up circuit 2 for VGH and VGL voltage generation.

FS12	FS11	FS10	Operation Frequency of Step-up Circuit 2
0	0	0	Fosc/32
0	0	1	Fosc/64
0	1	0	Fosc/128
0	1	1	Fosc/256
1	0	0	Fosc/512
1	0	1	Fosc/1024
1	1	0	Fosc/2048
1	1	1	Fosc/4096

VDDDN_HZ: Choose external or internal VDDDN power.

VDDDN_HZ=0, VDDDN= -2.5V.

VDDDN_HZ=1, VDDDN output HZ. (For external VDDDN.)

DC_DIV[3:0]:

For PFM circuit: Set the operate frequency of DC/DC converter circuit for PFM design.
(PCCS[1:0]=0X)

DC_DIV3	DC_DIV2	DC_DIV1	DC_DIV0	Normal operate frequency of DC/DC converter
0	0	0	0	Fosc / 1
0	0	0	1	Fosc / 2
0	0	1	0	Fosc / 3
0	0	1	1	Fosc / 4
0	1	0	0	Fosc / 5
0	1	0	1	Fosc / 6
0	1	1	0	Fosc / 7
0	1	1	1	Fosc / 8
1	0	0	0	Fosc / 1
1	0	0	1	Fosc / 2
1	0	1	0	Fosc / 3
1	0	1	1	Fosc / 4
1	1	0	0	Fosc / 5
1	1	0	1	Fosc / 6
1	1	1	0	Fosc / 7
1	1	1	1	Fosc / 8

For HX5186-A circuit: Set the operate frequency of DC/DC converter circuit for HX5186-A design. (PCCS[1:0]=1X)

DC_DIV3	DC_DIV2	DC_DIV1	DC_DIV0	Normal operate frequency of DC/DC converter
0	0	0	0	Fosc / 2
0	0	0	1	Fosc / 2
0	0	1	0	Fosc / 4
0	0	1	1	Fosc / 8
0	1	0	0	Fosc / 16
0	1	0	1	Fosc / 32
0	1	1	0	Fosc / 64
0	1	1	1	Fosc / 128
1	0	0	0	Fosc / 256
1	0	0	1	Fosc / 512
1	0	1	0	Fosc / 1024
1	0	1	1	Fosc / 2048
1	1	0	0	Fosc / 4096
1	1	0	1	Fosc / 8192
1	1	1	0	Fosc / 16384
1	1	1	1	Fosc / 32768

DC[1:0]: Set the operating frequency of DC/DC clock for the internal DC/DC circuit

When using the higher frequency, the driving ability of the DC/DC circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption. No use for HX5186-A design.

foscD = Divided oscillator frequency

DC1	DC0	Operation Frequency of DC/DC Clock
0	0	foscD / 4
0	1	foscD / 6
1	0	foscD / 8
1	1	foscD / 12

DT[1:0]: Delay time of power on and power off sequence.

DT1	DT0	Delay time of power on and power off sequence on (ms)
0	0	5ms
0	1	10ms
1	0	15ms
1	1	20ms

DTP[2:0]:

For PFM circuit: Set the operating duty cycle of DC/DC clock for VSP.
(PCCS[1:0]=0X)

1 duty cycle = 1 foscD clock

DTP2	DTP1	DTP0	Operation Duty Cycle of DC/DC Clock for VSP Generation
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

For HX5186-A circuit: Set the operating pump mode. (PCCS[1:0]=1X)

DTP2	DTP1	DTP0	VDD3 pumping ratio for VSP/VSN Generation
0	0	1	X 3 Pump
0	1	0	X 2 Pump
1	0	0	X 1.5 Pump
Others		Inhibited	

DTPS[2:0]: Set the soft start operating duty cycle of DC/DC circuit. (PFM DC/DC circuit).
No use for HX5186-A design.

1 duty cycle = 1 foscD clock

DTPS2	DTPS1	DTPS0	Soft start operating duty cycle of DC/DC circuit
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DTN[2:0]:

For PFM circuit: Set the operating duty cycle of DC/DC clock for VSN.
(PCCS[1:0]=0X)

1 duty cycle = 1 foscD clock

DTN2	DTN1	DTN0	Operation Duty Cycle of DC/DC Clock for VSN Generation
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

For HX5186-A circuit: Set the operating feedback mode. If feedback bump mode turns on,
VSP/VSN stop bumping when they reach target voltage.
(PCCS[1:0]=1X)

DTN2	DTN1	DTN0	Pumping mode selection for VSP/VSN Generation
0	0	1	No feedback bump mode
0	1	1	Feedback bump mode
Others		Inhibited	

DTNS[2:0]: Set the soft start operating duty cycle of DC/DC circuit. (PFM DC/DC circuit).
No use for HX5186-A design.

1 duty cycle = 1 foscD clock

DTNS2	DTNS1	DTNS0	Soft start operating duty cycle of DC/DC circuit
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

BTP[4:0]: Switch the output factor for DC/DC circuit. The LCD drive voltage level VSP can be selected according to the characteristic of liquid crystal which panel used.
For HX5186-A design, if DTN[2:0]=001(No feedback bump mode), depend on DTP[2:0] setting, the $VSP=1.5^*VDD3/2^*VDD3/3^*VDD3$.

BTP4	BTP3	BTP2	BTP1	BTP0	VSP
0	0	0	0	0	3.01
0	0	0	0	1	3.15
0	0	0	1	0	3.29
0	0	0	1	1	3.46
0	0	1	0	0	3.60
0	0	1	0	1	3.74
0	0	1	1	0	3.91
0	0	1	1	1	4.05
0	1	0	0	0	4.19
0	1	0	0	1	4.36
0	1	0	1	0	4.50
0	1	0	1	1	4.64
0	1	1	0	0	4.81
0	1	1	0	1	4.95
0	1	1	1	0	5.09
0	1	1	1	1	5.26
1	0	0	0	0	5.40
1	0	0	0	1	5.54
1	0	0	1	0	5.71
1	0	0	1	1	Inhibit
1	0	1	0	0	Inhibit
1	0	1	0	1	Inhibit
1	0	1	1	0	Inhibit
1	0	1	1	1	Inhibit
1	1	0	0	0	Inhibit
1	1	0	0	1	Inhibit
1	1	0	1	0	Inhibit
1	1	0	1	1	Inhibit
1	1	1	0	0	Inhibit
1	1	1	0	1	Inhibit
1	1	1	1	0	Inhibit
1	1	1	1	1	Inhibit

BTN[4:0]: Switch the output factor of DC/DC circuit for VSN voltage generation. The LCD drive voltage level VSN can be selected according to the characteristic of liquid crystal which panel used. No use for HX5186-A design. For HX5186-A design, VSN = -VSP.

BTN4	BTN3	BTN2	BTN1	BTN0	VSN
0	0	0	0	0	-3.01
0	0	0	0	1	-3.15
0	0	0	1	0	-3.29
0	0	0	1	1	-3.46
0	0	1	0	0	-3.60
0	0	1	0	1	-3.74
0	0	1	1	0	-3.91
0	0	1	1	1	-4.05
0	1	0	0	0	-4.19
0	1	0	0	1	-4.36
0	1	0	1	0	-4.50
0	1	0	1	1	-4.64
0	1	1	0	0	-4.81
0	1	1	0	1	-4.95
0	1	1	1	0	-5.09
0	1	1	1	1	-5.26
1	0	0	0	0	-5.40
1	0	0	0	1	-5.54
1	0	0	1	0	-5.71
1	0	0	1	1	Inhibit
1	0	1	0	0	Inhibit
1	0	1	0	1	Inhibit
1	0	1	1	0	Inhibit
1	0	1	1	1	Inhibit
1	1	0	0	0	Inhibit
1	1	0	0	1	Inhibit
1	1	0	1	0	Inhibit
1	1	0	1	1	Inhibit
1	1	1	0	0	Inhibit
1	1	1	0	1	Inhibit
1	1	1	1	0	Inhibit
1	1	1	1	1	Inhibit

AP[2:0]: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP[2:0] = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit. The default setting for AP[2:0] = 100 in order to avoid the power supply circuit stopped. If you use this register, every time this register must be sent again after SLPOUT(11h) command.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	0.5μA
0	1	0	1.0μA
0	1	1	1.5μA
1	0	0	2.0μA
1	0	1	2.5μA
1	1	0	3.0μA
1	1	1	3.5μA

VRHP[7:0]: VSPR regulator output control setting for source data output driving.

VRHP[7:0]								VSPR
0	0	0	0	0	0	0	0	3.488
0	0	0	0	0	0	0	1	3.516
0	0	0	0	0	0	1	0	3.544
0	0	0	0	0	0	1	1	3.572
0	0	0	0	0	1	0	0	3.600
0	0	0	0	0	1	0	1	3.628
0	0	0	0	0	1	1	0	3.656
0	0	0	0	0	1	1	1	3.684
0	0	0	0	1	0	0	0	3.713
0	0	0	0	1	0	0	1	3.741
0	0	0	0	1	0	1	0	3.769
0	0	0	0	1	0	1	1	3.797
0	0	0	0	1	1	0	0	3.825
0	0	0	0	1	1	0	1	3.853
0	0	0	0	1	1	1	0	3.881
0	0	0	0	1	1	1	1	3.909
0	0	0	1	0	0	0	0	3.938
0	0	0	1	0	0	0	1	3.966
0	0	0	1	0	0	1	0	3.994
0	0	0	1	0	1	0	1	4.022
0	0	0	1	0	1	0	0	4.050
0	0	0	1	0	1	0	1	4.078
0	0	0	1	0	1	1	0	4.106
0	0	0	1	0	1	1	1	4.134
0	0	0	1	1	0	0	0	4.163
0	0	0	1	1	0	0	1	4.191
0	0	0	1	1	0	1	0	4.219
0	0	0	1	1	0	1	1	4.247
0	0	0	1	1	1	0	0	4.275
0	0	0	1	1	1	0	1	4.303
0	0	0	1	1	1	1	0	4.331
0	0	0	1	1	1	1	1	4.359
0	0	1	0	0	0	0	0	4.388
0	0	1	0	0	0	0	1	4.416
0	0	1	0	0	0	1	0	4.444
0	0	1	0	0	0	1	1	4.472
0	0	1	0	0	1	0	0	4.500
0	0	1	0	0	1	0	1	4.528
0	0	1	0	0	1	1	0	4.556
0	0	1	0	0	1	1	1	4.584
0	0	1	0	1	0	0	0	4.613
0	0	1	0	1	0	0	1	4.641
0	0	1	0	1	0	1	0	4.669
0	0	1	0	1	0	1	1	4.697
0	0	1	0	1	1	0	0	4.725
0	0	1	0	1	1	0	1	4.753
0	0	1	0	1	1	1	0	4.781
0	0	1	0	1	1	1	1	4.809

	0	0	1	1	0	0	0	0	4.838
	0	0	1	1	0	0	0	1	4.866
	0	0	1	1	0	0	1	0	4.894
	0	0	1	1	0	0	1	1	4.922
	0	0	1	1	0	1	0	0	4.950
	0	0	1	1	0	1	0	1	4.978
	0	0	1	1	0	1	1	0	5.006
	0	0	1	1	0	1	1	1	5.034
	0	0	1	1	1	0	0	0	5.063
	0	0	1	1	1	0	0	1	5.091
	0	0	1	1	1	0	1	0	5.119
	00111011 ~ 01111110								Inhibit
	0	1	1	1	1	1	1	1	VSP
	10000000 ~ 11111110								Inhibit
	1	1	1	1	1	1	1	1	HZ

VRHN[7:0]: VSNR regulator output control setting for source data output driving.
When set VSNR=VSN, VCOM output is 0V.

VRHN[7:0]								VSNR
0	0	0	0	0	0	0	0	-3.263
0	0	0	0	0	0	0	1	-3.291
0	0	0	0	0	0	1	0	-3.319
0	0	0	0	0	0	1	1	-3.347
0	0	0	0	0	1	0	0	-3.375
0	0	0	0	0	1	0	1	-3.403
0	0	0	0	0	1	1	0	-3.431
0	0	0	0	0	1	1	1	-3.459
0	0	0	0	1	0	0	0	-3.488
0	0	0	0	1	0	0	1	-3.516
0	0	0	0	1	0	1	0	-3.544
0	0	0	0	1	0	1	1	-3.572
0	0	0	0	1	1	0	0	-3.600
0	0	0	0	1	1	0	1	-3.628
0	0	0	0	1	1	1	0	-3.656
0	0	0	0	1	1	1	1	-3.684
0	0	0	1	0	0	0	0	-3.713
0	0	0	1	0	0	0	1	-3.741
0	0	0	1	0	0	1	0	-3.769
0	0	0	1	0	0	1	1	-3.797
0	0	0	1	0	1	0	0	-3.825
0	0	0	1	0	1	0	1	-3.853
0	0	0	1	0	1	1	0	-3.881
0	0	0	1	0	1	1	1	-3.909
0	0	0	1	1	0	0	0	-3.938
0	0	0	1	1	0	0	1	-3.966
0	0	0	1	1	0	1	0	-3.994
0	0	0	1	1	0	1	1	-4.022
0	0	0	1	1	1	0	0	-4.050
0	0	0	1	1	1	0	1	-4.078
0	0	0	1	1	1	1	0	-4.106
0	0	0	1	1	1	1	1	-4.134
0	0	1	0	0	0	0	0	-4.163
0	0	1	0	0	0	0	1	-4.191
0	0	1	0	0	0	1	0	-4.219
0	0	1	0	0	0	1	1	-4.247
0	0	1	0	0	1	0	0	-4.275
0	0	1	0	0	1	0	1	-4.303

0	0	1	0	0	1	1	0	-4.331
0	0	1	0	0	1	1	1	-4.359
0	0	1	0	1	0	0	0	-4.388
0	0	1	0	1	0	0	1	-4.416
0	0	1	0	1	0	1	0	-4.444
0	0	1	0	1	0	1	1	-4.472
0	0	1	0	1	1	0	0	-4.500
0	0	1	0	1	1	0	1	-4.528
0	0	1	0	1	1	1	0	-4.556
0	0	1	0	1	1	1	1	-4.584
0	0	1	1	0	0	0	0	-4.613
0	0	1	1	0	0	0	1	-4.641
0	0	1	1	0	0	1	0	-4.669
0	0	1	1	0	0	1	1	-4.697
0	0	1	1	0	1	0	0	-4.725
0	0	1	1	0	1	0	1	-4.753
0	0	1	1	0	1	1	0	-4.781
0	0	1	1	0	1	1	1	-4.809
0	0	1	1	1	0	0	0	-4.838
0	0	1	1	1	0	0	1	-4.866
0	0	1	1	1	0	1	0	-4.894
0	0	1	1	1	0	1	1	-4.922
0	0	1	1	1	1	0	0	-4.950
0	0	1	1	1	1	1	0	-4.978
0	0	1	1	1	1	1	0	-5.006
0	0	1	1	1	1	1	1	-5.034
0	1	0	0	0	0	0	0	-5.063
0	1	0	0	0	0	0	1	-5.091
0	1	0	0	0	0	1	0	-5.119
01000011 ~ 01111110								Inhibit
0	1	1	1	1	1	1	1	VSN
10000000 ~ 11111110								Inhibit
1	1	1	1	1	1	1	1	HZ

VRMP[5:0]: The positive polarity gamma amplitude voltage setting (VSPR-VGSP).

VRMP[5:0]						VSPR-VGSP
0	0	0	0	0	0	2.588
0	0	0	0	0	1	2.644
0	0	0	0	1	0	2.700
0	0	0	0	1	1	2.756
0	0	0	1	0	0	2.813
0	0	0	1	0	1	2.869
0	0	0	1	1	0	2.925
0	0	0	1	1	1	2.981
0	0	1	0	0	0	3.038
0	0	1	0	0	1	3.094
0	0	1	0	1	0	3.150
0	0	1	0	1	1	3.206
0	0	1	1	0	0	3.263
0	0	1	1	0	1	3.319
0	0	1	1	1	0	3.375
0	0	1	1	1	1	3.431
0	1	0	0	0	0	3.488
0	1	0	0	0	1	3.544

0	1	0	0	1	0	3.600
0	1	0	0	1	1	3.656
0	1	0	1	0	0	3.713
0	1	0	1	0	1	3.769
0	1	0	1	1	0	3.825
0	1	0	1	1	1	3.881
0	1	1	0	0	0	3.938
0	1	1	0	0	1	3.994
0	1	1	0	1	0	4.050
0	1	1	0	1	1	4.106
0	1	1	1	0	0	4.163
0	1	1	1	0	1	4.219
0	1	1	1	1	0	4.275
0	1	1	1	1	1	4.331
1	0	0	0	0	0	4.388
1	0	0	0	0	1	4.444
1	0	0	0	1	0	4.500
1	0	0	0	1	1	4.556
1	0	0	1	0	0	4.613
1	0	0	1	0	1	4.669
1	0	0	1	1	0	4.725
1	0	0	1	1	1	4.781
1	0	1	0	0	0	4.838
1	0	1	0	0	1	4.894
1	0	1	0	1	0	4.950
1	0	1	0	1	1	5.006
1	0	1	1	0	0	5.063
1	0	1	1	0	1	5.119
1	0	1	1	1	0	Inhibit
1	0	1	1	1	1	Inhibit
1	1	0	0	0	0	Inhibit
1	1	0	0	0	1	Inhibit
1	1	0	1	0	0	Inhibit
1	1	0	1	1	0	Inhibit
1	1	0	1	1	1	Inhibit
1	1	1	0	0	0	Inhibit
1	1	1	0	0	1	Inhibit
1	1	1	0	1	0	Inhibit
1	1	1	0	1	1	Inhibit
1	1	1	1	0	0	Inhibit
1	1	1	1	0	1	Inhibit
1	1	1	1	1	0	Inhibit
1	1	1	1	1	1	Inhibit
1	1	1	1	1	1	VSPR(VGSP=VSSA)

VRMN[5:0]: The negative polarity gamma amplitude voltage setting (VSNR-VGSN).

VRMN[5:0]						VSNR-VGSN
0	0	0	0	0	0	-2.588
0	0	0	0	0	1	-2.644
0	0	0	0	1	0	-2.700
0	0	0	0	1	1	-2.756
0	0	0	1	0	0	-2.813

0	0	0	1	0	1	-2.869
0	0	0	1	1	0	-2.925
0	0	0	1	1	1	-2.981
0	0	1	0	0	0	-3.038
0	0	1	0	0	1	-3.094
0	0	1	0	1	0	-3.150
0	0	1	0	1	1	-3.206
0	0	1	1	0	0	-3.263
0	0	1	1	0	1	-3.319
0	0	1	1	1	0	-3.375
0	0	1	1	1	1	-3.431
0	1	0	0	0	0	-3.488
0	1	0	0	0	1	-3.544
0	1	0	0	1	0	-3.600
0	1	0	0	1	1	-3.656
0	1	0	1	0	0	-3.713
0	1	0	1	0	1	-3.769
0	1	0	1	1	0	-3.825
0	1	0	1	1	1	-3.881
0	1	1	0	0	0	-3.938
0	1	1	0	0	1	-3.994
0	1	1	0	1	0	-4.050
0	1	1	0	1	1	-4.106
0	1	1	1	0	0	-4.163
0	1	1	1	0	1	-4.219
0	1	1	1	1	0	-4.275
0	1	1	1	1	1	-4.331
1	0	0	0	0	0	-4.388
1	0	0	0	0	1	-4.444
1	0	0	0	1	0	-4.500
1	0	0	0	1	1	-4.556
1	0	0	1	0	0	-4.613
1	0	0	1	0	1	-4.669
1	0	0	1	1	0	-4.725
1	0	0	1	1	1	-4.781
1	0	1	0	0	0	-4.838
1	0	1	0	0	1	-4.894
1	0	1	0	1	0	-4.950
1	0	1	0	1	1	-5.006
1	0	1	1	0	0	-5.063
1	0	1	1	0	1	-5.119
1	0	1	1	1	0	Inhibit
1	0	1	1	1	1	Inhibit
1	1	0	0	0	0	Inhibit
1	1	0	0	1	0	Inhibit
1	1	0	0	1	1	Inhibit
1	1	0	1	0	0	Inhibit

	1	1	0	1	0	1	Inhibit
	1	1	0	1	1	0	Inhibit
	1	1	0	1	1	1	Inhibit
	1	1	1	0	0	0	Inhibit
	1	1	1	0	0	1	Inhibit
	1	1	1	0	1	0	Inhibit
	1	1	1	0	1	1	Inhibit
	1	1	1	1	0	0	Inhibit
	1	1	1	1	0	1	Inhibit
	1	1	1	1	1	0	Inhibit
	1	1	1	1	1	1	VSNR(VGSN=VSSA)
Restriction	SETEXTC turn on to enable this command						
Register Availability	Status	Availability					
	Sleep Out	Yes					
	Sleep In or Booster Off	Yes					
Default	Status	Default Value					
	Power On Sequence	AP[2:0] = 100, others OTP value					
	S/W Reset	AP[2:0] = 100, others OTP value					
	H/W Reset	AP[2:0] = 100, others OTP value					
Flow Chart							

6.2.35 SETRGBIF: Set RGB interface related register (B3h)

B3 H		SETRGBIF(Set RGB interface related register)																						
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	0	1	1	0	0	1	1	B3														
1 st parameter	1	-	-	-	-	DPL (0)	HSPL (0)	VSPL (0)	EPL (0)	-														
Description		This command is used to set RGB interface related register EPL: Specify the polarity of Enable pin in RGB interface mode.																						
		<table border="1"> <tr> <th>EPL</th> <th>ENABLE pin</th> <th>Display</th> </tr> <tr> <td>0</td> <td>0</td> <td>Enable</td> </tr> <tr> <td>0</td> <td>1</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>1</td> <td>Enable</td> </tr> </table>										EPL	ENABLE pin	Display	0	0	Enable	0	1	Disable	1	0	Disable	1
EPL	ENABLE pin	Display																						
0	0	Enable																						
0	1	Disable																						
1	0	Disable																						
1	1	Enable																						
VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.																								
HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active																								
DPL: The polarity of DCK pin. When DPL=0, the data is read on the rising edge of DCK signal. When DPL=1, the data is read on the falling edge of DCK signal.																								
Restrictions																								
SETEXTC turn on to enable this command																								
Register Availability		<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes															
Status	Availability																							
Sleep Out	Yes																							
Sleep In or Booster Off	Yes																							
<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>OTP value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP value</td> </tr> </table>		Status	Default Value	Power On Sequence	OTP value	S/W Reset	OTP value	H/W Reset	OTP value															
Status	Default Value																							
Power On Sequence	OTP value																							
S/W Reset	OTP value																							
H/W Reset	OTP value																							
Flow Chart																								

6.2.36 SETCYC: Set Display Waveform Cycle (B4h)

SETCYC(Set display waveform cycles)																																																																																																																																																																																																																																																										
B4H	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																																																																																																																
Command	0	1	0	1	1	0	1	0	0	B4																																																																																																																																																																																																																																																
1 st parameter	1					NW[1:0]																																																																																																																																																																																																																																																				
2 nd Parameter	1					SON[7:0]																																																																																																																																																																																																																																																				
3 rd Parameter	1					SOFF[7:0]																																																																																																																																																																																																																																																				
4 th Parameter	1					EQS[7:0]																																																																																																																																																																																																																																																				
5 th Parameter	1					EQON[7:0]																																																																																																																																																																																																																																																				
6 th Parameter	1					GDON[7:0]																																																																																																																																																																																																																																																				
7 th Parameter	1					GDOFF[7:0]																																																																																																																																																																																																																																																				
8 th Parameter	1					GVSSP1[7:0]																																																																																																																																																																																																																																																				
9 th Parameter	1					GVSSP2[7:0]																																																																																																																																																																																																																																																				
This command is used to get setting of display waveform cycles																																																																																																																																																																																																																																																										
NW[1:0]: Inversion type setting																																																																																																																																																																																																																																																										
<table border="1"> <thead> <tr> <th>NW1</th><th>NW0</th><th>Inversion type</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Column inversion</td></tr> <tr> <td>0</td><td>1</td><td>1-dot inversion</td></tr> <tr> <td>1</td><td>0</td><td>2-dot inversion</td></tr> <tr> <td>1</td><td>1</td><td>Inhibit</td></tr> </tbody> </table>											NW1	NW0	Inversion type	0	0	Column inversion	0	1	1-dot inversion	1	0	2-dot inversion	1	1	Inhibit																																																																																																																																																																																																																																	
NW1	NW0	Inversion type																																																																																																																																																																																																																																																								
0	0	Column inversion																																																																																																																																																																																																																																																								
0	1	1-dot inversion																																																																																																																																																																																																																																																								
1	0	2-dot inversion																																																																																																																																																																																																																																																								
1	1	Inhibit																																																																																																																																																																																																																																																								
SON[7:0]: Specify the valid source output start time and illustrate on the follow figure.																																																																																																																																																																																																																																																										
<table border="1"> <thead> <tr> <th colspan="8">SON [7:0]</th><th>Source output start time</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>Inhibit</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td></td><td>1 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td></td><td>2 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td></td><td>3 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td></td><td>4 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td></td><td>5 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td></td><td>6 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td></td><td>7 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td></td><td>8 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td></td><td>9 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td></td><td>10 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td></td><td>11 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td></td><td>12 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td></td><td>13 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td></td><td>14 timing clock</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td></td><td>15 timing clock</td></tr> <tr> <td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td></td><td>250 timing clock</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td></td><td>251 timing clock</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td></td><td>252 timing clock</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td></td><td>253 timing clock</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td></td><td>254 timing clock</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td></td><td>255 timing clock</td></tr> </tbody> </table>											SON [7:0]								Source output start time	0	0	0	0	0	0	0	0		Inhibit	0	0	0	0	0	0	0	1		1 timing clock	0	0	0	0	0	0	1	0		2 timing clock	0	0	0	0	0	0	1	1		3 timing clock	0	0	0	0	0	1	0	0		4 timing clock	0	0	0	0	0	1	0	1		5 timing clock	0	0	0	0	0	1	1	0		6 timing clock	0	0	0	0	0	1	1	1		7 timing clock	0	0	0	0	1	0	0	0		8 timing clock	0	0	0	0	1	0	0	1		9 timing clock	0	0	0	0	1	0	1	0		10 timing clock	0	0	0	0	1	0	1	1		11 timing clock	0	0	0	0	1	1	0	0		12 timing clock	0	0	0	0	1	1	0	1		13 timing clock	0	0	0	0	1	1	1	0		14 timing clock	0	0	0	0	1	1	1	1		15 timing clock	1	1	1	1	1	0	1	0		250 timing clock	1	1	1	1	1	0	1	1		251 timing clock	1	1	1	1	1	1	0	0		252 timing clock	1	1	1	1	1	1	1	0		253 timing clock	1	1	1	1	1	1	1	0		254 timing clock	1	1	1	1	1	1	1	1		255 timing clock
SON [7:0]								Source output start time																																																																																																																																																																																																																																																		
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0	0	0	0	1	1	1	1		15 timing clock																																																																																																																																																																																																																																																	
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1	1	1	1	1	0	1	0		250 timing clock																																																																																																																																																																																																																																																	
1	1	1	1	1	0	1	1		251 timing clock																																																																																																																																																																																																																																																	
1	1	1	1	1	1	0	0		252 timing clock																																																																																																																																																																																																																																																	
1	1	1	1	1	1	1	0		253 timing clock																																																																																																																																																																																																																																																	
1	1	1	1	1	1	1	0		254 timing clock																																																																																																																																																																																																																																																	
1	1	1	1	1	1	1	1		255 timing clock																																																																																																																																																																																																																																																	
1 timing clock = 1 * the frequency of OSC clock																																																																																																																																																																																																																																																										
SOFF[7:0]: Specify the valid source output end time and illustrate on the follow figure.																																																																																																																																																																																																																																																										

SOFF [7:0]								Source output end time
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	1 timing clock
0	0	0	0	0	0	1	0	2 timing clock
0	0	0	0	0	0	1	1	3 timing clock
0	0	0	0	0	1	0	0	4 timing clock
0	0	0	0	0	1	0	1	5 timing clock
0	0	0	0	0	1	1	0	6 timing clock
0	0	0	0	0	1	1	1	7 timing clock
0	0	0	0	1	0	0	0	8 timing clock
0	0	0	0	1	0	0	1	9 timing clock
0	0	0	0	1	0	1	0	10 timing clock
0	0	0	0	1	0	1	1	11 timing clock
0	0	0	0	1	1	0	0	12 timing clock
0	0	0	0	1	1	0	1	13 timing clock
0	0	0	0	1	1	1	0	14 timing clock
0	0	0	0	1	1	1	1	15 timing clock
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1	1	1	1	1	0	1	0	250 timing clock
1	1	1	1	1	0	1	1	251 timing clock
1	1	1	1	1	1	0	0	252 timing clock
1	1	1	1	1	1	0	1	253 timing clock
1	1	1	1	1	1	1	0	254 timing clock
1	1	1	1	1	1	1	1	255 timing clock

1 timing clock = 1 * the frequency of OSC clock

GDON[7:0]: Specify the valid gate output start time and illustrate on the follow figure.

GDON [7:0]								Gate output start time
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	1 timing clock
0	0	0	0	0	0	1	0	2 timing clock
0	0	0	0	0	0	1	1	3 timing clock
0	0	0	0	0	1	0	0	4 timing clock
0	0	0	0	0	1	0	1	5 timing clock
0	0	0	0	0	1	1	0	6 timing clock
0	0	0	0	0	1	1	1	7 timing clock
0	0	0	0	1	0	0	0	8 timing clock
0	0	0	0	1	0	0	1	9 timing clock
0	0	0	0	1	0	1	0	10 timing clock
0	0	0	0	1	0	1	1	11 timing clock
0	0	0	0	1	1	0	0	12 timing clock
0	0	0	0	1	1	0	1	13 timing clock
0	0	0	0	1	1	1	0	14 timing clock
0	0	0	0	1	1	1	1	15 timing clock
.
.
.
1	1	1	1	1	0	1	0	250 timing clock
1	1	1	1	1	0	1	1	251 timing clock
1	1	1	1	1	1	0	0	252 timing clock
1	1	1	1	1	1	0	1	253 timing clock
1	1	1	1	1	1	1	0	254 timing clock
1	1	1	1	1	1	1	1	255 timing clock

1 timing clock = 1 * the frequency of OSC clock

GDOFF[7:0]: Specify the gate output end time and illustrate on the follow figure.

GDOFF [7:0]								Gate output end time
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	1 timing clock
0	0	0	0	0	0	1	0	2 timing clock
0	0	0	0	0	0	1	1	3 timing clock
0	0	0	0	0	1	0	0	4 timing clock
0	0	0	0	0	1	0	1	5 timing clock
0	0	0	0	0	1	1	0	6 timing clock
0	0	0	0	0	1	1	1	7 timing clock
0	0	0	0	1	0	0	0	8 timing clock
0	0	0	0	1	0	0	1	9 timing clock
0	0	0	0	1	0	1	0	10 timing clock
0	0	0	0	1	0	1	1	11 timing clock
0	0	0	0	1	1	0	0	12 timing clock
0	0	0	0	1	1	0	1	13 timing clock
0	0	0	0	1	1	1	0	14 timing clock
0	0	0	0	1	1	1	1	15 timing clock
.
1	1	1	1	1	0	1	0	250 timing clock
1	1	1	1	1	0	1	1	251 timing clock
1	1	1	1	1	1	0	0	252 timing clock
1	1	1	1	1	1	0	1	253 timing clock
1	1	1	1	1	1	1	0	254 timing clock
1	1	1	1	1	1	1	1	255 timing clock

1 timing clock = 1 * the frequency of OSC clock

EQON[7:0]: Specify the valid Equalize output start time and illustrate on the follow figure.
(Please note that the EQON[7:0] < EQS[7:0]-1).

EQON [7:0]								Gate output start time
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	1 timing clock
0	0	0	0	0	0	1	0	2 timing clock
0	0	0	0	0	0	1	1	3 timing clock
0	0	0	0	0	1	0	0	4 timing clock
0	0	0	0	0	1	0	1	5 timing clock
0	0	0	0	0	1	1	0	6 timing clock
0	0	0	0	0	1	1	1	7 timing clock
0	0	0	0	1	0	0	0	8 timing clock
0	0	0	0	1	0	0	1	9 timing clock
0	0	0	0	1	0	1	0	10 timing clock
0	0	0	0	1	0	1	1	11 timing clock
0	0	0	0	1	1	0	0	12 timing clock
0	0	0	0	1	1	0	1	13 timing clock
0	0	0	0	1	1	1	0	14 timing clock
0	0	0	0	1	1	1	1	15 timing clock
.
1	1	1	1	1	0	1	0	250 timing clock
1	1	1	1	1	0	1	1	251 timing clock
1	1	1	1	1	1	0	0	252 timing clock
1	1	1	1	1	1	0	1	253 timing clock
1	1	1	1	1	1	1	0	254 timing clock
1	1	1	1	1	1	1	1	255 timing clock

1 timing clock = 1 * the frequency of OSC clock

EQS[7:0]: Specify the Equalize time of source output and illustrate on the follow figure. (Please note that the EQS[7:0] ≤ SON-1).

EQS [7:0]								Equalize time of source output
0	0	0	0	0	0	0	0	Equalize function off
0	0	0	0	0	0	0	1	1 timing clock
0	0	0	0	0	0	1	0	2 timing clock
0	0	0	0	0	0	1	1	3 timing clock
0	0	0	0	0	1	0	0	4 timing clock
0	0	0	0	0	1	0	1	5 timing clock
0	0	0	0	0	1	1	0	6 timing clock
0	0	0	0	0	1	1	1	7 timing clock
0	0	0	0	1	0	0	0	8 timing clock
0	0	0	0	1	0	0	1	9 timing clock
0	0	0	0	1	0	1	0	10 timing clock
0	0	0	0	1	0	1	1	11 timing clock
0	0	0	0	1	1	0	0	12 timing clock
0	0	0	0	1	1	0	1	13 timing clock
0	0	0	0	1	1	1	0	14 timing clock
0	0	0	0	1	1	1	1	15 timing clock
.
.
1	1	1	1	1	0	1	0	250 timing clock
1	1	1	1	1	0	1	1	251 timing clock
1	1	1	1	1	1	0	0	252 timing clock
1	1	1	1	1	1	1	0	253 timing clock
1	1	1	1	1	1	1	0	254 timing clock
1	1	1	1	1	1	1	1	255 timing clock

1 timing clock = 1 * the frequency of OSC clock

GVSSP1[7:0]: Specify the stop time of first Gate EQ of two step gate output and illustrate on the follow figure.

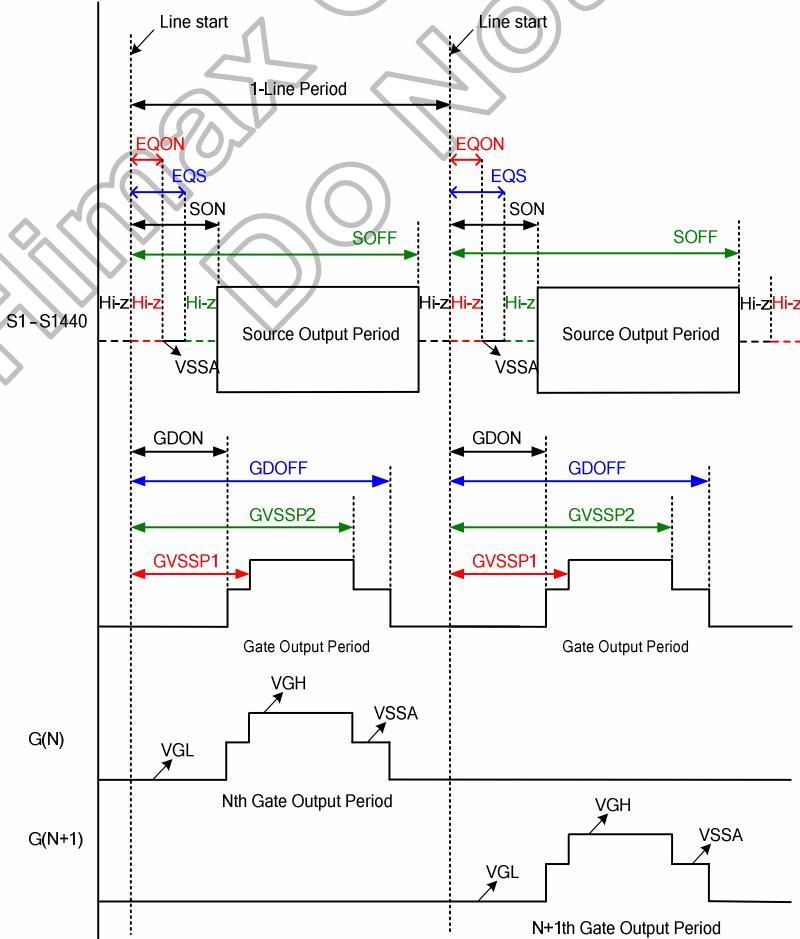
GVSSP1 [7:0]								Stop time of 1 st Gate EQ
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	1 timing clock
0	0	0	0	0	0	1	0	2 timing clock
0	0	0	0	0	0	1	1	3 timing clock
0	0	0	0	0	1	0	0	4 timing clock
0	0	0	0	0	1	0	1	5 timing clock
0	0	0	0	0	1	1	0	6 timing clock
0	0	0	0	0	1	1	1	7 timing clock
0	0	0	0	1	0	0	0	8 timing clock
0	0	0	0	1	0	0	1	9 timing clock
0	0	0	0	1	0	1	0	10 timing clock
0	0	0	0	1	0	1	1	11 timing clock
0	0	0	0	1	1	0	0	12 timing clock
0	0	0	0	1	1	0	1	13 timing clock
0	0	0	0	1	1	1	0	14 timing clock
0	0	0	0	1	1	1	1	15 timing clock
.
.
1	1	1	1	1	0	1	0	250 timing clock
1	1	1	1	1	0	1	1	251 timing clock
1	1	1	1	1	1	0	0	252 timing clock
1	1	1	1	1	1	1	0	253 timing clock
1	1	1	1	1	1	1	0	254 timing clock
1	1	1	1	1	1	1	1	255 timing clock

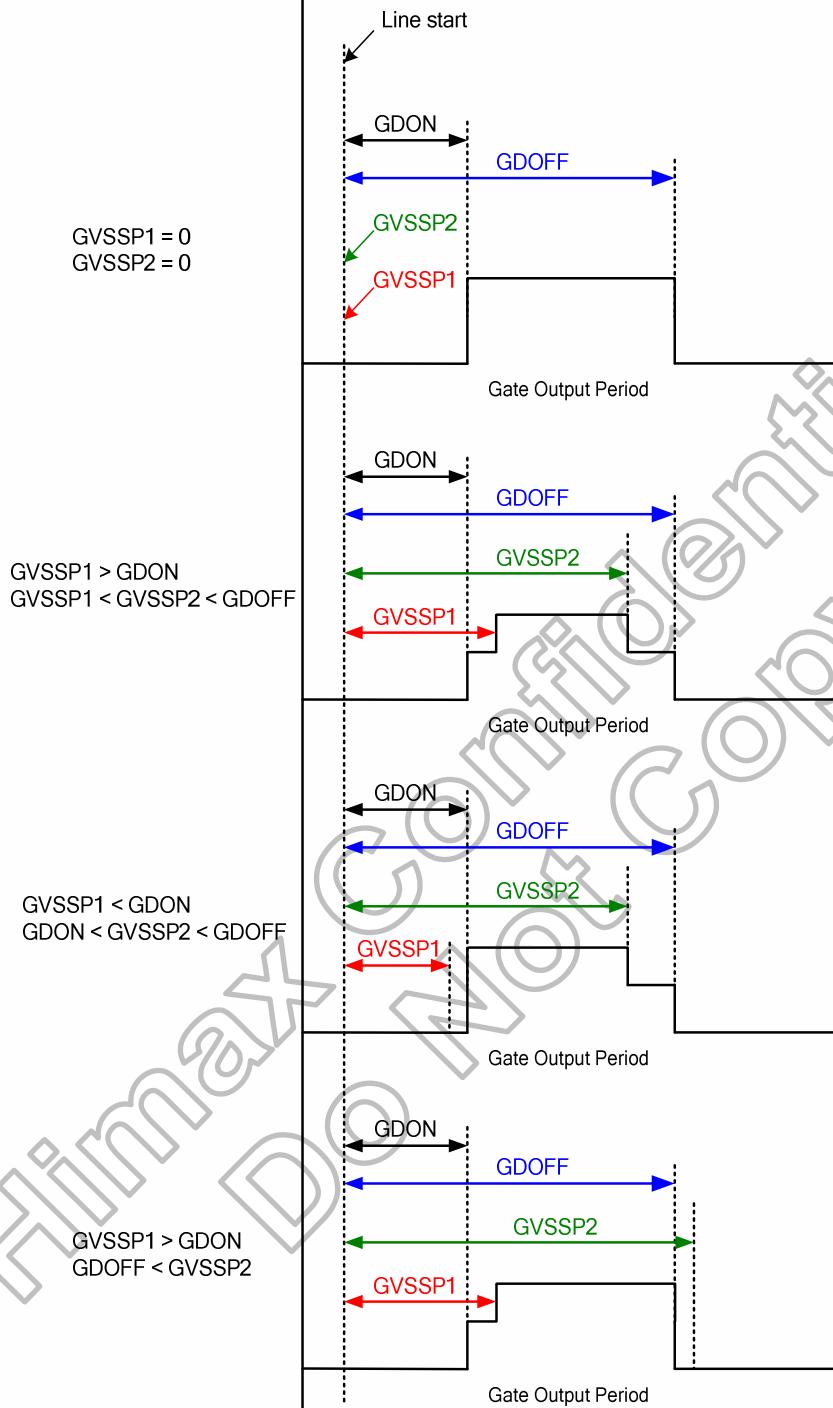
1 timing clock = 1 * the frequency of OSC clock

GVSSP2[7:0]: Specify the start time of second Gate EQ of two step gate output and illustrate on the follow figure.

GVSSP2 [7:0]									Start time of 2 nd Gate EQ
0	0	0	0	0	0	0	0	Inhibit	
0	0	0	0	0	0	0	1	1 timing clock	
0	0	0	0	0	0	1	0	2 timing clock	
0	0	0	0	0	0	1	1	3 timing clock	
0	0	0	0	0	1	0	0	4 timing clock	
0	0	0	0	0	1	0	1	5 timing clock	
0	0	0	0	0	1	1	0	6 timing clock	
0	0	0	0	0	1	1	1	7 timing clock	
0	0	0	0	1	0	0	0	8 timing clock	
0	0	0	0	1	0	0	1	9 timing clock	
0	0	0	0	1	0	1	0	10 timing clock	
0	0	0	0	1	0	1	1	11 timing clock	
0	0	0	0	1	1	0	0	12 timing clock	
0	0	0	0	1	1	0	1	13 timing clock	
0	0	0	0	1	1	1	0	14 timing clock	
0	0	0	0	1	1	1	1	15 timing clock	
.
.
1	1	1	1	1	1	0	1	0	250 timing clock
1	1	1	1	1	1	0	1	1	251 timing clock
1	1	1	1	1	1	1	0	0	252 timing clock
1	1	1	1	1	1	1	0	1	253 timing clock
1	1	1	1	1	1	1	1	0	254 timing clock
1	1	1	1	1	1	1	1	1	255 timing clock

1 timing clock = 1 * the frequency of OSC clock





Restrictions	SETEXTC turn on to enable this command	
Register Availability	Status	Availability
	Sleep Out	Yes
Default	Sleep In or Booster Off	Yes
	Status	Default Value
	Power On Sequence	OTP value
S/W Reset		
H/W Reset		
Flow Chart		

6.2.37 SETVCOM: Set VCOM Voltage (B6h)

B6 H	SETVCOM (Set VCOM Voltage)									
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	0	1	1	0	B6
1 st parameter	1	VCMC7	VCMC6	VCMC5	VCMC4	VCMC3	VCMC2	VCMC1	VCMC0	-
This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage										
Description	VCMC[7:0]: DC VCOM voltage setting . When set VSNR=VSN, VCOM output is 0V.								VCOM	
	0	0	0	0	0	0	0	0	-2	
	0	0	0	0	0	0	0	1	-1.984	
	0	0	0	0	0	0	1	0	-1.968	
	0	0	0	0	0	0	1	1	-1.952	
	0	0	0	0	0	1	0	0	-1.936	
	0	0	0	0	0	1	0	1	-1.92	
	0	0	0	0	0	1	1	0	-1.904	
	0	0	0	0	0	1	1	1	-1.888	
	0	0	0	0	1	0	0	0	-1.872	
	0	0	0	0	1	0	0	1	-1.856	
	0	0	0	0	1	0	1	0	-1.84	
	0	0	0	0	1	0	1	1	-1.824	
	0	0	0	0	1	1	0	0	-1.808	
	0	0	0	0	1	1	0	1	-1.792	
	0	0	0	0	1	1	1	0	-1.776	
	0	0	0	0	1	1	1	1	-1.76	
	0	0	0	1	0	0	0	0	-1.744	
	0	0	0	1	0	0	0	1	-1.728	
	0	0	0	1	0	0	1	0	-1.712	
	0	0	0	1	0	0	1	1	-1.696	
	0	0	0	1	0	1	0	0	-1.68	
	0	0	0	1	0	1	0	1	-1.664	
	0	0	0	1	0	1	1	0	-1.648	
	0	0	0	1	0	1	1	1	-1.632	
	0	0	0	1	1	0	0	0	-1.616	
	0	0	0	1	1	0	0	1	-1.6	
	0	0	0	1	1	0	1	0	-1.584	
	0	0	0	1	1	0	1	1	-1.568	
	0	0	0	1	1	1	0	0	-1.552	
	0	0	0	1	1	1	0	1	-1.536	
	0	0	0	1	1	1	1	0	-1.52	
	0	0	0	1	1	1	1	1	-1.504	
	0	0	1	0	0	0	0	0	-1.488	
	0	0	1	0	0	0	0	1	-1.472	
	0	0	1	0	0	0	1	0	-1.456	
	0	0	1	0	0	0	1	1	-1.44	
	0	0	1	0	0	1	0	0	-1.424	
	0	0	1	0	0	1	0	1	-1.408	
	0	0	1	0	0	1	1	0	-1.392	
	0	0	1	0	0	1	1	1	-1.376	
	0	0	1	0	1	0	0	0	-1.36	
	0	0	1	0	1	0	0	1	-1.344	
	0	0	1	0	1	0	1	0	-1.328	
	0	0	1	0	1	0	1	1	-1.312	
	0	0	1	0	1	1	0	0	-1.296	
	0	0	1	0	1	1	0	1	-1.28	

		0	0	1	0	1	1	0	0	-1.296
		0	0	1	0	1	1	0	1	-1.28
		0	0	1	0	1	1	1	0	-1.264
		0	0	1	0	1	1	1	1	-1.248
		0	0	1	1	0	0	0	0	-1.232
		0	0	1	1	0	0	0	1	-1.216
		0	0	1	1	0	0	1	0	-1.2
		0	0	1	1	0	0	1	1	-1.184
		0	0	1	1	0	1	0	0	-1.168
		0	0	1	1	0	1	0	1	-1.152
		0	0	1	1	0	1	1	0	-1.136
		0	0	1	1	0	1	1	1	-1.12
		0	0	1	1	1	0	0	0	-1.104
		0	0	1	1	1	0	0	1	-1.088
		0	0	1	1	1	0	1	0	-1.072
		0	0	1	1	1	0	1	1	-1.056
		0	0	1	1	1	1	0	0	-1.04
		0	0	1	1	1	1	0	1	-1.024
		0	0	1	1	1	1	1	0	-1.008
		0	0	1	1	1	1	1	1	-0.992
		0	1	0	0	0	0	0	0	-0.976
		0	1	0	0	0	0	0	1	-0.96
		0	1	0	0	0	0	1	0	-0.944
		0	1	0	0	0	0	1	1	-0.928
		0	1	0	0	0	1	0	0	-0.912
		0	1	0	0	0	1	0	1	-0.896
		0	1	0	0	0	1	1	0	-0.88
		0	1	0	0	0	1	1	1	-0.864
		0	1	0	0	1	0	0	0	-0.848
		0	1	0	0	1	0	0	1	-0.832
		0	1	0	0	1	0	1	0	-0.816
		0	1	0	0	1	0	1	1	-0.8
		0	1	0	0	1	1	0	0	-0.784
		0	1	0	0	1	1	0	1	-0.768
		0	1	0	0	1	1	1	0	-0.752
		0	1	0	0	1	1	1	1	-0.736
		0	1	0	1	0	0	0	0	-0.72
		0	1	0	1	0	0	0	1	-0.704
		0	1	0	1	0	0	1	0	-0.688
		0	1	0	1	0	0	1	1	-0.672
		0	1	0	1	0	1	0	0	-0.656
		0	1	0	1	0	1	0	1	-0.64
		0	1	0	1	0	1	1	0	-0.624
		0	1	0	1	0	1	1	1	-0.608
		0	1	0	1	1	0	0	0	-0.592
		0	1	0	1	1	0	0	1	-0.576
		0	1	0	1	1	0	1	0	-0.56
		0	1	0	1	1	0	1	1	-0.544
		0	1	0	1	1	1	0	0	-0.528
		0	1	0	1	1	1	0	1	-0.512
		0	1	0	1	1	1	1	0	-0.496
		0	1	0	1	1	1	1	1	-0.48
		0	1	1	0	0	0	0	0	-0.464
		0	1	1	0	0	0	0	1	-0.448
		0	1	1	0	0	0	1	0	-0.432
		0	1	1	0	0	0	1	1	-0.416
		0	1	1	0	0	1	0	0	-0.4

0	1	1	0	0	1	0	1	-0.384
0	1	1	0	0	1	1	0	-0.368
0	1	1	0	0	1	1	1	-0.352
0	1	1	0	1	0	0	0	-0.336
0	1	1	0	1	0	0	1	-0.32
0	1	1	0	1	0	1	0	-0.304
0	1	1	0	1	0	1	1	-0.288
0	1	1	0	1	1	0	0	-0.272
0	1	1	0	1	1	0	1	-0.256
0	1	1	0	1	1	1	0	-0.24
0	1	1	0	1	1	1	1	-0.224
0	1	1	1	0	0	0	0	-0.208
0	1	1	1	0	0	0	1	-0.192
0	1	1	1	0	0	1	0	-0.176
0	1	1	1	0	0	1	1	-0.16
0	1	1	1	0	1	0	0	-0.144
0	1	1	1	0	1	0	1	-0.128
0	1	1	1	0	1	1	0	-0.112
0	1	1	1	0	1	1	1	-0.096
0	1	1	1	1	0	0	0	-0.08
0	1	1	1	1	0	0	1	-0.064
0	1	1	1	1	0	1	0	-0.048
0	1	1	1	1	0	1	1	-0.032
0	1	1	1	1	1	0	0	-0.016
01111101 ~ 01111101								Inhibit
0	1	1	1	1	1	1	0	VCOMR
0	1	1	1	1	1	1	1	VSSA
10000000 ~ 11111110								Inhibit
1	1	1	1	1	1	1	1	HZ

Restrictions SETEXTC turn on to enable this command

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	Status	Default Value
	Power On Sequence	OTP value
	S/W Reset	OTP value
	H/W Reset	OTP value

Flow Chart

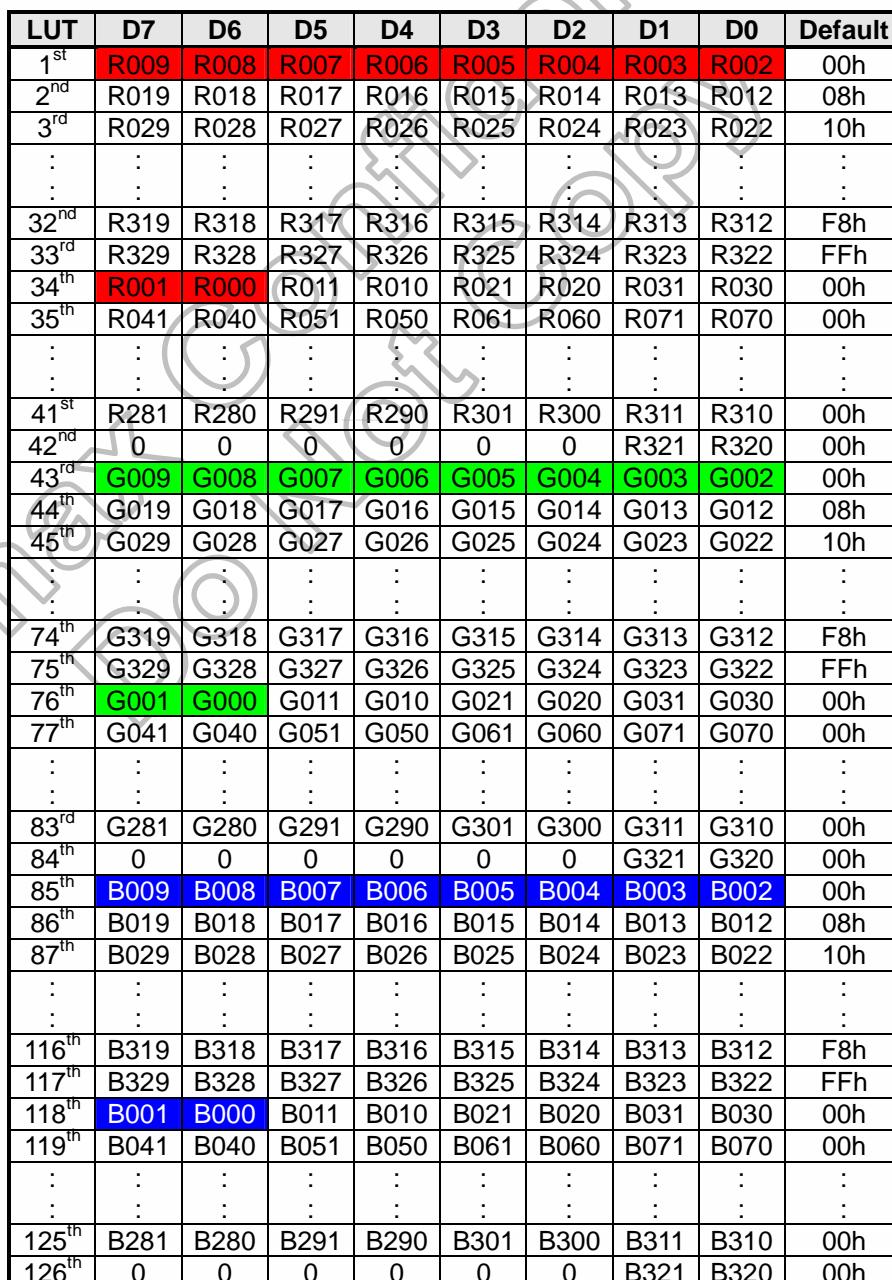
6.2.38 SETEXTC: Enable extension command (B9h)

SETEXTC (Set extended command set)										HEX
B9 H	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	0	0	1	B9
1 st parameter	1					EXTC1[7:0](00)				-
2 nd parameter	1					EXTC2[7:0](00)				-
3 rd parameter	1					EXTC3[7:0](00)				-
Description	This command is used to set extended command set access enable.									
	Extend cmd	Command description								
	Enable	After command (B9h), must write 3 parameters (ffh,83h,63h) by order								
	Disable(default)	After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (ffh,83h,63h)								
Restrictions										
Register Availability	Status		Availability							
	Sleep Out		Yes							
	Sleep In or Booster Off		Yes							

6.2.39 SETOTP: Set OTP (BBh)

BB H	SETOTP(Set OTP Related Setting)																			
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
Command	0	1	0	1	1	1	0	1	1	BB										
1 st parameter	1	OTP_LO AD_DISABLE (0)	-	OTP_PC E	OTP_PW E (0)	OTP_PT[2:0]			OTP_PR OG											
2 nd parameter	1	OTP_MASK[7:0] (8'b0)								-										
3 rd parameter	1	OTP_INDEX[7:0] (8'b1111_1111)								-										
4 th parameter	1	OTP_DATA_READ								-										
Description	This command is used to set OTP Related Setting. OTP_MASK[7:0]: Bit programming mask, if 1, means this bit can't be programmed. OTP_INDEX[7:0]: Set index of OTP table for programming. OTP_PWE: OTP program write enable, if 1, means OTP is able to be programmed. OTP_PROG: When set to 1, the register content of OTP index is programmed. OTP_DATA_READ: When set to 1, read back the content of the index within OTP table. OTP_LOAD_DISABLE: Normally the internal registers are auto-loaded from OTP when the SLOUT command is received. Nevertheless, if this bit is set to 1, it will disable the auto loading function when the SLOUT command was received. In general, this bit is used when OTP is not yet programmed. OTP_PCE: Not open, internal use. OTP_PT[2:0]: Not open, internal use.																			
Restrictions	SETEXTC turn on to enable this command																			
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes				
Status	Availability																			
Sleep Out	Yes																			
Sleep In or Booster Off	Yes																			
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_READ=0, OTP_PROG=0, OTP_LOAD_DISABLE=0, OTP_PWE=0, OTP_PCE=0, OTP_PT[2:0]=3'b000</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">OTP_MASK[7:0]=No Change, OTP_INDEX[7:0]= No Change, OTP_READ= No Change, OTP_PROG= No Change, OTP_LOAD_DISABLE= No Change, OTP_PWE=No Change, OTP_PCE= No Change, OTP_PT[2:0]= No Change</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_READ=0, OTP_PROG=0, OTP_LOAD_DISABLE=0, OTP_PWE=0, OTP_PCE=0, OTP_PT[2:0]=3'b000</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_READ=0, OTP_PROG=0, OTP_LOAD_DISABLE=0, OTP_PWE=0, OTP_PCE=0, OTP_PT[2:0]=3'b000	S/W Reset	OTP_MASK[7:0]=No Change, OTP_INDEX[7:0]= No Change, OTP_READ= No Change, OTP_PROG= No Change, OTP_LOAD_DISABLE= No Change, OTP_PWE=No Change, OTP_PCE= No Change, OTP_PT[2:0]= No Change	H/W Reset	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_READ=0, OTP_PROG=0, OTP_LOAD_DISABLE=0, OTP_PWE=0, OTP_PCE=0, OTP_PT[2:0]=3'b000		
Status	Default Value																			
Power On Sequence	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_READ=0, OTP_PROG=0, OTP_LOAD_DISABLE=0, OTP_PWE=0, OTP_PCE=0, OTP_PT[2:0]=3'b000																			
S/W Reset	OTP_MASK[7:0]=No Change, OTP_INDEX[7:0]= No Change, OTP_READ= No Change, OTP_PROG= No Change, OTP_LOAD_DISABLE= No Change, OTP_PWE=No Change, OTP_PCE= No Change, OTP_PT[2:0]= No Change																			
H/W Reset	OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_READ=0, OTP_PROG=0, OTP_LOAD_DISABLE=0, OTP_PWE=0, OTP_PCE=0, OTP_PT[2:0]=3'b000																			
Flow Chart																				

6.2.40 SETDGCLUT: Set DGC LUT (C1h)

C1 H	SETDGCLUT (Set DGC LUT)									
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	0	1	C1
1 st parameter									DGC_EN	
2 nd parameter	1				D1[7:0]					--
:		1			Dn[7:0]					--
127 th parameter	1				D126[7:0]					--
Description	This command is used to set DGC LUT. DGC_EN: Enable the DGC function DGC_EN=0, DGC function is disabled. DGC_EN=1, DGC function is enabled. D1[7:0] ~ D126[7:0]: 									
Restrictions	SETEXTC turn on to enable this command									

Register Availability	Status	Availability
Sleep Out	Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	OTP value
	S/W Reset	OTP value
	H/W Reset	OTP value
Flow Chart		

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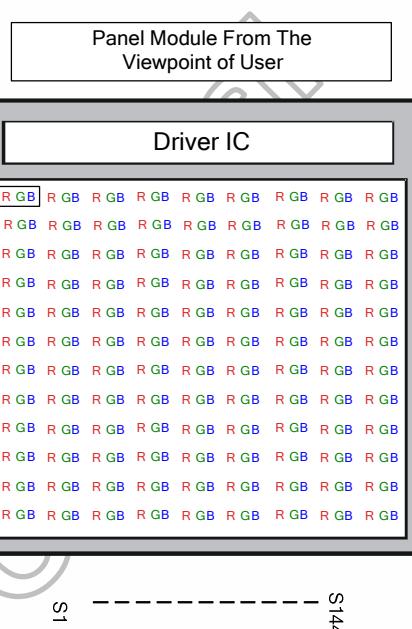
6.2.41 SETID: Set ID (C3h)

C3 H	SETID (Set ID)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	0	0	0	1	1	C3								
1 st parameter	1					ID1[7:0](8'b0)				-								
2 nd parameter	1					ID2[6:0](7'b0)				-								
3 rd parameter	1					ID3[7:0](8'b0)				-								
Description	This command is used to set DAh, DBh, DCh value																	
Restrictions	SETEXTC turn on to enable this command																	
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes										
Status	Availability																	
Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>OTP value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP value</td> </tr> </table>		Status	Default Value	Power On Sequence	OTP value	S/W Reset	OTP value	H/W Reset	OTP value								
Status	Default Value																	
Power On Sequence	OTP value																	
S/W Reset	OTP value																	
H/W Reset	OTP value																	
Flow Chart																		

6.2.42 SETDDB: Set DDB (C4h)

C4 H	SETDDB (Set DDB)									HEX									
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	1	0	0	0	1	0	0	C4									
1 st parameter	1				DDB1[7:0](8'b0)					-									
2 nd parameter	1				DDB2[7:0](8'b0)					-									
3 rd parameter	1				DDB3[7:0](8'b0)					-									
4 th parameter	1				DDB4[7:0](8'b0)														
Description	This command is used to set A1h DDB1~4 value																		
Restrictions	SETEXTC turn on to enable this command																		
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes											
Status	Availability																		
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Status	Default Value																		
Power On Sequence	OTP value																		
S/W Reset	OTP value																		
H/W Reset	OTP value																		
Flow Chart																			

6.2.43 SETPANEL (CCh)

CC H	SETPANEL(Set panel related register)																	
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	0	1	1	0	0	CC								
1 st parameter	1	-	-	-	SM_PANEL	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	-								
Description	<p>This command is used to set setting of panel related register and make panel module meets below spec from viewpoint of user</p> <p>Portrait type (mux 1:3)</p> <p>480(H) x RGB(H) x 864(V) 480(H) x RGB(H) x 854(V) 480(H) x RGB(H) x 800(V) 480(H) x RGB(H) x 640(V) 360(H) x RGB(H) x 640(V)</p> <p>The default position (display driver, glass, filter order, etc.) of the panel module is always as follow, when MADCTL's (36h) parameter is 00h. The color filter order is always RGB (if color filters are used).</p> <p>The 1st pixel on the display This is also the 1st access location of the frame memory (driver IC) when there is displayed the 1st visible pixel</p> 																	
Restrictions	SETEXTC turn on to enable this command																	
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes										
Status	Availability																	
Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>OTP value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP value</td> </tr> </table>		Status	Default Value	Power On Sequence	OTP value	S/W Reset	OTP value	H/W Reset	OTP value								
Status	Default Value																	
Power On Sequence	OTP value																	
S/W Reset	OTP value																	
H/W Reset	OTP value																	
Flow Chart																		

6.2.44 SET SPI READ INDEX (FEh)

FE H	SET SPI READ INDEX (Set SPI READ Command Address)																		
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	1	1	1	1	1	1	0	FE									
1 st parameter	1	CMD_ADD[7:0]							-										
Description SET SPI READ Command Address for User Define Command																			
Restrictions SETEXTC turn on to enable this command																			
Register Availability	Status		Availability																
	Sleep Out		Yes																
	Sleep In or Booster Off		Yes																
Default	Status		Default Value																
	Power On Sequence		00h																
	S/W Reset		No Change																
	H/W Reset		00h																
Flow Chart																			

6.2.45 SPIREAD (FFh)

FF H	SPIREAD (Read SPI Command Data)															
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
Command	0	1	1	1	1	1	1	1	1	FF						
1 st parameter	1				CMD_DATA1[7:0]					-						
:	1				:					-						
N th parameter	1				CMD_DATAN[7:0]					-						
Description	Read SPI Command Data for User Define Command															
Restrictions	SETEXTC turn on to enable this command															
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>		Status	Availability	Sleep Out	Yes	Sleep In or Booster Off	Yes								
Status	Availability															
Sleep Out	Yes															
Sleep In or Booster Off	Yes															
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>No Change</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	No Change	H/W Reset	00h						
Status	Default Value															
Power On Sequence	00h															
S/W Reset	No Change															
H/W Reset	00h															
Flow Chart																

6.2.46 SETGAMMA: Set Gamma Curve Related Setting (E0h)

E0H	SETGAMMAR (Set Gamma Curve Related Setting)									
	DNC	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	0	0	0	0	0	E0
1 st parameter	1	-	-			G1_VRP0[5:0]				
2 nd parameter	1		G1_CGMP0[1:0]			G1_VRP1[5:0]				
3 rd Parameter	1		G1_CGMP1[1:0]			G1_VRP2[5:0]				
4 th Parameter	1		G1_CGMP2[1:0]			G1_VRP3[5:0]				
5 th Parameter	1		G1_CGMP3[1:0]			G1_VRP4[5:0]				
6 th Parameter	1		G1_CGMP5 G1_CGMP4			G1_VRP5[5:0]				
7 th Parameter	1	-	G1_PRP0[6]	-		G1_PKP0[4:0]				
8 th Parameter	1		G1_PRP0[5:4]	-		G1_PKP1[4:0]				
9 th Parameter	1		G1_PRP0[3:2]	-		G1_PKP2[4:0]				
10 th Parameter	1		G1_PRP0[1:0]	-		G1_PKP3[4:0]				
11 th Parameter	1	-	G1_PRP1[6]	-		G1_PKP4[4:0]				
12 th Parameter	1		G1_PRP1[5:4] (11)	-		G1_PKP5[4:0]				
13 th Parameter	1		G1_PRP1[3:2] (10)	-		G1_PKP6[4:0]				
14 th Parameter	1		G1_PRP1[1:0] (00)	-		G1_PKP7[4:0]				
15 th Parameter	1	-	-	-		G1_PKP8[4:0]				
16 th Parameter	1	-	-			G1_VRN0[5:0]				
17 th Parameter	1		G1_CGMN0[1:0]			G1_VRN1[5:0]				
18 th Parameter	1		G1_CGMN1[1:0]			G1_VRN2[5:0]				
19 th Parameter	1		G1_CGMN2[1:0]			G1_VRN3[5:0]				
20 th Parameter	1		G1_CGMN3[1:0]			G1_VRN4[5:0]				
21 st Parameter	1		G1_CGMN5 G1_CGMN4			G1_VRN5[5:0]				
22 nd Parameter	1			G1_PRN0[6]	-	G1_PKN0[4:0]				
23 rd Parameter	1		G1_PRN0[5:4]	-		G1_PKN1[4:0]				
24 th Parameter	1		G1_PRN0[3:2]	-		G1_PKN2[4:0]				
25 th Parameter	1		G1_PRN0[1:0]	-		G1_PKN3[4:0]				
26 th Parameter	1			G1_PRN1[6]	-	G1_PKN4[4:0]				
27 th Parameter	1		G1_PRN1[5:4]	-		G1_PKN5[4:0]				
28 th Parameter	1		G1_PRN1[3:2]	-		G1_PKN6[4:0]				
29 th Parameter	1		G1_PRN1[1:0]	-		G1_PKN7[4:0]				
30 th Parameter	1	-	-	-	-	G1_PKN8[4:0]				
Description	This command is used to set Red Gamma Curve 1 related setting									
	Register Groups	Positive Polarity	Negative Polarity	Description						
	Center Adjustment	G1_PRP0 6-0	G1_PRN0 6-0	Variable resistor (PRP/N0) for center adjustment						
		G1_PRP1 6-0	G1_PRN1 6-0	Variable resistor (PRP/N1)for center adjustment						
	Macro Adjustment	G1_PKP0 4-0	G1_PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)						
		G1_PKP1 4-0	G1_PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)						
		G1_PKP2 4-0	G1_PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)						
		G1_PKP3 4-0	G1_PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)						
		G1_PKP4 4-0	G1_PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)						
		G1_PKP5 4-0	G1_PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)						
		G1_PKP6 4-0	G1_PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)						
		G1_PKP7 4-0	G1_PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)						
		G1_PKP8 4-0	G1_PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)						
		G1_VRP0 5-0	G1_VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment						
Offset Adjustment		G1_VRP1 5-0	G1_VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment						
		G1_VRP2 5-0	G1_VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment						
		G1_VRP3 5-0	G1_VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment						
		G1_VRP4 5-0	G1_VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment						
		G1_VRP5 5-0	G1_VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment						
Restriction	SETEXTC turn on to enable this command									

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In or Booster Off	Yes
Default	Status	Default Value
	Power On Sequence	OTP value
	S/W Reset	OTP value
	H/W Reset	OTP value
Flow Chart		

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7. Power Supply

7.1 Power Supply Setup

7.1.1 Architecture 1 with PFM circuit

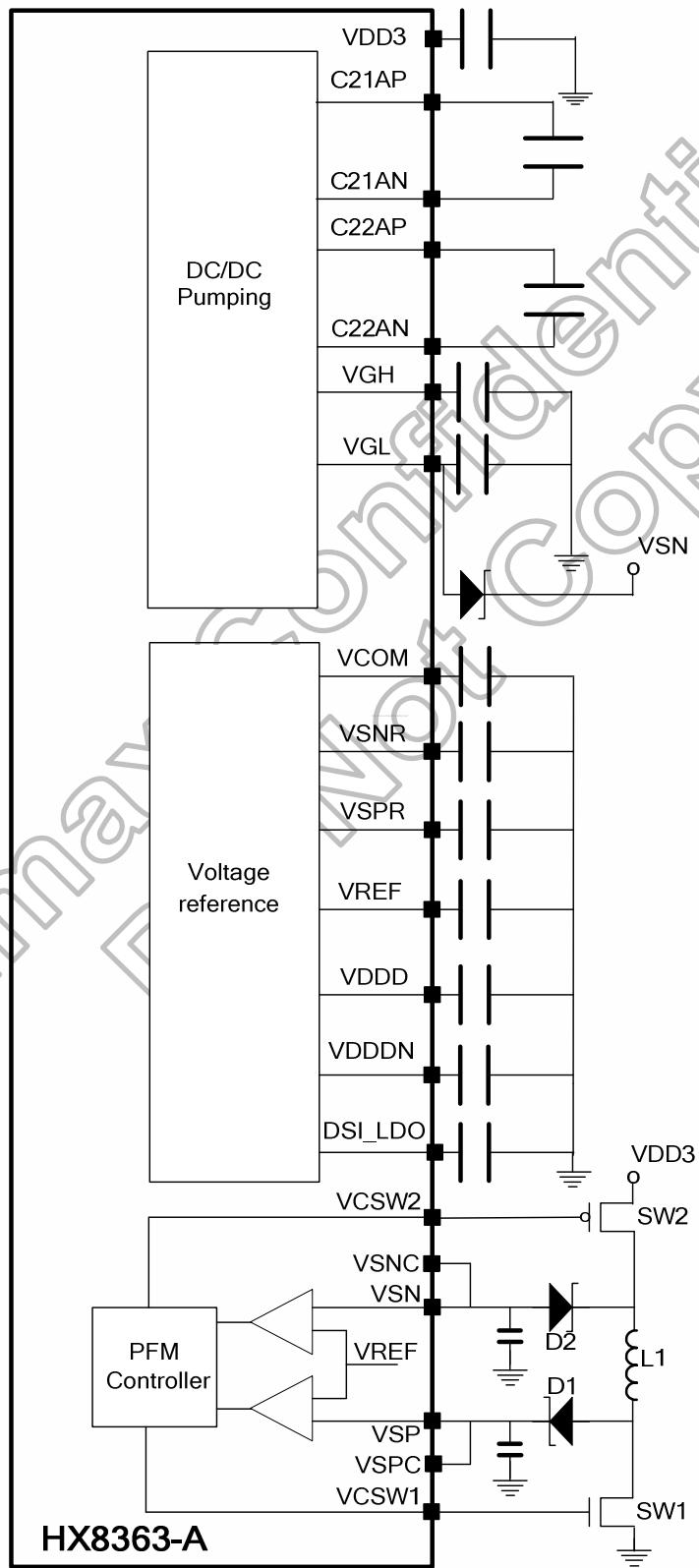


Figure 7.1: Power supply with PFM circuit

7.1.2 Architecture 2 with HX5186-A

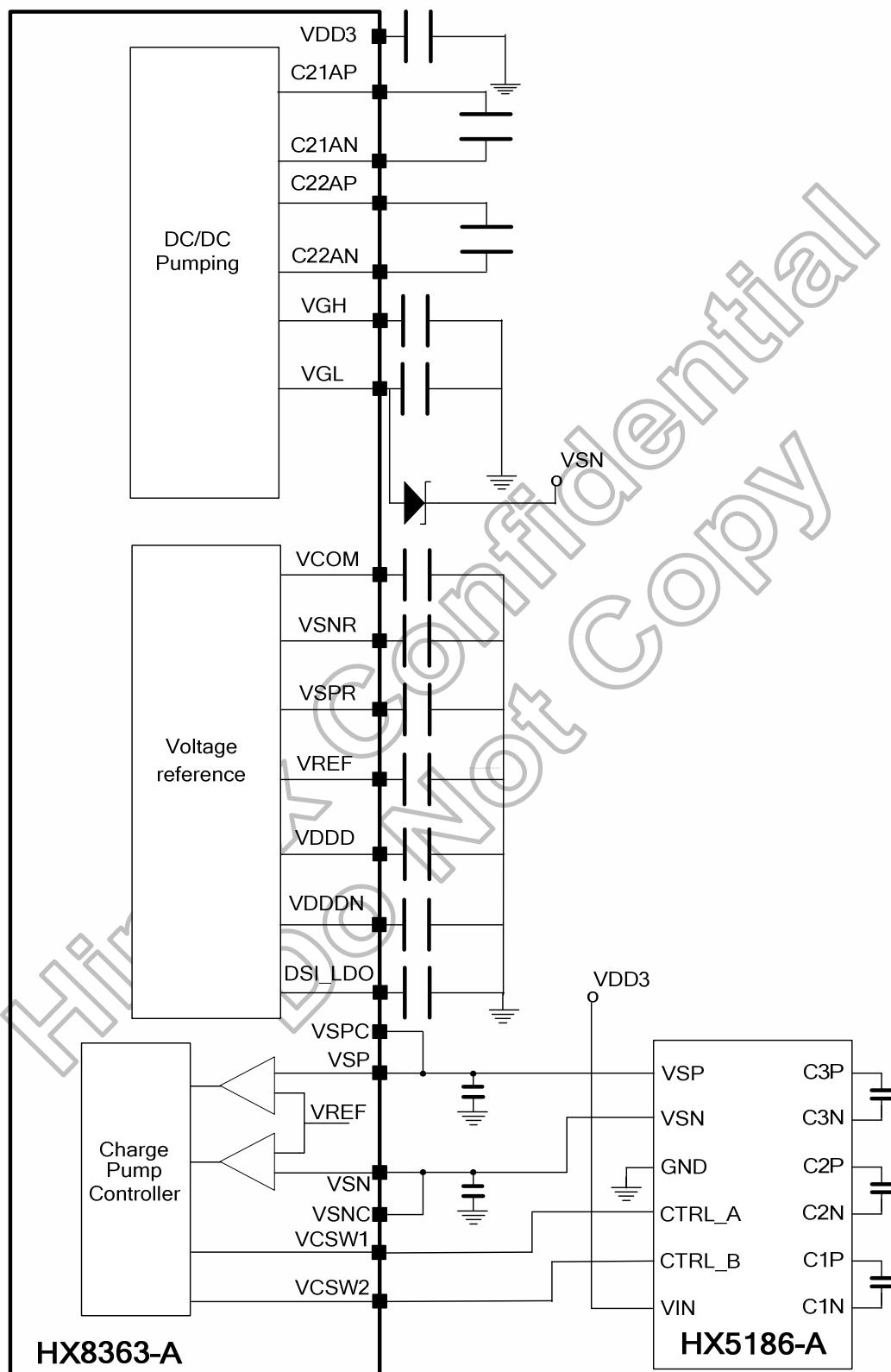


Figure 7.2: Power supply with HX5186-A

7.2 Voltage Configuration

The HX8363-A has an internal power supply circuit to drive TFTLCD panel. Please set up each voltage output according to the LCD panel.

Name	Function	Set up Value	Note
VREF	Reference voltage from internal band gap circuit	1.8V	-
VSP	DC/DC converter circuit output	4.7V ~ 5.5V	Do not exceed 6 V
VSN	DC/DC converter circuit output	-4.7V ~ -5.5V	Do not exceed 6V
VSPC	DC/DC converter circuit output	4.7V ~ 5.5V	Do not exceed 6 V
VSNC	DC/DC converter circuit output	-4.7V ~ -5.5V	Do not exceed 6V
VSPR	Reference voltage for gamma circuit	3.5V ~ (VSP - 0.5V)	Reference register
VSNR	Reference voltage for gamma circuit	-3.5V ~ (VSN + 0.5V)	Reference register
VDDDN	Logic power supply	-2.5V	-
VGH	Positive gate driver output voltage level	15V, 18V, 20V	Depend on VSP and VSN
VGL	Negative gate driver output voltage level	-8V, -10V, -12V	Depend on VSP and VSN
VCOM	VCOM DC voltage	-2V ~ 0V	-
VCOMR	External VCOM DC voltage	-2V ~ 0V	-
DSI_LDO	Analog power for MIPI DSI circuit	1.2V ~ 1.3V	-

Table 7.1: Power Supply Voltage Configuration

Pad Name	Connection	Typical Component Value
VCOM	Connect to Capacitor (Max 6V): VCOM ---(-)--- --- (+)--- VSSA	2.2µF
VGH	Connect to Capacitor (Max 25V): VGH ---(+)- --- (-)--- VSSA	1.0µF
C22AP - C22AN	Connect to Capacitor (Max 16V): C22AP ---(+)- --- (-)---C22AN	1.0µF
C21AP - C21AN	Connect to Capacitor (Max 16V): C21AP ---(+)- --- (-)---C21AN	1.0µF
VSPR	Connect to Capacitor (Max 10V): VSPR ---(+)- --- (-)---VSSA	1.0µF
VSNR	Connect to Capacitor (Max 10V): VSNR ---(+)- --- (-)---VSSA	1.0µF
VDDD	Connect to Capacitor (Max 6V): VDDD ---(+)- --- (-)---VSSA	1.0µF
VDDDN	Connect to Capacitor (Max 6V): VDDDN ---(+)- --- (-)---VSSA	1.0µF
VREF	Connect to Capacitor (Max 5V): VREF ---(-)--- --- (+)--- VSSA	1.0µF
VSP	Connect to Capacitor (Max 10V): VSP ---(+)- --- (-)---VSSA	2.2µF
	Schottky Diode for VSP(VR≥30V)	VF < 0.35V / 10mA @ 25°C, VR ≥30V (Recommended diode: KDR720F)
VSN	Connect to Capacitor (Max 10V): VSN ---(+)- --- (-)---VSSA	2.2µF
	Schottky Diode for VSN(VR≥30V)	VF < 0.35V / 10mA @ 25°C, VR ≥30V (Recommended diode: KDR720F)
VDD3	Connect to Capacitor (Max 6V): VDD3 ---(+)- --- (-)---VSSA	1.0µF
DSI_LDO	Connect to Capacitor (Max 6V): DSI_LDO ---(+)- --- (-)---DSI_VSS	1.0µF
VGL	Connect to Capacitor (Max 25V): VGL ---(-)--- --- (+)--- VSSA	1.0µF
	Connect to Schottky Diode(VR≥30V): VGL ---(+)--> --- (-)--- VSN	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)

Table 7.2: Adoptability of Component

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

The absolute maximum ratings are listed on Table 8.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDD1~VSSD	V	-0.3 to +4.6	Note ^{(1),(2)}
Power Supply Voltage 2	VDD2~VSSA	V	-0.3 to +4.6	Note ^{(1),(3)}
Power Supply Voltage 3	VDD3~VSSA	V	-0.3 to +4.6	Note ^{(1),(4)}
Power Supply Voltage 4	DSI_VCC ~ DSI_VSS	V	-0.3 to +4.6	Note ^{(1),(5)}
Power Supply Voltage 5	VSP~VSSA	V	-0.3 to +6	Note ⁽⁶⁾
Power Supply Voltage 6	VSSA~VSN	V	0 to -6	Note ⁽⁷⁾
Power Supply Voltage 7	VGH~VSSA	V	-0.3 to +25	Note ⁽⁸⁾
Power Supply Voltage 8	VSSA~VGL	V	0 to -16	Note ⁽⁹⁾
Input Voltage	V _{IN}	V	-0.3 to VDD1+0.3	Note ⁽¹⁰⁾
DSI Input Voltage	V _{DSIIN}	V	-0.3 to +2	Note ⁽¹¹⁾
Operating Temperature	T _{opr}	°C	-40 to +85	Note ⁽¹²⁾
Storage Temperature	T _{stg}	°C	-55 to +110	Note ⁽¹³⁾

Note: (1) VDD1, VSSD must be maintained.

(2) To make sure VDD1 ≥ VSSD.

(3) To make sure VDD2 ≥ VSSA.

(4) To make sure VDD3 ≥ VSSA.

(5) To make sure DSI_VCC ≥ DSI_VSS.

(6) To make sure VSP ≥ VSSA.

(7) To make sure VSSA ≥ VSN.

(8) To make sure VGH ≥ VSSA.

(9) To make sure VSSA ≥ VGL

VGH +|VGL| < 32V

(10) This specifications include input signals but without following: DSI_CP, DSI_CN, DSI_D0P, DSI_D0N, DSI_D1P, DSI_D1N.

(11) This specifications include following signals: DSI_CP, DSI_CN, DSI_D0P, DSI_D0N, DSI_D1P, DSI_D1N.

(12) For die and wafer products, specified up to +85°C.

(13) This temperature specifications apply to the TCP package.

Table 8.1: Absolute Maximum Rating

8.2 ESD Protection Level

Mode	Test Condition	Criteria	Standard
Human Body Model	C=100pF, R=1.5kΩ	±2.0KV	MIL-STD-883F Method 3015.7
Machine Model	C=200pF, R=0.0Ω	±200V	EIA/JEDEC JESD22-A115-A

Table 8.2: ESD Protection Level

8.3 DC Characteristics

(VDD2/3= 2.5~3.3V, VDDI = 1.65~3.3V, TA = -30 ~ 70 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V _{IH}	V	VDD1= 1.65 ~ 3.3V VDD2= 2.5 ~ 3.3V VDD3= 2.5 ~ 3.3V	0.7VDD1	-	VDD1	V
Input low voltage	V _{IL}	V		0	-	0.3VDD1	V
PVSS	V _{IH}	V	PVSS	7.25V	7.5V	7.75V	V
	V _{IL}	V					
Output high voltage (SDO, CABC_PWM_OUT)	V _{OH1}	V	I _{OH} = -1.0mA	0.8VDD1	-	VDD1	V
Output low voltage (SDO, CABC_PWM_OUT)	V _{OL1}	V	VDD1= 1.65 ~ 2.4V I _{OL} = 1.0mA	0	-	0.2VDD1	V
Logic High level input current	I _{IH}	μA	VSYNC, HSYNC	-	-	1	μA
			NRESET, SCL, NCS	-	-	1	μA
	I _{IHD}	μA	DB[23...0], SDI, SCL	-	-	1	μA
			DB[23...0]	-	-	1	μA
Logic Low level input current	I _{IL}	μA	VSYNC, HSYNC	-1	-	-	μA
			NRESET, (SCL), NCS	-1	-	-	μA
	I _{ILD}	μA	DB[23...0], SDI, SCL	-1	-	-	μA
			DB[17...0]	-1	-	-	μA

Note: (1) The PVSS pin is open on normal and setting when OTP programming condition.

Table 8.3: DC Characteristics

(VDD2/3= 2.5~3.3V, VDDI = 1.65~3.3V, TA = -30 ~ 70 °C)

Mode of operation	Image	Current consumption		
		IDD1 (mA)	IDD2 (mA)	IDD3 (mA)
Sleep Out Mode	Note ⁽¹⁾	0.02	0.05	9.1
	Note ⁽²⁾	0.86	0.05	32
	Note ⁽³⁾	0.44	0.05	15
	Note ⁽⁴⁾	0.02	0.05	9.8
Sleep In Mode	N/A	0.005	0.005	0.015

Note: (1) All pixels black.

(2) Checker board one by one.

(3) Checker board 4 by 4.

(4) Grayscale from top to bottom.

(5) Current consumption depends on panel loading 45pF, measure with HX5186-A, column inversion.

Table 8.4: Power consumptions

8.4 AC Characteristics

8.4.1 Serial Interface Characteristics (3-Pin Serial)

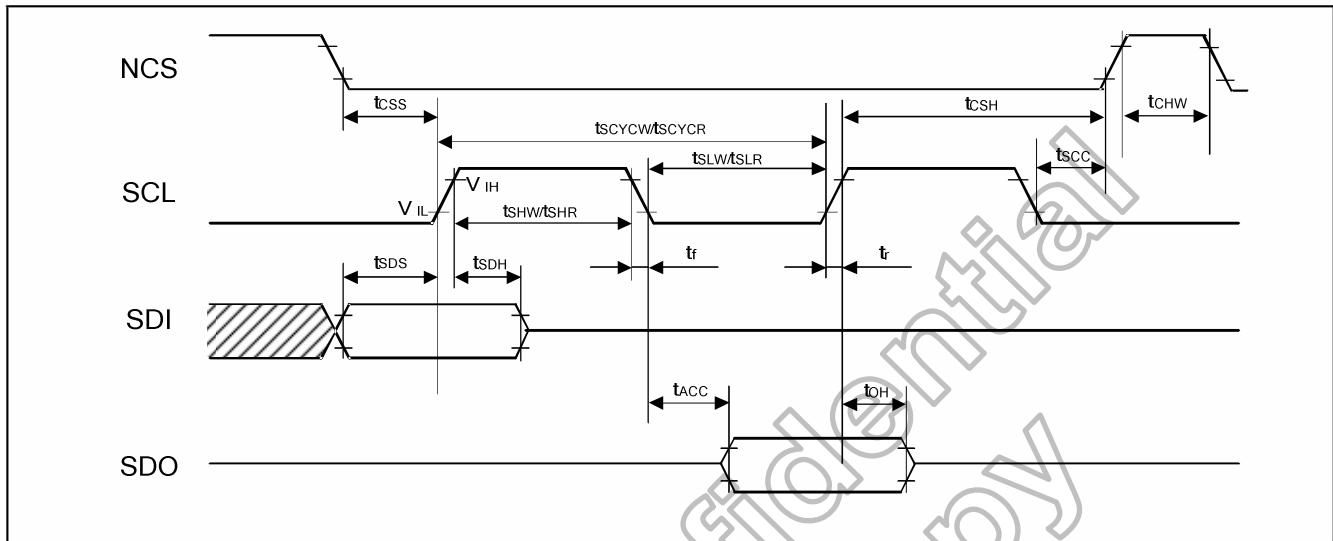


Figure 8.1: 3-pin Serial Interface Characteristics

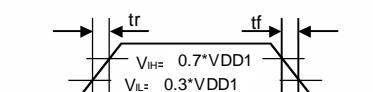
(VSSA=VSSD=0V, VDD1=1.65V to 1.95V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write)	t _{SCYCW}		80	-	-	ns
SCL "H" pulse width (Write)	t _{SHW}	SCL	30	-	-	
SCL "L" pulse width (Write)	t _{SLW}		30	-	-	
Data setup time (Write)	t _{SDS}	SDI	10	-	-	ns
Data hold time (Write)	t _{SDH}		10	-	-	
Serial clock cycle (Read)	t _{SCYCR}		150	-	-	ns
SCL "H" pulse width (Read)	t _{SHR}	SCL	60	-	-	
SCL "L" pulse width (Read)	t _{SLR}		60	-	-	
Access rime	t _{ACC}	SDO For maximum C _L =30pF For maximum C _L =8pF	10	-	60	ns
Output disable time	t _{OH}	SDO For maximum C _L =30pF For maximum C _L =8pF	15	-	100	ns
SCL to Chip select	t _{SCC}	NCS	30	-	-	ns
NCS "H" pulse width	t _{CHW}	NCS	60	-	-	ns
NCS-SCL time (write)	t _{CSW}	NCS	30	-	-	ns
NCS-SCL time (write)	t _{CSH}	NCS	30	-	-	ns
NCS-SCL time (Read)	t _{CSW}	NCS	60	-	-	ns
NCS-SCL time (Read)	t _{CSH}	NCS	65	-	-	ns

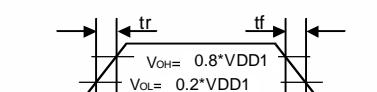
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Input Signal Slope



Output Signal Slope



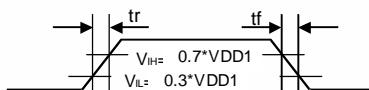
(VSSA=VSSD=0V, VDD1=1.95V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, TA = -30 to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write) SCL "H" pulse width (Write) SCL "L" pulse width (Write)	tSCYCW	SCL	80	-	-	
	tSHW		30	-	-	ns
	tSLW		30	-	-	ns
Data setup time (Write) Data hold time (Write)	tsDS	SDI	10	-	-	ns
	tsDH		10	-	-	ns
Serial clock cycle (Read) SCL "H" pulse width (Read) SCL "L" pulse width (Read)	tSCYCR	SCL	150	-	-	
	tSHR		60	-	-	ns
	tSLR		60	-	-	ns
Access rime	tACC	SDO For maximum CL=30pF For maximum CL=8pF	5	-	60	ns
Output disable time	tOH	SDO For maximum CL=30pF For maximum CL=8pF	8	-	100	ns
SCL to Chip select	tsCC	NCS	30	-	-	ns
NCS "H" pulse width	tCHW	NCS	60	-	-	ns
NCS-SCL time (write) NCS-SCL time (write)	tcSS	NCS	30	-	-	ns
	tCSH		30	-	-	ns
NCS-SCL time (Read) NCS-SCL time (Read)	tcSS	NCS	60	-	-	ns
	tCSH		65	-	-	ns

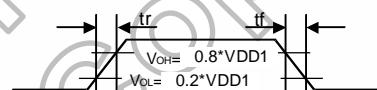
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Input Signal Slope



Output Signal Slope



8.4.2 RGB Interface Characteristics

Vertical Timings for RGB I/F

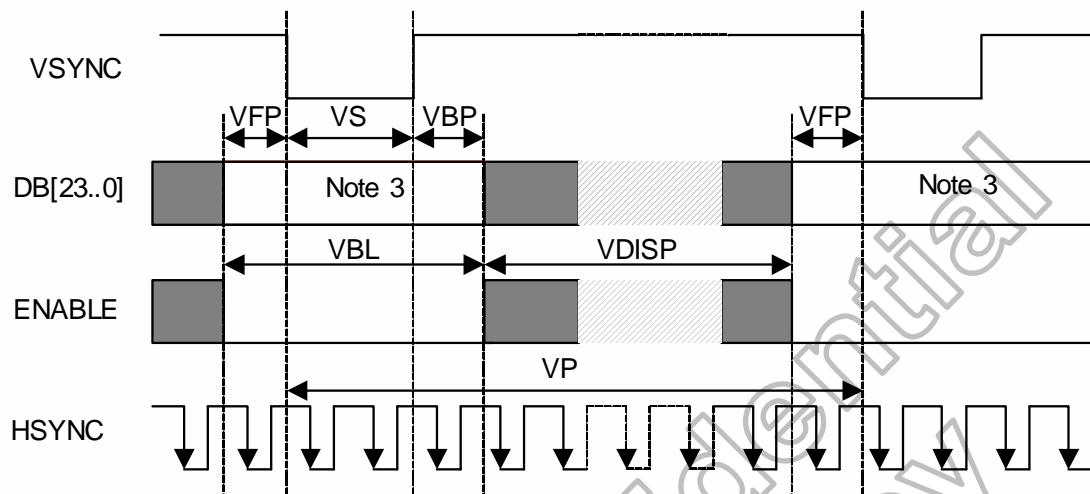


Figure 8.2: Vertical Timings for RGB I/F

(Resolution=480x854, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, $T_A = -30$ to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	860	-	864	Line
Vertical low pulse width	VS	-	2	-	4	Line
Vertical front porch	VFP	-	2	-	4	Line
Vertical back porch	VBP	-	2	-	4	Line
Vertical data start point	-	VS+VBP	4	-	8	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	10	Line
Vertical active area	-	VDISP	-	854	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by $0.30 \times \text{VDD1}$ for low state and $0.70 \times \text{VDD1}$ for high state.

(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(4) VRR must keep from 50Hz to 70Hz when adjust other items

(Resolution=480x800, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, $T_A = -30$ to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	806	-	810	Line
Vertical low pulse width	VS	-	2	-	4	Line
Vertical front porch	VFP	-	2	-	4	Line
Vertical back porch	VBP	-	2	-	4	Line
Vertical data start point	-	VS+VBP	4	-	8	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	10	Line
Vertical active area	-	VDISP	-	800	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by $0.30 \times \text{VDD1}$ for low state and $0.70 \times \text{VDD1}$ for high state.

(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(4) VRR must keep from 50Hz to 70Hz when adjust other items

Table 8.5: Vertical Timings for RGB I/F

Horizontal Timings for RGB I/F

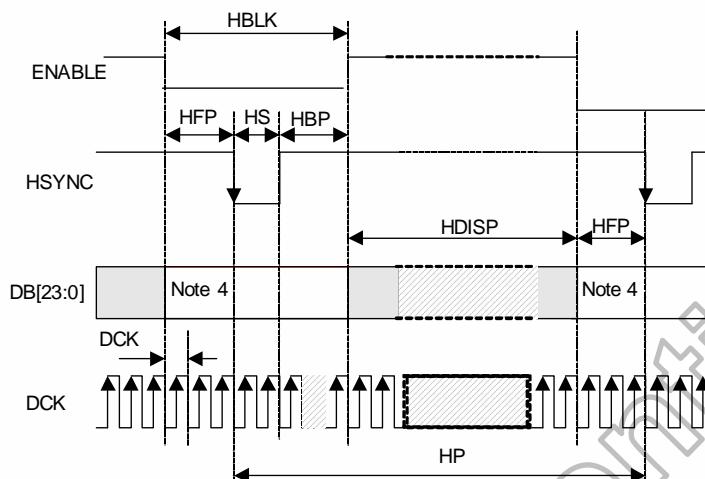


Figure 8.3: Horizontal Timing for RGB I/F

(Resolution=480x854, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, $T_A = -30$ to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note ⁽³⁾	504	-	568	DCK
HS low pulse width	HS	-	5	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal data start point	-	HS+HBP	19	-	83	DCK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCK
Horizontal active area	HDISP	-	-	480	-	DCK
Pixel clock frequency	DCK	VRR = Min. 50Hz	21.6	-	34.3	MHz
When RGB I/F is running		- Max. 70Hz	29.1	-	46.2	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by $0.30 \times \text{VDD1}$ for low state and $0.70 \times \text{VDD1}$ for high state.

(3) HP is multiples of eight DCK.

(4) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(5) VRR must keep from 50Hz to 70Hz when adjust other items.

(Resolution=480x800, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, $T_A = -30$ to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note ⁽³⁾	504	-	568	DCK
HS low pulse width	HS	-	5	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal data start point	-	HS+HBP	19	-	83	DCK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCK
Horizontal active area	HDISP	-	-	480	-	DCK
Pixel clock frequency	DCK	VRR = Min. 50Hz	20.3	-	32.2	MHz
When RGB I/F is running		- Max. 70Hz	31	-	49.2	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by $0.30 \times \text{VDD1}$ for low state and $0.70 \times \text{VDD1}$ for high state.

(3) HP is multiples of eight DCK.

(4) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(5) VRR must keep from 50Hz to 70Hz when adjust other items.

Table 8.6: Horizontal Timings for RGB I/F

General Timings for RGB I/F

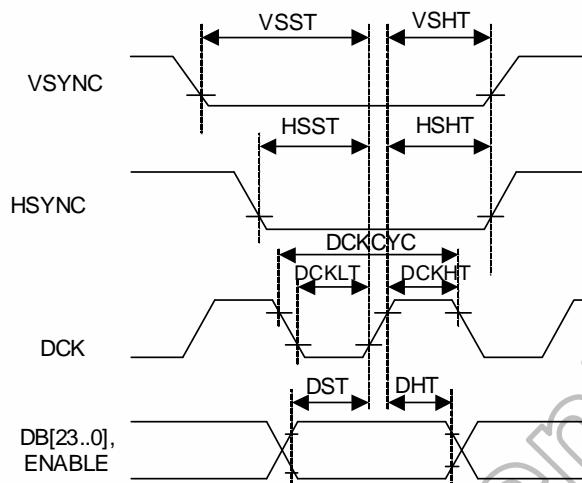


Figure 8.4: General Timings for RGB I/F

(Resolution=480x854, VSSA=VSSD=0V, VDD1=1.65V to 3.3V,
VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, TA = -30 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. Setup time	VSST	-	5	-	-	ns
Vertical sync. Hold time	VSHT	-	5	-	-	ns
Horizontal sync. Setup time	HSST	-	5	-	-	ns
Horizontal sync. Hold time	HSHT	-	5	-	-	ns
Pixel clock cycle When RGB I/F is running	DCKCYC	VRR = Min . 50 Hz Max. 70 Hz	29.1 ⁽³⁾	-	46.2 ⁽⁴⁾	ns
Pixel clock low time	DCKLT	-	5	-	-	ns
Pixel clock high time	DCKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data Hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.

(3) 34.3 MHz

(4) 21.6 MHz

(Resolution=480x800, VSSA=VSSD=0V, VDD1=1.65V to 3.3V,
VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, TA = -30 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. Setup time	VSST	-	5	-	-	ns
Vertical sync. Hold time	VSHT	-	5	-	-	ns
Horizontal sync. Setup time	HSST	-	5	-	-	ns
Horizontal sync. Hold time	HSHT	-	5	-	-	ns
Pixel clock cycle When RGB I/F is running	DCKCYC	VRR = Min . 50 Hz Max. 70 Hz	31 ⁽³⁾	-	49.2 ⁽⁴⁾	ns
Pixel clock low time	DCKLT	-	5	-	-	ns
Pixel clock high time	DCKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data Hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.

(3) 32.2MHz

(4) 20.3MHz

Table 8.7: General Timings for RGB I/F

8.4.3 The Electrical Characteristics of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 8.5 shows the complete set of electrical functions required for a fully featured PHY transceiver.

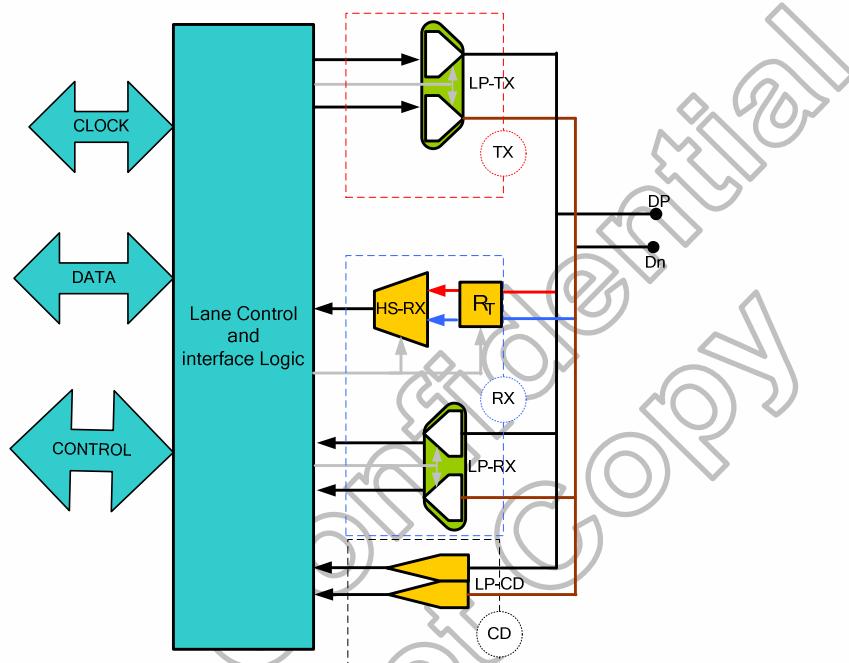


Figure 8.5: Electrical Functions of a Fully D-PHY Transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 8.6 shows both the HS and LP signal levels on the left and right sides, respectively. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

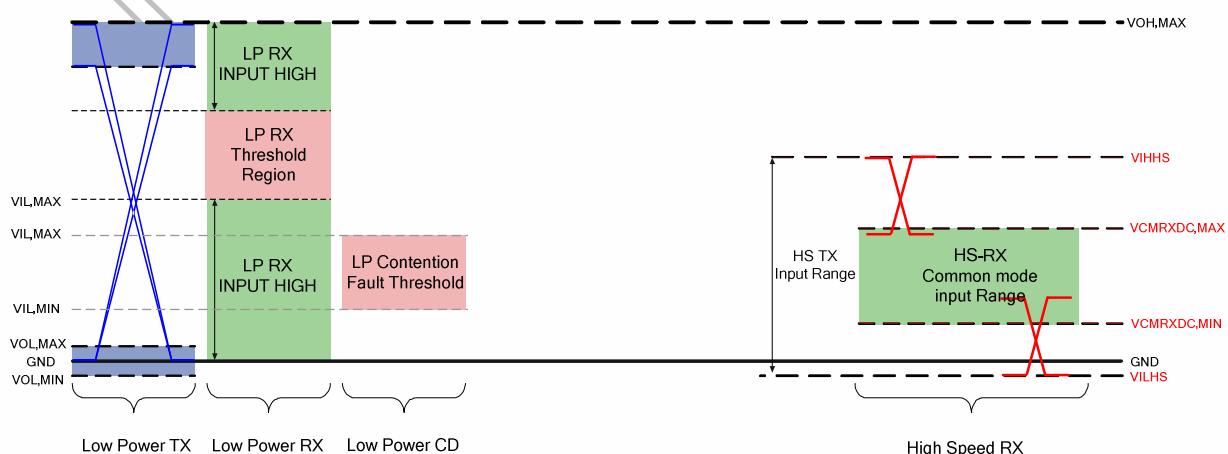


Figure 8.6: Shows both the HS and LP signal levels

The Electrical Characteristics of Low-Power Transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes. It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Description	Min.	Typ.	Max	Unit	Note
V_{OL}	Thevenin output low level	-50	-	50	mV	-
V_{OH}	Thevenin output high level	1.1	-	1.3	V	-
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	1

Note: Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 8.8: LP Transmitter DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	1, 4
$\delta V/\delta t_{SR}$	Slew rate	30	-	500	mV/ns	1, 2, 3, 4
C_{LOAD}	Load capacitance	-	-	70	pF	

Note: (1) When the output is loaded with a capacitive load CLOAD.

(2) When the output voltage is between 15% and below 85% of the fully settled LP signal levels.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage

Table 8.9: LP Transmitter AC Specifications

The Electrical Characteristics of Receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver.

Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

High-Speed Receiver

The HS receiver is a differential line receiver. It contains a switchable parallel input termination, Z_{ID} , between the positive input pin D_p and the negative input pin D_n. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IDTH}	Differential input high threshold	-	-	110	mV	1, 4
V_{IDTL}	Differential input low threshold	-110	-	-	mV	1, 4
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	2
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	2
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	2, 3
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) The summation of transmission line and bonding pad resistance is assumed to be less than 5 ohm for each input pin.

(2) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(3) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

(4) One data lane configuration

Table 8.10: HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	1
C_{CM}	Common mode termination	-	-	60	pF	2

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 8.11: HS Receiver AC Specifications

Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than e_{SPIKE} . The filter shall allow pulses wider than T_{MIN} to propagate through the LP receiver. The related diagram shows as Figure 8.7 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

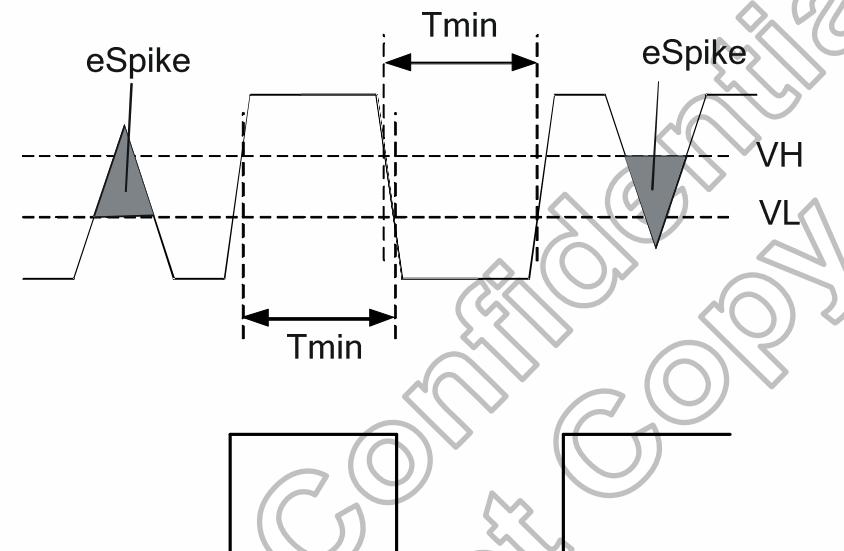


Figure 8.7: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IL}	Logic 0 input threshold	-	-	550	mV	-
V_{IH}	Logic 1 input threshold	880	-	-	mV	-

Table 8.12: LP Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

(4) An input pulse greater than this shall toggle the output.

Table 8.13: LP Receiver AC Specifications

Line Contention Detection

Contention can be inferred from any of the following conditions:

- A. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than V_{IL} .
- B. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin Voltage is greater than V_{ILF} .

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 8.14: Contention Detector DC Specifications

Input Characteristics

No structure within the PHY may be damaged when a DC signal that is within the signal voltage range V_{PIN} is applied to a pad pin for an indefinite period of time. $V_{PIN(absmax)}$ is the maximum transient output voltage at the transmitter pin. The voltage on the transmitter's output pin shall not exceed $V_{PIN(MAX)}$ for a period greater than $T_{VPIN(absmax)}$.

The ground supply voltages shifts between a Master and Slave shall be less than $V_{GND SH}$.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{PIN}	Pin signal voltage range	-50	-	1350	mV	-
$V_{GND SH}$	Ground shift	-50	-	50	mV	-
$V_{PIN(absmax)}$	Transient pin voltage level	-0.15	-	1.45	V	1
$T_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	-	-	20	ns	2

Note: (1) This value includes ground shift.

(2) The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

Table 8.15: Pin Characteristic Specifications

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.8.

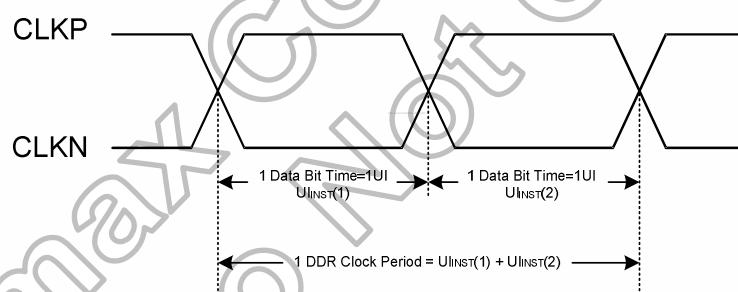


Figure 8.8: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in Table 8.15.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI _{INST}	2.5	-	12.5	ns	1, 2

Note: (1) This value corresponds to a minimum 80 Mbps data rate and one data lane configuration.

(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Table 8.16: Re verse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.9. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

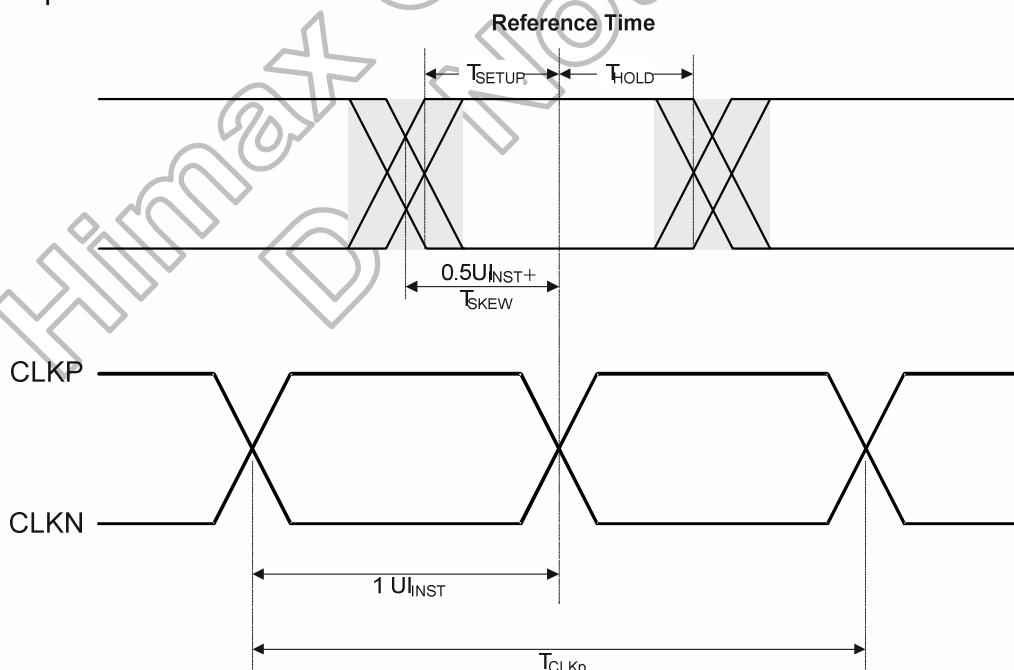


Figure 8.9: Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value UIINST, MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, TSKEW[TX], is the allowed deviation of the data launch time to the ideal $\frac{1}{2}$ UIINST displaced quadrature clock edge. The setup and hold times, TSETUP[RX] and THOLD[RX], respectively, describe the timing relationships between the data and clock signals. TSETUP[RX] is the minimum time that data shall be present before a rising or falling clock edge and THOLD[RX] is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4 \times \text{UIINST}$, i.e. $\pm 0.2 \times \text{UIINST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [receiver]	$T_{\text{SETUP}[\text{RX}]}$	0.35	-	-	UIINST	1
Clock to Data Hold Time [receiver]	$T_{\text{HOLD}[\text{RX}]}$	0.25	-	-	UIINST	1

Note: (1) One data lane condition

Table 8.17: Data to Clock Timing Specifications

8.4.4 Reset Input Timing

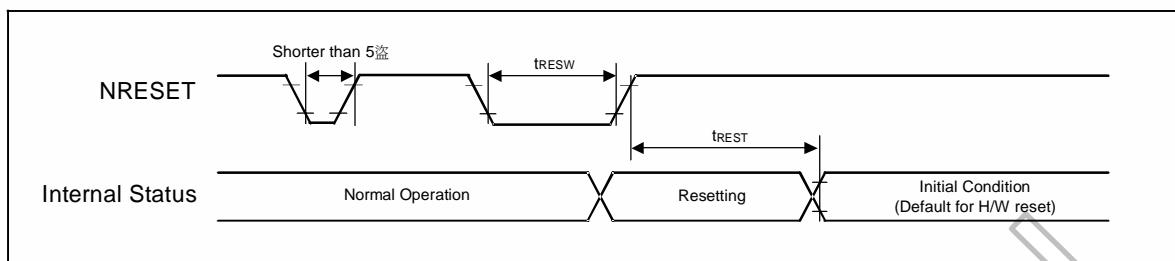


Figure 8.10: Reset Input Timing

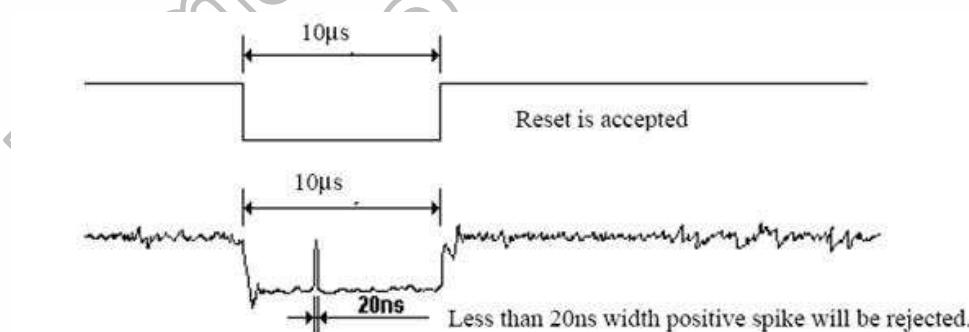
Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width ⁽¹⁾	NRESET	10	-	-	-	μs
tREST	Reset complete time ⁽²⁾	-	-	-	5	When reset is applied during Sleep In mode	ms
		-	-	-	120	When reset is applied during Sleep Out mode	ms

Table 8.18: Reset Timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
- (3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown below:



- (5) When Reset is applied during Sleep In Mode.
- (6) When Reset is applied during Sleep Out Mode.
- (7) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

8.4.5 Power On/Off Timing

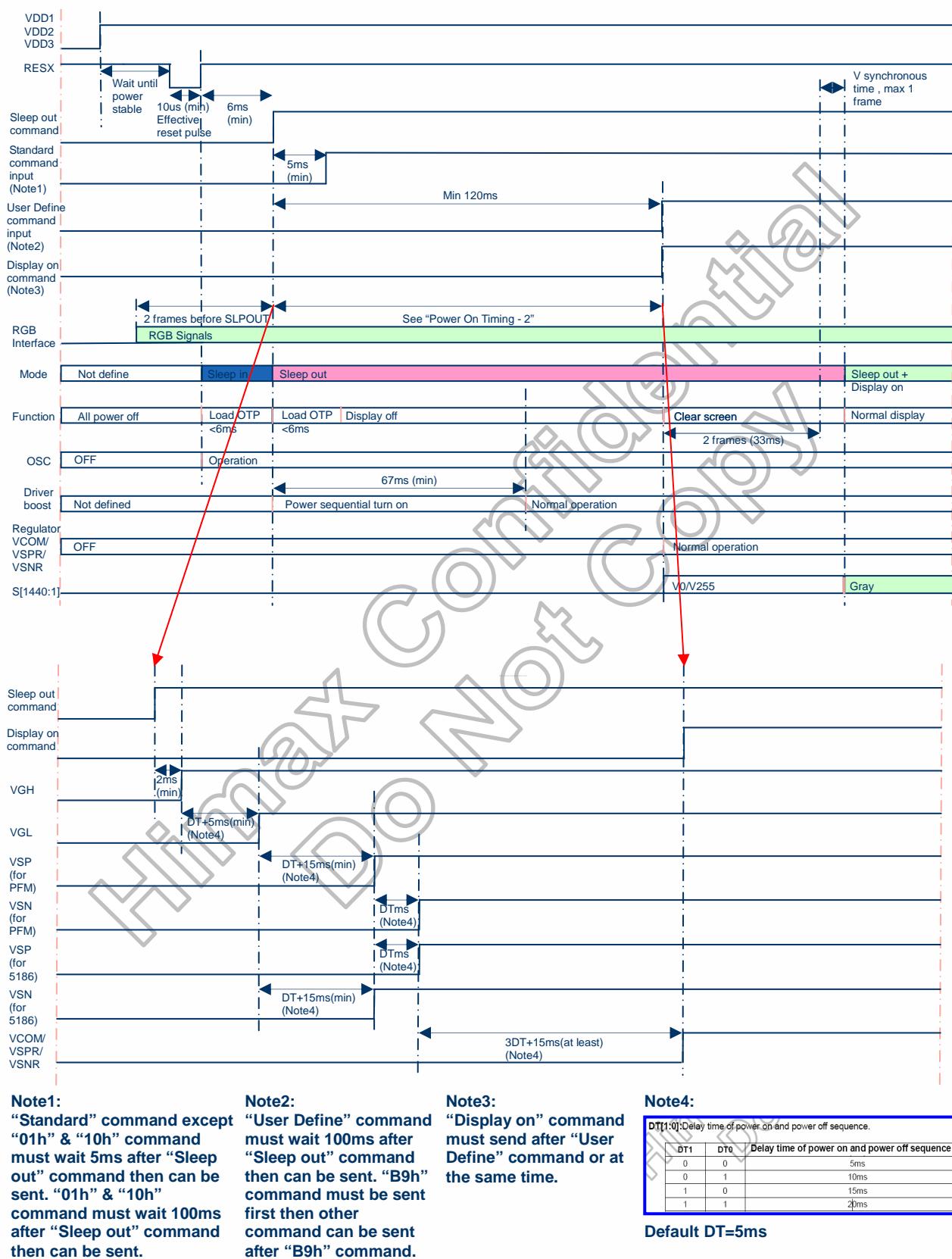


Figure 8.11: Power On Timing

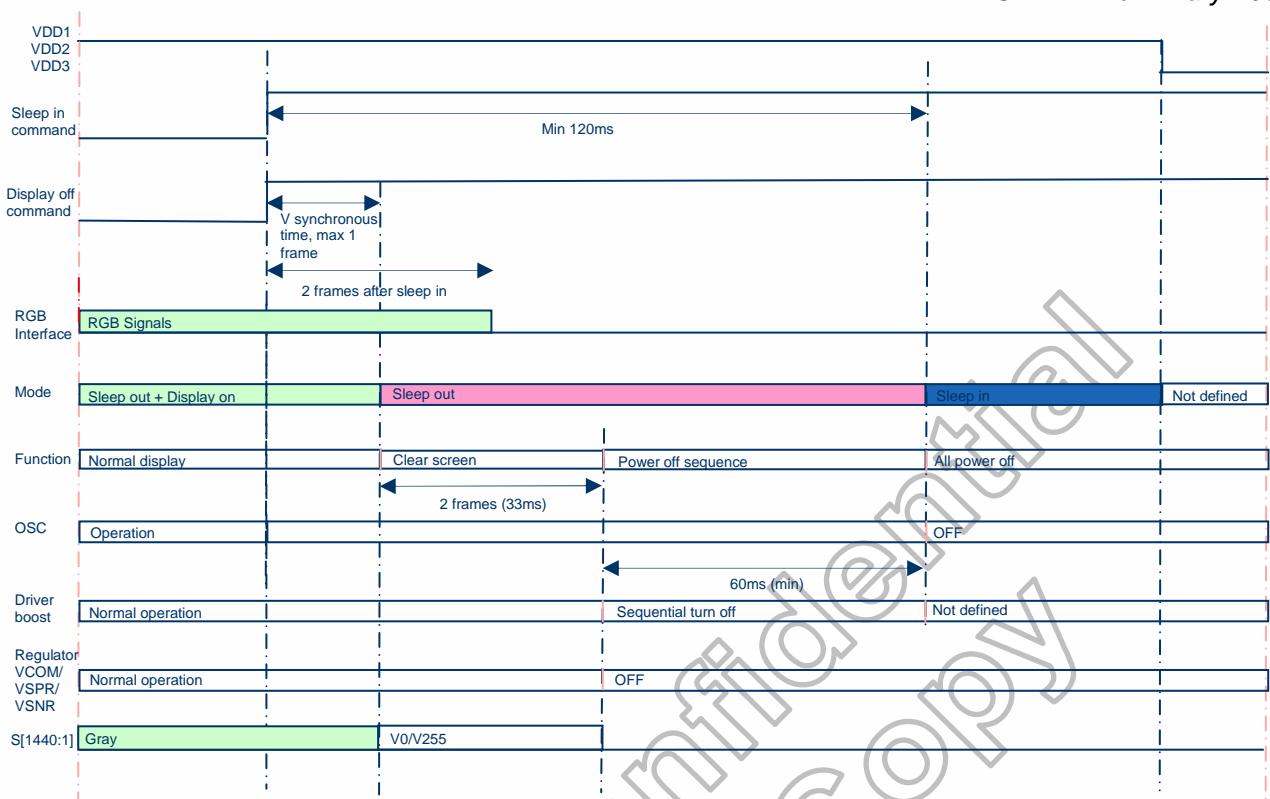


Figure 8.12: Power Off Timing

9. Layout Recommendation

9.1 Reference Layout

9.1.1 Reference Layout 1 with PFM circuit

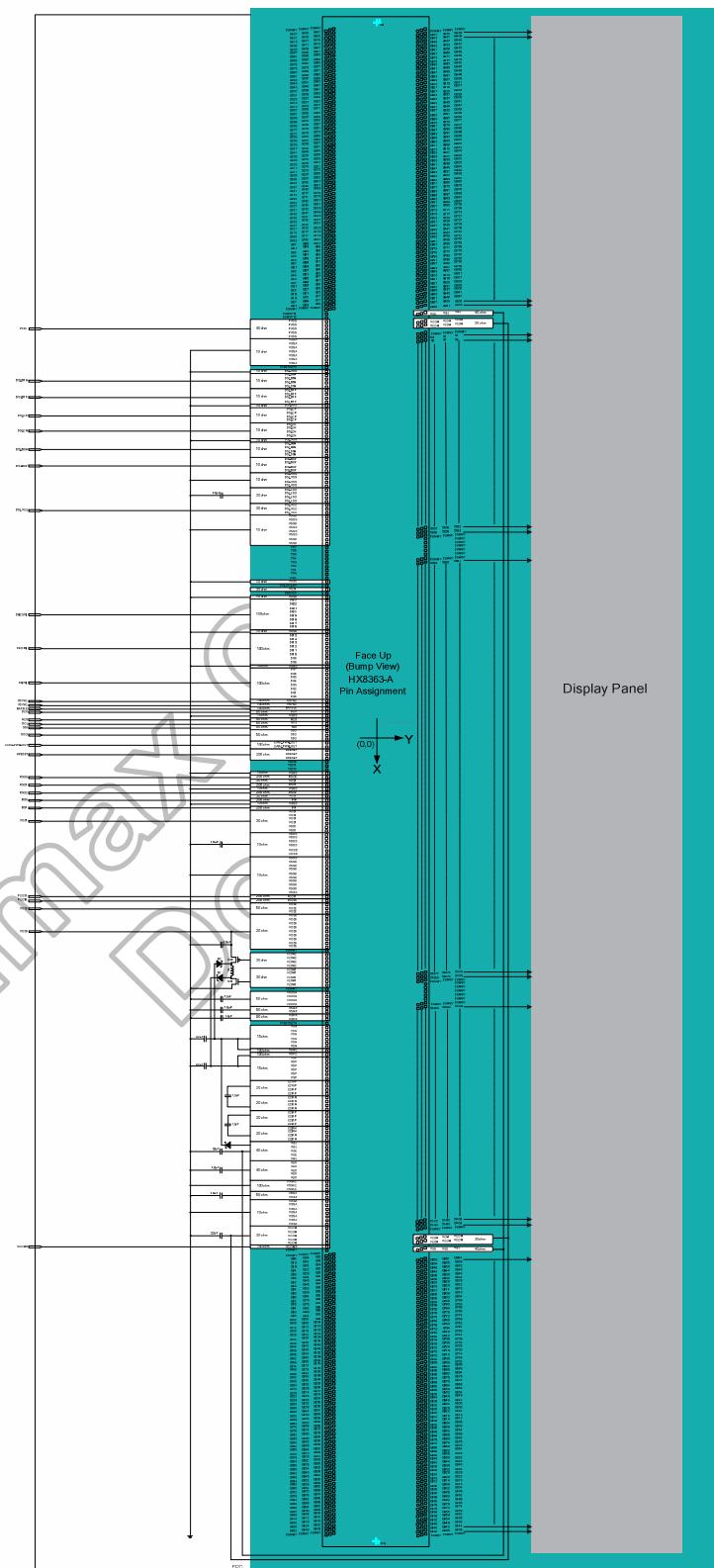


Figure 9.1: Reference layout with PFM circuit

9.1.2 Reference Layout 2 with HX5186-A

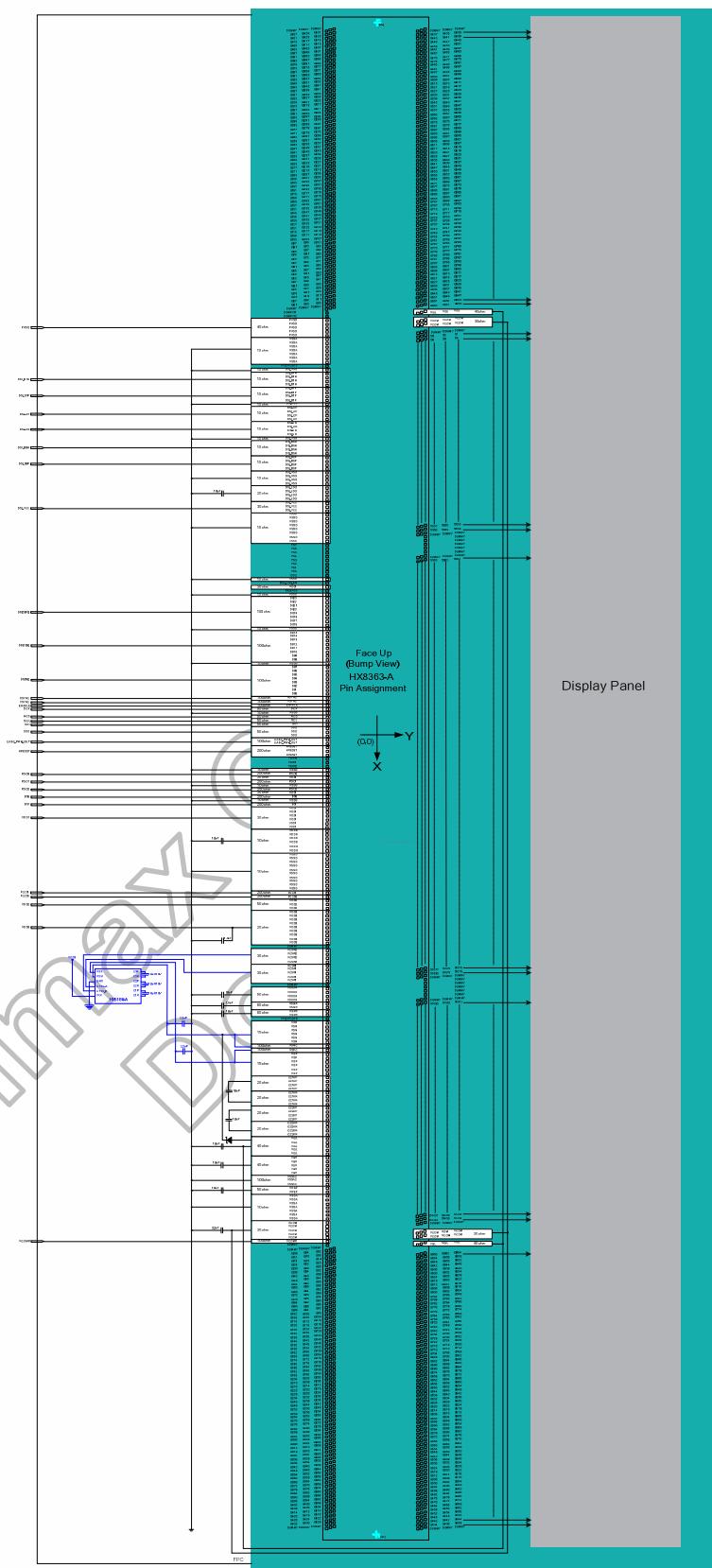


Figure 9.2: Reference layout with HX5186-A

9.2 Maximum Layout Resistance

Name	Type	Maximum Series Resistance	Unit
VDD2	Power supply	50	Ω
VDD3	Power supply	20	Ω
VDD1	Power supply	30	Ω
VSSD	Power supply	10	Ω
VSSA	Power supply	10	Ω
DSI_VCC	Power supply	30	Ω
DSI_VSS	Power supply	10	Ω
VSSAC	Power supply	100	Ω
PVSS	Input	40	Ω
RSO2-0	Input	200	Ω
PCCS0, PCCS1	Input	200	Ω
VCSW1, VCSW2	Output	30	Ω
NRESET	Input	200	Ω
DCK	Input	50	Ω
HSYNC, VSYNC, ENABLE	Input	100	Ω
NCS	Input	50	Ω
SCL, SDI	Input	50	Ω
SDO	Output	50	Ω
DB[23:0]	Output	100	Ω
CABC_PWM_OUT	Output	100	Ω
VCOM	Output	30	Ω
VCOMR	Input	100	Ω
BS0, BS1	Input	200	Ω
DSI_D0P	Input + Output	10	Ω
DSI_D0N	Input + Output	10	Ω
DSI_CP	Input	10	Ω
DSI_CN	Input	10	Ω
DSI_D1P	Input	10	Ω
DSI_D1N	Input	10	Ω
VDDD	Capacitor Connection	10	Ω
VDDDN	Capacitor Connection	50	Ω
VSP, VSN	Capacitor Connection	15	Ω
VSPC, VSNC	Capacitor Connection	100	Ω
VSPR, VSNR	Capacitor Connection	80	Ω
VREF	Capacitor Connection	50	Ω
VGH, VGL	Capacitor Connection	40	Ω
DSI_LDO	Capacitor Connection	20	Ω
C21AP,C21AN,C22AP,C22AN	Capacitor Connection	20	Ω

Table 9.1: Maximum Layout Resistance

10. OTP Programming

10.1 OTP table

		HEX	D7	D6	D5	D4	D3	D2	D1	D0	
B1	SETPOWER	0A	Valid_POWER	FS12	FS11	FS10	-	-	-	-	
		0B	-	-	-	-	BT3	BT2	BT1	BT0	
		0C	DT1	DT0	DC1	DC0	DC_DIV3	DC_DIV2	DC_DIV1	DC_DIV0	
		0D	-	DTPS2	DTPS1	DTPS0	-	DTP2	DTP1	DTP0	
		0E	-	DTNS2	DTPN1	DTNS0	-	DTN2	DTN1	DTN0	
		0F	-	-	-	BTP4	BTP3	BTP2	BTP1	BTP0	
		10	-	-	-	BTN4	BTN3	BTN2	BTN1	BTN0	
		11	VRHP7	VRHP6	VRHP5	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0	
		12	VRHN7	VRHN6	VRHN5	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0	
		13	-	-	VRMP5	VRMP4	VRMP3	VRMP2	VRMP1	VRMP0	
		14	-	-	VRMN5	VRMN4	VRMN3	VRMN2	VRMN1	VRMN0	
B3	SETRGBIF	1A	Valid_RGBIF	-	-	-	DPL (0)	HSPL (0)	VSPL (0)	EPL (1)	
B4	SETCYC	1B	Valid_CYC	-	-	-	NW[1:0] (01)	-	-	-	
		1C	-	-	-	-	SON[7:0]	-	-	-	
		1D	-	-	-	-	SOFF[7:0]	-	-	-	
		1E	-	-	-	-	EQS[7:0]	-	-	-	
		1F	-	-	-	-	EQ_ON[7:0]	-	-	-	
		20	-	-	-	-	GDON[7:0]	-	-	-	
		21	-	-	-	-	GDOFF[7:0]	-	-	-	
		22	-	-	-	-	GVSSP1[7:0]	-	-	-	
		23	-	-	-	-	GVSSP2[7:0]	-	-	-	
		26	VCMC07	VCMC06	VCMC05	VCMC04	VCMC03	VCMC02	VCMC01	VCMC00	
B6	SETVCOM (OTPx3)	27	VCMC17	VCMC16	VCMC15	VCMC14	VCMC13	VCMC12	VCMC11	VCMC10	
C1	SETDGCLUT	28	VCMC27	VCMC26	VCMC25	VCMC24	VCMC23	VCMC22	VCMC21	VCMC20	
C4	SETDDB-0	2C	Vaild_DGCLUT	-	-	-	-	-	-	DGC_EN	
		2D	-	-	-	-	DDB1[7:0](8'b0)	-	-	-	
		2E	-	-	-	-	DDB2[7:0](8'b0)	-	-	-	
		2F	-	-	-	-	DDB3[7:0](8'b0)	-	-	-	
C4	SETDDB-1	30	-	-	-	-	DDB4[7:0](8'b0)	-	-	-	
		31	-	-	-	-	DDB1[7:0](8'b0)	-	-	-	
		32	-	-	-	-	DDB2[7:0](8'b0)	-	-	-	
		33	-	-	-	-	DDB3[7:0](8'b0)	-	-	-	
C4	SETDDB-2	34	-	-	-	-	DDB4[7:0](8'b0)	-	-	-	
		35	-	-	-	-	DDB1[7:0](8'b0)	-	-	-	
		36	-	-	-	-	DDB2[7:0](8'b0)	-	-	-	
		37	-	-	-	-	DDB3[7:0](8'b0)	-	-	-	
		38	-	-	-	-	DDB4[7:0](8'b0)	-	-	-	
CC	SETPANEL	3D	Valid_PANEL	-	-	-	SM_PANEL(0)	SS_PANEL(0)	GS_PANEL(0)	REV_PANEL(1)	BGR_PANEL(0)
DA	RDID1	3E	-	-	-	-	-	-	-	-	module's manufacturer[7:0]
DB	RDID2	3F	Valid_RDID	-	-	-	-	-	-	-	LCD module/driver version [6:0]
DC	RDID3	40	-	-	-	-	-	-	-	-	LCD module/driver ID[7:0]
E0	SETGAMMAR-GC0 (OTPx1)	66	Valid_GAMMA0	-	-	-	-	-	-	-	G1_VRP0[5:0]
		67	G1_CGMP0[1:0]	-	-	-	-	-	-	-	G1_VRP1[5:0]
		68	G1_CGMP1[1:0]	-	-	-	-	-	-	-	G1_VRP2[5:0]
		69	G1_CGMP2[1:0]	-	-	-	-	-	-	-	G1_VRP3[5:0]
		6A	G1_CGMP3[1:0]	-	-	-	-	-	-	-	G1_VRP4[5:0]
		6B	G1_CGMP5	G1_CGMP4	-	-	-	-	-	-	G1_VRP5[5:0]
		6C	*	G1_PRP0[6]	-	-	-	-	-	-	G1_PKP0[4:0]
		6D	G1_PRP0[5:4]	-	-	-	-	-	-	-	G1_PKP1[4:0]
		6E	G1_PRP0[3:2]	-	-	-	-	-	-	-	G1_PKP2[4:0]
		6F	G1_PRP0[1:0]	-	-	-	-	-	-	-	G1_PKP3[4:0]
		70	-	G1_PRP1[6]	-	-	-	-	-	-	G1_PKP4[4:0]
		71	G1_PRP1[5:4]	-	-	-	-	-	-	-	G1_PKP5[4:0]
		72	G1_PRP1[3:2]	-	-	-	-	-	-	-	G1_PKP6[4:0]
		73	G1_PRP1[1:0]	-	-	-	-	-	-	-	G1_PKP7[4:0]
		74	-	-	*	-	-	-	-	-	G1_PKP8[4:0]
		75	*	*	-	-	-	-	-	-	G1_VRN0[5:0]
		76	G1_CGMN0[1:0]	-	-	-	-	-	-	-	G1_VRN1[5:0]
		77	G1_CGMN1[1:0]	-	-	-	-	-	-	-	G1_VRN2[5:0]
		78	G1_CGMN2[1:0]	-	-	-	-	-	-	-	G1_VRN3[5:0]
		79	G1_CGMN3[1:0]	-	-	-	-	-	-	-	G1_VRN4[5:0]

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July, 2011

		7A	G1_CGMN5	G1_CGMN4		G1_VRN5[5:0]
		7B	*	G1_PRN0[6]	-	G1_PKN0[4:0]
		7C	G1_PRN0[5:4]		-	G1_PKN1[4:0]
		7D	G1_PRN0[3:2]		-	G1_PKN2[4:0]
		7E	G1_PRN0[1:0]		-	G1_PKN3[4:0]
		7F		G1_PRN1[6]	-	G1_PKN4[4:0]
		80	G1_PRN1[5:4]		-	G1_PKN5[4:0]
		81	G1_PRN1[3:2]		-	G1_PKN6[4:0]
		82	G1_PRN1[1:0]		-	G1_PKN7[4:0]
		83			-	G1_PKN8[4:0]
		84	Valid_GAMMA1	-		G1_VRP0[5:0]
		85	G1_CGMP0[1:0]			G1_VRP1[5:0]
		86	G1_CGMP1[1:0]			G1_VRP2[5:0]
		87	G1_CGMP2[1:0]			G1_VRP3[5:0]
		88	G1_CGMP3[1:0]			G1_VRP4[5:0]
		89	G1_CGMP5	G1_CGMP4		G1_VRP5[5:0]
		8A	*	G1_PRP0[6]	-	G1_PKP0[4:0]
		8B	G1_PRP0[5:4]		-	G1_PKP1[4:0]
		8C	G1_PRP0[3:2]		-	G1_PKP2[4:0]
		8D	G1_PRP0[1:0]		-	G1_PKP3[4:0]
		8E	-	G1_PRP1[6]	-	G1_PKP4[4:0]
		8F	G1_PRP1[5:4]		-	G1_PKP5[4:0]
		90	G1_PRP1[3:2]		-	G1_PKP6[4:0]
		91	G1_PRP1[1:0]		-	G1_PKP7[4:0]
E0	SETGAMMAR- GC1 (OTPx2)	92			*	G1_PKP8[4:0]
		93	*	*		G1_VRN0[5:0]
		94	G1_CGMN0[1:0]			G1_VRN1[5:0]
		95	G1_CGMN1[1:0]			G1_VRN2[5:0]
		96	G1_CGMN2[1:0]			G1_VRN3[5:0]
		97	G1_CGMN3[1:0]			G1_VRN4[5:0]
		98	G1_CGMN5	G1_CGMN4		G1_VRN5[5:0]
		99	*	G1_PRN0[6]	-	G1_PKN0[4:0]
		9A	G1_PRN0[5:4]		-	G1_PKN1[4:0]
		9B	G1_PRN0[3:2]		-	G1_PKN2[4:0]
		9C	G1_PRN0[1:0]		-	G1_PKN3[4:0]
		9D	-	G1_PRN1[6]	-	G1_PKN4[4:0]
		9E	G1_PRN1[5:4]		-	G1_PKN5[4:0]
		9F	G1_PRN1[3:2]		-	G1_PKN6[4:0]
		A0	G1_PRN1[1:0]		-	G1_PKN7[4:0]
		A1			-	G1_PKN8[4:0]
E0	SETGAMMAR- GC2 (OTPx3)	A2	Valid_GAMMA2	-		G1_VRP0[5:0]
		A3	G1_CGMP0[1:0]			G1_VRP1[5:0]
		A4	G1_CGMP1[1:0]			G1_VRP2[5:0]
		A5	G1_CGMP2[1:0]			G1_VRP3[5:0]
		A6	G1_CGMP3[1:0]			G1_VRP4[5:0]
		A7	G1_CGMP5	G1_CGMP4		G1_VRP5[5:0]
		A8	*	G1_PRP0[6]	-	G1_PKP0[4:0]
		A9	G1_PRP0[5:4]		-	G1_PKP1[4:0]
		AA	G1_PRP0[3:2]		-	G1_PKP2[4:0]
		AB	G1_PRP0[1:0]		-	G1_PKP3[4:0]
		AC	-	G1_PRP1[6]	-	G1_PKP4[4:0]
		AD	G1_PRP1[5:4]		-	G1_PKP5[4:0]
		AE	G1_PRP1[3:2]		-	G1_PKP6[4:0]
		AF	G1_PRP1[1:0]		-	G1_PKP7[4:0]
		B0			*	G1_PKP8[4:0]
		B1	*	*		G1_VRN0[5:0]
		B2	G1_CGMN0[1:0]			G1_VRN1[5:0]
		B3	G1_CGMN1[1:0]			G1_VRN2[5:0]
		B4	G1_CGMN2[1:0]			G1_VRN3[5:0]
		B5	G1_CGMN3[1:0]			G1_VRN4[5:0]
		B6	G1_CGMN5	G1_CGMN4		G1_VRN5[5:0]
		B7	*	G1_PRN0[6]	-	G1_PKN0[4:0]
		B8	G1_PRN0[5:4]		-	G1_PKN1[4:0]
		B9	G1_PRN0[3:2]		-	G1_PKN2[4:0]
		BA	G1_PRN0[1:0]		-	G1_PKN3[4:0]
		BB	-	G1_PRN1[6]	-	G1_PKN4[4:0]
		BC	G1_PRN1[5:4]		-	G1_PKN5[4:0]

		BD	G1_PRN1[3:2]	-	G1_PKN6[4:0]
		BE	G1_PRN1[1:0]	-	G1_PKN7[4:0]
		BF		-	G1_PKN8[4:0]
	SETGAMMAR- GC3 (OTPx4) E0	C0	Valid_GAMMA3	-	G1_VRP0[5:0]
		C1	G1_CGMP0[1:0]	-	G1_VRP1[5:0]
		C2	G1_CGMP1[1:0]	-	G1_VRP2[5:0]
		C3	G1_CGMP2[1:0]	-	G1_VRP3[5:0]
		C4	G1_CGMP3[1:0]	-	G1_VRP4[5:0]
		C5	G1_CGMP5	G1_CGMP4	G1_VRP5[5:0]
		C6	*	G1_PRP0[6]	G1_PKP0[4:0]
		C7	G1_PRP0[5:4]	-	G1_PKP1[4:0]
		C8	G1_PRP0[3:2]	-	G1_PKP2[4:0]
		C9	G1_PRP0[1:0]	-	G1_PKP3[4:0]
		CA	-	G1_PRP1[6]	G1_PKP4[4:0]
		CB	G1_PRP1[5:4]	-	G1_PKP5[4:0]
		CC	G1_PRP1[3:2]	-	G1_PKP6[4:0]
		CD	G1_PRP1[1:0]	-	G1_PKP7[4:0]
		CE		*	G1_PKP8[4:0]
		CF	*	*	G1_VRN0[5:0]
		D0	G1_CGMN0[1:0]	-	G1_VRN1[5:0]
		D1	G1_CGMN1[1:0]	-	G1_VRN2[5:0]
		D2	G1_CGMN2[1:0]	-	G1_VRN3[5:0]
		D3	G1_CGMN3[1:0]	-	G1_VRN4[5:0]
		D4	G1_CGMN5	G1_CGMN4	G1_VRN5[5:0]
		D5	*	G1_PRN0[6]	G1_PKN0[4:0]
		D6	G1_PRN0[5:4]	-	G1_PKN1[4:0]
		D7	G1_PRN0[3:2]	-	G1_PKN2[4:0]
		D8	G1_PRN0[1:0]	-	G1_PKN3[4:0]
		D9		G1_PRN1[6]	G1_PKN4[4:0]
		DA	G1_PRN1[5:4]	-	G1_PKN5[4:0]
		DB	G1_PRN1[3:2]	-	G1_PKN6[4:0]
		DC	G1_PRN1[1:0]	-	G1_PKN7[4:0]
		DD		-	G1_PKN8[4:0]

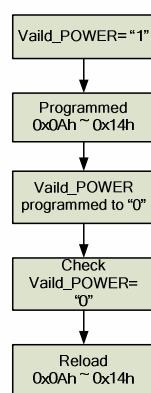
Table 10.1: OTP table

Note: (1) The default value of OTP memory bits are all "1".

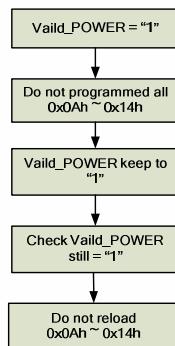
(2) VALID_xxx bit decide the OPT reload Enable/Disable, the default value is "1". If the own OTP area of VALID_xxx bit had been programmed, the VALID_xxx bit will be changed to "0" automatically and execute the OTP reload.

For example:

Condition 1: Programmed all index of 0x0Ah ~ 0x14h and Valid_POWER bit



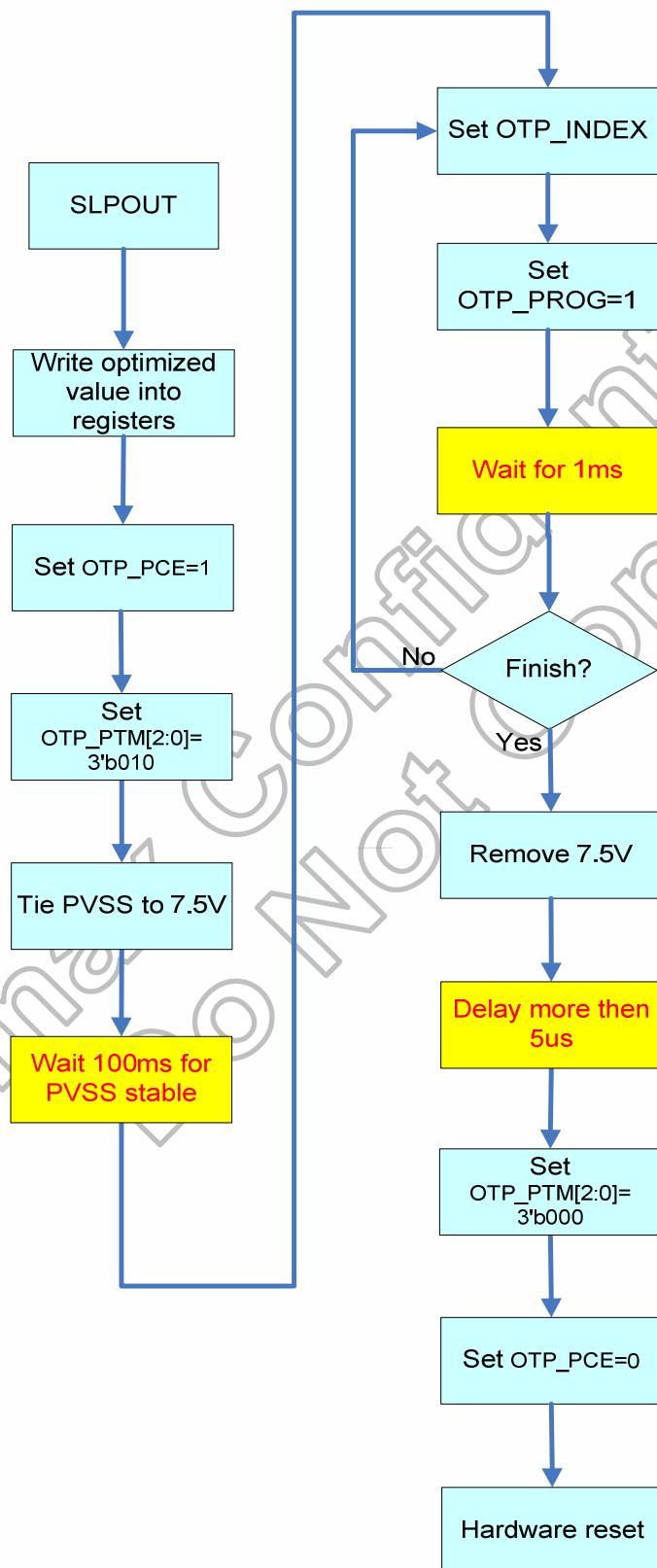
Condition 2: Do not program all index of 0x0Ah ~ 0x14h and Valid_POWER bit



(3) There are some conditions that HX8363-A can reload OTP.

- a. Hardware reset
- b. Software reset
- c. SLPOUT command

10.2 OTP programming flow



Note: The input voltage (7.5V) should be removed from PVSS after OTP programming finished.

Figure 10.1: OTP Programming Sequence

10.3 Programming sequence

Step	Operation		
1	Power on and reset the module then SLPOUT		
2	Write optimized value to related register		
	Command	Register	Description
	SETPOWER	B1h	Set power related setting
	SETRGBIF	B3h	Set RGB interface related register
	SETCYC	B4h	Set Display Waveform Cycle
	SETVCOM	B6h	Set VCOM Voltage
	SETDGLUT	C1h (DGC_EN)	Set DGC LUT
	SETDDB	C4h	Set DDB
	SETPANEL	CCh (SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL, GBR_PANEL)	Set panel related register
	SETID	C3h	SET ID
	SETGAMMA	E0h	Set Gamma Curve Related Setting
3	Set OTP_PCE=1		
4	Set OTP_PTM[2:0]=3'b010		
5	Connect external power 7.5V to PVSS pin		
6	Wait 100ms for PVSS stable		
7	Specify OTP_index (Note 1, 3)		
	OTP_index (Write – For Program)	OTP_index (Read – For get OTP value)	Parameter
	0Ah ~ 14h	0Ah ~ 14h	SETPOWER value
	1Ah	1Ah	DPL, HSPL, VSPL, EPL
	1Bh ~ 25h	1Bh ~ 25h	SETCYC value
	26h	26h	VCMC0[7:0]
	26h	27h	VCMC1[7:0]
	26h	28h	VCMC2[7:0]
	2Ch	2Ch	DGC_EN
	2Dh ~ 30h	2Dh ~ 30h	DDB1~4[7:0]
	2Dh ~ 30h	31h ~ 34h	DDB1~4[7:0]
	2Dh ~ 30h	35h ~ 38h	DDB1~4[7:0]
	3Dh	3Dh	SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL, GBR_PANEL
	3Eh	3Eh	module's manufacturer[7:0]
	3Fh	3Fh	LCD module/driver version [6:0]
	40h	40h	LCD module/driver ID[7:0]
	66h ~ DDh	66h ~ DDh	SETGAMMAR value
8	Set OTP_Mask=0x00h, programming the entire bit of one parameter.		
9	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.		
10	Wait 1 ms (Note 2, 4)		
11	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (7). Otherwise, remove the external power from PVSS pin.		
12	Wait more then 5μs		
13	Set OTP_PTM[2:0]=3'b000		
14	Set OTP_PCE=0		
15	Hardware reset		

- Note:**
- (1) When do the OTP program on gamma setting (GC0: 66h~83h, GC1: 84h~A1h, GC2: A2h~BFh, GC3: C0h~DDh), user just specify the 66h, the all settings of GC0 will be programmed. Similarly the same condition is also on programming GC1, GC2 and GC3. (GC1: 84h, GC2: A2h, GC3: C0h).
 - (2) When do the OTP program on gamma setting, it must wait 6ms delay time after setting OTP_PROG=1.
 - (3) When do the OTP program on DDB setting (SETDDB-0: 2Dh~30h, SETDDB-1: 31h~34h, SETDDB-2: 35h~38h), user just specify the 2Dh, the all settings of DDB will be programmed to SETDDB-0, SETDDB-1 and SETDDB-2 automatically.
 - (4) When do the OTP program on DDB setting, it must wait 2ms delay time after setting OTP_PROG=1.

10.4 OTP Programming Circuitry

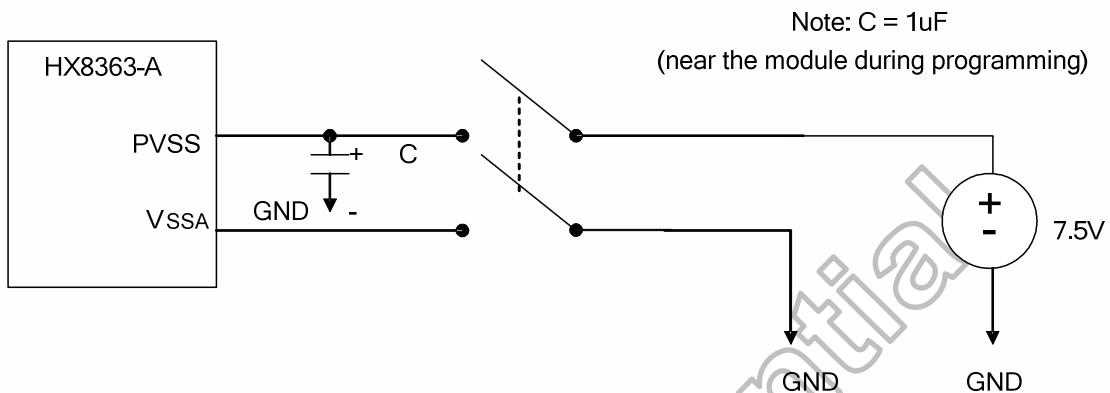


Figure 10.2: OTP Programming Circuitry

11. Ordering Information

Part No.	Package
HX8363-A000 <u>PDxxx</u>	PD: mean COG xxx: mean chip thickness (μm), (default: 250 μm)

12. Revision History

Version	Date	Description of Changes
01	2008/10/15	New setup
	2008/10/21	<p>1. Modify (Add) the description of 2. Features (page 9)</p> <p>2. Modify some typing error on 3.2 Pin Description (page 11)</p> <p>Modify the typing error on the page16 and page 17.</p> <p>4. Delete the word "GRAM" and modify the Figure 5.2: Idle Mode Grayscale Control (page 27)</p> <p>5. Delete the word "GRAM" and modify the Figure 5.3: Grayscale Control (page 29)</p> <p>6. Modify the "standby off" to "SLPOUT" on Figure 5.14: OTP Programming Sequence (page 80)</p> <p>7. Modify the typing error on Figure 5.16: Case 1 – NRESET line is held High or Unstable by Host at Power On (page 83)</p> <p>8. Delete the DSTB of command SETPOWER (B2h) (page 93 and page 142)</p> <p>9. Modify the bit "STB" to "SLP" on command SETPOWER (B2h) (page 93, page 142 and page149)</p> <p>10. Delete the word "partial mode" (page 99 ~ page 178)</p> <p>11. Modify the flow chart of command Read Display Identification Information (04h) (page 100)</p> <p>12. Modify the flow chart of command Read Red Color (06h) (page 101)</p> <p>13. Modify the flow chart of command Read Green Color (06h) (page 102)</p> <p>14. Modify the flow chart of command Read Blue Color (06h) (page 103)</p> <p>15. Modify the description of Read Display Status (09h) (page 104)</p> <p>16. Modify the flow chart of Read Display Status (09h) (page 107)</p> <p>17. Modify the description of Read Display Power Mode (0Ah) (page 108)</p> <p>18. Modify the flow chart of Read Display Power Mode (0Ah) (page 109)</p> <p>19. Modify the description of Read Display MADCTL (0Bh)(page 110)</p> <p>20. Modify the flow chart of Read Display MADCTL (0Bh)(page 111)</p> <p>21. Modify the flow chart of Read Display Pixel Format (0Ch)(page 113)</p> <p>22. Modify the flow chart of Read Display Image Mode (0Dh) (page 115)</p> <p>23. Delete the command Read Display Signal Mode (0Eh) (page116)</p>

	24. Modify the flow chart of Read Display Self-Diagnostic Result (0Fh)(page 117) 25. Modify the flow chart of Sleep In (10h)(page 118) 26. Modify the flow chart of Sleep Out (11h) (page 119) 27. Modify the description of Memory Access Control (36h)(page 125) 28. Delete the CSEL_NOR[2:0] on command Interface Pixel Format (3Ah) (page 91 and page 128) 29. Modify the description and flow chart on command Write CTRL Display (53h) (page 131 and page 132) 30. Modify the description and flow chart on command Read CTRL Value Display (54h) (page 133) 31. Modify the flow chart of Read Content Adaptive Brightness Control (56h) (page 135) 32. Modify the flow chart of Read CABC minimum brightness (5Fh) (page 137) 33. Modify the flow chart of Read ID1 (DAh) (page 138) 34. Modify the flow chart of Read ID2 (DBh) (page 139) 35. Modify the flow chart of Read ID3 (DCh) (page 140) 36. Modify the setting of VRHP[7:0] , VRHN[7:0], VRMP[5:0] and VRMN[5:0] on command SETPOWER (B1h) (page 147 ~ page 152) 37. Modify the description of command SETDISP (B2h) (page 153) 38. Modify the description and add SON[7:0], EQS[7:0], GDON[7:0], GDOF[7:0], GDT[7:0] on command SETCYC (B4h) (page 93, page156 ~ page 160) 39. Modify the typing error of description on command SETPANEL (CCh) (page 174) 40. Modify the Table 7.2: Adoptability of Capacitor (page 180) 41. Modify the Table 8.1: Absolute Maximum Rating (page 181) 42. Modify the Table 8.4: Power consumptions (delete partial mode) (page 183)
2008/10/24	1. Modify the description of 5.3 Gamma Characteristic Correction Function(page28 ~ page 31) 2. Modify the description of 5.11 Power On/Off Sequence(page82) 3. Delete the command Read display signal mode(0Eh)(page 90) 4. Modify the description of the command Software Reset(01h) (page 98) 5. Modify the flow chart of Read Blue Color (08h) (page 102) 6. Modify the description of the command Read Display Status (09h) (page 103) 7. Modify the description of the command Read Display Power Mode (0Ah) (page 107) 8. Modify the description of the command Read Display MADCTL (0Bh) (page 109) 9. Modify the description of the command Read Display Image Mode (0Dh) (page 113) 10. Modify the description of the command Sleep In (10h) (page 116)

	<ul style="list-style-type: none"> 11. Modify the description of the command Display Off (28h) (page 121) 12. Modify the description of the command Display On (29h) (page 122) 13. Modify the description of the command Idle Mode On (39h) (page 125) 14. Modify the description of the command Set Display Waveform Cycle (B4h) (page 157) 15. Modify the description of the command Set OTP (BBh) (page 94 and page 163) 16. Add the DGC_EN of command Set DGC LUT (C1h) (page 94 and page 164) 17. Modify the description of the command Set CABC Control (C9h) (page 94 and page 167) 18. Modify the description of the command SETPANEL (CCh) (page 172 and page 173)
2008/11/07	<ul style="list-style-type: none"> 1. Modify the description of 1 General Description (page 8) 2. Delete the description of Idle Mode On (page9) 3. Modify the description of 2.3 Display/Control Interface (page 10) 4. Modify the Block Diagram of 3 Device Overview (page 11) 5. Add BS0 ~ BS1, REGVDD, DSI_LDO_EN, DSI_LDO, DSI_D0P, DSI_D0N, DSI_CP, DSI_CN, DSI_D1P, DSI_D1N, DSI_VCC, DSI_VSS of 3.2 Pin Description (page12 ~ page 14) 6. Modify the description of VDDD (page 13) 7. Modify the description of 4.1 System Interface (page 18) 8. Add 4.3 DSI Protocol (page28 ~ page 39) 9. Delete 5.2 Idle Display (page41) 10. Modify Table 5.40: Voltage Calculation Formula of 256-Grayscale Voltage (Positive/Negative Polarity) (page82 ~ page 84) 11. Modify Figure 5.8: LCD Power Generation Scheme (page 88) 12. Modify the description of 5.7 DC/DC Converter Circuit (page 89 and page 90) 13. Modify Figure5.13: OTP Programming Sequence (page 94) 14. Delete the command Read Display Identification Information (04h) (page 104 and page 113) 15. Add the command Read number of the parity errors (05h) (page 104 and page 114) 16. Delete the command Read Red Color (06h) (page 104 and page 115) 17. Delete the command Read Green Color (07h) (page 104 and page 116) 18. Delete the command Read Blue Color (08h) (page 104 and page 117) 19. Modify the description of the command Read Display Status (09h) (page 118 and page 119) 20. Modify the description of the command Read Display

	<ul style="list-style-type: none"> 21. Power Mode (0Ah) (page 122) 22. Modify the description of the command Read Display MADCTL(0Bh) (page 124) 23. Add the command Read Display Signal Mode (0Eh) (page 104 and page 130 ~ page 131) 24. Modify the description of the command Memory Access Control (36h) (page 140) 25. Delete the command Idle Mode Off (38h) (page 105 and page 142) 26. Delete the command Idle Mode On (39h) (page 105 and page 143) 27. Add the command Read DDB start (A1h) (page 105 and page 145 ~ page 146) 28. Add the command Read_DDB_continue (A8h) (page 105 and page 147) 29. Modify the description of the command Set Power (B1h) (page 167 and page 168) 30. Modify the command Set Display Waveform Cycle (B4h) (page 107 and page 174) 31. Modify the description of the command Set VCOM Voltage (B6h) (page 180 and page 182) 32. Modify the description of the command Set ID(C4h) (page 108 and page 187) 33. Delete the description "Idle Mode On" and "Idle Mode Off" from "Register Availability" (page 120 ~ page 198) 34. Modify the description of 7. Power supply (page 199 and page 200) 35. Modify Table7.1: Power Supply Voltage Configuration (page 201) 36. Modify Table7.2: Adoptability of Capacitor (page 201) 37. Modify Table 8.1: Absolute Maximum Rating (page 202) 38. Modify Table 8.4: Power consumptions (page 204) 39. Modify Table 9.1: Maximum Layout Resistance (page 211)
2008/11/10	<ul style="list-style-type: none"> 1. Modify the description of 3 Gamma macro adjustment registers (page 44) 2. Modify Figure 5.4: Gamma Resister Stream and Gamma Reference Voltage (page 45) 3. Modify Table 5.39: Voltage Calculation Formula of 64-Grayscale Voltage (Negative Polarity) (page 80)
2008/11/14	<ul style="list-style-type: none"> 1. Modify the description of S1~S1440 for 3.2 Pin Description (page 13) 2. Modify the description of VDDD for 3.2 Pin Description (page 13) 3. Modify 6.1.1 Standard Command for RDNUMPE (05h) (page 102) 4. Modify 6.1.1 Standard Command for MADCTL (36h) (page 103) 5. Modify the description of the command Set Display Waveform Cycle (B4h) (page 105 and page 165) 6. Modify Table7.1: Power Supply Voltage Configuration (page 191)

	2008/11/24	<ol style="list-style-type: none"> 1. Modify the description of 3.1 Block Diagram (page 11) 2. Modify the description of 3.2 Pin Description (page 13 and page 14) 3. Modify the Figure 4.3: 3 wire Serial Interface protocol, read mode (page 21) 4. Modify the Table 5.38: Voltage Calculation Formula of 64-Grayscale Voltage (Positive Polarity) (page 78) 5. Modify the Table 5.39: Voltage Calculation Formula of 64-Grayscale Voltage (Negative Polarity) (page 80) 6. Modify the Figure 5.8: DC/DC Converter Circuit (PFM) (page 87) 7. Modify the Figure 5.9: DC/DC Converter Circuit (HX5182-A) (page 88) 8. Modify the description of 5.10 Power On/Off Sequence (page 94) 9. Modify the command Read number of the parity errors (05h) (page 111) 10. Add the command Read Red Color (06h) (page 102 and page 112) 11. Add the command Read Green Color (07h) (page 102 and page 113) 12. Add the command Read Blue Color (08h) (page 102 and page 114) 13. Modify the command Read Display Pixel Format (0Ch) (page 122) 14. Modify the command Read Display Image Mode (0Dh) (page 124) 15. Modify the command Memory Access Control (36h) (page 103, page 136 and page 137) 16. Modify the command Read DDB start (A1h) (page 139) 17. Modify the command Set Internal Oscillator (B0h) (page 105 and page 154) 18. Modify the command Set Power (B1h) (page 105, page 155, page 156, page 164 and page 165) 19. Modify the command Set Display Related Register (B2h) (page 105, page 166 and page 167) 20. Modify the command Set Display Waveform Cycle (B4h) (page 105, page 169 ~ 171 and page 173) 21. Modify the command Set VCOM Voltage (B6h) (page 177) 22. Modify the Figure 7.1: Power supply with PFM circuit (page 194) 23. Modify the Figure 7.2: Power supply with HX5182-A (page 195) 24. Modify the Table 7.1: Power Supply Voltage Configuration (page 196) 25. Modify the Table 7.2: Adoptability of Component (page 196) 26. Modify the Table 9.1: Maximum Layout Resistance (page 206)
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	2008/11/28	<ol style="list-style-type: none"> 1. Add PCCS1 and PCCS0 of 3.2 Pin Description (page13) 2. Modify the command Read Display Signal Mode (0Eh) (page 126) 3. Modify the command Read_DDB_start (A1h) (page 103 and page 139) 4. Modify the command Read_DDB_continue (A8h) (page 103 and page 141) 5. Add the command SET SPI READ INDEX (FEh) (page 106 and page 191) 6. Add the command SET SPI READ INDEX (FEh) (page 106 and page 192) 7. Remove the dummy read parameter from all Standard Command and User Define Command (page 102, page 103, page 104, page 115, page 118, page 120, page 122, page 124, page 126, page 128, page 139, page 141, page 143, page 146, page 148, page 150, page 151, page 152 and page 153)
	2008/12/01	<ol style="list-style-type: none"> 1. Add the command Idle Mode Off (38h) (page 104 and page 139) 2. Add the command Idle Mode On (39h) (page 104 and page 140) 3. Modify the command Set Display Waveform Cycle (B4h) (page 106 and page 172 ~ page 178) 4. Add the description relate to Idle Mode (page 9, page 41, page 104, page 116, page 117, page 118, page 119, page 121, page 123, page 125, page 127, page 129, page 132, page 133, page 134, page 135, page 136, page 137, page 139, page 140, page 141, page 142, page 144, page 154, page 155, page 156, page 157, page 168, page 170, page 171, page 178, page 182, page 183, page 184, page 185, page 187, page 189, page 192, page 194, page 196, page 197, page 198, page 200 and page 206)
	2008/12/02	<ol style="list-style-type: none"> 1. Add 3.3 Pin Assignment (page 15) 2. Add 3.4 PAD Coordinate (page 16 ~ page 27) 3. Modify the command Set Power (B1h) (page 117, page 169 and page 170) 4. Add Figure 9.1: Layout Recommendation (page 223) 5. Modify Table 9.1: Maximum Layout Resistance (page 224)
	2008/12/04	<ol style="list-style-type: none"> 1. Modify 3.3 Pin Assignment (page 15) 2. Modify the command SETPANEL (CCh) (page 118, page 205 and page 206) 3. Modify Figure 9.1: Layout Recommendation (page 223)

	2008/12/05	<ol style="list-style-type: none"> 1. Modify 3.4 PAD Coordinate (page 27) 2. Delete the command Idle Mode Off (38h) (page 115 and page 150) 3. Delete the command Idle Mode On (39h) (page 115 and page 151) 4. Modify the command Set Display Waveform Cycle (B4h) (page 117 and page 183) 5. Delete the description relate to Idle Mode (page 9, page 52, page 115, page 127, page 128, page 129, page 130, page 132, page 134, page 136, page 138, page 140, page 143, page 144, page 145, page 146, page 147, page 148, page 150, page 151, page 152, page 153, page 155, page 165, page 166, page 167, page 168, page 179, page 181, page 182, page 189, page 193, page 194, page 195, page 196, page 198, page 200, page 203, page 206, page 207, page 208, page 209, page 211 and page 217) 6. Modify 11 Ordering Information (page 226)
	2008/12/08	<ol style="list-style-type: none"> 1. Add the command Set BGP Voltage (B5h) (page 115 and page 188) 2. Add the command Set MIPI (BAh) (page 116 and page 193) 3. Add the command Set Internal Digital Voltage (BCh) (page 116 and page 195) 4. Add the command Logic debug (BEh) (page 116 and page 196) 5. Add the command Set Power Option (BFh) (page 116 and page 197) 6. Add the command Set Source Option (C0h) (page 116 and page 198)
	2008/12/09	<ol style="list-style-type: none"> 1. Add the command Set CPCRC (B8h) (page 115 and page 192) 2. Add the command SETROM (C5h) (page 116 and page 203) 3. Add the command SETECO (C6h) (page 116 and page 204)
02	2008/12/30	<ol style="list-style-type: none"> 1. Modify the description for Read Display Power Mode (0Ah) (page 120) 2. Modify the description for Read Display MADCTL (0Bh) (page 122) 3. Modify the description for Read Display Pixel Format (0Ch) (page 124) 4. Modify the description for Interface Pixel Format (3Ah) (page 139)

	2009/01/23	<ol style="list-style-type: none"> 1. Modify the description for 3.2 Pin Description (page 12) 2. Modify the description for 3.4.1 Bump Arrangement (page 27 and page 28) 3. Modify the description for 6.2.40 Set DGC LUT (C1h) (page 180) 4. Modify the description for 6.2.43 SETPANEL (CCh) (page 184 and page 185) 5. Modify the description for Set Gamma Curve Related Setting (E0h) (page 188) 6. Modify the Figure 7.1: Power supply with PFM circuit (page 190) 7. Modify the Figure 7.2: Power supply with HX5186-A (page 191) 8. Modify the description for 10.1 OTP table (page 203) 9. Modify the description for Figure10.1: OTP Programming Sequence (page 208)
	2009/02/04	<ol style="list-style-type: none"> 1. Modify the Figure 5.8: DC/DC Converter Circuit (PFM) (page 98) 2. Modify the description for 6.2.60 SETPANEL (CCh) (page 185) 3. Modify the Figure 7.1: Power supply with PFM circuit (page 190) 4. Modify the Table 7.2: Adoptability of Component (page 192) 5. Modify the Figure 9.1: Layout Recommendation (page 201) 6. Change the "REGVDD" pin to "DUMMY" pin (page 12, page 15, page 17, page 201, page 202)
	2009/02/10	<ol style="list-style-type: none"> 1. Modify the description for 6.2.34 Set Power (B1h) (page 156 ~ page 160) 2. Modify the description for 8.4 AC Characteristics (page 197 ~ page 202)
	2009/02/12	<ol style="list-style-type: none"> 1. Modify the Table 8.6: Horizontal Timings for RGB I/F (page 199 ~ page 200)
	2009/03/05	<ol style="list-style-type: none"> 1. Modify the description for 2.2 Display Module (page 9) 2. Modify the description for 3.2 Pin Description (page 13, page 14) 3. Modify the alignment mark type (page 15, page 204) 4. Modify the description for 3.4.1 Bump Arrangement (page 27, page 28) 5. Modify the description for 6.1.2 User Define Command List Table (page 113) 6. Modify the description for 6.2.34 Set Power (B1h) (page 157 ~ page 159)
	2009/05/08	<ol style="list-style-type: none"> 1. Modify the Figure 4.6: 16 bit/pixel Color Order on the RGB I/F (page 35) 2. Modify the Figure 4.7: 18 bit/pixel Color Order on the RGB I/F (page 36) 3. Modify the description for 6.2.38 Set Power (B1h) (page 157) 4. Modify the description for 6.2.43 SETPANEL (CCh) (page 185)

	2009/06/12	<ol style="list-style-type: none"> 1. Modify the description for 6.2.12 Sleep In (10h) (page 131) 2. Modify the description for 6.2.13 Sleep Out (11h) (page 132) 3. Modify the chapter for 8.3 DC characteristics (page 195, page 196)
	2009/07/16	<ol style="list-style-type: none"> 1. Modify the description for 6.2.2 Software Reset (01h) (page 117) 2. Add the description for 8.4.3 The Electrical Characteristics of D-PHY Layer (page 203 ~ page 210)
	2009/07/27	<ol style="list-style-type: none"> 1. Modify the description for pin REGVDD (page 12, page 15, page 17, page 212) 2. Modify the description for pin DSI_LDO_EN (page 12, page 212, page 213)
	2009/08/04	<ol style="list-style-type: none"> 1. Modify the description for 5.10 Power On/Off Sequence (page 103)
	2009/08/25	<ol style="list-style-type: none"> 1. Modify the description for 6.2.38 Set Power (B1h) (page 159, page 162) 2. Modify the description for 6.2.43 Set VCOM Voltage (B6h) (page 176) 3. Modify the Table 7.2: Adoptability of Component (page 193) 4. Add the description for 8.4.5 Power On/Off Timing (page 212) 5. Add the description for 9.1 Reference Layout (page 213, page 214) 6. Modify the description for 10.3 Programming sequence (page 222)
	2009/09/09	<ol style="list-style-type: none"> 1. Modify the description for pin G1 ~ G864 (page 13) 2. Modify the description for 6.2.10 Read Display Signal Mode (page 128) 3. Modify the description for 6.2.19 Memory Access Control (page 139) 4. Modify the description for 6.2.38 Enable extension command (page 179)
	2009/09/11	<ol style="list-style-type: none"> 1. Modify the OTP programming flow for UMC update (page 221, page 222)
	2009/09/18	<ol style="list-style-type: none"> 1. Modify the Figure 4.4: 3 wire Serial Interface protocol, read mode for user define command (page 33) 2. Modify the description for 6.2.20 Interface Pixel Format (page 140) 3. Modify the description for 6.2.34 Set Power (B1h) (page 156) 4. Modify the description for 6.2.40 Set DGC LUT (C1h) (page 181) 5. Modify the description for 8.4.5 Power On/Off Timing (page 212, page 213)
	2009/09/29	<ol style="list-style-type: none"> 1. Modify the description for 6.2.34 Set Power (B1h) (page 161) 2. Modify the description for 8.4.2 RGB Interface Characteristics (page 198, page 199, page 200)

	2009/11/17	<ol style="list-style-type: none"> 1. Modify the description for 3.2 Pin Description (page 12, page 13) 2. Remove the Schottky Diode for VGL (page 191, page 192, page 193, page 214, page 215) 3. Modify the description for Table 8.4: Power consumptions (page 196) 4. Modify the operation voltage range for VDD2 & VDD3 (page 10, page 13, page 195, page 196, page 197, page 198, page 199, page 201)
	2009/11/24	<ol style="list-style-type: none"> 1. Modify the description for register AP[2:0] (page 154, page 160, page 205)
03	2009/11/25	<ol style="list-style-type: none"> 1. Modify the description for 6.2.41 Set ID (C3h) (page 175) 2. Modify the description for 8.4.1 Serial Interface Characteristics (page 188) 3. Modify the description for Table 8.7 General Timings for RGB I/F (page 191)
	2009/12/9	<ol style="list-style-type: none"> 1. Modify the operation voltage range for VDD1 (page 186, page 189, page 190) 2. Modify the description for 3.2 Pin Description (page 14) 3. Modify the description for Table 4.2 Data Types for Processor-sourced Packets (page 43) 4. Delete Color Mode Off/On Description (page 44) 5. Modify the description for Table 4.3 Error Report Bit Definitions (page 49) 6. Modify the description for 6.2.21 Read_DDB_start (A1h) (page 136) 7. Modify the description for 6.2.22 Read_DDB_continue (A8h) (page 137) 8. Add the Schottky Diode for VGL (page 182, page 183, page 184, page 203, page 204) 9. Modify the description for Figure 8.11 Power On Timing (page 201)
	2010/01/21	<ol style="list-style-type: none"> 1. Modify the description for 3.4.1 Bump arrangement (page 28)
	2010/01/27	<ol style="list-style-type: none"> 1. Modify the Table 8.1 Absolute Maximum Rating (page 185)
	2010/02/24	<ol style="list-style-type: none"> 1. Modify the Table 8.1 Absolute Maximum Rating (page 185) 2. Modify the description for 8.4.3 The Electrical Characteristics of D-PHY Layer (page 197)
	2010/04/09	<ol style="list-style-type: none"> 1. Modify the description for 6.2.34 Set Power (B1h) (page 153)
	2010/09/06	<ol style="list-style-type: none"> 1. Modify the description for 3.4.1 Bump arrangement (page 29) 2. Modify the description for 6.2.36 Set Display Waveform Cycle (B4h) (page 167)
	2011/07/22	<ol style="list-style-type: none"> 1. Modify the Table 4.2 Data types for processor-sourced packets (page 43)