

# Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics

#### **Programmer's Reference Manual**

For the 2015 - 2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform

Volume 2a Addendum: Command Reference: Instructions (Command Opcodes) for the HEVC Micro-Controller (HuC)

May 2016, Revision 1.0

**Command Reference: Instructions** 



#### **Creative Commons License**

**You are free to Share** - to copy, distribute, display, and perform the work under the following conditions:

- **Attribution.** You must attribute the work in the manner specified by the author or licensor (but not in any way that suggests that they endorse you or your use of the work).
- No Derivative Works. You may not alter, transform, or build upon this work.

#### **Notices and Disclaimers**

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Implementations of the I2C bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.

Intel and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

\* Other names and brands may be claimed as the property of others.

**Copyright © 2016, Intel Corporation. All rights reserved.** 

#### **Command Reference: Instructions**



# **Table of Contents**

HUC_CFG_STATE	1
HUC_DMEM_STATE	3
HUC_IMEM_STATE	5
 HUC_IND_OBJ_BASE_ADDR_STATE	
HUC_PIPE_MODE_SELECT	9
HUC_START	11
HUC_STREAM_OBJECT	13
HUC_VIRTUAL_ADDR_STATE	16



### **HUC\_CFG\_STATE**

# **HUC\_CFG\_STATE**

Source: VideoCS

Length Bias: 2

The HUC is selected with the Media Instruction Opcode "Bh" for all HUC Commands. Each HUC command has assigned a media instruction command as defined in DWord 0, BitField 22:16.

The HUC\_CFG\_STATE command is used to force the P24C (MinuteIA) into a reset condition as well as forcing it out of a reset condition. This command is not normally required since the hardware will handle placing the P24C into a reset condition and releasing it from reset, but there may be conditions that require a forced reset.

DWord	Bit	Description					
0	31:29	Command Type					
		Default Value:	3h PARA	ALLEL_VIDE	O_PIPE	PIPE	
		Format:	OpCode	9			
	28:27	Pipeline Type					
		Default Value:			2h		
		Format:			OpCo	ode	
	26:23	Media Instruction Op	ocode				
		Default Value:	Bh Coo	dec/Engine	Name		
		Format:	OpCod	OpCode			
		Codec/Engine Name = HUC = Bh					
	22:16	Media Instruction Command					
		Default Value:	3h	3h HUC_CFG_STATE			
		Format: OpCode					
	15:12	Reserved					
		Format: M			MBZ		
	11:0	Dword Length					
		Format:				=n	
		(Excludes Dwords 0, 1).					
		Value			Name		
		0h					
1	31:1	Reserved		,			
		Format:			MBZ		



HUC_CFG_STATE							
	0	P24C (MinuteIA)					
		Format:		U1			
		Value	Name	Description			
		0	Normal operation	No reset.			
		1	Force reset				



### **HUC\_DMEM\_STATE**

# **HUC\_DMEM\_STATE**

Source: VideoCS

Length Bias: 2

The HUC is selected with the Media Instruction Opcode "Bh" for all HUC Commands. Each HUC command has assigned a media instruction command as defined in DWord 0, BitField 22:16.

The HUC\_DMEM\_STATE command is used to fetch the HUC data from the graphics memory and load it into the HUC 96KB L2 storage RAM. The HUC\_DMEM\_STATE specifies the data source base address in graphics memory.

When the HUC\_DMEM\_STATE command is received, the data is loaded by the HUC DMA into the 96KB L2 storage RAM at the location provided in the HUC\_DMEM\_STATE command. This command also specifies the length of the data, which is specified in bytes but must be in increments of 64 byte cache lines.

DWord	Bit	Description					
0	31:29	<b>Command Type</b>					
		Default Value:	3h PARALLEL_VIDEO_PIPE				
		Format:	OpCode				
	28:27	Pipeline Type					
		Default Value:			2h		
		Format:			ОрСо	de	
	26:23	Media Instruction Opcode					
		Default Value:	Bh Codec	dec/Engine Name			
		Format:	OpCode				
		Codec/Engine Name = HUC = Bh					
	22:16	Media Instruction Command					
		Default Value:	2h HUC_I	DMEM_STA	DMEM_STATE		
		Format:	OpCode				
	15:12	Reserved					
		Format:		1	MBZ		
	11:0	Dword Length					
		Format: =n					
		(Excludes Dwords 0, 1).					
		Value				Name	
		4h					



	WHALS HISK					
		F F	IUC_DMEM_STATE			
12	63:0	<b>HUC Data Source Ba</b>				
		Format:	plitBaseAddress64ByteAligned			
		Specifies the 64 byte	aligned HUC data source base a	ddress in graphics memory.		
3	31:0	<b>HUC Data Source</b>				
		Format:	MemoryAddressAttributes			
4	31:17	Reserved				
		Format:		MBZ		
	16:6	<b>HUC Data Destination</b>	on Base Address			
		Format: GraphicsAddress[16:6]				
		1 -	e L2 storage RAM. The base address is			
		64 byte cache aligned	l.			
	5:0	Reserved				
		Format:		MBZ		
5	31:17	Reserved				
		Format:		MBZ		
	16:6	HUC Data Length				
		Format:	GraphicsAddress[16:6]			
		Specifies the length in bytes of the HUC Data. The length must be in increments of 64				
		cache lines.				
	5:0	Reserved				
		Format:		MBZ		
		<del></del>				



# **HUC\_IMEM\_STATE**

		HUC	_IM	EM_S	TATE				
Source:		VideoCS							
Length E	Bias:	2							
		ected with the Media Instruction dia instruction command as defin	•				ds. Each HUC command ha	S	
DWord	Bit			Desci	ription				
0	31:29	Command Type	Command Type						
		Default Value:	3h PARALLEL_VIDEO_P			PIPE			
		Format:	OpCode						
	28:27	Pipeline Type							
		Default Value:				2h			
		Format:				OpCod	de		
	26:23	Media Instruction Opcode							
		Default Value:	Bh Codec/Engine Name			me			
		Format:	t: OpCode						
		Codec/Engine Name = HUC = Bh							
-	22:16	Media Instruction Command							
		Default Value:	1h HUC_IMEM_			ATE			
		Format:	OpCode						
	15:12	Reserved							
		Format:				MBZ			
	11:0	Dword Length							
		Format:					=n		
		(Excludes Dwords 0, 1).							
		Value					Name		
		3h							
1	31:0	Reserved							
		Format:				MBZ			
2	31:0	Reserved							
		Format:				MBZ			
3	31:0	Reserved							
		Format:				MBZ			
4	31:8	Reserved							
		Format:				MBZ			



# **HUC\_IMEM\_STATE**

7:0 **HUC Firmware Descriptor** 

Format: U8

This field specifies 1 of 255 firmware descriptors which describe which firmware is be loaded in the L2 storage RAM. If the firmware descriptor is set to zero, the HUC will not load the firmware.

Value	Name	Description		
0		Illegal		
[1,255]		Firmware Descriptor		



## HUC\_IND\_OBJ\_BASE\_ADDR\_STATE

# HUC\_IND\_OBJ\_BASE\_ADDR\_STATE

VideoCS Source:

2 Length Bias:

The HUC is selected with the Media Instruction Opcode "Bh" for all HUC Commands. Each HUC command has assigned a media instruction command as defined in DWord 0, BitField 22:16.

The HUC IND OBJ BASE ADDR STATE command is used to define the indirect object base address of the

stream	in grap	hics memory. This is a frame					,,	
DWord	Bit			Desci	ription			
0	31:29	<b>Command Type</b>						
		Default Value:	3h P	PARALLE	L_VIDEO_F	IPE		
2		Format:	ОрС	Code				
	28:27	Pipeline Type						
		Default Value:				2h		
		Format:				OpCo	de	
	26:23	Media Instruction Opcode	•					
		Default Value:	Bh Codec			me		
		Format:		oCode				
		Codec/Engine Name = HUC = Bh						
	22.16	Madia Tantanatian Camanand						
	22:16	Media Instruction Comma  Default Value:			ASE ADDE	STATE		
		Format:	5h HUC_IND_OBJ_BASE_ADDR_STATE OpCode					
	15:12							
	15.12	Reserved Format:				MBZ		
	11:0					IVIDE		
	11.0	Dword Length Format:					=n	
		(Excludes Dwords 0, 1).					-11	
		Value					Name	
		9h						
12	63:0	<b>HUC Indirect Stream In Ol</b>	bjectBase Ac	ddress				
		Format: SplitBaseAddress4KByteAligned						
		Specifies the 4K-byte aligned memory base address for the read-only indirect data object						
		pointed in the HUC_STREAM	M_OBJECT co	mmand	for fetchir	ng (readi	ing) the bit stream data.	
3	31:0	<b>HUC Indirect Stream In Ol</b>	bjectBase At	ttribute	s			
		Format: Me	emoryAddres	sAttribu	tes			
45	63:0	<b>HUC Indirect Stream In Ol</b>	bjectAccess	Upper E	Bound			



		HUC	IND_OBJ_BASE_ADDR_STATE				
		Format: SplitBaseAddress4KByteAligned					
		This field specifies the 4K-byte aligned maximum memory address access by the indirect data object in the HUC_STREAM_OBJECT command for the input bit stream. Indirect data accessed at this address or greater will cause the HUC to stop issuing requests to the GAC.					
	62.0		0 will cause this range to be ignored by the HUC.				
67	63:0	HUC Indirect Stream Out ObjectBase Address  Format: SplitBaseAddress4KByteAligned  Specifies the 4K-byte aligned memory base address for the indirect data object pointed in the HUC_STREAM_OBJECT command for writing the bit stream data.					
8	31:0	<b>HUC Indirect Stream</b>	m Out ObjectBase Attributes				
		Format:	MemoryAddressAttributes				
910	63:0	<b>HUC Indirect Stream</b>	m Out ObjectAccess Upper Bound				
		Format:	SplitBaseAddress4KByteAligned				
		This field specifies the 4K-byte aligned maximum memory address access by the indirect data object in the HUC_STREAM_OBJECT command for the output bit stream. Indirect data accessed at this address or greater will cause the HUC to stop issuing requests to the GAC.  Setting this field to 0 will cause this range to be ignored by the HUC.					



# **HUC\_PIPE\_MODE\_SELECT**

		HUC_PI	PE_MODI	SELECT				
Source:		VideoCS						
Length E	Bias:	2						
		ected with the Media Instruction dia instruction command as defin	•		ch HUC command has			
The HU	C_PIPE	_MODE_SELECT command is resp t once for a single stream decode	onsible for gen	eral pipeline level config				
DWord	Bit		Desc	ription				
0	31:29	Command Type						
		Default Value:	3h PARALL	L_VIDEO_PIPE				
		Format:	OpCode	OpCode				
	28:27	Pipeline Type						
		Default Value:	2h					
		Format:		OpCode				
	26:23	3 Media Instruction Opcode						
		Default Value:	Bh Codec	Engine Name				
		Format:	OpCode					
		Codec/Engine Name = HUP = BI						
	22:16	<b>Media Instruction Command</b>						
		Default Value:	0h HUC_PIPE_	MODE_SELECT				
		Format:	OpCode					
	15:12	Reserved						
		Format:		MBZ				
	11:0	DWord Length						
		Format:		=n				
		(Excludes Dwords 0, 1).						
		Value		Na	me			
		1h						
1	31.5	Reserved						

 $\mathsf{MBZ}$ 

Format:



	HUC_PIPE_MODE_SELECT						
	4	Indirect Stream O	Indirect Stream Out Enable				
		Format:		Enable			
				•	emory buffer is addressed through the		
		HuC Indirect Stream	n Out ObjectBase Address	5.			
		Value		Nar	ne		
		0h	Disable Indirect Stream	Out			
		1h	Enable Indirect Stream C	Out			
	3:0	Reserved					
		Format:	MBZ				
2	31:0	Media Soft Reset	Counter (per 1000 clocks	s)			
		Format:			U32		
		In decoder modes, this counter value specifies the number of clocks (per 1000) of GAC inactivity before a media soft-reset is applied to the HCP and HuC. If counter value is set to 0, the media soft-reset feature is disabled and no reset will occur.					
		•	ncoder modes, this counter must be set to 0 to disable media soft reset. This feature is not ported for the encoder.				
			Value		Name		
		0		Disable			



# **HUC\_START**

		HUC	STAR	Γ				
Source:		VideoCS						
Length Bias:		2						
		Desc	cription					
		with the Media Instruction Opcod truction command as defined in [				s. Each HUC command has		
DWord	Bit	Description						
0	31:29	<b>Command Type</b>						
		Default Value:	3h PARAL	LEL_VIDEO	_PIPE			
		Format:	ormat: OpCode					
	28:27	Pipeline Type						
		Default Value:			2h			
		Format:		OpCode				
	26:23	Media Instruction Opcode						
		Default Value: Bh Codec/Engine Name						
		Format: OpCode						
		Codec/Engine Name = HUC = B	h					
-	22:16	Media Instruction Command						
		Default Value:		21h HUC_S	TART			
				OpCode	pCode			
	15:12	Reserved						
		Format:			MBZ			
	11:0	Dword Length						
		Format:				=n		
		(Excludes Dwords 0, 1).						
		Value		Name				
		0h						
1	31:3	Reserved						
		Format:			MBZ			
-								

2:1

Reserved



			HUC_ST	ART					
	0	LastStre	amObject						
	Format: U1								
	cription								
		1	Last stream object in the workload.						
		0	NotLastStreamObject	Not the last stream obje	ct in the workload.				



### **HUC STREAM OBJECT**

HUC_	SIKE	:AIVI_UBJE	:C1					
			HUC_STI	REAM_C	<b>DBJECT</b>	•		
Source:		VideoCS						
Length Bi	ias:	2						
			edia Instruction Ope mmand as defined			ommands. Each HUC command has		
						ess offset to the Stream Indirect		
Object b	ase Ad					the HUC operates upon is specified		
DWord	Bit			Desc	ription			
0	31:29	Command Typ	e					
		Default Value:		3h PARALLE	EL_VIDEO_PI	IPE		
		Format:		OpCode				
	28:27	Pipeline Type						
		Default Value:				2h		
		Format:			OpCode			
	26:23	Media Instruct	ion Opcode					
		Default Value:		Bh Codec	/Engine Nan	ne		
		Format:	Format: OpCode					
		Codec/Engine N	Name = HUC = Bh					
	22:16	Media Instruct	ion Command					
		Default Value:		20h HUC_ST	REAM_OBJE	СТ		
		Format:		OpCode	pCode			
	15:12	Reserved						
		Format:			MBZ			
	11:0	Dword Length						
		Format:				=n		
		(Excludes Dword	ds 0, 1).					
			Value			Name		
		3h						
1	31:0	Indirect Stream In Data Length						
		Format:				U32		
		'	ngth in bytes of the		nput data.			
		Value	Name		1	Description		
		[0,268435455]	Data_Length_with_ 	_28_bits_only	_	ge is only from 0 to 268435455, orresponding to lower 28 bits.		

Reserved

31



				HUC	C_STREAM	_OBJECT				
	30:29	Reserve	ed							
		Format	t:			N	MBZ			
	28:0	Indirect Stream In Start Address								
		Format	Format: U29							
		Specifies the byte-aligned graphics memory starting address of the input bit stream relative to the <b>HUC Indirect Stream In ObjectBase Address [31:12]</b> .								
3	31:29	Reserve	ed							
		Format	t:			N	MBZ			
	28:0	Indirec	t Stream	Out Start	Address					
		Format	t:				U29			
		•	-		graphics memory <b>Dut ObjectBase</b> <i>I</i>	-		ne output bit stream relative	to:	
4	31:30	Reserve	ed							
		Format:								
	29	HuC Bitstream Enable								
		Format: Enable								
			Enables the bitstream to be sent to the HuC							
				Value		Name				
		0h				Disable				
		1h				Enable				
	28:27									
		Format	<u>t:</u>					U2		
		Value	N	ame		Des	scriptio	on		
		00b	Start Co	de Mode	Stops on a start					
		01b	Length	Mode	Stops after a nu	mber of bytes a	are rea	ched in the length counter		
		10b	Reserve	ed		·				
		11b	Reserve	ed						
	25	Emulat	ion Prev	ention Byt	e Removal					
	25 <b>Emulation Prevention Byte Removal</b> Format:		Enable							
		Value				Descripti				
		0			ulation Preventic					
		1	Enable	Emulation engine.	prevention bytes	will be remove	ed afte	r the start code search		



			HUC_STREAM_OB.	JECT					
24	Start C	ode Search Engine							
	Forma	t:		Enable					
	Value	Name	D						
	0	Disable	Bypass Start Code Search Engine	Bypass Start Code Search Engine					
	1	Enable	Enables the start code search enging defined by <b>Start Code Byte [2:0]</b> of						
23:16	Start C	ode Byte	[2]	T 1					
	Forma	t:		U8					
	Third byte of the start code								
15:8	Start C	ode Byte	· [1]						
	Forma	t:		U8					
	Second	byte of t	he start code						
7:0	Start C								
	Forma	t:		U8					
	First by	First byte of the start code							



## **HUC\_VIRTUAL\_ADDR\_STATE**

# **HUC\_VIRTUAL\_ADDR\_STATE**

Source: VideoCS

Length Bias: 2

HUC is selected with the Media Instruction Opcode "Bh" for all HUC Commands. Each HUC command has assigned a media instruction command as defined in DWord 0, BitField 22:16.

The HUC\_VIRTUAL\_ADDR\_STATE command is used to define the 48-bit HUC Surface Base Address and HUC Surface for each region.

Word	Bit						
0	31:29	Command Type					
		Default Value:	3h	n PARALL	.EL_VIDEO_P	PIPE	
		Format:		pCode			
	28:27	Pipeline Type					
		Default Value:				2h	
		Format:				OpCode	
	26:23	Media Instruction (	Opcode				
		Default Value:		Bh Codec/Engine Name			
		Format:		OpCode			
		Codec/Engine Name = HUC = Bh					
	22:16	Media Instruction Command					
		Default Value:	4h HL	h HUC_VIRTUAL_ADDR_STATE			
		Format: OpCode					
	15:12	Reserved					
		Format: MBZ					
	11:0	Dword Length					
		Format:				=n	
		(Excludes Dwords 0,					
			'alue			Name	
		2Fh					
148	95:64	HUC Surface (Virtu					
		Format:					
	63:0	HUC Surface Base Address (VirtualAddrRegion[0-15])					
		Format: SplitBaseAddress4KByteAligned					