550:AL
550:BL
instr_req_o = 1'b1;
csr_save_if_o = 1'b0;
csr_save_id_o = 1'b0;
csr_restore_mret_id_o = 1'b0;
csr_restore_dret_id_o = 1'b0;
csr_save_cause_o = 1'b0;
csr_mtval_o = 1'sb0;
pc_mux_o = PC_BOOT;
pc_set_o = 1'b0;
exc_pc_mux_o = EXC_PC_IRQ;
exc_cause_o = EXC_CAUSE_INSN_ADDR_MISA;
ctrl_fsm_ns = ctrl_fsm_cs;
ctrl_busy_o = 1'b1;
halt_if = 1'b0;
flush_id = 1'b0;
debug_csr_save_o = 1'b0;
debug_cause_o = DBG_CAUSE_EBREAK;
debug_mode_d = debug_mode_q;
nmi_mode_d = nmi_mode_q;
perf_tbranch_o = 1'b0;
perf_jump_o = 1'b0;
572:CS
ctrl_fsm_cs
ctrl_fsm_cs
ctrl_fsm_cs
ctrl_fsm_cs
ctrl_fsm_cs
ctrl_fsm_cs
ctrl_fsm_cs
ctrl_fsm_cs
ctrl_fsm_cs
ctrl_fsm_cs
ctrl_fsm_cs
694:CA
641:CA
615:CA
602:CA
663:CA
754:CA
573:CA
680:CA
580:CA
586:CA
593:CA
694:BL
halt_if = 1'b1;
flush_id = 1'b1;
ctrl_fsm_ns = DECODE;
751:IF
enter_debug_mode
752:BS
ctrl_fsm_ns = DBG_TAKEN_IF;
698:IF
(exc_req_q || store_err_q || load_err_q)
698:BL
pc_set_o = 1'b1;
pc_mux_o = PC_EXC;
exc_pc_mux_o = (debug_mode_q)? EXC_PC_DBG_EXC : EXC_PC_EXC;
csr_save_id_o = 1'b1;
csr_save_cause_o = 1'b1;
!((exc_req_q || store_err_q || load_err_q))
704:IF
instr_fetch_err
!(instr_fetch_err)
704:BL
exc_cause_o = EXC_CAUSE_INSTR_ACCESS_FAULT;
csr_mtval_o = pc_id_i;
708:IF
!(illegal_insn_q)
illegal_insn_q
708:BL
exc_cause_o = EXC_CAUSE_ILLEGAL_INSN;
csr_mtval_o = (instr_is_compressed_i)? { 16'b0, instr_compressed_i } : instr_i;
712:IF
!(ecall_insn)
ecall_insn
713:BS
exc_cause_o = (priv_mode_i == PRIV_LVL_M)? EXC_CAUSE_ECALL_MMODE : EXC_CAUSE_ECALL_UMODE;
714:IF
ebrk_insn
!(ebrk_insn)
714:BL
715:IF
!((debug_mode_q | ebreak_into_debug))
(debug_mode_q | ebreak_into_debug)
723:BS
exc_cause_o = EXC_CAUSE_BREAKPOINT;
715:BL
pc_set_o = 1'b0;
csr_save_id_o = 1'b0;
csr_save_cause_o = 1'b0;
ctrl_fsm_ns = DBG_TAKEN_ID;
flush_id = 1'b0;
725:IF
store_err_q
!(store_err_q)
725:BL
exc_cause_o = EXC_CAUSE_STORE_ACCESS_FAULT;
csr_mtval_o = lsu_addr_last_i;
729:BL
exc_cause_o = EXC_CAUSE_LOAD_ACCESS_FAULT;
csr_mtval_o = lsu_addr_last_i;
734:IF
!(mret_insn)
mret_insn
734:BL
pc_mux_o = PC_ERET;
pc_set_o = 1'b1;
csr_restore_mret_id_o = 1'b1;
741:IF
dret_insn
!(dret_insn)
741:BL
pc_mux_o = PC_DRET;
pc_set_o = 1'b1;
debug_mode_d = 1'b0;
csr_restore_dret_id_o = 1'b1;
747:IF
wfi_insn
!(wfi_insn)
748:BS
ctrl_fsm_ns = WAIT_SLEEP;
749:IF
(csr_pipe_flush && handle_irq)
750:BS
ctrl_fsm_ns = IRQ_TAKEN;
738:IF
nmi_mode_q
739:BS
nmi_mode_d = 1'b0;
641:BL
ctrl_fsm_ns = DECODE;
642:IF
handle_irq
642:BL
pc_mux_o = PC_EXC;
pc_set_o = 1'b1;
exc_pc_mux_o = EXC_PC_IRQ;
csr_save_if_o = 1'b1;
csr_save_cause_o = 1'b1;
648:IF
(irq_nm_i && !nmi_mode_q)
!((irq_nm_i && !nmi_mode_q))
648:BL
exc_cause_o = EXC_CAUSE_IRQ_NM;
nmi_mode_d = 1'b1;
652:IF
(csr_mfip_i != 15'b0)
!((csr_mfip_i != 15'b0))
653:BS
exc_cause_o = sv2v_cast_89EA8({ 2'b11, mfip_id });
654:IF
!(csr_meip_i)
csr_meip_i
655:BS
exc_cause_o = EXC_CAUSE_IRQ_EXTERNAL_M;
656:IF
!(csr_msip_i)
csr_msip_i
659:BS
exc_cause_o = EXC_CAUSE_IRQ_TIMER_M;
657:BS
exc_cause_o = EXC_CAUSE_IRQ_SOFTWARE_M;
615:BL
616:IF
instr_valid_i
616:BL
617:IF
special_req
!(special_req)
617:BL
ctrl_fsm_ns = FLUSH;
halt_if = 1'b1;
621:IF
(branch_set_i || jump_set_i)
621:BL
pc_mux_o = PC_JUMP;
pc_set_o = 1'b1;
perf_tbranch_o = branch_set_i;
perf_jump_o = jump_set_i;
627:IF
((enter_debug_mode || handle_irq) && stall)
628:BS
halt_if = 1'b1;
630:IF
(!stall && !special_req)
631:IF
enter_debug_mode
!(enter_debug_mode)
631:BL
ctrl_fsm_ns = DBG_TAKEN_IF;
halt_if = 1'b1;
635:IF
handle_irq
635:BL
ctrl_fsm_ns = IRQ_TAKEN;
halt_if = 1'b1;
flush_id = 1'b1;
602:BL
610:IF
enter_debug_mode
610:BL
ctrl_fsm_ns = DBG_TAKEN_IF;
halt_if = 1'b1;
605:IF
handle_irq
605:BL
ctrl_fsm_ns = IRQ_TAKEN;
halt_if = 1'b1;
flush_id = 1'b1;
603:IF
id_in_ready_o
604:BS
ctrl_fsm_ns = DECODE;
663:BL
ctrl_fsm_ns = DECODE;
664:IF
(debug_single_step_i || debug_req_i)
664:BL
flush_id = 1'b1;
pc_mux_o = PC_EXC;
pc_set_o = 1'b1;
exc_pc_mux_o = EXC_PC_DBD;
csr_save_if_o = 1'b1;
debug_csr_save_o = 1'b1;
csr_save_cause_o = 1'b1;
debug_mode_d = 1'b1;
672:IF
debug_single_step_i
!(debug_single_step_i)
673:BS
debug_cause_o = DBG_CAUSE_STEP;
675:BS
debug_cause_o = DBG_CAUSE_HALTREQ;
754:BL
instr_req_o = 1'b0;
ctrl_fsm_ns = 1'bX;
573:BL
instr_req_o = 1'b0;
pc_mux_o = PC_BOOT;
pc_set_o = 1'b1;
577:IF
fetch_enable_i
578:BS
ctrl_fsm_ns = BOOT_SET;
680:BL
flush_id = 1'b1;
pc_mux_o = PC_EXC;
pc_set_o = 1'b1;
exc_pc_mux_o = EXC_PC_DBD;
debug_mode_d = 1'b1;
ctrl_fsm_ns = DECODE;
685:IF
(ebreak_into_debug && !debug_mode_q)
685:BL
csr_save_cause_o = 1'b1;
csr_save_id_o = 1'b1;
debug_csr_save_o = 1'b1;
debug_cause_o = DBG_CAUSE_EBREAK;
580:BL
instr_req_o = 1'b1;
pc_mux_o = PC_BOOT;
pc_set_o = 1'b1;
ctrl_fsm_ns = FIRST_FETCH;
586:BL
ctrl_busy_o = 1'b0;
instr_req_o = 1'b0;
halt_if = 1'b1;
flush_id = 1'b1;
ctrl_fsm_ns = SLEEP;
593:BL
instr_req_o = 1'b0;
halt_if = 1'b1;
flush_id = 1'b1;
597:IF
(irq_nm_i || irq_pending_i || debug_req_i || debug_mode_q || debug_single_step_i)
!((irq_nm_i || irq_pending_i || debug_req_i || debug_mode_q || debug_single_step_i))
598:BS
ctrl_fsm_ns = FIRST_FETCH;
600:BS
ctrl_busy_o = 1'b0;
Leaf_550:AL