SiliconMotion

DYNA FAMILY

SM3267

SuperSpeed USB 3.0 Flash Drive Controller

Datasheet

Revision 1.0 **Apr 2014**

Revision History

Revision	Date	Description
0.1	May 10, 2013	Preliminary release
1.0	Apr 11, 2014	• Added the built-in voltage regulators in Key Features (1.2) • Added the E-LQFP-48 pin assignments and package outline (2.1, 2.2 and 4.2) • Updated Block Diagram (1.3) • Added the ordering numbers (5)

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1. Overview

1.1 Product Description

The SM3267 is a USB 3.0 single-channel flash drive controller offering high performance and high compatibility for SLC, MLC, TLC, and high-speed Toggle and ONFI DDR NAND. For USB 3.0 Flash Disk applications, this controller supports high capacity of up to 4 NAND flash devices.

The SM3267 delivers high data transfer rate, and ensures data accuracy and reliability with the powerful ECC engine which can overcome the read/write disturbances on new generation NAND. By integrating an embedded crystal and other components, the controller can reduce customer overall cost at a system level. The SM3267 is available in QFN-48 and E-LQFP-48 green packages with manufacturing-ready turnkey solution.

1.2 Key Features

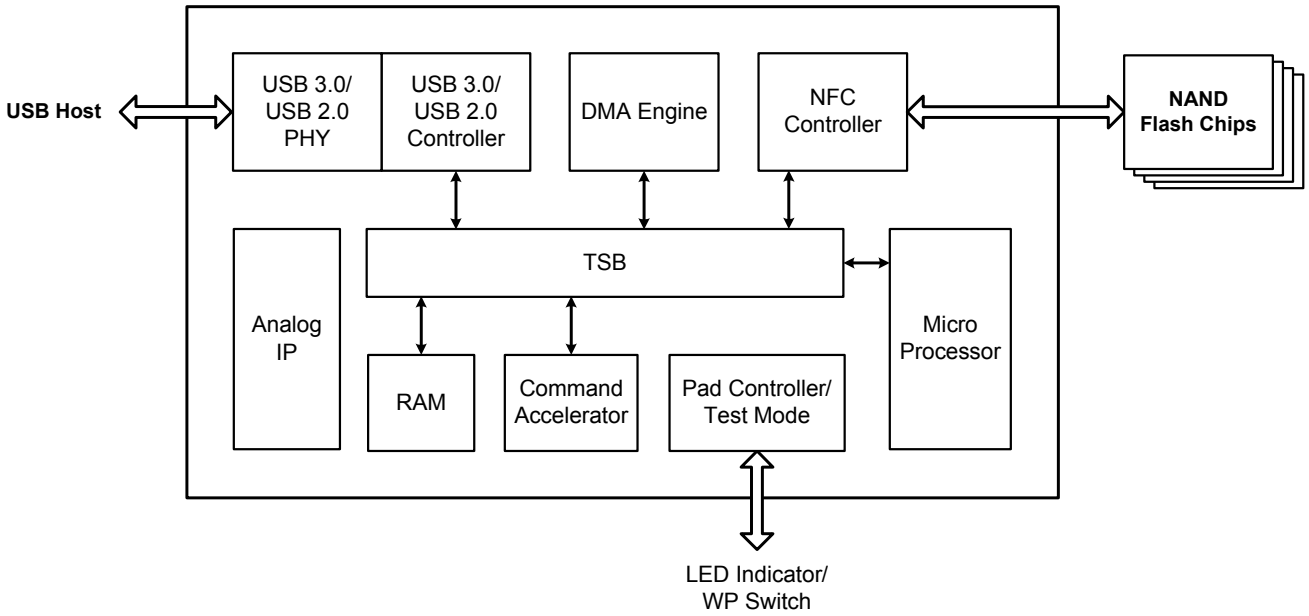
- USB 3.0 SuperSpeed (5 Gbps) and USB High-Speed Interface
  - Compliant with USB 3.0 Specification Rev. 1.0
  - Compliant with USB 2.0 Specification Rev. 2.0
  - USB Mass Storage Class Specification Rev. 1.0
  - USB Mass Storage Class Bulk-Only Transport Protocol
  - Supports USB 3.0 multi-level link power management
- NAND Flash Support
  - Single-channel flash interface
  - Supports 2-way and 4-way interleave operation
  - Configurable ECC engine with correction capability up to 72-bit/1KB
  - Supports SLC/MLC/TLC with 4KB/8KB/16KB page
  - Supports Toggle/ONFI DDR NAND flash
  - Supports 3.3V/1.8V NAND Flash
  - Supports Bad Column Management
- The crystal-less design offers lower BOM cost
- Built-in 3.3V/1.2V voltage regulators
- Supports “Write Protect” security function to protect the data in USB Flash Disk
- Supports LED indicator to indicate the access status
- Supports VID, PID, serial number, and vender information update
- Supports firmware in-system programming (ISP) function for firmware upgrade
- Low power 1.2V core operation

- Supports the operating systems:
  - Windows 8, Windows 7, Windows Vista, Windows XP, Windows 2000, Windows ME, Windows 98/98SE[1]
  - Mac OS 10.x
  - Linux kernel 2.4
- Supports Windows 8, Windows 7, and Windows Vista ReadyBoost function
- Package Option (Lead-free and RoHS compliant)
  - 48-pin QFN
  - 48-pin E-LQFP

[1]: Driver for Windows 98/98SE/ME/2000 is not available in SuperSpeed mode.

1.3 Block Diagram

Figure 1: SM3267 Block Diagram



2. Pin Assignments and Signal Descriptions

2.1 Pin Assignments

Figure 2: 48-Pin QFN Pin Assignments (Top View)

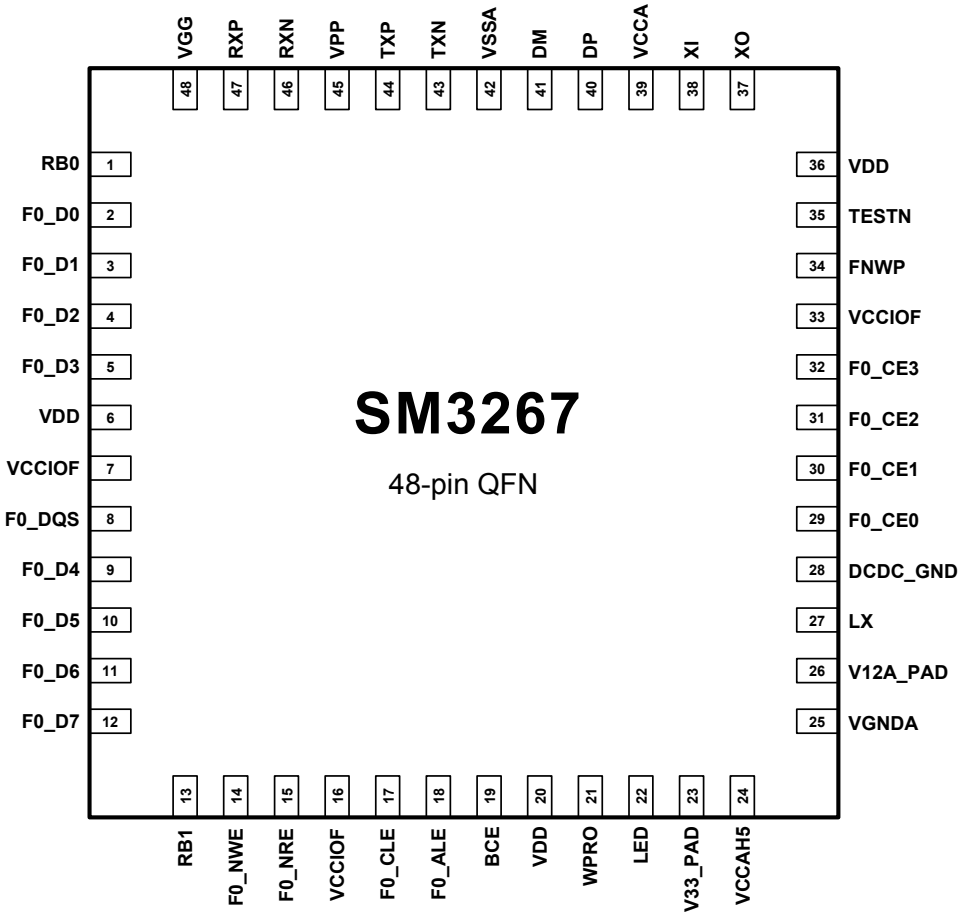
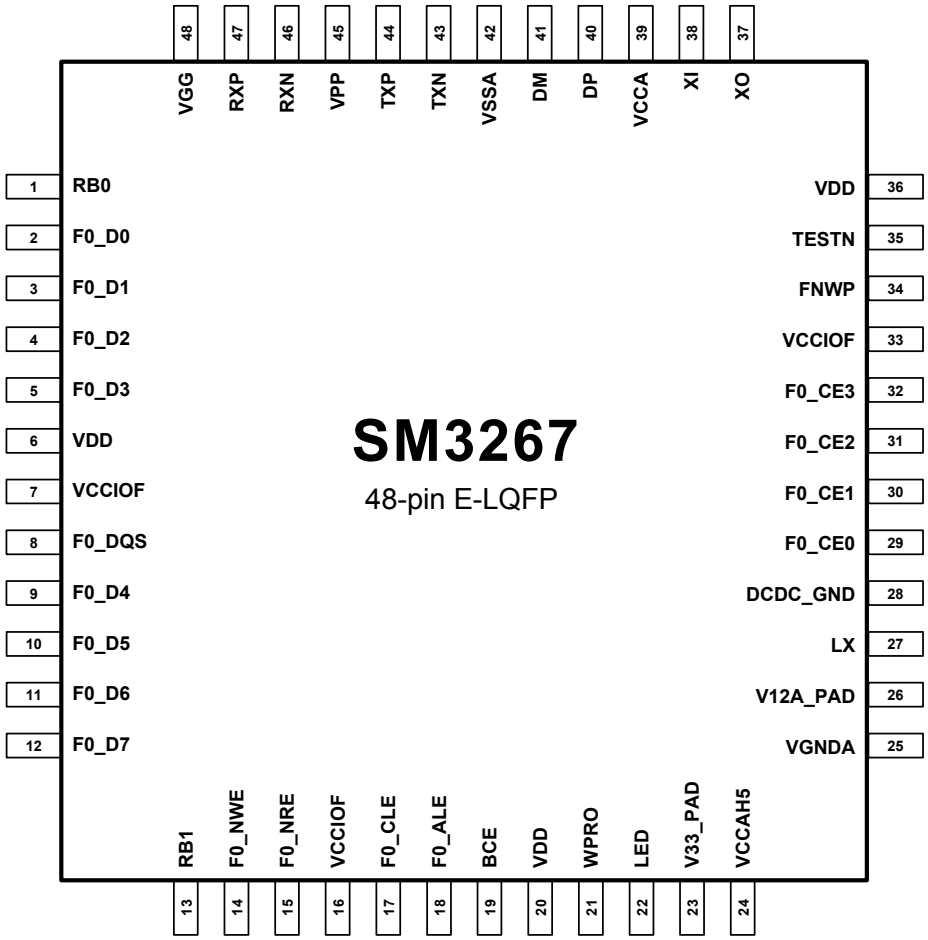


Figure 3: 48-Pin E-LQFP Pin Assignments (Top View)



2.2 Signal Descriptions

Table 1: SM3267 Signal Descriptions

Pin No.	Signal	Type	Description
1	RB0	I	Flash Ready/Busy Signal
2	F0_D0	I/O	Flash Data Bus Bit 0
3	F0_D1	I/O	Flash Data Bus Bit 1
4	F0_D2	I/O	Flash Data Bus Bit 2
5	F0_D3	I/O	Flash Data Bus Bit 3
6	VDD	PWR	Core Power
7	VCCIOF	PWR	Flash I/O Power (3.3V/1.8V)
8	F0_DQS	I/O	Flash Data Strobe
9	F0_D4	I/O	Flash Data Bus Bit 4
10	F0_D5	I/O	Flash Data Bus Bit 5
11	F0_D6	I/O	Flash Data Bus Bit 6
12	F0_D7	I/O	Flash Data Bus Bit 7
13	RB1	I	Flash Ready/Busy Signal
14	F0_NWE	O	Flash Write Enable (active low)
15	F0_NRE	O	Flash Read Enable (active low)
16	VCCIOF	PWR	Flash I/O Power (3.3V/1.8V)
17	F0_CLE	O	Flash Command Latch Enable
18	F0_ALE	O	Flash Address Latch Enable
19	BCE	I	Bad Column Function Enable
20	VDD	PWR	Core Power
21	WPRO	I	Chip Write Protect
22	LED	O	USB LED Indicator
23	V33_PAD	PWR	Regulator 3.3V Power Output
24	VCCAH5	PWR	Regulator 5V Power Input
25	VGNDA	GND	Ground for PLL
26	V12A_PAD	PWR	PLL Power
27	LX	I/O	Connect to external inductor (DC-to-DC converter)
28	DCDC_GND	GND	Ground for DC-to-DC converter
29	F0_CE0	O	Flash Chip Enable 0
30	F0_CE1	O	Flash Chip Enable 1
31	F0_CE2	O	Flash Chip Enable 2
32	F0_CE3	O	Flash Chip Enable 3
33	VCCIOF	PWR	Flash I/O Power (3.3V/1.8V)
34	FNWP	O	Flash Write Protect (active low)

Pin No.	Signal	Type	Description
35	TESTN	I	Test Mode (active low)
36	VDD	PWR	Core Power
37	XO	O	24 MHz PHY Crystal Output
38	XI	I	24 MHz PHY Crystal Input
39	VCCA	PWR	USB 2.0 PHY Power (3.3V)
40	DP	I/O	USB 2.0 Data Positive Pin
41	DM	I/O	USB 2.0 Data Negative Pin
42	VSSA	GND	Ground for USB 2.0 PHY
43	TXN	O	USB 3.0 TX Data Negative Pin
44	TXP	O	USB 3.0 TX Data Positive Pin
45	VPP	PWR	USB 3.0 PHY Power (1.2V)
46	RXN	I	USB 3.0 RX Data Negative Pin
47	RXP	I	USB 3.0 RX Data Positive Pin
48	VGG	GND	Ground for USB 3.0 PHY

3. Electrical Characteristics

3.1 DC Characteristics

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{STG}	-55	+150	°C
Voltage with Respect to Ground		-0.3	+5.5	V
Core Power Supply Voltage	VDD	1.08	1.32	V
Regulator Power Supply Voltage	VCCAH5	4.0	5.5	V
1.8V Flash I/O Supply Voltage	VCCIOF	1.62	1.98	V
3.3V Flash I/O Supply Voltage	VCCIOF	3.0	3.6	V
USB 2.0 PHY 3.3V Input Voltage	VCCA	3.0	3.6	V
USB 3.0 PHY 1.2V Input Voltage	VPP	1.02	1.32	V
PLL 1.2V Input Voltage	V12A_PAD	1.02	1.32	V

Table 3: DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Regulator Power Voltage	VCCAH5	4.0	5.0	5.5	V
Regulator Power Output	V33_PAD		3.3		
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
Peak Voltage on All Lines		-0.5		3.6	V
All Input Leakage Current		-10		10	µA
All Output Leakage Current		-10		10	µA
Bus Line Capacitance	C_L			20	pF

3.2 Flash Interface AC Characteristics

3.2.1 Legacy NAND

Table 4: AC Timing Parameters for Legacy NAND

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS	1		tCK
CLE Hold Time	tCLH	1		tCK
CE Setup Time	tCS	>20		ns
CE Hold Time	tCH	1		tCK
ALE Setup Time	tALS	1		tCK
ALE Hold Time	tALH	1		tCK
WE Pulse Width	tWP	1		tCK
Data Setup Time	tDS	1		tCK
Data Hold Time	tDH	1		tCK
Write Cycle Time	tWC	2		tCK
WE High Hold Time	tWH	1		tCK
Read Cycle Time	tRC	2		tCK
RE High Hold Time	tREH	1		tCK
R/B ready to RE low	tRR	5		tCK

Note: tCK = system clock operation period.

Figure 4: Command Latch Cycle Timing

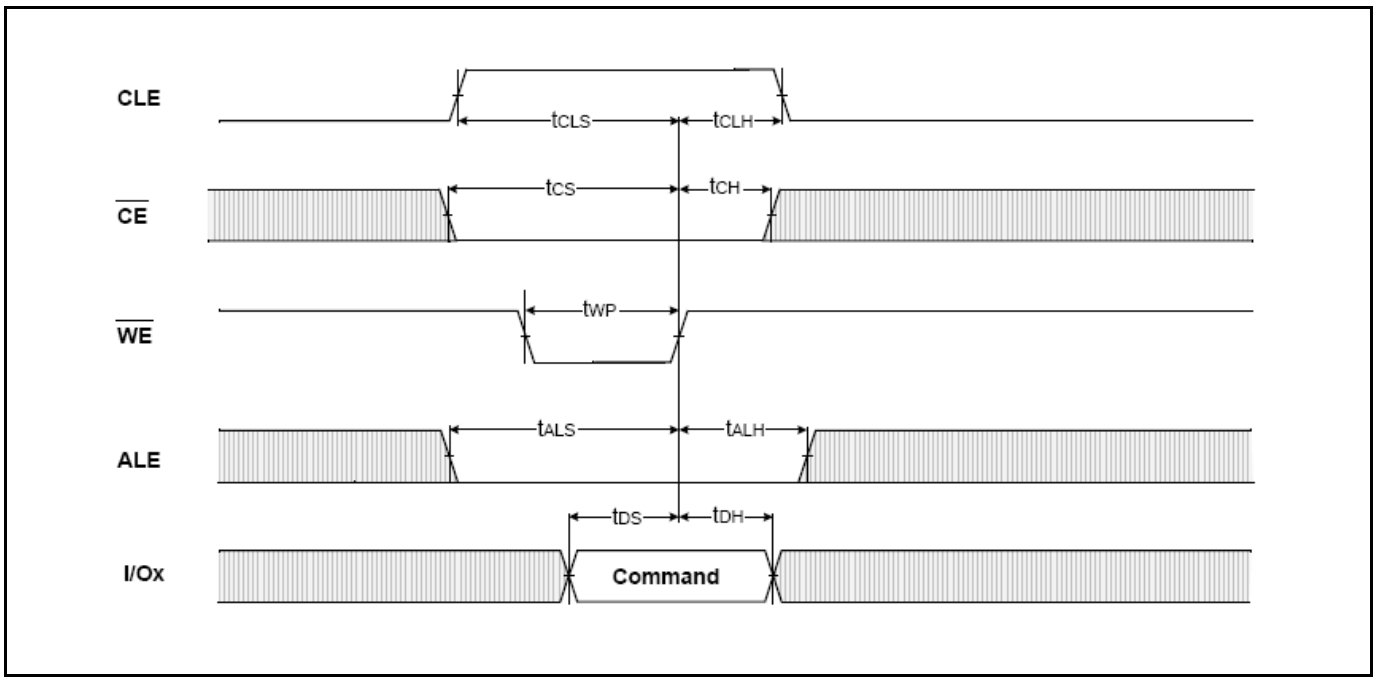


Figure 5: Address Latch Cycle Timing

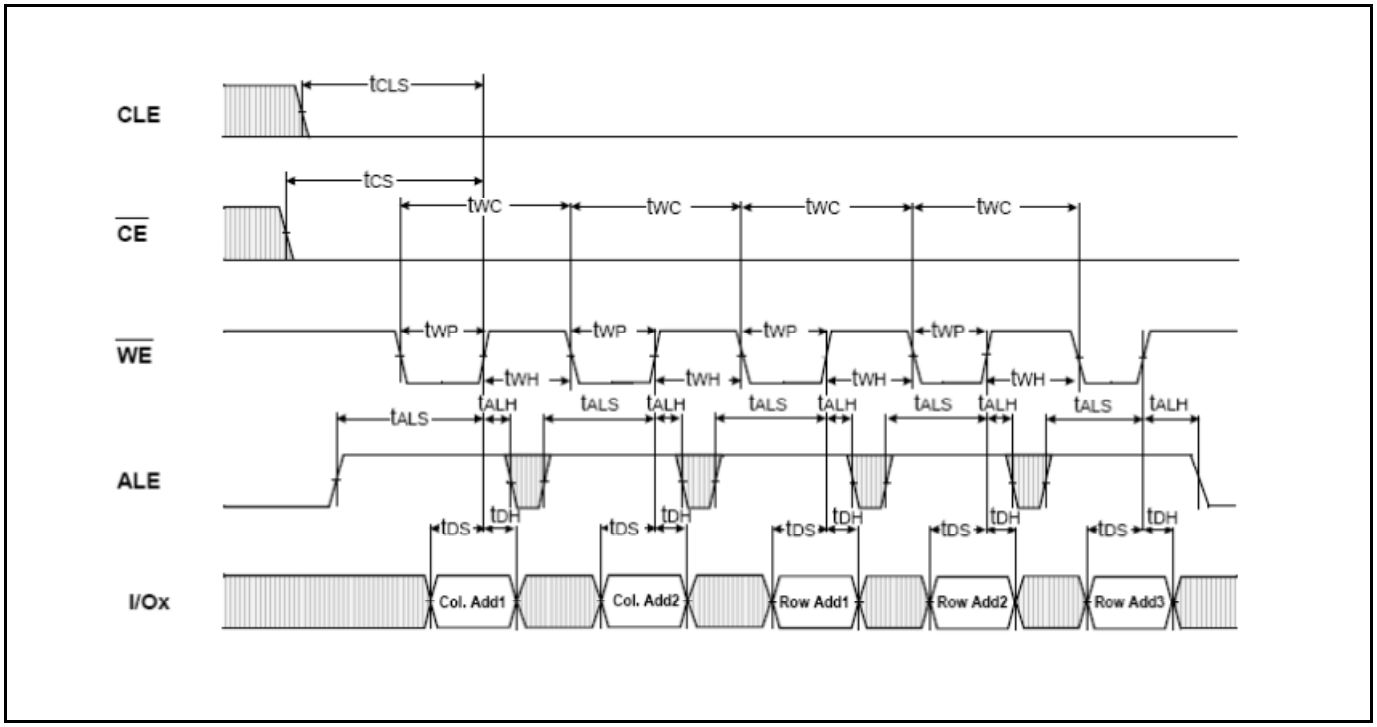


Figure 6: Input Data Latch Cycle Timing

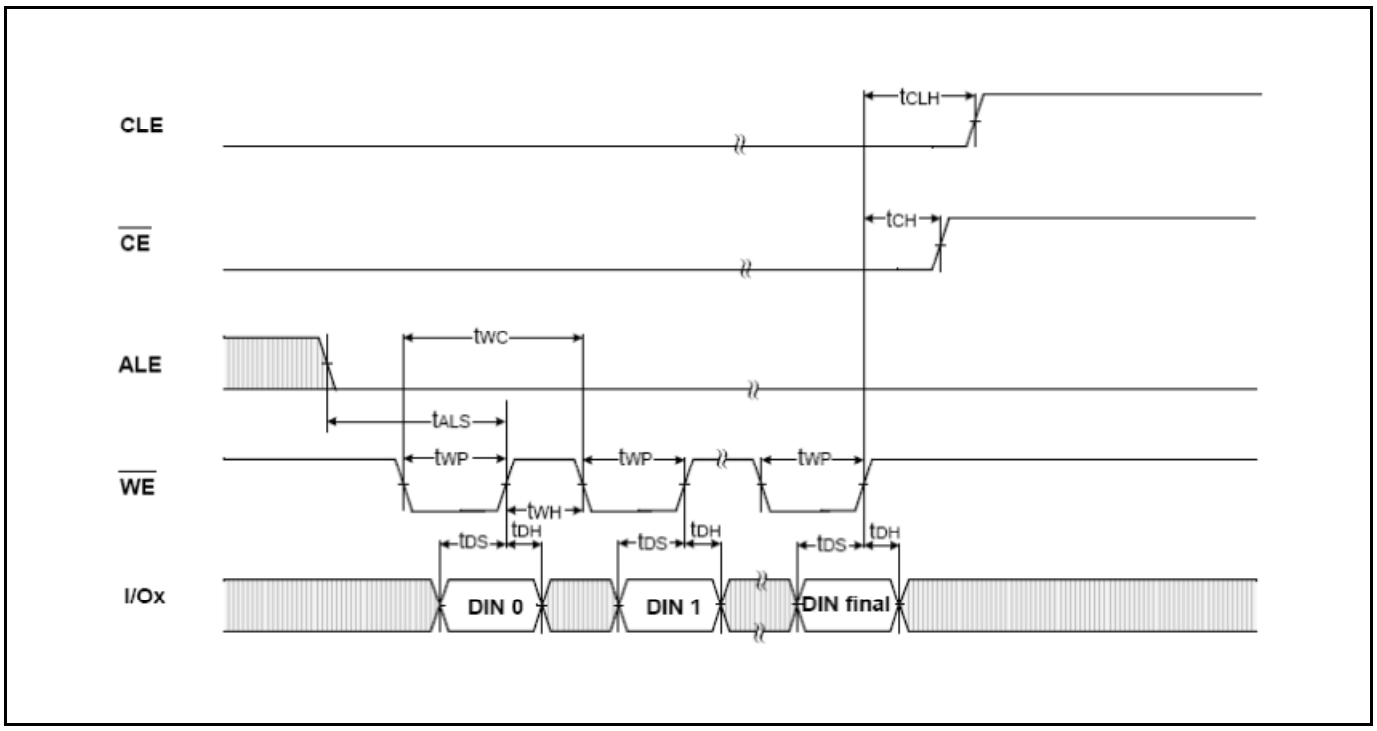
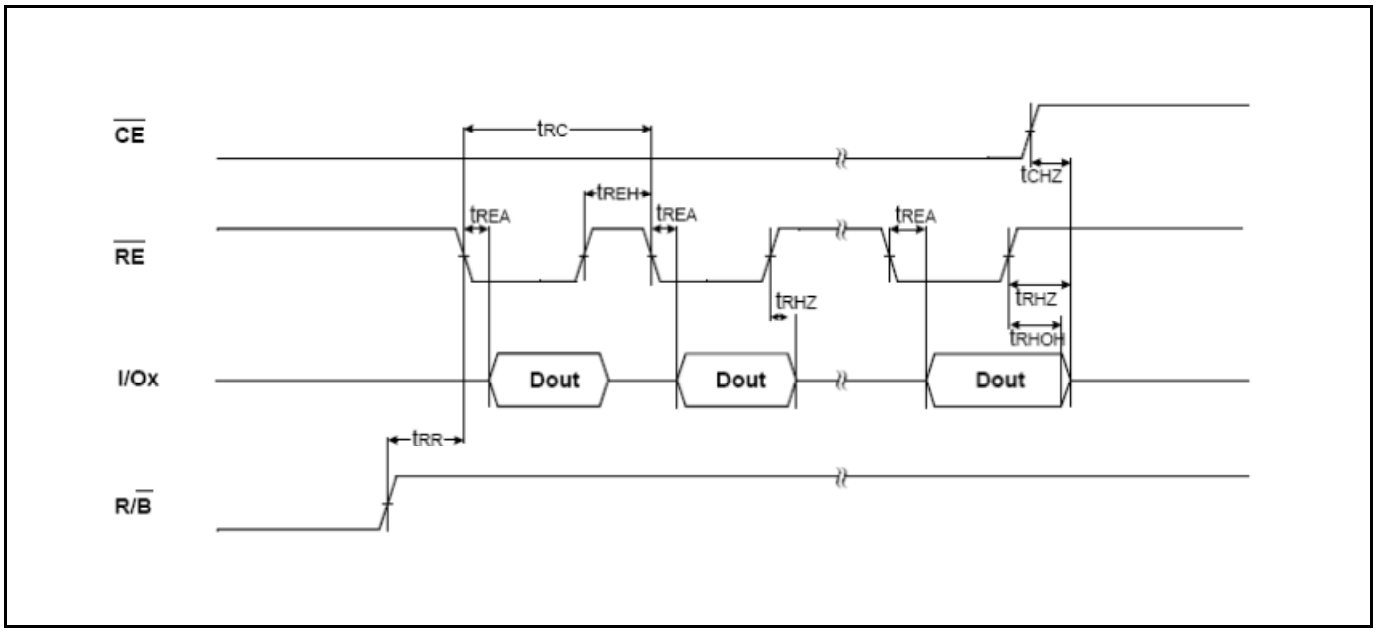


Figure 7: Serial Access Cycle after Read



3.2.2 Toggle NAND

Table 5: AC Timing Parameters for Toggle DDR NAND

Parameter	Symbol	Min	Max	Unit
CLE/ALE Setup Time	tCALS	1		tCK
CLE/ALE Hold Time	tCALH	1		tCK
DQS Setup Time for Data Input Start	tCDQSS	> 100		ns
CE Setup Time	tCS	> 20		ns
CE Hold Time	tCH	> 5		ns
Command/Address Setup Time	tCAS	1		tCK
Command/Address Hold Time	tCAH	1		tCK
Data Setup Time	tDS	0.5		tCK
Data Hold Time	tDH	0.5		tCK
Write Cycle Time	tWC	2		tCK
WE High Pulse Width	tWH	1		tCK
WE Low Pulse Width	tWP	1		tCK
Read Cycle Time	tRC	2		tCK
RE High Pulse Width	tREH	1		tCK
RE Low Pulse Width	tRP	1		tCK
Data Strobe Cycle Time	tDSC	2		tCK
DQS Input Low Pulse Width	tDQSL	1		tCK
DQS Input High Pulse Width	tDQSH	1		tCK
Read Preamble	tRPRE	2		tCK
Read Postamble	tRPST	> 100		ns
Read Postamble Hold Time	tRPSTH	> 100		ns
Write Preamble	tWPRE	> 83		ns
Write Postamble	tWPST	> 83		ns
Write Postamble Hold Time	tWPSTH	> 5		ns

Figure 8: Toggle NAND Command Latch Cycle Timing

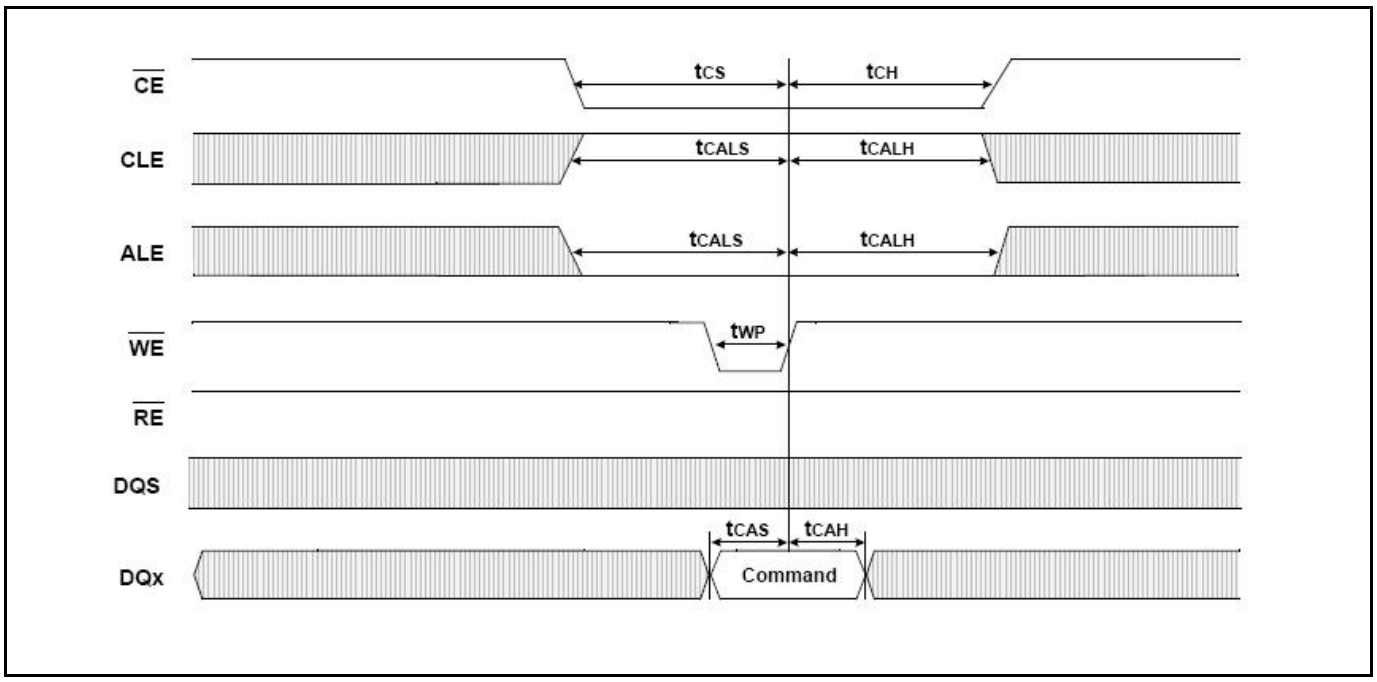


Figure 9: Toggle NAND Address Latch Cycle Timing (1)

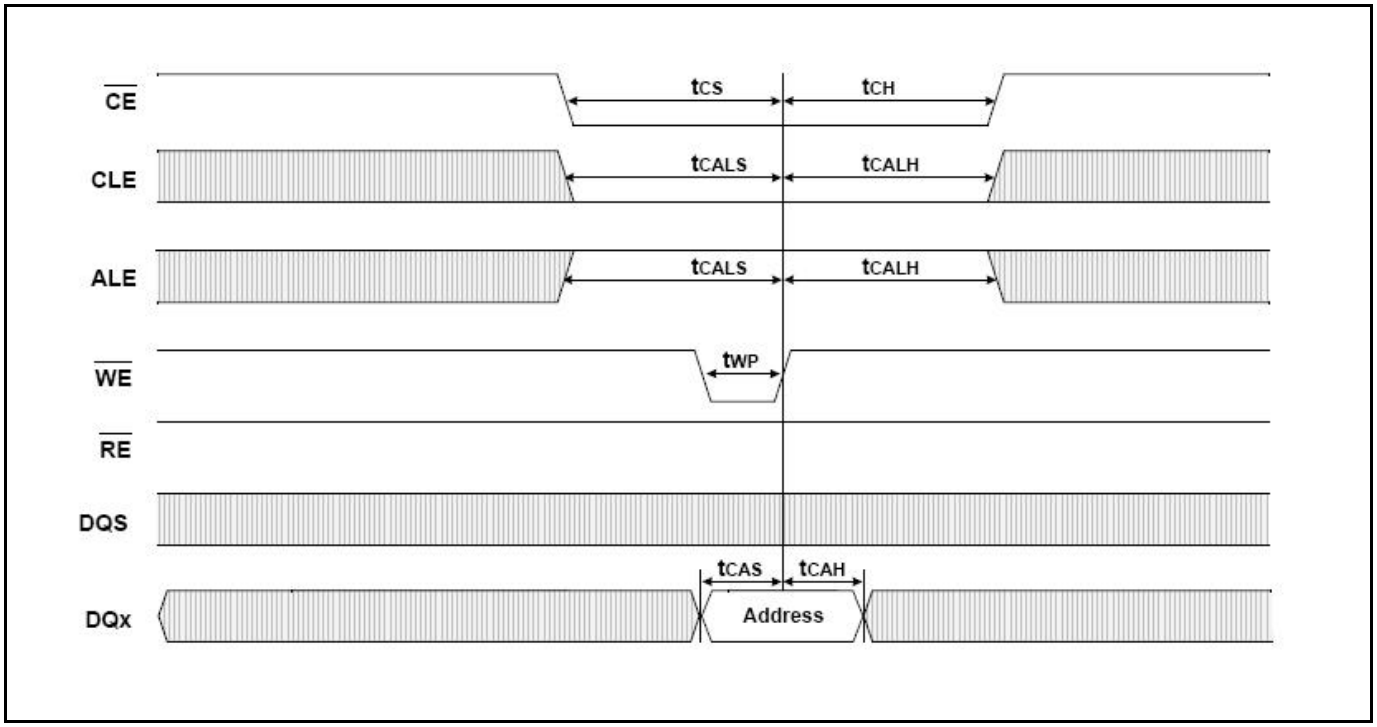


Figure 10: Toggle NAND Address Latch Cycle Timing (2)

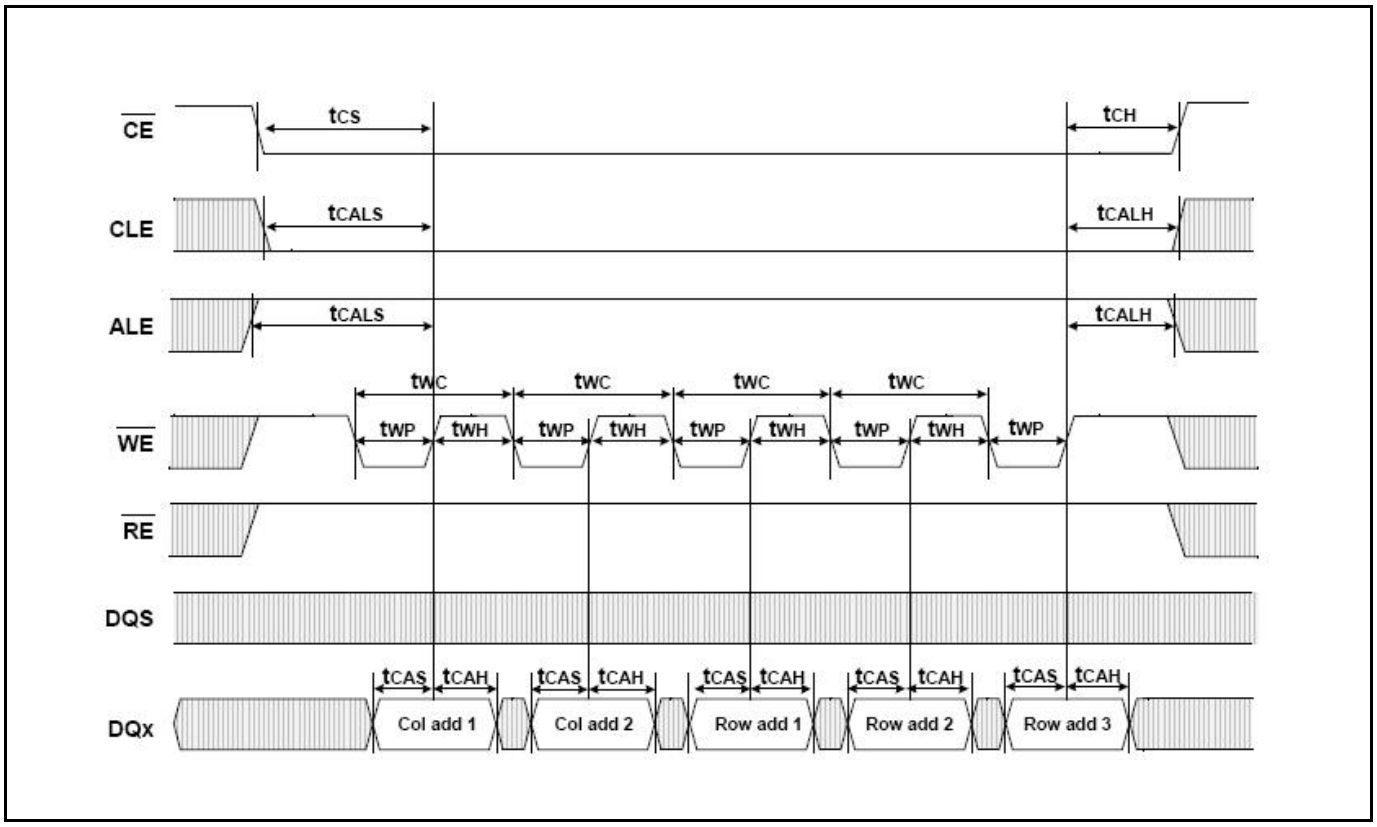


Figure 11: Toggle NAND Output Data (Write) Cycle Timing

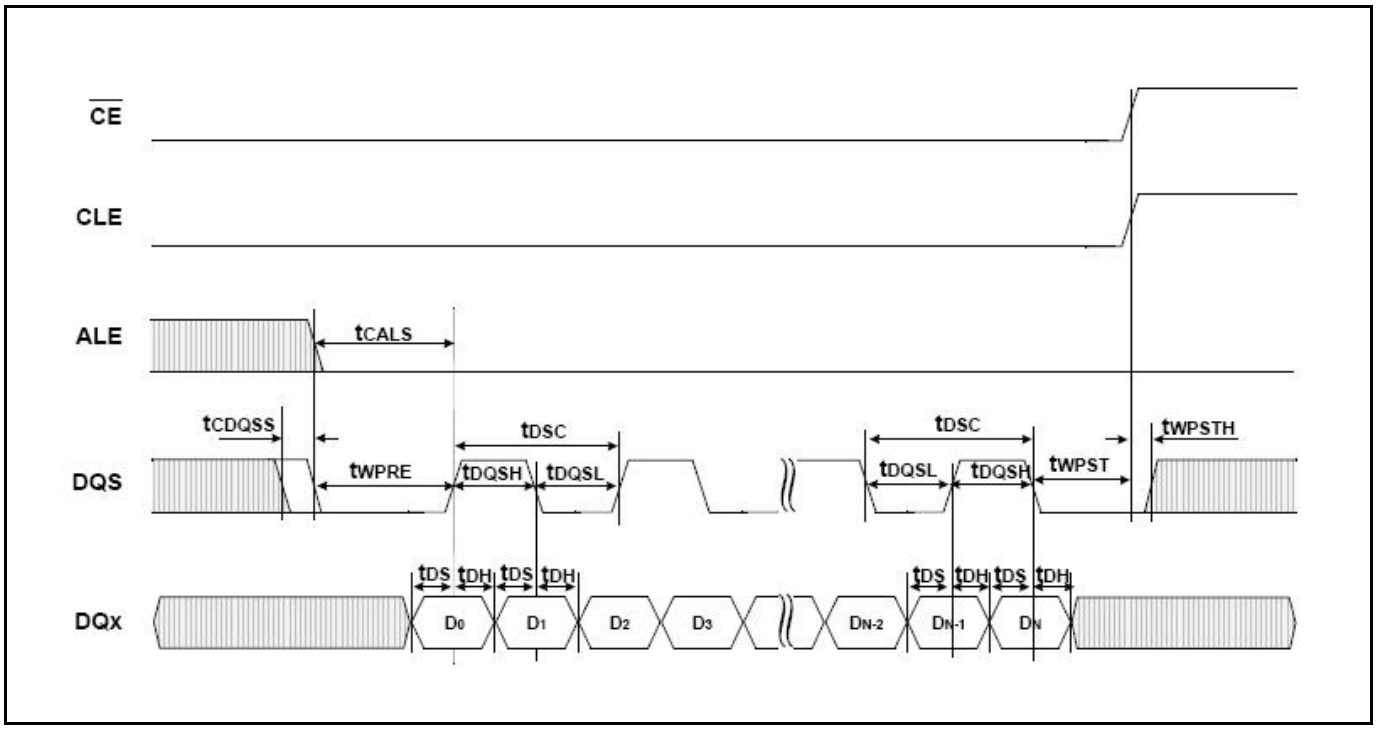
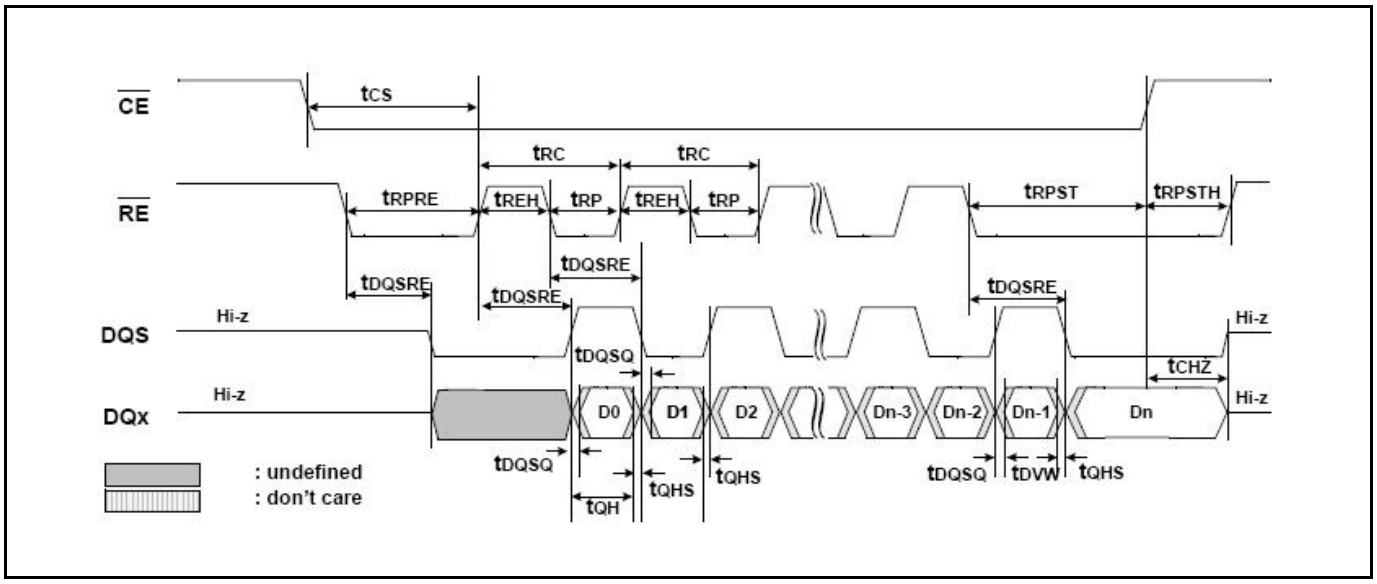
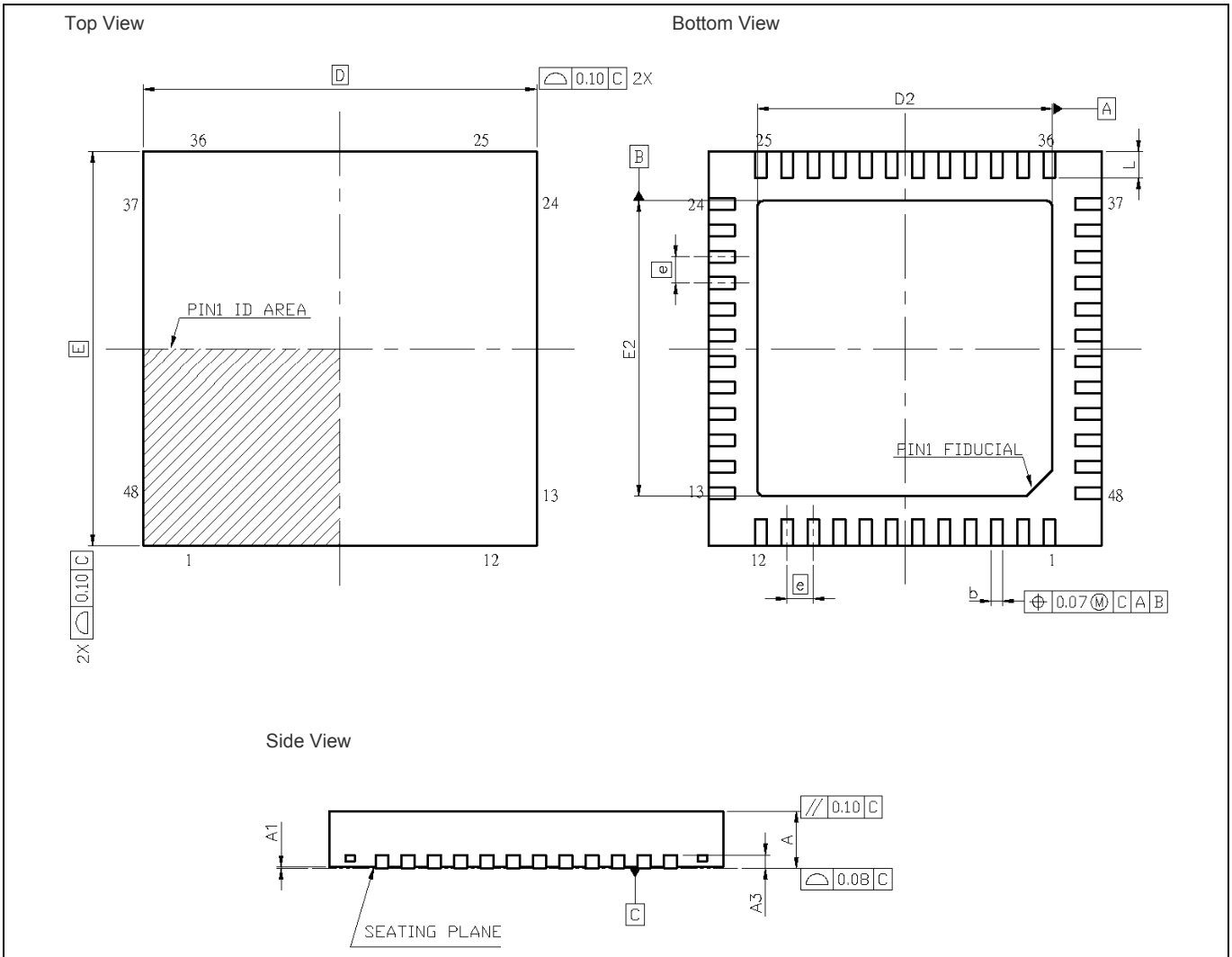


Figure 12: Toggle NAND Input Data (Read) Cycle Timing



4. Package Information

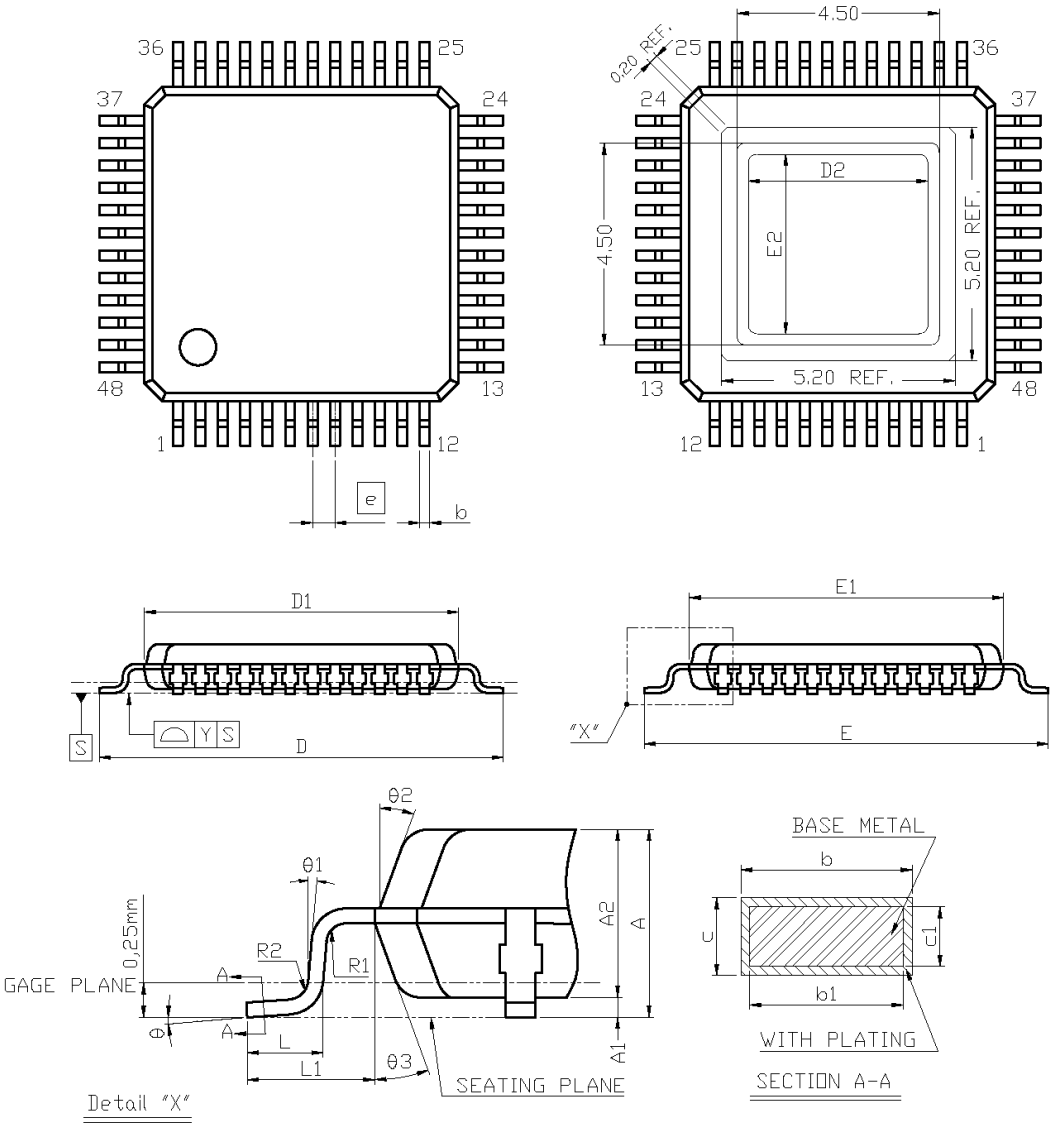
4.1 48-Pin QFN Package Outline



SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90	D2	4.40	4.50	4.60
A1	0	0.02	0.05	E	5.90	6.00	6.10
A3	0.203 REF			E2	4.40	4.50	4.60
b	0.15	0.20	0.25	e	0.40 BSC		
D	5.90	6.00	6.10	L	0.30	0.40	0.50

Notes:
1. All dimensions are in Millimeters.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Refer to JEDEC Standard MO-220 issue “K” WJJE.
4. Leadframe material is OLIN194 and thickness is 0.203 mm (8 Mil).

4.2 48-Pin E-LQFP Package Outline



SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	---	---	1.60	E2	3.9	4.0	4.1
A1	0.05	---	0.15	e	0.50 BSC		
A2	1.35	1.40	1.45	L	0.45	0.60	0.75
b	0.17	0.22	0.27	L1	1.00 REF		
b1	0.17	0.20	0.23	R1	0.08	---	---
c	0.09	---	0.20	R2	0.08	---	0.20
c1	0.09	---	0.16	Y	---	---	0.075
D	8.9	9.0	9.1	θ	0°	3.5°	7°
D1	6.9	7.0	7.1	θ1	0°	---	---
D2	3.9	4.0	4.1	θ2	11°	12°	---
E	8.9	9.0	9.1	θ3	11°	12°	13°
E1	6.9	7.0	7.1				

Notes:

1. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side D1 and E1 are maximum plastic body size dimension including mold mismatch.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm.
3. All dimensions are in millimeters.
4. Exposed pad 4.0 x 4.0 mm.

4.3 Top Marking

Figure 13: Top Marking of 48-Pin QFN

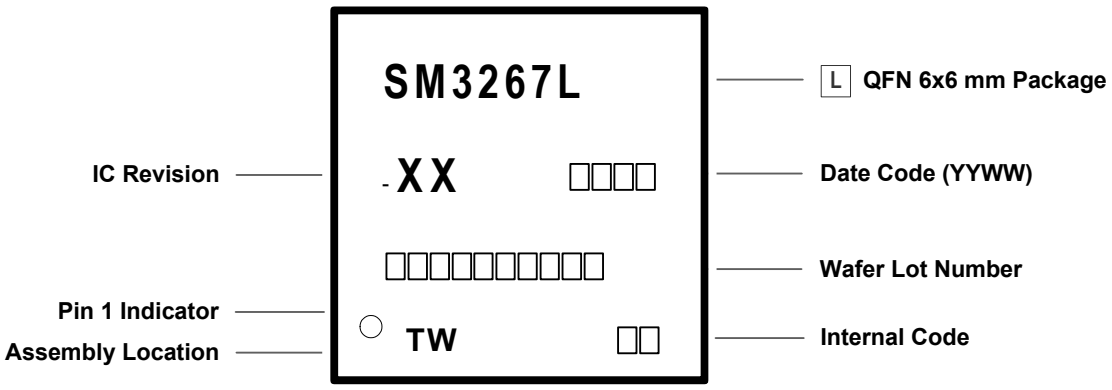
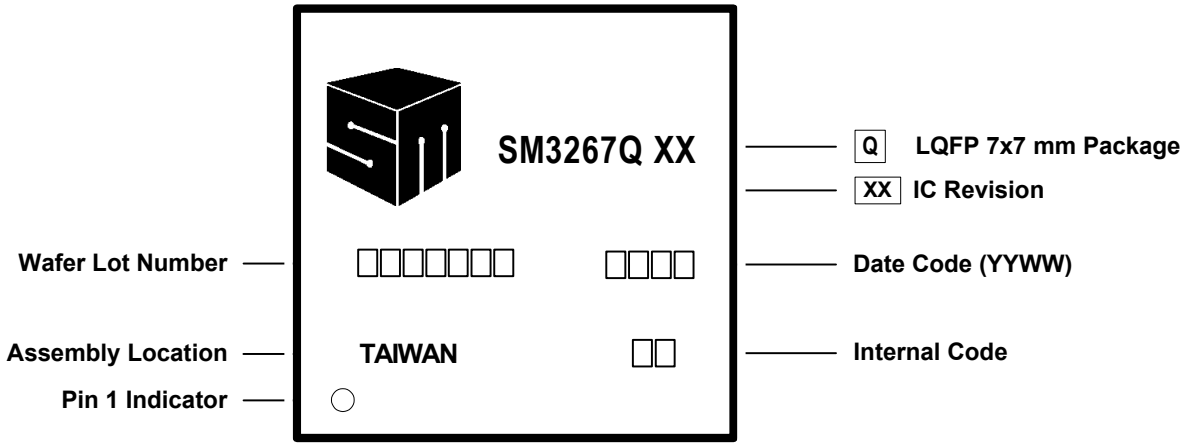


Figure 14: Top Marking of 48-Pin E-LQFP



5. Product Ordering Information

Table 6: Ordering Information

Ordering Number	Operating Temperature	Package Type	Dimension
SM326LX070000-XX	0°C ~ 70°C	48-pin QFN	6 x 6 x 0.9 (mm)
SM326QX070000-XX	0°C ~ 70°C	48-pin E-LQFP	7 x 7 x 1.4 (mm)

Note: The suffix “XX” denotes the IC revision.