



המכללה האקדמית להנדסה סמי שמעון

המחלקה להנדסת חשמל ואלקטרוניקה

מערכת תקשורת אלחוטית של שליטה מרחוק בטכנולוגיית VLSI
Wireless communication system of remote control in VLSI
technology

פרויקט הנדסי

דו"ח מכין פרויקט גמר

הוכן לשם השלמת הדרישות לקבלת
תואר ראשון בהנדסה B. Sc

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תאריך לועזי

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חתימת הסטודנט: _____

חתימת המנחה: _____

אישור ועדת הפרויקטים: _____



המכללה האקדמית להנדסה סמי שמעון

המחלקה להנדסת חשמל ואלקטרוניקה

**עמוד אופציונלי - הפרויקט ההנדסי נעשה בשיתוף עם שם החברה/מפעל
בהנחיית תוארו המקצועי ושם המנחה הנוסף – אם קיים**

יש להכניס את העמוד בספר הסופי בלבד.

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מיקרומחשבים, מעגלים אלקטרוניים (Microelectronics)

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RF (Radiofrequency)

עיבוד אותות (Signal Processing)

עיבוד תמונות ווידאו (Image and Video Processing)

מערכות הספק אלקטרוניות (Electronic Power Systems, Power Electronics)

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המחלקה להנדסת חשמל ואלקטרוניקה

עמוד אופציונלי – הקדשה (בספר הסופי בלבד)

ל.....
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המכללה האקדמית להנדסה סמי שמעון

המחלקה להנדסת חשמל ואלקטרוניקה

עמוד אופציונלי – הבעת תודות (בספר הסופי בלבד)

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תקציר

מערכות שליטה מרחוק ממלאות תפקיד בתעשיות שונות כגון צבא, רפואה ותחבורה על ידי מתן שליטה ממקומות מרוחקים. פרויקט זה מתמקד ביישום מערכת שלט רחוק באמצעות כרטיסי FPGA וממשק בקרה באמצעות פיתון. הדו"ח מתחיל בחקירה של היסודות התיאורטיים של מערכות שלט רחוק. לאחר מכן הוא מתאר את דרישות המערכת הכוללות מרחק שידור, זמני תגובה של המערכת וזיהוי שגיאות. כחלק מסקירת הספרות, ניתנים הסברים מפורטים לגבי הידע הדרוש לתכנון ובניית המערכת. על מנת לפתח מערכת כזו יש צורך להשתמש בשני בקרי FPGA והתקנים חיצוניים שיפורטו בהמשך. פרויקט זה נועד להציג את היישום המעשי של מערכות שליטה מרחוק המשתמשות בטכנולוגיית FPGA, תוך עמידה בקריטריונים ביצועיים ותרחיש העולם האמיתי.



המכללה האקדמית להנדסה סמי שמעון

המחלקה להנדסת חשמל ואלקטרוניקה

Abstract

Remote control systems fulfill roles in various industries such as military, healthcare, and transportation by providing control from distant locations. This project focuses on implementing a remote-control system using FPGA cards and control interface through Python. The report begins with an investigation of the theoretical foundations of remote-control systems. It then describes the system requirements including transmission distance, system response times, and error detection. As a part of literature review, detailed explanations are provided regarding the knowledge required for system design and construction. In order to develop a system that meets response time requirements, utilizes error detection polynomials, and determines transmission distance, the use of two FPGA controllers and external devices will be detailed further. This project system aims to demonstrate the practical application of remote-control systems utilizing FPGA technology, with a focus on meeting performance criteria and real-world scenarios.

Contents

1. Introduction	1
1.1 Communication	1
1.2 Wire Communication	1
1.2.1 Wireless Communication and Wireless Communication System	2
1.2.2 VLSI Technology in Wireless Communication System	3
1.3 FPGA	3
1.4 Project Description and Requirements	4
2. Literature Review	5
2.1 FPGA	5
2.2 Control System	7
2.3 Serial and Parallel Communication	7
2.4 UART Communication	8
2.5 BiPhase	9
2.6 CRC	10
3. Conclusion	11
4. References	12

List of Figures

Figure 1.1 Basic elements of telecommunication [1].....	1
Figure 1.2 Basic block diagram of communication system.....	3
Figure 1.3 FPGA Board (top view).....	4
Figure 2. 1 General architecture of FPGA [10]	5
Figure 2. 2 General architecture of CLB [10].....	6
Figure 2. 3 Block diagram of a closed-loop control system [12].....	7
Figure 2. 4 Biphase waveforms- biphase-S [16]	9

List of Tables

Table 1.1 Differences between wireline and wireless channels [1]..... 2

1. Introduction

In this chapter we will discuss the understanding of the general background in which the system deals, a control communication system based on FPGAs controllers. The purpose of the system according to its requirements and a general description of a system.

1.1 Communication

Communication has been an essential aspect of human interaction and technological systems for centuries. Before the advent of wireless communication, traditional methods heavily relied on physical mediums such as electrical conductors and optical fibers for the transfer of information. In telecommunication, the exchange of data occurred through these guided channels, establishing a network of connected points. Devices like television, radio, telephones, and mobile phones, connected through networks, facilitate widespread communication. The aim remains transferring information between geographically separated users, creating an exchange of information across distances, whether through voice, real-world images, or digital data, harnessing the sensory capabilities of eyes and ears [1]. An example illustrating the transfer of information between users is shown in Figure 1.1:

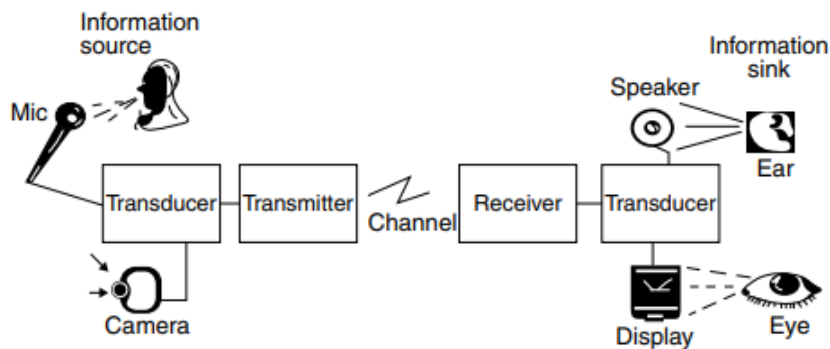


Figure 1.1 Basic elements of telecommunication [1]

1.2 Wire Communication

Optical fibers, known for their ability to transmit data through pulses of light, offer vast bandwidth, targeted user connections, low transmission loss, and extended relay distances. However, are sensitive to physical damage, potentially disrupting communication channels. Additionally, are more challenging and costly to install and maintain, especially in remote or difficult-to-reach locations. Due to these hurdles, in certain cases, it is preferable to utilize wireless communication [2]. An example of comparison between wired and wireless channels is shown in Table 1.1:

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Wireless communication	Wire-line communication
Air channel is used as the medium, which is a public channel	Generally, copper wire or fiber optic cables are used as medium and these are private channels (belonging to operator)
Signal is transmitted as electromagnetic waves	Signal is transmitted as electrical signal
The characteristic of air channel varies frequently with respect to time and frequency; the channel is unpredictable most of the time	The characteristic of wire channel does not vary much with respect to time (for example, over a long period of time, it is almost constant)
Channel loss is more	Channel loss is less
Generally receiver is mobile	Receiver is stationary
Generally the channel is characterized by Rayleigh, Rician distribution	Generally channel is characterized by AWGN
Security is a major threat	As the lines belong to specific operators, so although security is a major concern, it is less severe than wireless channel, where anyone can eavesdrop into the public air channel

Table 1.1 Differences between wireline and wireless channels [1]

1.2.1 Wireless Communication and Wireless Communication System

Wireless communication involves the transmission of information between two or more points without the need for a continuous guided medium. Instead, it harnesses electromagnetic waves, particularly radio waves, to enable communication. Radio waves are used as a means of conveying information between the transmitter and the receiver of a wireless communications system.

Simple wireless communication system consists of several key components that work together to transmit and receive information wirelessly. The transmitter component generates the information (voice, data, etc.) to be transmitted, modifies the signal to be suitable for wireless transmission. This may involve changing the frequency, amplitude, or phase of the signal and converts the electrical signal into electromagnetic waves for transmission into the air. The channel is the air or free space through which the electromagnetic waves travel from the transmitter to the receiver. The receiver component captures the incoming electromagnetic waves, extracts the original signal from the received modulated waveform, enhances the received signal, filtering out noise and interference, decodes the information for further processing and in the end delivers the reconstructed information to the destination or end-user [1], [3]. An example illustrating the simple wireless communication system is shown in Figure 1.2:

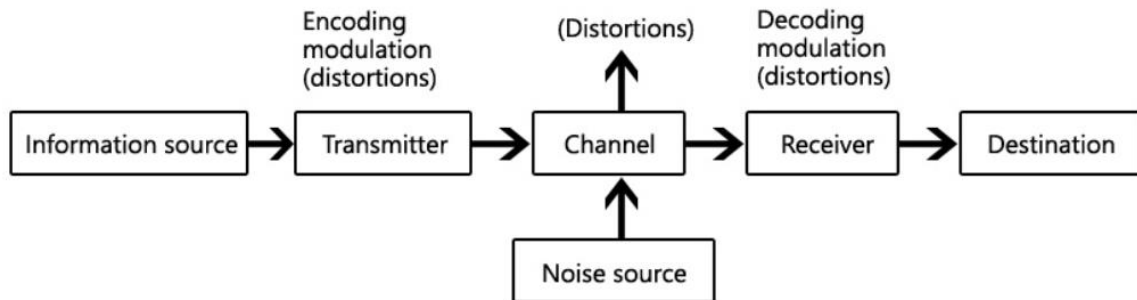


Figure 1.2 Basic block diagram of communication system

1.2.2 VLSI Technology in Wireless Communication System

Integrated Circuits, commonly referred to as Very Large-Scale Integration (VLSI) chips, wield significant control over an extensive array of devices in our external environment. These electronic systems are embedded within a small volume of processed silicon. They govern the functionalities of diverse technologies, ranging from IP routers managing Internet traffic, personal computers, and smartphones to the intricate components of car engines and everyday household appliances [4]. VLSI involves the integration of numerous electronic components onto a single chip, allowing for compact, energy efficient and high-performance implementations. In the context of wireless communication system, VLSI chips can be dedicated to handling tasks such as modulation, demodulation, encoding, decoding and signal processing [5], [6], [7].

1.3 FPGA

Field programmable gate array (FPGA) is a type of digital integrated circuit chip that provides reconfigurable parallel processing capability, this feature allows multiple machines to work together seamlessly in real time, thanks to powerful and flexible control functions, can be programmed in the field after production using hardware description languages such as Verilog or VHDL, and has three basic building blocks: logic gates, flip-flops + memories, and wires [8], [9]. An example of FPGA board is shown in Figure 1.3:

MAX10 10M50DAF484

USB Blaster II

ADC Header

WS2812B 3-pin RGB LED Expansion Header x2

WS2812B RGB LED x4

JTAG

LED x4

Switch x4

5V Input 2-pin Header (Reserved)

2x6 TMD Header

Key x2

1.4 Project Description and Requirements

The project is to develop a wireless remote-control system utilizing two FPGA MAX 10 cards, a laptop computer, STX882 transmitter, SRX882 receiver, CC1101 transceiver and USB transformation TTL adapter. one card will be connected to the computer in a wired manner through an adapter to receive information. The first card will wirelessly transmit the information received to the second card using the STX/SRX882 for short-distance communication and CC1101 for long-distance transmission. The received information on the second card will be showcased through LEDs and RGB LEDs, serving as a control mechanism.

The objective is to create the system described above when following the requirements below: A wired interface between a computer and an FPGA through communication protocol. Additionally, wireless communication is utilized for contactless data transfer between two FPGAs. Error-checking mechanisms, like CRC. A mobile interface, either computer-based or through an app, is developed for remote system control. The system will support short to long-range wireless transmission, spanning from a few meters to kilometers. Real-time operation, considering latency from both wired and wireless communication. Lastly, LEDs on the FPGAs provide visual feedback.

In the next chapter we will learn about tools for understanding the system. We will introduce FPGA controllers and their uses, we will learn about serial and parallel communication and their protocols, uses and presentation of different methods of signal decoding/encoding and error checking. In later chapters, we will implement and test the entire system.

2. Literature Review

As we mentioned, our project is built from two FPGA cards that communicate between them effectively, which simulates a remote-control system using FPGA, to understand the continuation of the project, we must get to the details of the following topics:

2.1 FPGA

FPGAs are semiconductor structures composed of a matrix of configurable logic blocks (CLBs) interconnected via programmable links. Unlike Application-Specific Integrated Circuits (ASICs), which are tailor-made for specific applications, FPGAs offer post-manufacturing re-configurability to suit various functionalities. These devices consist of configurable logic blocks (CLBs), input/output blocks (IOBs), and interconnection networks, forming the backbone of their flexible architecture. An example of General architecture of FPGA is shown in Figure 2.1:

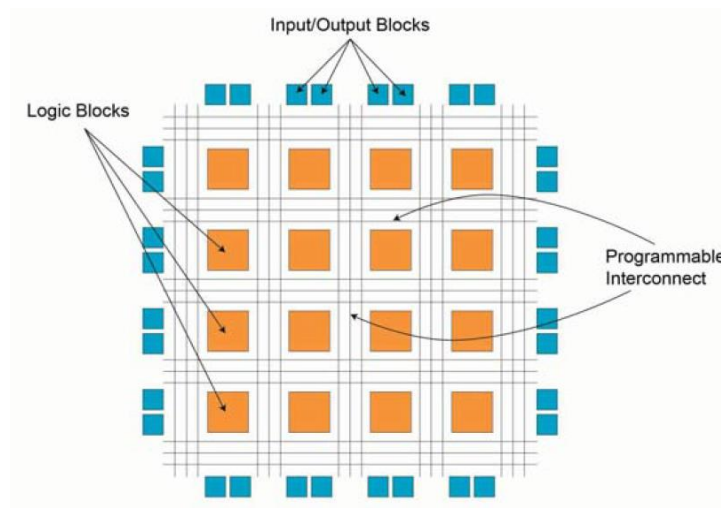


Figure 2. 1 General architecture of FPGA [11]

CLBs execute complex logic functions, implement memory functions, and synchronize code on the FPGA. They consist of flip-flops (FFs), look-up tables (LUTs), and multiplexers (MUX), enabling diverse logic implementations. FFs store logic states, LUTs provide fast output retrieval, and MUX selects inputs, collectively facilitating efficient FPGA functionality. This architectural understanding is crucial for leveraging FPGA capabilities effectively in various applications, including robotic computing. An example of General architecture of CLB is shown in Figure 2.2:

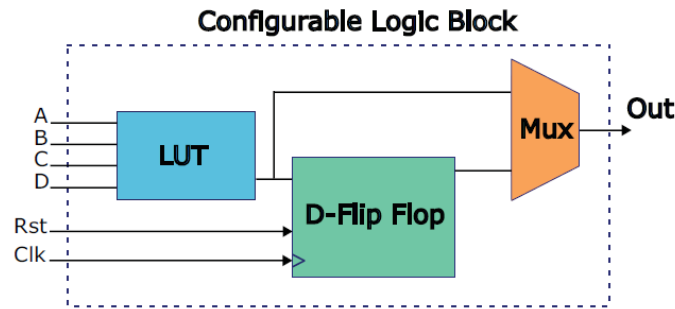


Figure 2. 2 General architecture of CLB [11]

IOBs act as bridges between FPGAs and external devices, enabling seamless data and control signal exchange. Programmable Interconnects encompass a network of wires and configurable switches responsible for establishing connections between CLBs and other internal components within the FPGA.

Reprogrammability is a standout feature of FPGAs, enabling quick iteration and testing of designs without expensive fabrication processes.

Modern FPGAs come in various types - Static Random Access Memory (SRAM) is a type of semiconductor memory characterized by its fast access times and volatile nature, meaning data is retained only as long as power is applied. Organized into a matrix of rows and columns, each cell typically stores one bit of data. SRAM supports both read and write operations and field reprogrammability. Antifuse FPGAs, are one-time programmable and have complex fabrication processes. Flash-based FPGAs, while non-volatile and reprogrammable, are not recommended for runtime reconfiguration due to potential destructive effects from radiation [11], [12].

2.2 Control System

A control system, one of the fields that can be implemented with FPGA, is a mechanism designed to regulate or manage the behavior of a system. The control system monitors the output of a process and adjusts the input to maintain a desired state. This often involves a feedback loop where the system continuously compares actual output with the desired output and takes corrective actions. An example of closed loop control system block diagram is shown in figure 2.3:

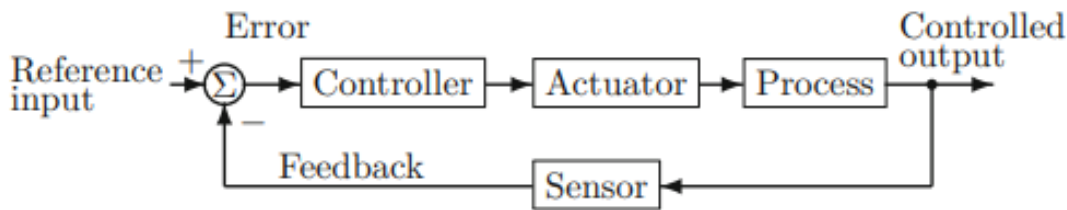


Figure 2. 3 Block diagram of a closed-loop control system [13]

Control systems managing communication systems that utilize wave frequencies, regulate signal transmission, reception, and processing to communication. In wave frequency communication, control systems help with tasks like signal modulation, amplification, and noise reduction. They adjust parameters like frequency, phase, and amplitude for signal transmission and reception.

Transducers convert electromagnetic waves into electrical signals and vice versa, enabling the integration and manipulation of signals between the physical and electronic domains. Closed-loop control systems continuously monitor feedback signals to make real-time adjustments, ensuring the system adapts to changing conditions such as signal strength or interference [13].

2.3 Serial and Parallel Communication

Serial communication, facilitated by Universal Asynchronous Receiver-Transmitter (UART) controllers, enables bidirectional data exchange between the Systems-on-Chip and external peripherals. These controllers support full-duplex communication, allowing simultaneous transmission and reception of data. They handle the conversion of parallel data from the CPU into serial format for transmission and vice versa. Parallel communication complements serial communication by providing high-speed bidirectional data transfer capabilities. Parallel protocol controllers implement synchronous control patterns and handshake signals to enable data exchange with peripherals [14].

2.4 UART Communication

UARTs, allowing the transmission of parallel data over a serial line. Typically, UARTs are employed alongside the Recommended Standard 232 standard, is a standard defining the electrical characteristics of interfaces between devices. It's commonly used for serial communication between computers and peripherals, which defines the characteristics of data communication equipment [15]. Voltage converter chip use to bridge the voltage gap between RS-232 and FPGA I/O pins. A UART comprises a transmitter and receiver, with the transmitter converting parallel data into serial format and the receiver performing the reverse operation. Data transmission commences with a start bit, is the initial component of a data frame and serves as a synchronization signal for the receiving device, it always has a logical value of '0'. When data transmission begins, the start bit indicates to the receiver that a new data frame is starting, allowing it to synchronize its internal clock with the incoming data stream. Followed by data bits, are the actual information being transmitted. These bits can vary in number, and they carry the binary representation of the data being sent. An optional parity bit for error detection, and stop bits, are marks the end of a data frame and provides a brief period of time for the receiving device to prepare for the next frame, it always has a logical value of 1. The baud rate, data bits, and stop bits must be agreed upon by both the transmitter and receiver beforehand, baud rate refers to the speed at which data is transmitted over the serial communication interface. It is the number of signal changes (or symbols) per second that the UART sends or receives, the commonly used baud rates are 2400, 4800, 9600, 19200 and 38400 up to 115200 bauds. To retrieve data at the receiver end, an oversampling scheme is utilized, estimating bit middle points to synchronize data reception. This oversampling scheme forms the basis for clock signal generation. The UART receiving subsystem comprises components for data retrieval via oversampling, which is 16, 24, and 32 for 1, 1.5, and 2 stop bits [16] .

2.5 BiPhase

Manchester encoding, a prominent biphas coding scheme. Biphas coding ensures clock recovery at the receiver's end. Since it guarantees a transition in the middle of each bit period, distinguishing between '1' and '0', the receiver can accurately extract the clock signal from the data stream. This helps maintain synchronization between the transmitter and receiver, adopts alternating phases within a single square wave cycle to denote binary digits.

Biphase-S works by encoding binary data into a waveform where each bit is represented by a transition within its interval. Specifically, a transition occurs at the beginning of each bit, and for a binary 0, a second transition takes place in the middle of the bit interval, while for a binary 1, there is no second transition. This encoding method performs timing information within each bit interval, enabling synchronization between the transmitter and receiver and clock recovery. The resulting waveform contains timing components due to the transitions, and the equal polarities of 0s and 1s eliminate DC wander. An example of Biphase waveforms - biphase-S is shown in Figure 2.3:

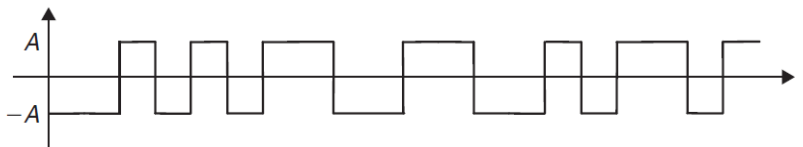


Figure 2. 4 Biphase waveforms- biphase-S [17]

Biphase-mark code introduces transitions at the start of each bit interval, with an additional transition at the midpoint for binary 1s, aiding in timing synchronization. Differential Manchester encoding enhances reliability by utilizing transitions to represent binary values, providing immunity to polarity reversals, and improving error detection. Additionally, hybrid schemes like code mark inversion (CMI) and differential mode inversion (DMI) combine biphase coding with other techniques, offering advantages such as energy and transmission in diverse communication environments [17].

In summary, biphase coding encompasses a range of encoding techniques, each with its own waveform characteristics and advantages. Despite variations in encoding rules and waveforms, these techniques share the common goal of enabling digital communication through precise timing synchronization.

2.6 CRC

Cyclic Redundancy Check codes employ Linear Feedback Shift Registers (LFSRs) to generate a signature based on the transmitted data, which can then be used to detect any modification or corruption of bits. Serial LFSRs generate one bit of output per clock cycle, but for high-speed applications.

CRC-8 is an error-detection technique used in digital data transmission or storage. It involves generating an 8-bit checksum based on the data being processed. The process starts with an initial value, typically all zeroes, and then each bit of the data is processed sequentially. For each bit, the CRC value is XORed with the data bit, shifted right by one bit, and XORed with a predefined polynomial, if the least significant bit was 1 before the shift. After processing all the data, the resulting CRC value serves as the checksum. When the data is received or read again, the CRC calculation is repeated, and if the calculated CRC matches the received CRC, it indicates that the data was likely transmitted or stored correctly. However, a mismatch suggests that an error occurred during transmission or storage. While CRC8 is for error detection, it cannot correct errors and its effectiveness depends on the chosen polynomial.

There are several Cyclic Redundancy Check (CRC) polynomials, notable examples include:

$$CRC8: P(x) = x^8 + x^2 + x^1 + 1 \text{ (HEX - 07)} \quad (2.1)$$

$$CRC12: P(x) = x^{12} + x^{11} + x^3 + x^2 + x^1 + 1 \text{ (HEX - 80F)} \quad (2.2)$$

$$CRC16: P(x) = x^{16} + x^{15} + x^2 + 1 \text{ (HEX - 8005)} \quad (2.3)$$

$$CRC32: P(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1 \text{ (HEX - 04C11DB7)} \quad (2.4)$$

These polynomials determine mathematical operations during CRC computation, significantly influencing error detection. When aligning the CRC polynomial with the system's specifications, if CRC8 yields an error rate sufficiently low for the system's requirements, there's no necessity to employ a higher CRC. The marginal decrease in error wouldn't justify the added complexity. Shift register operations are fundamental in hardware circuits implementing CRC computation. These operations involve shifting bits of the message and CRC register while performing XOR operations based on polynomial structures. [18], [19].

3. Conclusion

Wireless communication systems based on FPGA cards are useful for industries such as security, healthcare, automotive and others. So far, we have presented general knowledge about communication and wireless systems to understand the background of the project and the knowledge required for its implementation. In the future, the focus will be on creating a wireless communication system using FPGA cards as its core component. The goals will include designing hardware settings, system architecture, developing communication protocols and implementation simulations using VHDL. This system will allow wireless communication between two FPGA cards, marked as card A and card B, with Python as the operating interface.

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