Design of a 1.8V/3.3V 100Mbps GPIO Transmitter for Intel Max 10 FPGA

Thati Sethu Sumanth
VLSI
VEDAIIT
Hyderabad, India
sethusumanth08@gmail.com

G.VenkataMallikarjjuna Reddy
VLSI
INVECAS
Hyderabad, India
venkatamallikarjunareddy.ganda@invecas.com

A.Subha Kumar Reddy
VLSI
VEDAIIT
Hyderabad, India
subhakumarreddy.ankireddypalli@vedaiit.com

2022 IEEE Fourth International Conference on Advances in Electronics, Computers and Communications (ICAECC) | 978-1-6654-0239-2/22/$31.00 ©2022 IEEE | DOI: 10.1109/ICAECC54045.2022.9716630

***Abstract*—This paper presents the design of 1.8V/3.3V 100 Mbps General Purpose Input/Output (GPIO) transmitter for an Intel Max 10 FPGA. This transmitter works for both 1.8V and 3.3V IO supplies. The building blocks of this transmitter are level shifter and driver circuits. The level shifter is designed to level up the data levels from 0.8V to 1.8V/3.3V. A progressive sized driver circuit is designed to drive 50Ω termination resistance and the load capacitance of 5pF as per the requirement of Intel Max10. The overall design is carried out with 22nm technology node on cadence virtuoso platform and is simulated across PVT. The simulation results shows that the proposed design supports up to a data rate of 100Mbps with a power consumption of 1.59mW at 1.8V supply and with a power consumption of 2.93mW at 3.3V supply.**

Keywords—GPIO, Intel Max 10, Virtuoso, PVT, Transmitter.

I. INTRODUCTION

GPIO stands for General Purpose Input Output. It's a standard interface used to connect microcontrollers to other electronic devices. The voltage that the core circuit operates is different from the voltage applied at the input. It would be an ideal if a GPIO can be programmed to work with multiple voltages [1]. This paper deals with 1.8V as well as 3.3V by taking into account the stress effect and other lower node effects as the design is implemented in 22nm FDSOI [2] technology. The transmitter block is used in the communication from core circuitry to the output pin. The main blocks involved in the transmitter design are the level shifter, pre driver and main driver. The design of Pre driver depends on the load that the circuit can drive.

There are two forms of IO signaling schemes, they are single-ended signaling scheme and differential signaling scheme. In single-ended signaling scheme, the data transmits through the wire with reference to ground. In differential mode of signaling scheme, the data transmits through two wires in differential form such a way that the data transmitting in one wire is complementary to signals that are complementary are sent on a pair of wires and the voltage on one wire is measured with reference to the voltage at the other wire. This has the ability to reject common-mode noise..

The IO pins and IO buffers have several programmable features like single ended IO, differential IO etc and Intel Max 10 FGGA has many real time applications in the areas of industrial, medical and IOT.

The rest of the paper is organized as follows. Section-II describes the design of GPIO transmitter and its sub blocks along with their schematics. In Section-III simulation results of transmitter across process corners are presented with necessary explanations. In Section-IV, a conclusion is provided.

II. DESIGN OF GPIO TRANSMITTER

The basic block diagram of GPIO transmitter is shown in Fig.1. It receives input data from core domain which is sent to level shifter to level up input data to IO level. The levelled-up data is sent to driver in-order to drive the load capacitance of 5pF with termination impedance of 50Ω [6].

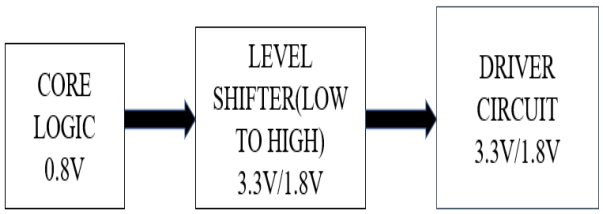

Fig.1 Block diagram of GPIO transmitter.

A. Level Shifter

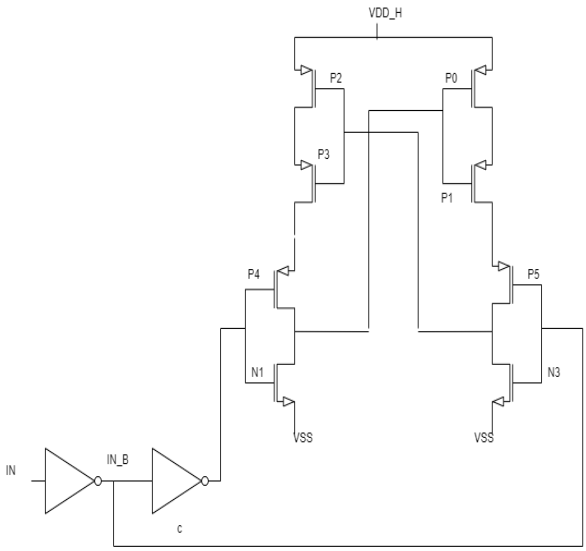

Fig.2 Level shifter schematic for 1.8V/3.3V

The input to GPIO transmitter comes from core domain operating at core supply of 0.8V. It cannot drive the main driver which can be operated at IO supply of 1.8V and 3.3V. Hence the input data to be level shifted to IO level.

The level shifter schematic designed for the transmitter is shown in Fig.2. The transistors P5, N3 are driven by IN_B and the transistors P4, N1 are driven by IN. When input is logic-0 N3 is ON and P5 is OFF. As gate of P2 is connected to drain terminal of N3, the ON N3 transistor forces the gate of P2 to logic-0, which turns ON the P2 transistor which makes the voltage at P2 drain terminal to go to logic-1. Similarly, as input is logic-0 P4 turns ON and N1 turns OFF. Now as the gate of P0 is connected to the drain terminal of N1, it forces gate of P0 to logic-1(P2 and P3 transistors are ON) which turns off P0 transistor and makes the voltage at P4 drain terminal to retain at logic -0.

The designed level shifter works for 1.8V as well as 3.3V. The stress effect is taken care such that the devices do not get any voltage greater than 1.8V between any two terminals of the device (gate-drain, gate-source and drain-source).

B. Driver

The level shifter alone cannot drive the load capacitance of 5pF, so a driver is designed for this purpose. The driver is a circuit which is used to drive the large capacitance loads by preserving the properties of input data.

The driver circuit can be implementable with a single stage buffer but it demands huge current to drive the large capacitance load [4]. Hence an alternative method called progressive sizing [3] is used in the design of driver and its schematic is shown in Fig. 3.

In this method the inverters are cascaded with increasing drive strength according to (1). Where A is sizing factor and N is number of stages, C_{IN} is the input capacitance and C_{OUT} is the output capacitance of last stage.

$$C_{IN} * A^N = C_{OUT} \quad (1)$$

As per the requirement for Intel Max 10 FPGA the driver need to drive a load capacitance of C_{Load} =5pF. The Input capacitance of first stage standard CMOS inverter is C_{IN} = 5fF. As per (1) the number of stages N is chosen as four and the sizing factor A is obtained as 5.68.

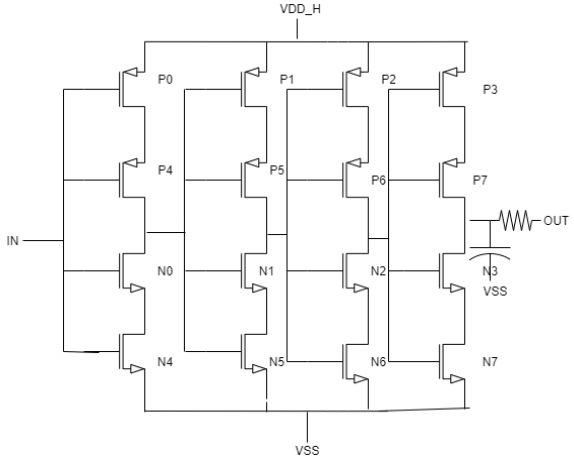

Fig.3 Driver schematic with progressive sizing to match output load capacitance.

Table1. Aspect Ratios of driver circuit

	First-stage	***Second-stage***	***Third-stage***	***Fourth-stage***
PMOS $(W/L)_{0,1,2,3}$	0.96 /0.2	5.76 /0.2	11.52 /0.2	66.66 /0.2
PMOS $(W/L)_{4,5,6,7}$	0.328 /0.2	1.968 /0.2	39.36 /0.2	44.608 /0.2
NMOS $(W/L)_{0,1,2,3}$	0.32 /0.2	1.968 /0.2	38.4 /0.2	43.52/0.2
NMOS $(W/L)_{4,5,6,7}$	0.32 /0.2	1.968 /0.2	38.4 /0.2	43.52/0.2

*All the aspect ratios are expressed in micrometer (μm) units

The aspect ratios of first stage CMOS inverter devices are selected as per the design of standard CMOS inverter (charging time is equal to discharging time). The aspect ratios of second stage CMOS inverter are sized up by A than its previous stage. Similarly, the third and fourth stages are sized up by A than their previous stages. The designed aspect ratios of all the devices are listed in Table1.

The overall power consumption is mainly dominated by the current consumed by the last stage of the driver. It needs to drive a large load capacitance of 5pF to meet 100Mbps data rate. The maximum current flowing through the load capacitor C_{Load} is given below.

$$I_{max} = C_{Load} * \left|\frac{dv_{out}}{dt}\right|_{max} \quad (2)$$

Here, $\left|\frac{dv_{out}}{dt}\right|_{max}$ is the maximum rate of change of the output data. Where dt is the rise-time / fall-time of output data (dt=1ns) and dVout is the difference between output data levels (1.8V/3.3V).

The I_{max} for 3.3V driver circuit is calculated below.

$$I_{max} = 5*10^{-12} *(3.3/10^{-9}) = 16.5mA \quad (3)$$

The I_{max} for 1.8V driver circuit is calculated below.

$$I_{max} = 5*10^{-12} *(1.8/10^{-9}) = 9\ mA \quad (4)$$

III. SIMULATION RESULTS

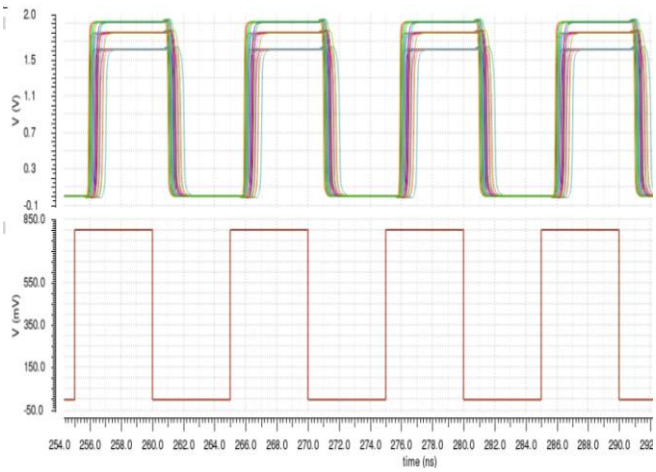

Fig.4 Simulation waveform of 1.8V level shifter across PVT

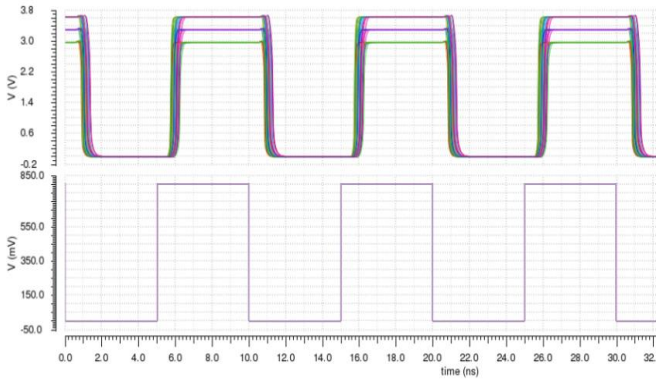

Fig.5 Simulation waveform of 3.3V level shifter across PVT

The proposed transmitter design is realized on cadence virtuoso platform with 22nm technology node. The simulations are carried out across process corners (ff_pre, fs_pre, sf_pre, ss_pre and tt_pre) , temperature T= -55^{0}C ,27^{0}C, 125^{0}C and voltage variations of +-10% for 1.8V and 3.3V.

The simulation waveforms of 1.8V and 3.3V level shifters for an incoming 0.8V data signal with 100Mbps data rate are shown in Fig.4 and Fig.5 respectively. From the simulations observed that the 1.8V level shifter leveled up the data to 1.789V and 3.3V level shifter leveled up the data to 3.27V for 1.8V and 3.3V respectively.

The eye diagrams of 1.8V/3.3V transmitter across PVT are shown in Fig 6 and Fig.7. The obtained eye-diagram specifications eye height and eye width along with power dissipation specifications for both 1.8V/3.3V transmitter are listed in Table 2. The obtained specifications are in compliance with Intel Max 10 FPGA

Table2. 1.8V/3.3V transmitter specifications

	Power Dissipation (mW)	Eye Height (V)	Eye Width (ns)
1.8V IO Transmitter	1.5971	1.799	4.789
3.3V IO Transmitter	2.93	3.297	4.768

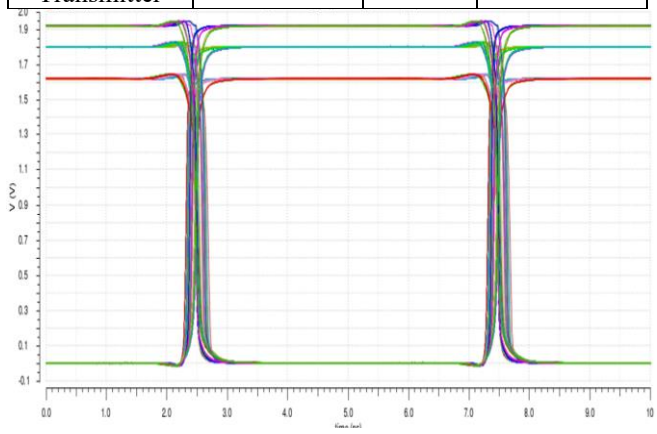

Fig.6 Eye diagram and Simulation waveform for1.8V across PVT

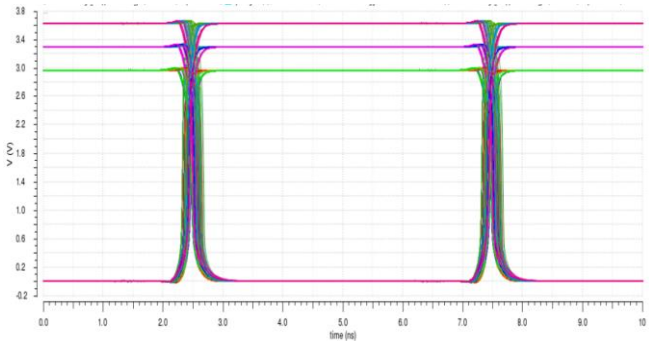

Fig.7 Eye diagram and Simulation waveform for3.3V across PVT

IV. CONCLUSION

In this paper, the design of GPIO transmitter for Intel Max 10 FPGA is presented. The proposed design is realized on cadence virtuoso platform with 22nm technology node. The obtained simulation results showed that this design is compliance with Intel Max 10 application and supports transmission rate up to 100Mbps with power consumption of 1.59mW and 2.93mW for 1.8V/3.3V transmitter.

REFERENCES

[1] R. Shrivastava and K. Sarawadekar, "Multi-Voltage GPIO Design and its Physical Implementation," 4th International Conference for Convergence in Technology SDMIT Ujire, Mangalore, India, 2018.

[2] B. Razavi , "Design of Analog CMOS Integrated Circuits" Tata McGraw Hill Editon 2002.

[3] R. J. Baker "CMOS Circuit Design Layout and Simulation" 3rd Edition 2010.

[4] S. Katare and N. Subramanya, "Configurable Hybrid Output Driver for GPIO with Voltage Range of 1.05V-3.70V,"IEEE 13th International Conference on ASIC (ASICON), 2019.

[5] "Intel MAX10 General Purpose I/O User Guide" Retrieved March 20, 2021 fromhttps://www.intel.com/content/www/programmable/us/en/pdfs/literature/hb/max -10/ug_m10_gpio.

[6] "Intel MAX10 FPGA Device Datasheet" Retrieved March 23, 2021 from https:// www.intel.com/content/dam/www/programmable/us /en/pdfs/literature/hb/max-10 /m10_datasheet.pdf.

.