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A New FPGA-based Real-Time Configurable System for Medical Image Processing

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***Abstract*—Given the importance of digital image processing and the significance of their implementations on hardware to achieve better performance, this paper reviews the advantages of using FPGA over softwares and DSPs as a platform for implementation of digital image processing applications. This work presents a hardware implementation of a FPGA-based real-time configurable system consisting of image processing low-level operators such as, contrast adjustment, brightness adjustment, inverting an image and pseudo-color operation. The paper presents a Verilog description of a real-time configurable system for digital image processing and focuses on medical images enhancement using this system. The solution provides an innovative hardware implementation and simulation, followed by immediate synthesis on FPGA.**

Keywords—digital image processing, Verilog HDL, reconfigurable hardware, image processing algorithms, real-time configurable system for digital image processing.

I. INTRODUCTION

Image processing is considered to be one of the most rapidly evolving areas of information technology, with growing applications in all fields of knowledge. It constitutes a core area of research within the computer science and engineering disciplines, given the interest of potential applications ranging from image enhancing to automatic image understanding, robotics and computer vision [1].

Implementing applications that involve different processes, such as image enhancement and object detection, could be easier on a general purpose computer, but not very time efficient due to additional constraints on memory and other peripheral devices. Hardware implementation of specific application offers much greater speed than a software implementation. With advances in the VLSI technology, hardware implementation has become an attractive alternative. Implementing complex computation tasks on hardware by exploiting parallelism and pipelining in algorithms yields significant reduction in execution times [2].

Also, to process the large amount of 3D data from medical instruments, intelligent high speed real-time systems have become imperative, which may process data before passing it to the human analyst [3].

Implementing image processing algorithms on reconfigurable hardware minimizes the time-to-market cost, enables rapid prototyping of complex algorithms and simplifies debugging and verification. Many image processing applications, especially medical image processing applications for object detection, require that several operations be performed on each pixel in the image resulting in an even large number of operations per second.

Reference [3] presents the advantages and limitations of FPGAs. The salient features of FPGAs that make them superior in speed, compared to conventional general-purpose hardware, are their greater I/O bandwidth to local memory, pipelining, parallelism and availability of optimizing compiler.

Therefore, FPGAs are an ideal choice for implementation of real time image processing. These reconfigurable devices have traditionally been configured using a hardware description languages and two main languages used are Verilog and VHDL, which allow designers to design at various levels of abstraction [3].

The hardware description languages larger availability allows the designers to not only logically describe circuit functionality but also to simulate and evaluate the processing performances using appropriate development and test environments [3]. While the simulation is generating the logical results, a natural step consists in extending the use of hardware simulators into the field of digital signal processing.

The proposed real-time configurable system can be used for medical applications because the speed of diagnosis of disease is sometimes vital and, with this system, was obtained the processed image with a delay of 17,78ns for a 400 x 400 size digital image.

For this purpose, the configurable system proposed for image processing in real time provides a topical solution, being complementary, alongside the other classical processes for real-time applications.

II. REAL-TIME SYSTEM FOR MEDICAL IMAGE PROCESSING

The real time image processing requirements demand a system ideally having characteristics such as high

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performance, flexibility, easy upgradability, low development cost.

This work proposes a novel hardware architecture of a real-time configurable system for digital image processing using Verilog HDL and reconfigurable architecture (Fig.1).

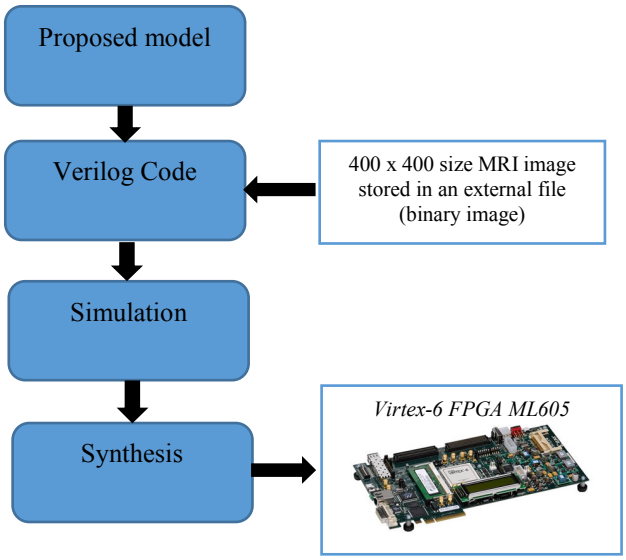

Fig. 1. Design Methodology.

Another hardware architecture of a real-time configurable system for digital image processing was proposed and tested by the author, in Reference [4], using a series of point operations such as gray operator, contrast manipulation, brightness manipulation and threshold operation.

The greater future potential of the proposed systems lies in the fact that it is not necessary to use an additional processor dedicated to image processing, which could slow down the flow: image acquisition → preprocessing the image → image use in order to establish a decision which can be human-type (in the case of a diagnosis based on medical images) or non-human-type (in the case of an industrial process) [4].

The configurable system described and tested in this paper contains four filters based on low-level image processing operators that can be classified as point operators, window operators and global operators. Using a single control input the system achieves the inter-change of filters *on-the-fly* (it is not necesary to switch off the reconfigurable equipment).

A class of low-level image processing operators was described in Reference [5]. The low-level image processing operators, called filters, used as internal components in the presented real-time configurable system for image processing are: Contrast filter, Brightness filter, Inverting filter and Pseudo-color filter. The hardware implementation using Verilog for pseudo-color algorithm is presented by the author in the article „Implementation of Medical Image Processing Algorithm on Reconfigurable Hardware".

Based on the filters as described, tested and optimized in Reference [5], using Verilog language, templates were created to smooth the filter system in order to allow easy replacement of components, providing greater flexibility to the system.

These filters are connected in a pipeline structure, with the possibility of amending the order of filters and the parameters of each filter features (Fig. 2).

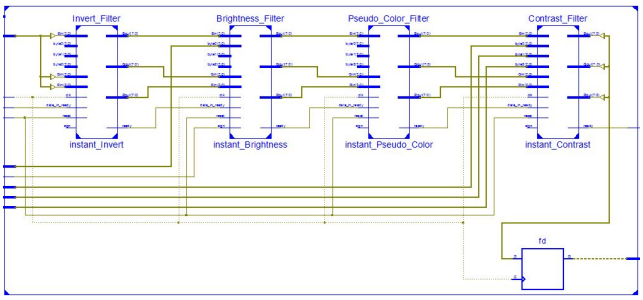

Fig. 2. Schematic structure of real-time configurable system for image processing (capture from Xilinx ISE Design Suite).

The system is described at Register Transfer Level (RTL). The images are processed by switching the order of filters and processing them to improve image.

A command was defined in order to control the inter-change of the filters in the structure of the system. This command will be used to inter-change *on-the-fly* (without the need to shut down or reconfigure the equipment) the filters which will process the image applied to the input.

TABLE I. VERILOG CODE FOR CONTROL OF FILTERS

```
input [7:0] filters_order;
wire  [1:0] order_pseudo_color;
wire  [1:0] order_contrast;
wire  [1:0] order_invert;
wire  [1:0] order_brightness;
      assign order_brightness = filters_order [7:6];
      assign order_invert = filters_order [5:4];
      assign order_contrast = filters_order [3:2];
      assign order_pseudo_color = filters_order [1:0];
```

In the system description I used continuous-type assignments (*assign*) that command variable type wire, being evaluated and updated when an input operand value changes, as well as the conditional operator.

TABLE II. VERILOG CODE FOR CONTRAST FILTER TEMPLATE

```
Contrast_Filter instant_Contrast (
  .Rin (RinContrast),
  .Gin (GinContrast),
  .Bin (BinContrast),
  .Rout (RoutContrast),
  .Gout (GoutContrast),
  .Bout (BoutContrast),
  .reset (reset),
  .clk (clk),
  .data_in_ready (data_in_readyContrast),
  ...    );
```

```
assign RinContrast =
      order_Contrast == 0 ? Rin :
      order_Contrast == 1 ? RGB_Out0[0] :
      order_Contrast == 2 ? RGB_Out1[0] :
                            RGB_Out2[0];
assign GinContrast =
      order_Contrast == 0 ? Gin :
      order_Contrast == 1 ? RGB_Out0[1] :
      order_Contrast == 2 ? RGB_Out1[1] :
                            RGB_Out2[1];
assign BinContrast =
      order_Contrast == 0 ? Bin :
      order_Contrast == 1 ? RGB_Out0[2] :
      order_Contrast == 2 ? RGB_Out1[2] :
                            RGB_Out2[2];
.....
```

III. EXPERIMENTAL RESULTS

The proposed design was tested on medical image (MRI - magnetic resonance imaging), shown in figures in each left panel.

The measurements were carried out under two different conditions:

1. changing the order of the filters in real-time;
2. changing filter parameters.

The processed image, obtained by inter-changing filters in the system using a single command input is shown in Fig. 4.

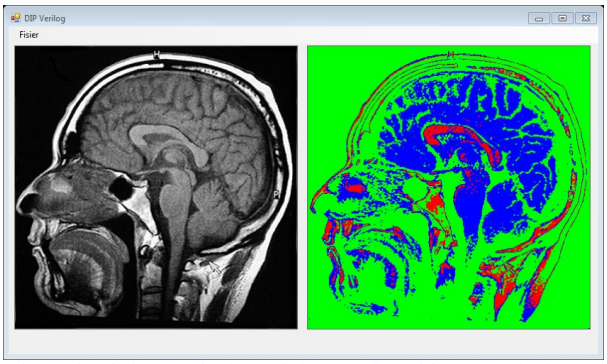

Fig. 4 Simulation results for real-time configurable system for image processing, using Xilinx ISE Design Suite.

The processed image as an effect of changing the parameters applied to filters is illustrated in the Fig. 5.

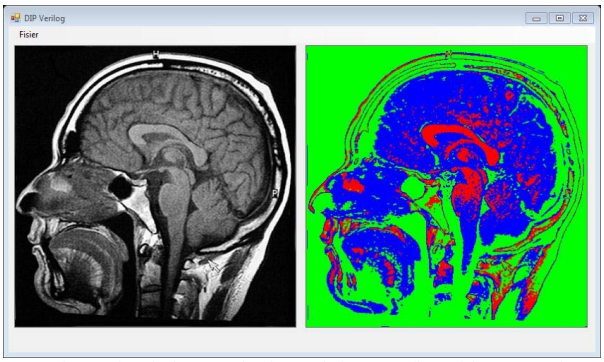

Fig. 5 Simulation results for real-time configurable system for image processing, using Xilinx ISE Design Suite.

The real-time configurable system for image processing was modeled in Verilog HDL and the design was synthesized with *Xilinx ISE Design Suite* environment on the platform *Xilinx Virtex-6 FPGA ML605*.

The synthesis shows that this real time configurable system for image processing provides good performance for different work conditions. The delay was 17,78 ns for a 400 x 400 size digital image processing, obtained as a result of the synthesis on a platform Virtex-6 containing a reconfigurable FPGA circuit.

Also, an evaluation of logic resources required was achieved for hardware implementation of the real-time configurable system for DIP, using the platform *Xilinx Virtex-6 FPGA*, and was performed and tabulated in Table II.

TABLE III. EXPERIMENTAL RESULTS WITH AREA OPTIMIZATION

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	90	301,440	1%
Number of Slice LUTs	284	150,720	1%
Number of fully used LUT-FF pairs	83	291	28%
Number of bonded IOBs	84	600	14%
Number of BUFG/ BUFGCTRLs	1	32	3%

This application offers solutions for problems that could be encountered in the real time processing of images, particularly in the case of medical applications and equipments or in any area where image processing is required in real time and the processing speed is vital.

The technique described in this paper is part of a larger research oriented on the use of hardware description languages in signal processing simulations area. Other hardware processing simulations are to be studied as future work. The use of the complex digital CAD tools in the signal processing field offers not only a different developing solution but also a new larger implementation method which has to be considered together with the future digital technologies.

IV. CONCLUSION

Image processing algorithms implemented in hardware have recently emerged as the most viable solution for improving the performance of image processing systems. This paper presents a versatile, modular and scalable real-time configurable system for image processing, implemented in hardware that may be used for testing and implementing of image preprocessing operations under real-time constraints.

In this real-time configurable system the images are processed by switching a series of filters and changing the filter parameters to improve the image. All the modules are designed and implemented using Verilog HDL and a platform *Virtex-6 FPGA ML605*. Different experimental results of the real-time configurable system are presented.

REFERENCES

[1] Griselda Saldana-Gonzalez, Miguel Arias-Estrada, "FPGA Based Acceleration for Image Processing Applications", Image Processing, Book, ISBN 978-953-307-026-1, pp. 572, INTECH, 2009.

[2] Daggu Venkateshwar Rao, Shruti Patil, Naveen Anne Babu, V Muthukumar, "Implementation and Evaluation of Image Processing Algoritms on Reconfigurable Architecture using C-based Hardware Descriptive Languages", International Journal of Theoretical and Applied Computer Sciences, vol. 1, no. 1, pp. 9-34, 2006.

[3] Sparsh Mittal, Saket Gupta, S. Dasgupta, "FPGA: An Efficient and promising Platform for Real Time Image Processing Applications", Proceedings of the National Conference on Research and Development in Hardware & Systems, 2008.

[4] Iuliana Chiuchişan, M. Cerlincă, „Implementation of Real-Time System for Medical Image Processing using Verilog Hardware Description Language", Proceedings of the 9th International Conference on Cellular and Molecular Biology, Biophysics and Bioengineering (BIO'13), ISSN: 1790-5125, ISBN: 978-960-474-326-1, pp.66-69, Chania, Creta, Greece, 2013.

[5] Iuliana Chiuchisan, M. Cerlinca, A.D. Potorac, A. Graur, "Image Enhancement Methods Approach using Verilog Hardware Description Language", Poceedings of the 11th International Conference on Development and Application Systems, "□tefan cel Mare" University of Suceava, ISSN 1844-5039, pg. 144-148, Romania,2012.

[6] C.T. Johnston, K. T. Gribbon, D. G. Bailey, "Implementing Image Processing Algorithms on FPGAs", Institute of Information Sciences & Technology, Massey University.

[7] A.B. Mahundi Bethord, Ding Xuewen, "FPGA- Based Parallelism For Real-Time Video Image Processing", International Journal of Engineering Research & Technology (IJERT), Vol. 2, Issue 3, 2013.

[8] Thomas B. Moeslund, "Introduction to Video and Image Processing – Building Real Systems and Applications", Springer, 2012.

[9] John C. Russ, "The Image Processing Handbook", 6th Edition, CRC Press, 2011.

[10] Wilhelm Burger, Mark J. Burge, "Principles of Digital Image Processing, Fundamental Techniques", Springer, 2009.

[11] Nasri Sulaiman, Zeyad Assi Obaid, M. H. Marhaban, M. N. Hamidon, "Design and Implementation of FPGA-Based Systems - A Review", Australian Journal of Basic and Applied Sciences, vol. 3(4), 2009.

[12] R. Gonzales, R. Woods, "Digital Image Processing", Prentice Hall, 2008.

[13] R. Woods, J. McAllister, G. Lightbody, Y. Yi, "FPGA-based implementation of signal processing systems", John Wiley and Sons, 2008.

[14] Nasser Kehtarnavaz, Mark Gamadia, "Real time image and video processing: From Research to Reality", University of Texas at Dallas, USA, 2006.

[15] Zainalabedin Navabi, "Digital Design and Implementation with Field Programmable Devices", Kluwer Academic Publishers, 2005.

[16] John L. Semmlow, "Biosignal and Biomedical Image Processing, Signal", Processing and Communications Series, 2004.

[17] Bernd Jahne, "Digital Image Processing", 5th revised and extended edition, Springer, 2002.

[18] S. Ramachandran, "Digital VLSI Systems Design. A Design Manual for Implementation of Projects on FPGAs and ASICs Using Verilog", Springer, 2007.

[19] Oana Geman, Cornel Turcu, "Partitioning Methods used in DBS Treatments Analysis Results", ISI Proceedings of the 2011 International Joint Conference on Neural Networks, July 31-August 5, San Jose, California, USA, IEEE Catalog Number CFP11IJS-PRT, ISBN 978-1-4577-1086-5, ISSN 2161-4393, CD Edition: IEEE Catalog Number CFP11IJS-CDR, ISBN 978-1-4244-9636-5, pp. 1788-1793, 2011.

[20] Oana Geman, Ciprian Zamfir, "Nonlinear Dynamics parameters and K-Means Clustering Algorithm used in DBS Treatments Analysis Results", Proceedings of 6th European Conference on Intelligent Systems and Technologies, Iasi, Romania, ISSN 2049-038x, pp. 272-284, 2010.