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Research on the design of FPGA-based radar signal processing system

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***Abstract*—Radar as an important part of modern air defense combat system has an extremely important use value. In recent decades, the research of radar signal processing has made great progress. Due to the wide application and rapid development of large-scale integrated circuits and digital technology, the overall performance of radar systems has been greatly improved. Meanwhile, FPGA is gradually becoming the core device of radar signal processing system. Based on this background, this paper focuses on the development status of radar signal processing system and FPGA, and organically combines the two, puts forward the FPGA design scheme of radar signal processing system, and finally points out the development trend of radar signal processing based on FPGA. It aims to promote the development of FPGA-based radar signal processing system and to strengthen the long progress of radar high-tech field research in this way.**

Keywords- Radar; FPGA; Signal Processing; System Design

I. INTRODUCTION

Radar is a high-tech system that concentrates various achievements of modern electronic science and technology, and has been successfully applied in the fields of shipboard, airborne, and satellite-based, etc. These radars perform various military and civilian tasks. Radar signal processing has not only greatly improved the ability of radar to detect targets in complex backgrounds, but also provided more information, such as imaging and identification of targets [1]. With the rapid development of radar signal processing algorithm research, signal processing is not only required to continuously improve the target detection probability, but also to extract target information in complex backgrounds (such as clutter, noise, interference) and further obtain more target information, and also to be able to detect interference characteristics (such as interference type, interference orientation, interference intensity, etc.) based on interference echoes.

The development of signal processing algorithms depends not only on theoretical research, but also on the hardware platform that will make it concrete. As the radar system becomes more and more powerful, the data processing accuracy requirement in digital signal processing becomes higher and higher, the data processing volume becomes larger and higher, the algorithm complexity also becomes higher and higher, the real-time operation of the system puts forward higher requirements, and the real-time signal processing is especially important. In this regard, FPGA has the characteristics of flexible design, low power consumption and high operation speed. And with the rapid development of ultra-large-scale integrated circuit technology, the number of logic gates of FPGAs is expanding and the logic resources are increasing [2]. And many FPGAs nowadays are able to perform floating-point operations, overcoming the problems of small dynamic range and insufficient precision when FPGAs perform data operations. And the embedded RAM resources, clock management resources, RocketIO resources and processor PowerPC resources make FPGAs more powerful. Therefore, FPGA is a good choice to realize modern radar signal high-speed processing. With the rapid development of digital circuits, the functions of FPGAs will become more and more powerful, and the use of FPGAs in the field of radar digital signal processing will definitely become a development direction of modern radar signal processing. In this context, this paper investigates the FPGA-based radar signal processing system to help the continuous advancement of this field of research.

II. DEVELOPMENT STATUS RESEARCH

A. Radar signal processing system development status

Radar signal processing system as the core part of radar nowadays, the design and implementation of radar signal processing algorithm directly affects the performance of the whole radar system. International research work on radar digital signal processing has been carried out since the early 1990s, but since the implementation technology of radar signal processing belongs to the military secrets protected by countries, it is difficult for us to know the existing research level abroad from the published literature [3]. With the complexity of radar signal processing algorithms, the processing speed and data throughput of digital signal processors have become more demanding, and the traditional method of using a single digital signal processor

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can no longer meet the current demand. At the early stage of development, a single or multi-chip DSP was mainly used as the core device to achieve digital signal processing. In recent years, with the introduction of multi-million gate FPGAs, another channel for radar signal processing has been provided. Since FPGA design can realize parallel processing, it can better accomplish the task of real-time digital signal processing, which is promoted in the current application of radar signal processing system.

B. FPGA development status

Due to the development of ultra-large-scale integrated circuit technology, the processing speed and integration degree of DSP and FPGA have been greatly improved. The current DSP processing speed has exceeded 1GHz, while the use of multi-core technology, the processing speed is very high, and DSP uses software programming, design flexibility and stability. However, DSP adopts serial processing, which limits the improvement of its real-time processing performance. FPGA structure framework determines the parallel processing characteristics, and the adoption of parallel processing technology has greatly improved the data processing speed, while IO pins can be configured, which makes the IO data throughput has been greatly improved, but with the diversification and complexity of radar signal processing algorithms, the limited logic resources and storage resources inside FPGA can not meet the huge algorithm implementation. storage resources, can not meet the needs of the huge algorithm implementation, and with the increased complexity of the design, the stability of the system is reduced. The signal processing tasks can be accomplished in a complementary way using the advantages and disadvantages between the two. In the current engineering implementation of radar signal processing algorithms, a combination of DSP and FPGA is mainly used [4]. For example, Liu Yucai and others from Xi'an University of Electronic Science and Technology designed and implemented a PD radar signal processor based on 8 TS201 chips as the core. 8 TS20IS processors do not share a bus and use a memory architecture. The FPGA on each DSP is connected to a high-performance PCI bridge chip from PLX through the bus. The host computer implements program loading and communication to the 8 DSPs through the PCI bus and accesses all resources on the board.

III. FPGA SCHEME DESIGN FOR RADAR SIGNAL PROCESSING SYSTEM

China's research in radar signal processing is still emerging, and in recent years, many fruitful researches on its implementation have been carried out by relevant universities and research institutes. Some radar signal processor prototypes and experimental systems have been developed one after another, and there are three main forms of design: one is based on "FPGA+DSP" structure; the other is based on DSP (ADSP) structure; the third is based on FPGA structure. This paper adopts the second one for specific research [5].

A. Overall solution design in FPGA

According to the functional requirements and hardware design of the radar signal processing system, the functions to be implemented on the FPGA chip are timing control, A/D sampling, digital IF quadrature sampling, anti-asynchronous interference, and interface communication [6]. The functions to be realized on the FPGA of the timing control board are timing control, A/D sampling, digital IF quadrature sampling, anti-asynchronous interference, interface communication: the functions to be realized on the signal processing board are intra-board and inter-board interface communication. the FPGA solution design can be divided into two parts, one is the signal processing module design, and the other is the interface communication design.

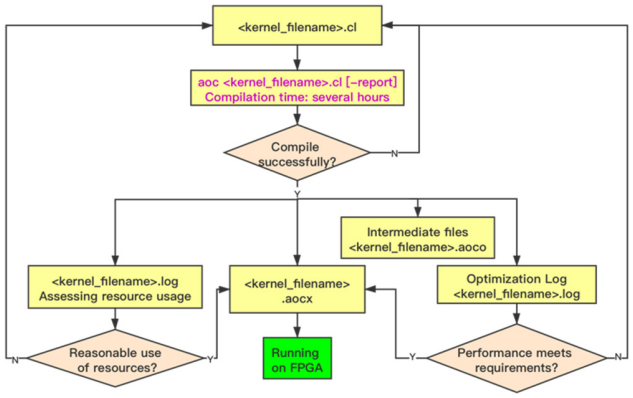

Figure 1. FPGA compilation process.

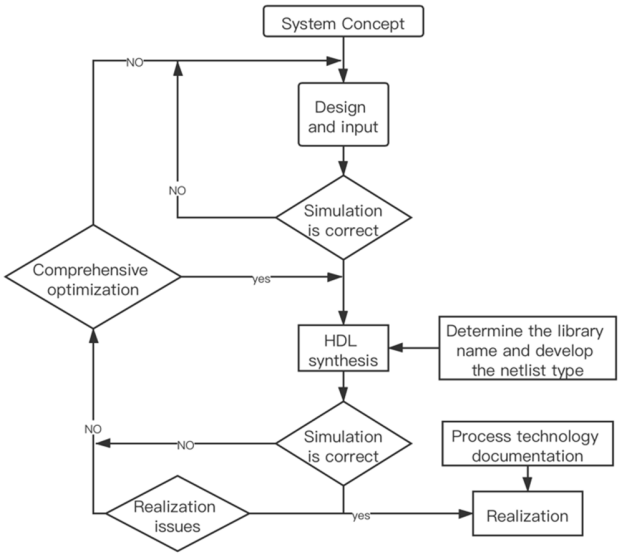

Figure 2. FPGA Design Flowchart.

The signal processing module design mainly refers to the clock management module, system reset module, control signal generation module, A/D sampling module, digital IF quadrature sampling module, anti-asynchronous interference module, point trace merging module and self-test module [7]. These signal processing modules can be divided into three stages according to the processing stage: pre-pulse pressure, post-pulse pressure and post-point trace. The interface communication design can be divided into three types according to the interface type: link port, serial port and optical fiber, and can be divided into intra-board communication, inter-board communication and interface communication with other subsystems according to the connection object [8].

B. Signal processing design in FPGA

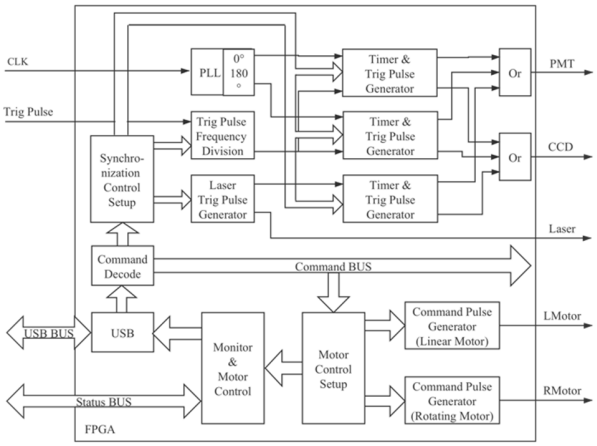

Figure 3. FPGA typical logic structure diagram.

1) Signal processing design before pulse voltage: The signal processing process before pulse pressure mainly contains AD sampling, digital IF quadrature sampling, anti-asynchronous interference, RAM cache, mode word and data merging, the data source is the IF analog signal from the receiver, and the data destination is the DSP on the radar timing control board. The receiver output IF analog signal is converted to digital signal after sampling by 16-bit AD chip, and then the data is extracted to reduce the data rate after digital IF quadrature sampling process, which is converted to I and Q quadrature low frequency data [9]. The data after DDC enters the anti-asynchronous interference module, the anti-asynchronous interference module has a control switch, only when the switch is turned on, the data will do the anti-asynchronous interference processing, otherwise the data goes directly to the next module, i.e. the RAM cache module of the data, then the mode word is added to the front of the cached data, then it is sent to the DSP of the radar timing control board through the link port at the same time to do the pulse compression processing, after doing the pulse compression the result of the pulse compression is sent to the FPGA through the link port.

2) Post pulse compression processing design: The process after the pulse pressure is mainly to combine the pulse pressure data into one way, the pulse pressure results and the received MTD results for the modulation process. The pulse pressure result data source is the DSP on the radar timing control board, the MTD result source is the signal processing board, the pulse pressure result after data merging goes to the signal processing board, the FPGA receives the pulse pressure data and divides it into two parts: one pulse pressure data is merged into one way first, and then transmitted to the signal processing board by the link port through the backplane. The signal processing board sends the processed MTD results to the FPGA through a pair of differential data lines and a pair of differential clock lines, and then does the modulation process in the FPGA to form the original video. The other copy is modulated in the PGA and converted to P/A raw video, which is selected by the monitor along with the MTD raw video and converted to analog data, and then amplified by the operational amplifier and sent to the recording terminal and monitor [10].

3) Post-track processing design: The post-dot trace process is mainly 1bit information extraction and dot trace merging. The source of data is the signal processing board and the destination of data is the recording terminal. The signal processing board sends the processed 1bit and point trace information to the FPGA through the link port, and the FPGA extracts the target distance information and converts it into 1bit video to the recording terminal, and also merges the point trace information, and then sends it to the recording terminal through the serial port [11].

C. Interface communication design in FPGA

1) Intra-board communication of timing control board: The analog IF signal enters the radar timing control board through SMA port, and after A/D sampling, the digital IF signal is obtained, and after a series of processing in FPGA, the digital signal is sent to DSP through the in-board link port, and then the DSP sends the result to FPGA through the link port after pulse compression.

2) Inter-board communication between timing control board and signal processing board: The pulse pressure result is sent from the FPGA of timing control board to the signal processing board through the inter-board link port, the signal processing board receives the data and does a series of detection and processing, and finally sends the Ibit and point trace information to the FPGA.

3) Interface communication with other subsystems: Radar signal processing system and monitoring interface signals are mainly: control commands and fault information. The monitoring subsystem will send various control instructions from the serial port to the FPGA of the timing control board, the FPGA receives the instructions and then decodes the various control information contained in the instructions, and then sends them out in two parts, one to the timing control module: one as a mode word sent to the signal processing board by the link port, the FPGA in accordance with the interface protocol to send the control information to the receiver, etc., in order to control other subsystems to work synchronously, and at the same time send the current working status back to the monitoring whether it is normal or not [12]. The interface signals between the radar signal processing system and the recording terminal mainly include: video selection and control, interference information, 1bit video and point trace information. When the sector mode is open, the recording terminal sends the video selection information to the PGA for execution: the FPGA sends the interference information detected in the agreed format to the recording terminal, and the FPGA also sends the 1bit video and point trace information to the recording terminal for display.

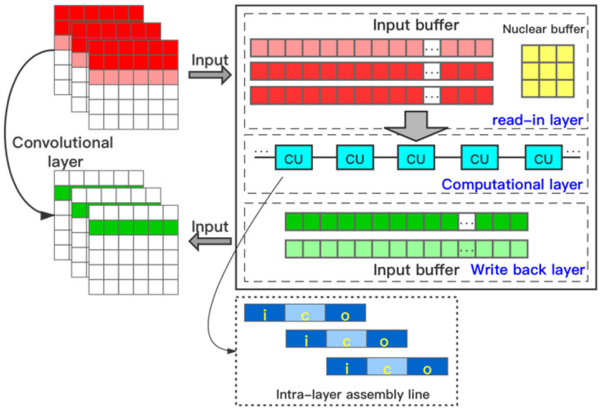

Figure 4. FPGA-based Communication Accelerator.

IV. Trends in FPGA-based Radar Signal Processing

The task of radar signal processing is to check and identify the target in the background of clutter, and the main research contents are array signal processing technology, target detection technology among others. Radar signal processing system is realized by an orderly combination of signal processing modules, therefore, it is expensive to provide users with feature-rich IP core resources. IP cores are modules with intellectual property rights provided by major FPGA manufacturers, which can be implemented by hardware description language HDL or optimized transistor-level layout. IP cores are divided into three main categories: hard cores, solid cores and soft cores. Hard cores are designed directly by the manufacturer in the chip and have high processing speed and stable and reliable performance. Solid cores (sometimes called semi-hard cores) mostly have a lot of configuration data that can be used in different application software [13]. A soft core is a network list (a column of logic and interconnected integrated circuits) or hardware description language (HDL) code that is more flexible and can be changed by the user as needed by the application.

IP technology is for reusable design, and this design model is also generally recognized and widely used. Such as DSP slice RAM, high-speed transceiver are IP core resources, which have the advantages of high operation speed and small resource occupation. Using IP cores for design provides great convenience and flexibility for system design, and can also shorten the development cycle and improve design efficiency. Therefore, it is very convenient to build a signal processing system with the flexible design method and rich IP core library of FPGAs, and with the powerful development tools provided by the manufacturers. The method of implementing radar signal processing with FPGA as the core processor has already received attention, and with the modularized and standardized design standard, its aspect of radar signal processing will have great development space in the future.

V. Conclusion

The introduction of digital logic programming devices FPGAs in the mid-1980s revolutionized the approach to practical signal processing. Nowadays, in the "FPGA+DSP" structure, FPGAs are mostly used for timing control, data transmission and simple algorithm implementation, and many features of FPGA chips have not been explored and their role has not been fully exploited. The research of engineering implementation methods will further promote the application of FPGA in the field of radar, and it will be the trend of future development for FPGA to complete radar signal processing independently. Research staff are continuously studying the implementation of general radar signal processing using FPGAs, and some results have been achieved. How to apply PGAs to high-resolution radar has caused people to think. The FPGAs used in this paper implement more functions and have some reference value for the comprehensive application of FPGAs in radar signal processing.

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