Real Time Implementation of a Hybrid Differential Manchester-PWM Encoding for Constant Data Rate under Variable Brightness in VLC Systems

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***Abstract*—A Hybrid Differential Manchester-PWM encoding for data transmission and brightness control is implemented in a real time system and successfully integrated to a visible light communication architecture. The proposed digital modulation, allows simultaneous control of brightness maintaining data transmission at constant bit rate. Transmission data is generated using a ZedBoard™ development kit, which has a ARM Cortex-A9 processor and a Artix-7 FPGA. The resulting electrical signal feeds a driver of a commercial white illumination light-emitting diodes (LEDs). We experimentally demonstrate a constant transmission speed of 50Kbps using three 10W white LEDs at a distance of 0.9 meters, with a range of brightness between 10% and 90% of the maximum luminous flux of the LED sources.**

***Index Terms*—Differential Manchester, PWM, FPGA, light-emitting diode (LED), VLC.**

I. Introduction

The data transmission on visible light (VLC), can be defined as a form of wireless transmission of short-range using the visible light spectrum (400-700 nm). VLC uses for data transmission the intensity modulation in solid state devices for lighting, such as light emitting diodes (LED) [1].

Currently, light emitting diodes (LEDs) are replacing conventional lighting devices such as fluorescent and incandescent lamps, and they are becoming the main source of indoor and outdoor lighting. LEDs have many advantages over conventionally lighting devices, such as high efficiency in energy consumption, longer life and environmentally friendly [2]. In addition, LEDs have a high switching capacity since they can be switched between On and Off states at high speeds, allowing them to be used in high-speed data communications [3].

A lighting system designed to support a VLC system needs to have the option of brightness control, because of the varying demand for illumination at different times of the day. Several researchers have proposed the use of different modulation techniques based on On-Off Keying (OOK) in search of obtaining simultaneously brightness control and constant data transmission rates. As an example, in [4] a system based on multiple pulse position modulation (MPPM) is proposed, this modulation varies the number of pulses within the duration of a symbol, according to the attenuation level. The attenuation factor can be expressed by the MPPM modulation parameters.

Also in [5], it is proposed the use of PPM in combination with PWM (pulse width modulation) for data transmission and attenuation control. In this case, the data in PPM format are added to the duty cycle in the PWM signal, for dimming control. The duty cycle in PWM signal is changed from 40 % to 80 % and the PWM rate is set to 1 kHz in order to avoid flickering. Finally, the PPM data rate is set to 20 kb/s.

In [6], a DFSOOK (Dimming Frequency Shift On-Off Keying) scheme is proposed and tested. PWM and additional digital frequency shift keying (FSK) are used for data transmission under frequency and periods variably adjusted. In [7], a VLC system is presented, which combines PWM for the illumination control, embedded in an MPPM scheme. Experimental results show a system efficiency of 80.8% with 1 $Mbps$ data rate.

One of the challenges to overcome in VLC systems for indoor use, it is the integration with existing technologies such as Ethernet (in its different versions) used in wired networks. This integration should be of low complexity in both hardware and the conversion of used modulation and coding formats. To achieve the above, it is possible to take the advantages of differential Manchester coding and the systems on Chip and Field Programmable Gate Array (SoC-FPGA). Differential Manchester is an auto-synchronized coding which allows the clock signal to be obtained from the data stream and its large signal format has a higher noise immunity. The SoC-FPGA systems have heterogeneous architectures based on ARM and FPGA to mix the capabilities of a processor to run sequential tasks, with the high degree of parallelism of reconfigurable hardware.

In this work, we proposed and experimentally validated a modulation scheme that uses the theory underlying the PWM technique (for dimming control) complemented by a modified differential Manchester encoding for data transmission using visible light, in order to achieve two main purposes: brightness control based on the variation of pulse width, and constant data rate independent of the luminous intensity. The paper is

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structured as follows: section 2 describes the proposed coding and system, section 3 shows the implementation and section 4 presents the results obtained.

II. Differential Manchester as PWM for dimming control

A. PWM overview

The LED is a device controlled by current, its brightness is proportional to the current through it, The amount of current that passes through the LED, can be controlled in two ways. The first method is to limit the current analogously, the second way is to use the pulse width modulation (PWM) [4].

In PWM, the duty cycle (D) of a periodic signal (usually square) is modified to control the amount of energy sent to a load. During the high state (pulse) of the PWM period, LED works at the voltage-current recommended operating point, this ensures that the variations in the CCT (Correlated Color Temperature) parameter are within the values set by the manufacturer. The ratio between pulse duration and the period (duty cicle) of the PWM signal, determines the average current and, therefore, the perceived brightness.

B. Differential Manchester encoding

Differential Manchester coding is a variant of Manchester coding. In this, a bit of value 1 is represented by the absence of transition at the beginning of the signal period, a 0 bit is indicated by the presence of a transition at beginning of the period. There is always one transition in the middle of the interval, which is used only for synchronization in the receiver.

C. Proposed Modified differential Manchester

In order to achieve the double purpose, the lighting control, and constant data rate, in this work, we propose and test a modified differential Manchester encoding (Fig. 1).

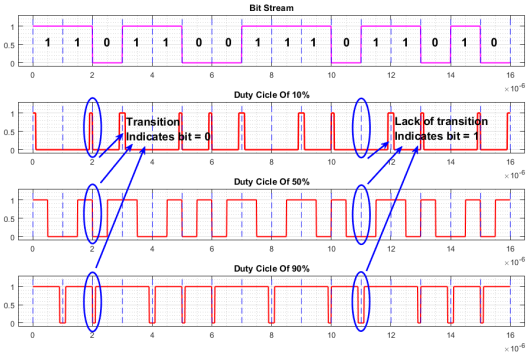

Fig. 1. Proposal of modified differential Manchester Encoding

A LED can be modeled as an RC circuit (like a low pass filter of the first order), the digital modulation of a LED involves two distinct states (ON and OFF). In ON/OFF applications the rise and fall times are limited by the LED intrinsic capacitance [8]. In order to achieve higher accuracy and improve system performance, it is necessary to take into account the values of the rise time (t_r) and the fall time (t_f) (Fig. 2) in the LED.

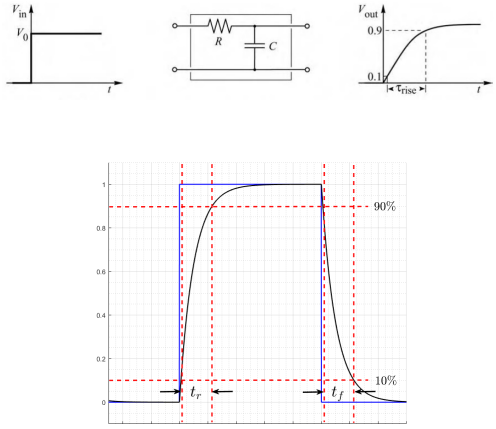

Fig. 2. Rise time (t_r) and fall time (t_f) in a LED

According to these two values, the minimum time of the Duty Cycle in the PWM signal (to reach the work point in the LED) must be:

$$t_{(minimum\ of\ D)} \geq (t_r + t_f) \tag{1}$$

In this proposal, the desired lighting level varies between 10% and 90% of the maximum light output in the LED. Under this conditions, the maximum speed of data transmission or bit rate (V) can be calculated as follows:

$$V = \frac{1}{10 * (t_r + t_f)}\ [bps] \tag{2}$$

III. System implementation on SoC-FPGA

A. Experimental Setup

Fig. 3 shows the complete experimental setup for the VLC system. The system was built in a wooden structure that holds the LEDs at the top. At the bottom part of the structure, there is a photodetector circuit and on both sides the FPGA boards used to implement encoding and decoding the proposed modified differential Manchester. Also, a scopometer was used to perform the visualization of bitstreams and its corresponding encoding signals, a dual power supply provides the current needed for each connected circuit in transmitter and receiver.

The prototype was developed using two ZedBoard™, one for the transmitter and the other for receiver. The board is a complete development kit with a Xilinx Zynq®-7000 All Programmable SoC. The architecture has a dual core ARM processor known as processing system (PS) and a FPGA Artix-7 by Xilinx that is known as programmable logic (PL). The algorithms for modified differential Manchester encoding were designed in Vivado® Design Suite HLx using RTL (Register-Transfer Level) methodology and VHDL (Very High Speed Integrated Circuit Hardware Description Language).

Table I presents the characteristics of LEDs used in the system. The LEDs were controlled from ZedBoard through

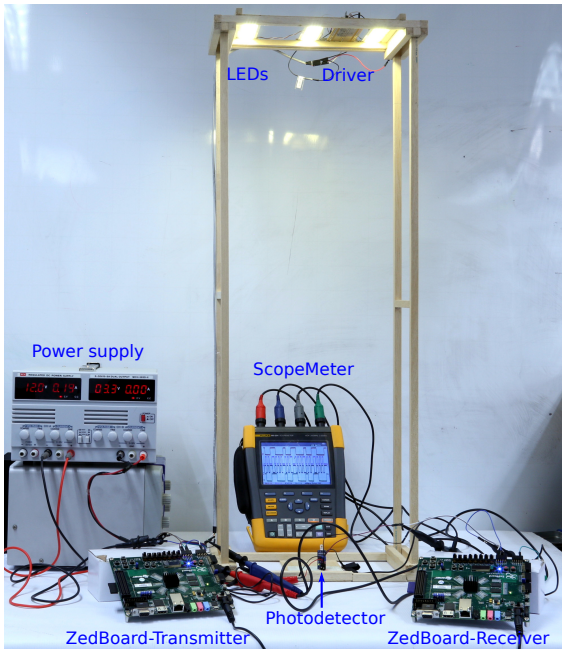

Fig. 3. Experimental setup for VLC system using modified Differential Manchester

a driver using power electronic circuits for ensuring power to LEDs and protection of digital boards. Fig. 4 shows the circuit design for the LEDs driver.

TABLE I
LED PARAMETERS

Type	COB strip
Power	$10W$
Voltage	$12 - 14\ V_{DC}$
Max Current	$600\ mA$
Emitting color	Natural white $(4200K)$
Luminous flux	$> 100\ LM/W$

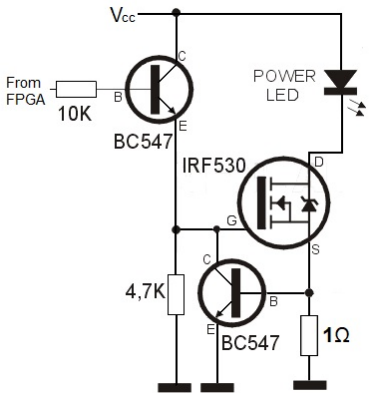

Fig. 4. Driver for LED

B. Transmitter System

A ZedBoard™ with the encoder algorithm was connected to the driver of transmitter LEDs. Tests were carried out using files read by PS using C++ language in binary format taking full advantage of ARM processor user friendliness, and they were sent to PL through AXI (Advanced eXtensible Interface) protocol. Files are read in binary format and split into 1024 bytes packets for transmission to FPGA, see Fig. 5. Finally, the FPGA encodes the bitstream in modified differential Manchester encoding according to the desired brightness level to be sent through the GPIO port to the LED driver. The details of the power electronic circuit are shown in Fig. 4.

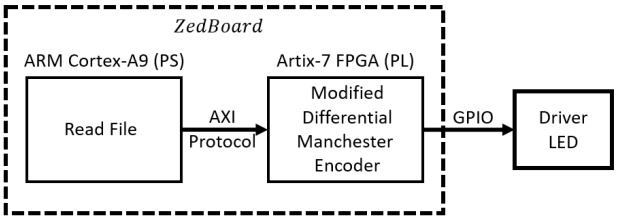

Fig. 5. Transmitter system on ZedBoard

The encoder is a VHDL module that is responsible for converting binary data located in BRAM (Block Random Access Memory) on the FPGA into data encoded in modified differential, using the level transition during the bit period to generate a PWM signal with variable duty cycle. The encoder uses a input clock signal to generate a counter from 0 to 19 dividing the bit period in 20 segments. This counter is used as a ramp signal that is compared with the desired duty cycle for the PWM signal. In this case, the duty cycle or its complement are compared with the ramp depending of previous value of encoded signal and the bit value of the input data, see Fig. 6.

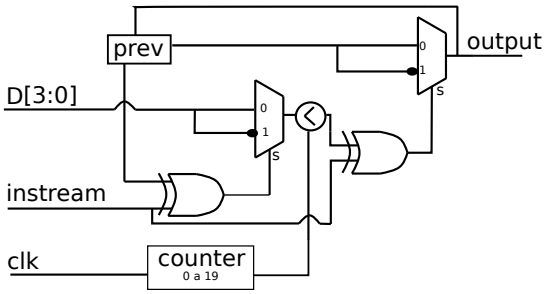

Fig. 6. Encoding using the modified differential Manchester

To ensure a change of the signal in the period, the encoder makes the comparisons with the counter from 2 to 17. Then, the duty cycle can be represented with 4 bit, in which the minimum duty cycle is 10 % ($D = 0000$) and the maximum is 90 % ($D = 1111$), and each increment of the ramp signal represents an increase of 5 % as shown in Fig. 7. In the figure, **a** is the instantaneous value of the counter that is compared with the Duty Cycle desired. For example, take a look in the time diagram on the top of the figure, in this case, the duty cycle is $D = 0100$ (30% of Duty Cycle), thus, **a** takes all

values from 0 to 19, but when **a** lower than D the output take the value of **prev** complement. The value **prev** represents the level of differential Manchester signal just before bit period, and takes is 0 value for low level of signal and 1 for high level. In the second time diagram the input bit (instream) is 1, in this case **a** complement is used to keep the brightness intensity of differential Manchester signal. The last two time diagrams show the cases when **prev** has a high level.

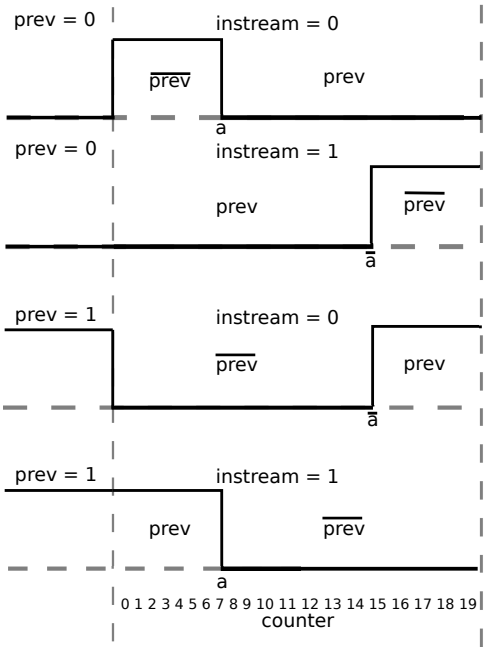

Fig. 7. Encoding using the modified differential Manchester

C. Receiver System

The receiver system is composed by a photodetector and a ZedBoard. In this case, the photodetector send the received signal from transmitter to the ZedBoard through GPIO. There, the FPGA is in charge of decode the Manchester signal and send data to the ARM using AXI protocol, finally, ARM saves data (see Fig. 8). The decoding process uses a counter whose clock has the same frequency as the clock of the clock of transmitter counter. When the counter reaches the number 19 (20 clock periods), the previous bit value stored in a flip-flop type D, is compared to the input encoded in modified differential Manchester using an XOR gate. Then, the result of comparison updates the flip-flop as the new previous value. Finally, these output bits are sent by AXI protocol to the ARM to be stored in a binary file, Fig. 9 shows the schematic of digital circuit implementation.

The signal sent by means of the LED is detected by phototransistor. The phototransistor converts the luminous intensity into electric current that passing through a 10K resistor generates a voltage; this voltage is entered into a comparator composed by one OPAMP $LM393$ (Fig. 10).

The comparison process performs a process of thresholding on the signal captured by the phototransistor. The thresholding

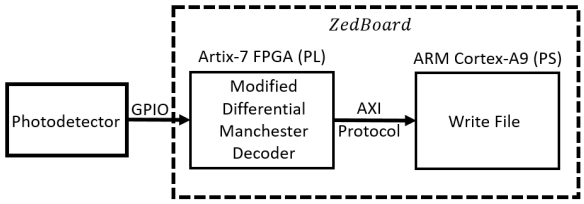

Fig. 8. Receiver system on ZedBoard

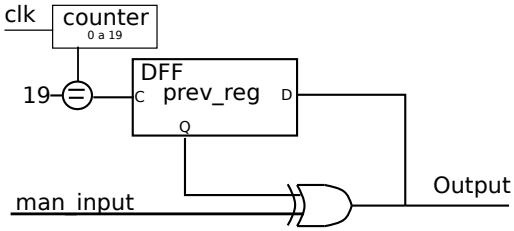

Fig. 9. Modified differential Manchester decoder

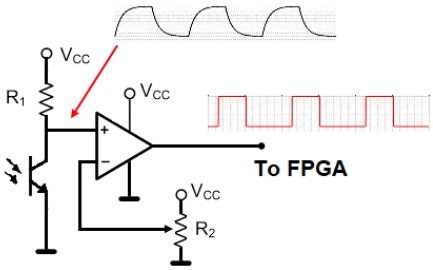

Fig. 10. Photodetector circuit

process does not change the period of the original signal, as can be seen in the Fig. 11.

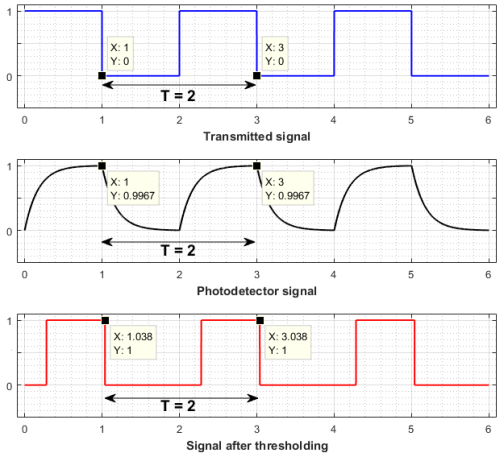

Fig. 11. Signal after theresholding

IV. Results

Fig. 12 shows the bit stream (green signal) and modified differential Manchester encoding (red signal) obtained in the real-time implementation system. Green signal is the representation of bits in the binary file, which will be transmitted using

the VLC system. This signal is sent to the modified differential Manchester encoder inside the FPGA, but for visualization the signal is sent to GPIO port of ZedBoard too. Red signal is visualized on the conexion point with the LED driver. The cursors are measuring a bit period of 20 μs resulting in a 50 $kbps$ bit rate. The figure shows the changes at the beginning of the bit period when the input bit is zero and the changes at half bit for ones, because the duty cycle is configured at 50 $\%$.

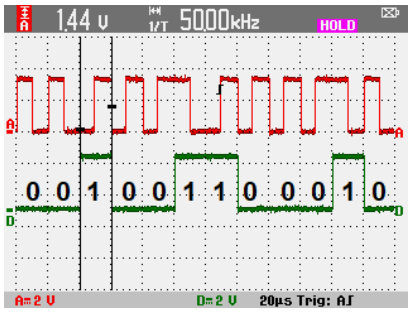

Fig. 12. Modified differential Manchester signal in implemented transmitter system and bit stream inside the FPGA.

Fig. 13 shows the signals in the real time implementation, where the bit stream transmitted is shown in red color. The transmitted signal encoded in modified differential Manchester with a 25 % of duty cycle is shown in blue color. The black color signal was measured on the phototransistor of the receiver system. Finally, the photodetector circuit compares the black signal with a threshold level and the green signal is obtained. The threshold is set by R2 resistor to obtain the desired signal taking into account that the output is inverted.

The signals (in the FPGAs) of the transmitter and receiver system are shown in Fig. 14. Red and green signals are sent from transmitter, the first one is the bitstream of the binary file and the second, the bits encoded using the modified differential Manchester. At the receiver, in the black signal we can see that: *i)* has a delay due to the thresholding process applied to the signal received in the photodetector circuit, and *ii)* the recovered signal, is inverted in relation to the signal sent. The above does not influence the decoding, because as stated, the thresholding process does not affect the period and in this process, only the change (or change absence) in the level of the signal at the beginning of the bit period is taken into account. The green signal is obtained after the decoding process on ZedBoard and this bitstream is store in a binary file.

V. Conclusions

A Manchester-PWM hybrid differential coding was proposed and it was experimentally demonstrated, that it is possible to maintain a constant bit rate, independent of the desired brightness level. The proposed modified differential Manchester for dimming control was implemented using a ZedBoard achieving constant 50 $kbps$ (due to the phototransistor limit) for brightness variations between 10% and 90% (in 5% steps).

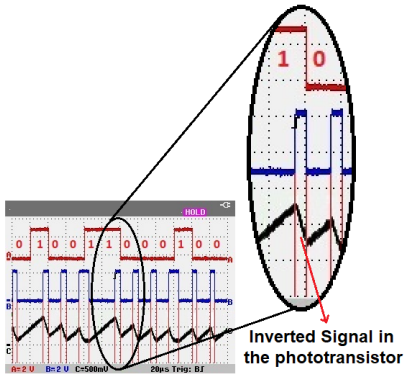

Fig. 13. Bit stream, modified differential Manchester, and photodetector circuit signals before threshold application

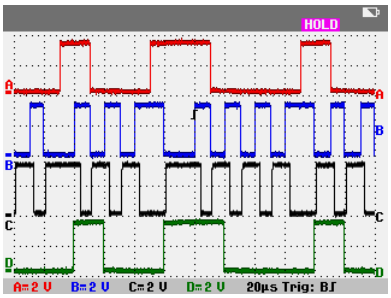

Fig. 14. Encoding and decoding modified differential Manchester

SoC-FPGA allowed the implementation of the complete VLC system, except for the LED driver and photodetector. On the ARM processor the files are managed using a software approach, and the FPGA accelerates the algorithms and guarantees the control of all signal in the transmitter and receiver processes. In addition, an application-specific integrated circuit (ASIC) can be developed using the design used on FPGA.

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