An FPGA Implementation of UAV SAR Real-time Imaging Algorithm

Jiaqi Pan*
Shanghai Satellite Engineering Research Institute
Shanghai, China
panjiaqi125@163.com

Zhaoyang Zeng
Shanghai Satellite Engineering Research Institute
Shanghai, China
1450828708@qq.com

Hui Wang
Shanghai Satellite Engineering Research Institute
Shanghai, China
huiwang@mml-ciss.org

Wei Hua
Shanghai Satellite Engineering Research Institute
Shanghai, China
yu34354420@126.com

Sili Wu
Shanghai Satellite Engineering Research Institute
Shanghai, China
wslleo@163.com

***Abstract*—This paper puts forward a valid method to design the Unmanned Aerial Vehicle (UAV) Synthetic Aperture Radar (SAR) real-time imaging processor based on FPGA, a block-wise Phase Gradient Autofocus (PGA)[4,5] is used to correct the space-variant phase error. The architecture of this processor designs with both fixed point operation and floating point operation to reduce hardware resource, also designs with both pipeline process and parallel process to reduce process time. Experiment results show that system works at 100MHz can process 512MB SAR raw data within about 8 seconds. The good experimental image also proves the validity and reliability of the proposed system.**

Keywords—Real-time imaging; Field Programmable Gate Array (FPGA); SAR

I. INTRODUCTION

Synthetic Aperture Radar(SAR)[1,2,3] is an important remote sensing technology with all-time, all-weather, and abundant microwave scattering information. It has great application potential in military, agriculture, forestry, marine and other fields . However, due to the large amount of raw data received by the high-resolution SAR system and the complicated 2-dimensional matched filtering process to obtain SAR images, even some application fields have high real-time requirements for SAR image acquisition, which makes high-speed imaging Processing technology has become a key technology in the SAR field. Therefore, studying the FPGA implementation of SAR real-time imaging algorithms has practical significance.

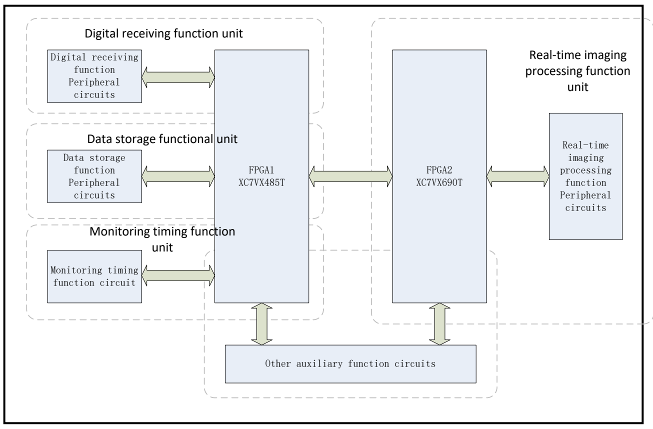
The imaging index directly determines the reconnaissance capability of the carrier aircraft, and the realization of the high index depends on the architecture of the radar real-time processing system and the corresponding imaging method. However, the traditional real-time processing of SAR usually uses a multi-DSP (digital signal processor) or DSP + FPGA (field programmable gate array) architecture. FPGA is used to complete AD conversion and pre-processing algorithms, and DSP is used to implement imaging algorithms. The adoption of this method leads to complex system structure, high power consumption, and low efficiency. Under certain load space and power requirements, the imaging algorithm can only be reduced or the system index can be reduced, and finally the imaging quality and scene observation range are sacrificed to meet the real-time processing requirements. , It is difficult to meet the high index requirements of modern radar. Therefore, a new processing system must be adopted to meet the needs of the development of SAR miniaturization. This article uses FPGA as the core to realize the SAR real-time imaging system. The flight test results show the effectiveness and practicability of the system.

II. REAL-TIME IMAGING SYSTEM ARCHITECTURE

In this article, the real-time imaging system uses two FPGAs as the core, assists with AD chips, and integrates storage chips and interface chips to achieve work timing control, intermediate frequency sampling, signal processing, data processing, and data storage functions. The highly integrated real-time imaging system first receives the echo signal from the antenna, and then the direct intermediate frequency sampling of the radar echo signal is completed by the AD module in the system, and the data after the AD sampling is sent to the signal processing and recording. The signal processing completes preprocessing such as decimation and filtering according to the requirements of the working mode. After the processing is completed, the result is sent to the data processing, and the data processing is sent to the image display via the interface module; Figure 1 shows the physical image of the SAR real-time imaging system.

Fig. 1. The physical image of SAR real-time imaging board

Fig. 2. The system functional block diagram



The real-time imaging processing system is used as the control center and operation center of the radar. As can be seen from Figure 2, the control and operation functions are all completed on the FPGA chip. The main performance parameters of the FPGA operation resources are shown in Table 1.

TABLE I. THE FPGA OPERATION RESOURCES

Device	XC7VX485T	XC7VX690T
logic cells	485,760	693,120
CLBs slices	75,900	106,300
dsp slices	2,800	3,600
block ram blocks	2,060	2,940
use i/o	700	1,000

III. SYSTEM REALIZATION METHOD

A. *System work timing control*

System communicates with the ground control computer through the wireless transmission module, accepts remote control instructions and configuration data injected by the ground control computer, and completes the unpacking, forwarding and execution of the instructions. According to the instructions, the power supply of the electronic equipment on the UAV is controlled on and off, and the power supply unit of the secondary power supply is controlled to control the power on and off of other single machines. Communicate with frequency synthesizer, stable platform controller, RF front-end, and receive remote measurement information of each single machine And complete the control of the system work sequence according to the system work mode.

B. *Signal sampling*

The intermediate frequency echo signal is output by the analog receiver through the SMA interface. When the system is working, the FPGA controls the working sequence of the AD chip, and realizes the buffering of the received data, and then performs real-time imaging processing.

C. *Imaging processing*

Real-time imaging is limited by resources such as time and memory. It is necessary to reduce the computational complexity as much as possible while satisfying imaging accuracy. Therefore, unnecessary calculation steps should be eliminated as much as possible when real-time imaging is achieved. At the same time, real-time imaging needs to adopt a streamlined design, that is, part of the data is processed first, until the data volume reaches the full aperture, the azimuth pulse compression map is performed. For a longer imaging process, first perform imaging processing for each two full-aperture data to produce respective images. In order to ensure that all points are fully resolved, only the image size of one full-aperture in each image is retained, and two adjacent images Image stitching is performed by overlapping in half. At this time, the data processing of the overlapping part can be retained as for the imaging process of the next image. By analyzing the parameters of the designed system, the complexity of the real-time algorithm is reduced. The system parameters are shown in Table 2.

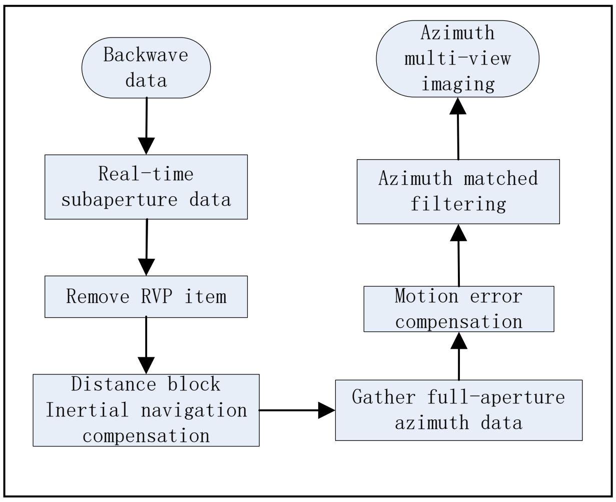
TABLE II. THE SYSTEM PARAMETERS

Parameter	Value
Transmit waveform	FMCW
Receiving method	Dechirp reception at 0 distance
Signal bandwidth /GHz	2
Pulse repetition frequency/Hz	2000
Distance resolution/m	0.075

The Dechirped signal needs to be processed in the RVP item to eliminate the influence of the remaining phase on the azimuth focus. For the Dechirp received signal, in order to better integrate with the imaging algorithm, the design adopts the processing method of Dechirp to direct acquisition and reception. Through calculation, it can be obtained that the beam width at a distance of 8° corresponds to a ground width of 222 m, and the oblique distance is 300 m on the plane. The number of sampling points with a width of 200 m and a distance resolution of 0.01 m is 2000 points. Considering that the beam width corresponds to 4,000 points in the scene, the maximum number of points for range imaging only needs to be 4 096 points. The optimal azimuth resolution is 0.11 m×1.2=0.13 m. The maximum azimuth bandwidth is less than 300 Hz. Considering the PRF of 2000, one azimuth data extraction can be done. The total aperture data points are within 2000 points. Considering the decimation of the azimuth, there are only 1000 points.

Through analysis, it can be known that due to the limitation of beam width, the designed system can meet the imaging width requirement with a maximum distance of 4,096 points, and the azimuth direction can meet the requirements of full-resolution imaging with azimuth at 2,048 points. At the same time, the distance migration is less than one distance unit, so the influence of distance migration can be ignored, thus canceling the steps of distance migration correction. The flow chart of the designed real-time imaging algorithm is shown in Figure 3.

Fig. 3. The real-time imaging algorithm flowchart



The recorded sub-aperture echo data is processed once. First, the RVP item is corrected to remove the azimuth phase modulation caused by the Dechirp reception. This step can process each recorded echo, and it does not have to be accumulated to a certain number of pulses. The sub-aperture echo data. Then the distance is divided into blocks to estimate the motion error[6,7]. This is because the distance change of the motion error cannot be ignored due to the short observation distance. It is necessary to realize the distance change estimation of the motion error through the fitting of multiple distance blocks. The motion error estimation of each sub-block is realized by PGA. When the data volume is accumulated to 2048 points, the azimuth data has reached two full aperture lengths. A full-resolution image with a full aperture size can be obtained through matched filtering, motion error compensation is performed on the data, and imaging is achieved through azimuth matched filtering. , And finally do the azimuth multi-view imaging[8,9,10].

IV. Imaging Test Results

The radar flight test platform is a small unmanned helicopter. After completing the joint test with the aircraft's avionics interface, it has undergone multiple flight test verifications. The various working modes of the radar have been evaluated. The radar image is well focused and has clear levels. Important indicators such as operating distance, width, and resolution in the mode meet the requirements. The real-time SAR image of a flight test in a certain place is given.

It can be seen from Figure 4 that the system in this paper can stably obtain high-quality real-time SAR images on a small UAV platform, which proves the effectiveness and reliability of the system.

Fig. 4. The real-time SAR image

V. Conclusion

This paper takes the SAR real-time processing system as the research focus, and verifies the effectiveness of the SAR real-time imaging processing system through the measured data processing results. The system uses FPGA as the core to realize SAR real-time imaging processing, and the external functional modules realize a highly integrated architecture, simple and lightweight structure; and through system monitoring to perform fault detection and diagnosis of the system, the miniature SAR system has a small size, light weight, Key technical requirements such as strong processing capability and high reliability; the results of the field test show that The technical scheme adopted by the SAR system is advanced and effective, and the real-time processing method is novel, and satisfactory imaging results have been achieved.

References

[1] Bao Zheng, Xing Meng-dao, and Wang Tong. Radar Imaging Technology[M]. Beijing: Publishing House of Electronics Industry, 2005: 186–220.

[2] Zhou Hui, Zhao Feng-jun, Yu Wei-dong, et al.. SAR imaging of ground moving targets with non-ideal motion error compensation[J]. Journal of Radars, 2015, 4(3): 265–275.

[3] WANG Hui, ZHAO Feng-Jun, DENG Yun-Kai. Development and application of the millimeter wave SAR[J]. J.Infrared Millim. Waves, 2015, 34(4):452~459.

[4] Wahl D E, Eichel P H, Ghiglia D C, et al.. Phase gradient autofocus-a robust tool for high resolution SAR phase correction[J]. IEEE Transactions on Aerospace and Electronic Systems, 1994, 30(3): 827–835.

[5] Qing Ji-ming, Xu Hao-yu, Liang Xing-dong, et al.. An improved phase gradient autofocus algorithm used in real time processing[J]. Journal of Radars, 2015, doi: 10.12000/JR15037.

[6] John Jr. C K. Motion compensation for synthetic aperture radar[J]. IEEE Transaction on Aerospace and Electronic Systems, 1975, 11(3): 338-348.

[7] Meng Da-di, Hu Dong-hui, and Ding Chi-biao. A new approachto airborne high resolution SAR motion compensation for large trajectory deviations[J]. Chinese Journal of Electronics, 2012, 21(4): 764-769.

[8] Wang H , Zhang H , Dai S , et al. Azimuth Multichannel GMTI Based on Ka-Band DBF-SCORE SAR System[J]. IEEE Geoscience and Remote Sensing Letters, 2018:1-5.

[9] Hui W , Chen Z , Zheng S . Preliminary Research of Low-RCS Moving Target Detection Based on Ka-Band Video SAR[J]. IEEE Geoscience and Remote Sensing Letters, 2017, PP(6):1-5.

[10] A Modification to the Complex-Valued MRF Modeling Filter of Interferometric SAR Phase[J]. IEEE Geoscience and Remote Sensing Letters, 2014, 12(3):681-685.