The Design of UART Controller Based on FPGA

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Abstract. This paper introduces a method to implement UART based on Field Programmable Gate Array（FPGA）. Its baud rate can be set and the states can be read. The structure of this system is divided in modularization so that can fit the method Top-Down. The hard core of this system is implemented with finite state machine （FSM） [1]. It makes the logic of control more intuitionistic and more briefness. The efficiency of the design is improved in a wide range. Simulating experiments, present at last to proved the validity and reliability in the whole design.

Keywords: UART, FSM, FPGA.

1 Introduction

Asynchronous serial communication that requires a few of Transmission lines, high reliability, and faraway transmission distance, is widely applied of the data exchangement of microcomputer and peripheral. Usually it is complimented by UART (Universal Asynchronous Receiver-Transmitter), For example of National INS 8250 as chip of serial interface in the IBM PC. In the practical application, some main functions of UART are required. Special interface chip may cause a waste of resources and high costs, especially the technology of SOC in the field of electronic design will implement the function of the whole system on single block or few blocks of chips. So designers should make the similar function module integrated into FPGA. This paper puts forward a way of realizing the function of UART using FPGA. The above problems can be resolved effectively.

2 Function Introduction

This UART controller transmit a frame serial data including 1 start bit, 8 bits of data and 1 bits stop bits. When ransmission, low bit is in the front, high bit is in the post. Receiver detects and confirmes the start bit, 8 data bits will be received. After receiving the stop bit ,Interrupt signal will be transmitted toward CPU, in the same time Data will be transmitted to the computer 's 8 bit data bus. When sending data ,Baud rate is seted up by CPU. Then the 8 bit parallel data plus the start bit and stop bit is sent to the peripheral. After sending the stop bit, Interrupt signal will be transmitted toward CPU.In the process of sending and receiving data, CPU can load control signal to read

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the working state of UART, in order to conduct real-time processing. The basic UART communication requires only two signal lines (RXD, TXD) to complete the data communication. Receiving and sending is duplex form.TXD is the UART's sending terminal, as output; RXD is UART 's receiver, as input.

3 The Realization of Function

3.1 The Overall Structure of the System

In large scale circuit designs, a hierarchical, structured design method is widely used. It will divide a complete hardware design tasks from the system level, into a number of operational module, work out corresponding model and simulation, finally make combination in the system level. This improves the design efficiency and the design quality, and is the major means of implementing complex system[2],witch is the basis of design idea in this paper. UART consists of three modules, namely the baud rate generator; the receiving module; transmitting module.

3.2 Design of Modules

3.2.1 Top Level Module

The top-level module of UART consists of a baud rate generator, a receiving module and a sending module.The UART transmitter is used to transform the parallel data for output in accordance with the basic UART frame format to TXD signal serial output.UART RXD receiver receives the serial signal, and converts it into parallel data[3].Baud rate generator specifically produces a local clock far higher rate than the baud rate to sample the input RXD continuously to enable the receiver to maintain synchronization with the transmitter。 Circuit diagram is shown in figure 1.

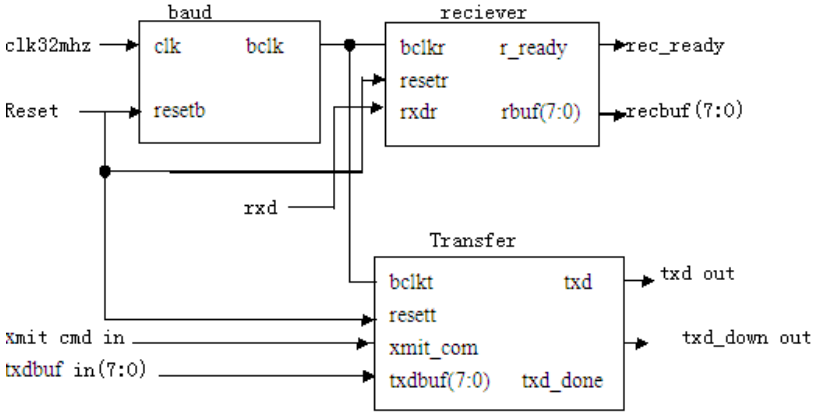

Fig. 1. Circuit diagram of top-level module

3.2.2 Baudrate Generator

Baudrate generator is a frequency divider in fact. We could calculate the baud divisor according to the given system clock and the required baud rate.Baud divisor needs to change according to different applications.The design needs to devide a frequency of 32MHz signal into that of 153600Hz signal.

3.2.3 The UART Receiver

Due to the serial data frame and a receive clock is asynchronous,by logic 1 to a logical 0 can be considered a data frame start bit.However,in order to avoid burr effect and get the correct starting bit , we must request that there is at least half of logic 0 in the received start signal in the process of sampling baudrate clock .Because internal sampling clock cycle is 16 times of transmitting or receiving baud rate clock cycle , the start bit requires that at least 8 consecutive BCLK cycle logic 0 was received.Then data bit and stop bit are sampled every 16 BCLK cycle time .

R_START STATE：After the UART receiver is resetted, the receive state machine is in this state when the state machine has been waiting for the RXD level jump, that from a logical 1 to logic 0 means the beginning of a new frame of UART data frame.Once the start bit is determined, the state machine will transfer to the R_CENTER state.RXD_SYNC signal is RXD sync signal.In the judgment of logic 1 or logic 0, we do not wish the detected signal is not stable, so we do not detect RXD signal.

R_CENTER STATE：For the asynchronous serial signal,in order to detect the correct position signal every time ,detecting in each of the midpoint is advisable.In this state,we calculate mid point of each bit through the number of BCLK counts.But most probably the count value " did not actually happen to the "1000", a state should to be considered, namely after a BCLK cycle, the 1 / 2 bit in sampling is hoped .

R_WAIT STATE：When the state machine is in this state,in the sixteenth BCLK, it enter the R_SAMPLE state for data bit sampling detection, but it also determines whether the data bit length has reached a data frame length (FRAMELEM), if it come, the stop bit is coming.

R_SAMPLE STATE： After the inspection of Data bit sampling , it refers to the R_WAIT state unconditionally, waiting for the next bit of data.

R_STOP STATE：The state machine is without the specific detection of RXD in R_STOP state, just output the end signal of frame receiving (REC_DONE < = ' 1'). After this state, state machine comes back to the R_START state, waiting for the start bit of the next frame .

3.2.4 The UART Transmitter

The transmitter output one data every 16 BCLK cycle , follow that the first bit is start bit, and the eighth is stop bit in order.

X_SHIFT STATE：After the UART is resetted, the state machine is in this state when the UART transmitter has been waiting for a data frame to send commands to XMIT_CMD.Because XMIT_CMD is an external signal, it is not possible to limit the XMIT_CMD pulse width.If the XMIT_CMD is still valid after he UART has sent a data frame , then the error is considered, a new command of data transmission is coming again.The UART transmitter will start sending frame of UART again. Obviously, the frame sent is wrong.In this time,XMIT_CMD is limited on the pulse

width , use XMIT_CMD_P instead of XMIT_CMD signal, XMIT_CMD_P is a short pulse signal.When XMIT_CMD_P = ' 1 ',the state machine refer to X_START STATE, ready to send the start bit.

X_START STATE：In this state,the UART transmitter sends a logic 0 of one bit time width to TXD, i.e. the start bit.The state machine come into X_WAIT stateFollowed.

X_WAIT STATE：In this state, the state machine waiting for the sixteenth BCLK, when it comes,it refer to the X_SHIFT state, to convert the parallel data to the serial data.

X_SHIFT STATE：State machine realizes conversion of data to send. After switching it comes back to the X_WAIT state.

X_STOP STATE：Stop bit send state namely.When the data frame is sent, the state machine comes into this state, and sends logic 1 signal of 16 BCLK cycle, i.e., 1 stop bit.After the stop bit is sent ,the state machine comes back to the X_IDLE state, waiting for another command to send a data frame.

4 The Simulation Results

During the verification process, I use Modelsim in the Company of Model Technology to conduct function simulation on the UART controller.

4.1 The Simulation Waveform of UART Receiver Is Shown in Figure 2

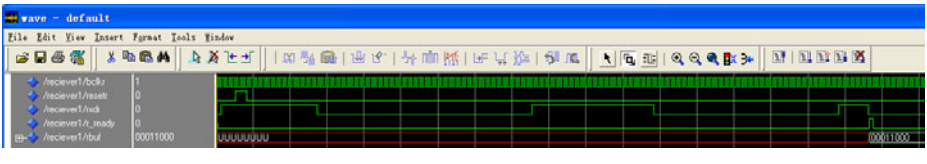

Fig. 2. The simulation waveform of UART receiver

4.2 The Simulation Waveform of Uart Transmitter Is Shown in Figure 3

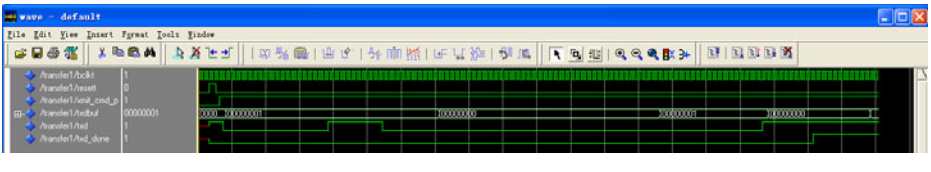

Fig. 3. The simulation waveform of UART transmitter

Through the simulation waveform , the design results correctly transmits and receives a frame data and generates a corresponding interrupt, CPU can read real-time working state.the correction and completion of this design is validated, all functions meet the expected requirements, but it also show that the design idea is completely feasible.

Using FPGA to achieve UART reduces the system area and the power consumption, improves the design of stability, but it also makes full use of the remaining resources in FPGA.The method of software realization of hardware has become the dominant trend in the field of electronic design.In many occasions, the UART controller can completely replace the dedicated IC chip.The design has already been downloaded to Xilinx 's Spartan3 series XC3S400 devices.Comprehensive report displays that the design has consumed 195 LE (Logic,Element) .in large-scale FPGA, this is only a small part of resources.

References

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