On the Implementation of VLSI Architecture of FM0/Manchester Encoding and Differential Manchester Coding for Short-Range Communications

Siva Jyothirmai Gali and Sudheer Kumar Terlapu

Abstract The encryption is the method for converting information into a desired format for a number of information processing needs. It encompasses data transmission storage and compression. In order to have safe data transmission, different types of encoding techniques are developed. Especially for short-range communications, various protocols are used to encode the information. Intelligent transport system needs modernized services for the management of traffic may generally uses Manchester and FM0 encoding. This process improves constancy in signal by dc balancing. The coding Manchester and FM0 methods of code control the VLSI architecture. Also similarly oriented logic simplification (SOLS) technique was proposed for controlling the hardware architecture. By using this technique, the (HUR) hardware utilization rate is increased from 58 to 100%. Also, differential Manchester encoding achieved good dc.

Keywords Dedicated short-range communications (DSRC) · FM0 Manchester · Similarly oriented logic simplification (SOLS) · DC balancing

1 Introduction

The dedicated short-range communication (DSRC) is a procedure of communication for one way, two way, and medium range [1]. DSRC was divided into two types, they are automobile–automobile and automobile–roadside. In the first type, DSRC activates the message transfer and broadcasts it to the automobiles [2]. The second type of DSRC is mainly targeted on intelligence transportation services, for example, electrical tollgate collection. Basically, the encoding process is done for

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safe transmission [3] of data. The basic block diagram of DSRC consists of two parts: upper and lower. The top part is for transmission of data and the bottom part is for receiving. Those are transmitter and receiver.

This paper developed Manchester encoding for safe communications [4]. RF-frontend sends and collects the wireless signal using antenna. The signal which is transmitted was supposed to get mean as zero for [5] tough issue. This will be mentioned as dc balancing. The signal which is transmitted contains binary series. Due to this, it is hard to get the dc balance. This [6] problem of dc balancing may be overcome by using FM0 and differential Manchester encoding. Cryptography been popularly used these days in the applications like intelligent transportation and Automated machines [7]. Multipliers of redundant basis were popular due to low complexity [8].

In this paper, first section briefly explains the introduction of the paper. The coding variety for both encodings severely controls the potentiality to draw VLSI structure which is reusable with one another. In this work, the VLSI structure was designed. And second section contains hardware structure of encoder. And its subsections clearly explain dc balance problem and area retime problems and their avoiding methods.

And differential Manchester encoder was explained in third section. Section 4 gives the simulation results of the given encoders with the explanation of operation, also the comparison for conventional and proposed structures.

2 Hardware Architecture for Fm0 and Manchester

Here, the two D-flip-flops (DFFs) which are used to store the state code and mux are used to select the logics of A(t) and B(t) by considering clock as select line. And finally, the mux with mode is used to select the type of encoding among FM0 and Manchester here mode is considered as selection line. If mode = 0, then it will select FM0 code and mode = 1 it will give Manchester code. To get the hardware utilization rate, we have to consider both active components and total components. It will be evaluated as HUR

The block diagram mainly contains two portions top and bottom. One is transceiver and receiver given in Fig. 1. The transceiver end consists of three units. They are baseband processing, RF-frontend, and microprocessor. The microprocessor takes the guidelines from media accessing control in order to program the function of baseband processor and RF-frontend. Baseband processing itself is reasonable for correcting errors, modulation, encoding, and clock synchronization.

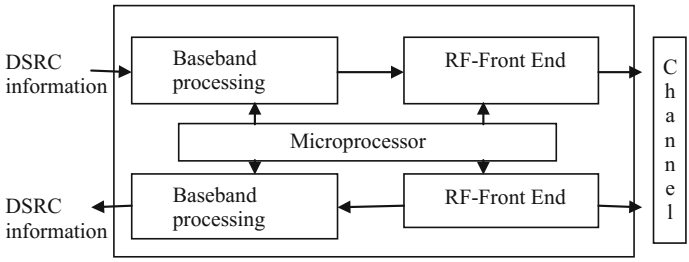

Fig. 1 Block diagram of DSRC

2.1 SOLS Technique

Similarity-oriented logic simplification (sols) is a fully reused structure of FM0 and Manchester. This technique is classified into two parts, they are: (i) Area compact retiming and (ii) Balance logic operation. The functioning of SOLS is given below.

The two encoders are given to mux so that FM0/Manchester output is obtained. The upper portion is FM0 encoding and down portion is Manchester code. The path will be selected as shown in Fig. 2 and the operation is carried out based on the given logic.

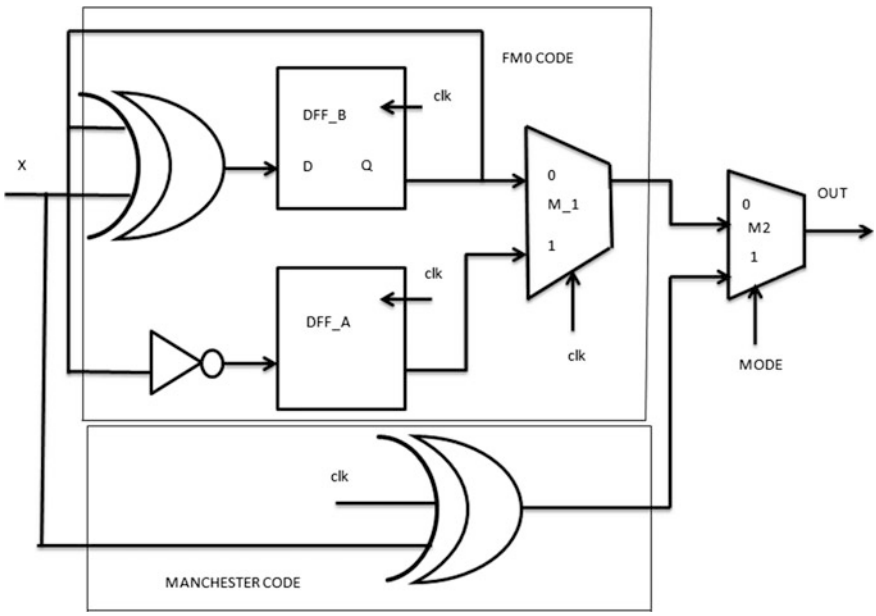

Fig. 2 Hardware architecture of FM0 and Manchester encoder

2.2 Area Compact Retiming

The components which we are used in the architecture are assumed as hardware as they perform operations logically. Here, the active components are nothing but the components which undergo work in the functioning of circuit. And the total components are the components of the entire circuit irrespective of those which involve in functioning. If the number of components which are not involving in operation is present in circuit, some of the hardware will be wasted due to this area and the power will increase. So that in order to make the HUR rate as 100%, the unusable components will be minimized or avoided, so that the count of transistor will also be reduced. For example in FM0 encoding, it consists of two DFFs, those two DFFs are for storing the states of A(t) and B(t). Instead of storing those values, it may be better to store the value which will be selected by mux among A(t) and B (t). So that the value will be stored in single DFF. Due to this, the hardware may reduce and HUR will become 100%. The architecture by considering both DFF is referred as FM0 without area compact retiming as shown in Fig. 3. Finally by reducing hardware that is one DFF is referred as FM0 with area compact retiming as shown below.

2.3 Balance Logic Operation Sharing

To avoid the dc balancing problem the architecture is modified by placing inverter after the mux_1. Due to irregular transmission of signal, dc balancing problem may occur which leads to logical errors in code.

Because of dc balancing, unbalancing calculating time may occur between logics and it may result in formation of glitches at mux_1, to avoid this unbalance calculating time, the logic is modified. If more selection of logic modification is done, the XOR operation may lead to inverting of its function at inverter again, to alleviate this problem, XOR is replaced with XNOR results in correct value of XOR at inverter. For selection of logic, mux with mode mux_2 is used so that it acts as

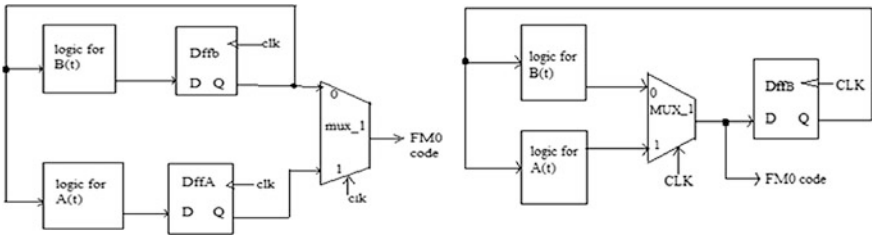

Fig. 3 FM0 without area compact retiming and by area compact retiming

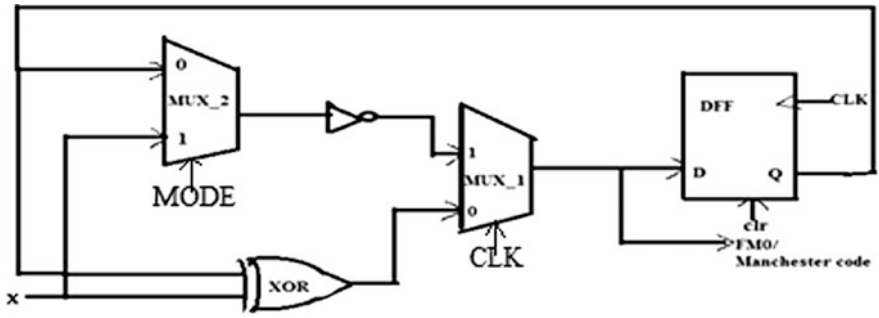

Fig. 4 Unbalanced computation

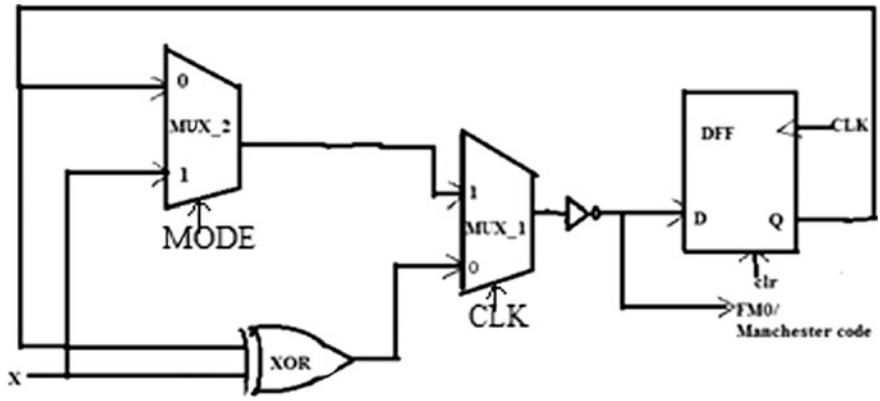

Fig. 5 VLSI architecture for balance logic

selection line. Finally, the assumption of FM0 or Manchester encoding depends on mode and also the clear (clr) is used in DFF. Hence, every component involved in working of FM0 and Manchester encoding given in Figs. 4 and 5. Further HUR is also increased.

3 Differential Manchester Encoding

The Manchester encoding was modified as differential Manchester encoding. Both Manchester and differential Manchester are visibly the same, but for a change in transitions at edge of the bit. Transition in between windows will occur at input "0" and no transition occurs at input "1". The architecture of differential Manchester encoding is as given in below figure. It contains a D-flip-flop which stores current state of A, after that mux in this architecture selects the state which is the next

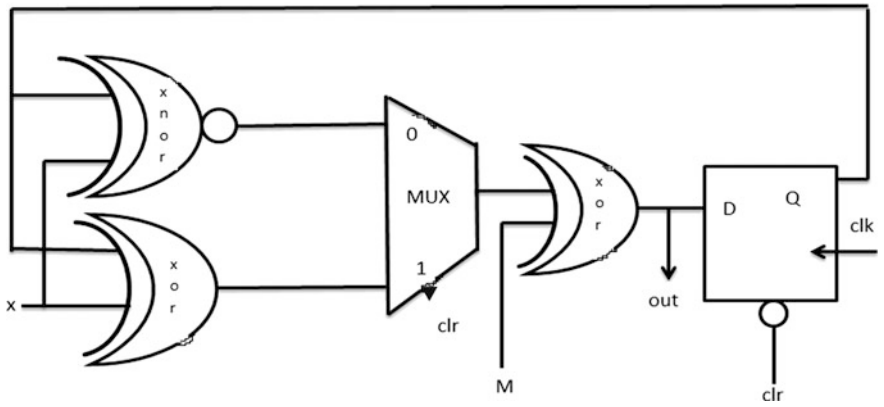

Fig. 6 Differential Manchester encoding

values of A and B as per the clock. Mode signals, flip-flop clear signal and M are used for selection among Manchester and differential Manchester.

In the mode of Manchester, clear is activated which makes "0" in the place of present value A and M = 1 which turns XOR_2 to play an inverter role. In differential Manchester as shown in Fig. 6, when mode = 0 and clr = 1, the present value of A is transferred as input to next state and XOR_2 behaves like a buffer (Table 1).

Table 1 Performance comparison table

Parameters	Existing	Proposed
Maximum frequency (MHz)	444.545	562.762
Slices	2	1
Flip-flops	2	1
LUTS	4	2
Bonded IOBS	5	6
Registers	2	1
XORS	2	1
Real time to Xst (s)	1	0
Cpu time to Xst (s)	0.19	0.20
Global min fanout	1000000	500
Path delay (ns)	6.125	5.776
Total real time (s)	5	4
Total cpu time (s)	4.45	4.40

4 Analysis of Experimental Results

The process of simulation is done by considering the Verilog code simulated in Xilinx. Clock (clk), clear (clr), mode, x acts as inputs for this process, whereas the output of DFF will be fed back to XNOR and first mux acts as inputs, output for complete circuit is taken at inverter output given as FM0/Manchester. Here, when the mode is 0 and clr is 1, it will generate the FM0 code, similarly Manchester code is generated for other values of mode and clr. FM0 code is based on clock, i.e., when clock is low it will get internal transitions. When clock is high, it remains constant till the next clock cycle.

Similarly in differential Manchester, encoding is also simulated in Xilinx. Clr and clk act as input in the circuit. Out is taken as output at second XOR. One of the inputs for first XOR and XNOR is fed back from flip-flop. Their simulated results are given in Figs. 7 and 8.

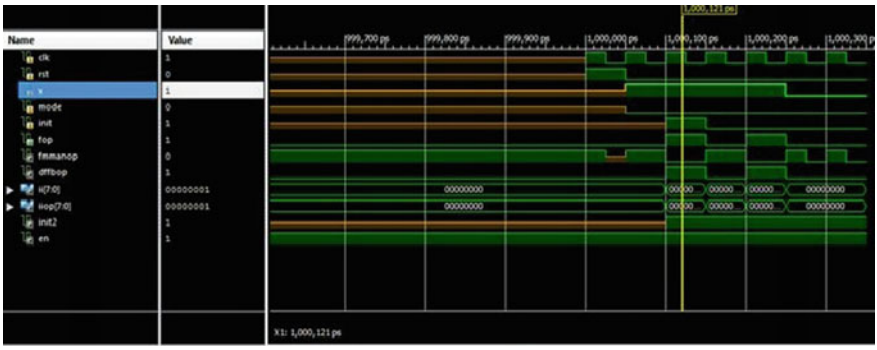

Fig. 7 Simulation results of FM0/Manchester encoder

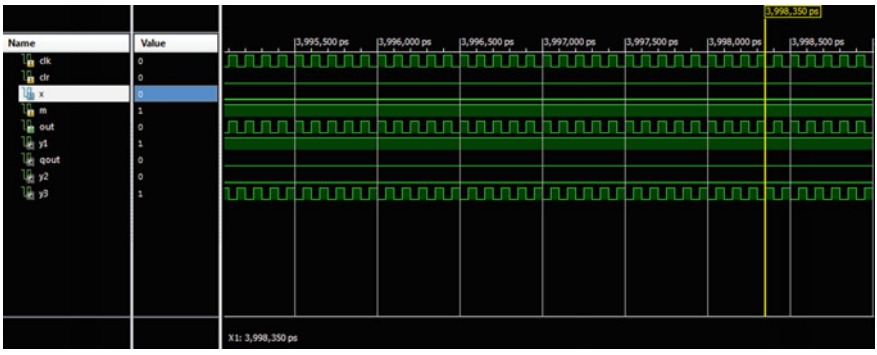

Fig. 8 Simulation results of differential Manchester encoding

5 Conclusion

The work contains completely integrated VLSI architectures of FM0 Manchester and differential Manchester encodings. These encrypting methods are generally used for short-range communications. This work is compared with the existing architecture so that it reduces the delay and hardware usage of circuit is also improved. By assuming the proposed work, the number of transistors is decreased. This work is performed in Xilinx. These architectures are examined with other existed designs. The resource usage estimated values are also reported in a tabular form.

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