# **End-to-End Test Strategy for Wireless Systems**

Madhuri Jarwala, Duy Le, Michael S. Heutmaker

# AT&T Bell Laboratories Engineering Research Center Princeton, NJ 08542

#### **Abstract**

This paper proposes an end-to-end test strategy for wireless systems described by using wireless microcell as a vehicle. It presents a framework for testing digital and Radio Frequency (RF) boards in a wireless system and provides an integrated solution. The test strategy is based on two concepts: using Boundary-Scan for digital testing, and using Boundary-Scan to provide a gateway for DSP-Based functional testing of RF circuits. The test signals are generated within the system and the test control and verification are also provided by the system leading to system self-test.

## 1 Introduction

Due to the continuing demand and growth in the wireless marketplace, high volume manufacturing of high frequency, high performance, miniaturized, wireless products has become necessary. These products present unique test challenges.

- The trend towards miniaturization of both the base station and terminal equipment has decreased test access and increased test complexity.
- The integration of digital, analog, and RF functions on the same board has made testing more difficult as the traditional methods of testing may not be adequate under these circumstances.
- High volume manufacturing requires test solutions that have high throughput and low cost.
- The globalization of the manufacturing process requires test techniques that do not need expensive test equipment, are portable, and integrated with design.

In this paper, an end-to-end system test strategy that proposes an integrated solution for digital, analog and RF circuits is presented which addresses the above test issues. In this scheme, the test signals are generated within the system and the control operations for testing and verification are also provided by the system. Therefore, this strategy provides a system level self-test approach.

An end-to-end test strategy is required because test spans the entire Product Realization Process (PRP). In the assembly hierarchy, testing is required at each level - device, board, and system and at each stage of product life cycle - design, prototype, manufacturing, system, installation, and field. An integrated test strategy can therefore have an impact on cost, time, and quality in the PRP. It can reduce test development time and improve time to market, reduce product cost by reducing the capital cost of the test equipment, and improve product quality by enabling innovative assembly and packaging techniques.

With the current revolution in the wireless marketplace, demand for miniaturized wireless products is expected to grow continuously. Some of the advanced manufacturing technologies that will be required to meet this demand are increased use of ASICs, custom logic, and MCMs, use of multilayer boards with active components on both sides, use of fine pitch components, BGAs, and testing boards from edge connector instead of in-circuit testing. Testing high density, miniaturized products assembled using these advanced manufacturing technologies will require the use of sophisticated test techniques such as Built-In Self-Test (BIST) and Boundary-Scan for digital testing and Digital Signal Processor (DSP)-based functional testing of RF and analog circuits. In the test strategy proposed here, Boundary-Scan testing [1] is combined with RF loop-back testing [2] and DSP-based functional testing [3] to provide an end-toend solution. This test strategy is described by using wireless microcell as a vehicle; however the test strategy can be generalized to any wireless system.

This paper is divided into six sections. In section 2, microcell architecture is described. The end-to-end test strategy to test wireless systems is proposed in section 3. Section 4 describes how this test strategy works with the five wire system test bus architecture. The benefits of the test strategy and issues related to implementation are discussed in section 5. Section 6 contains conclusions.

Paper T2.2 940 INTERNATIONAL TEST CONFERENCE

0-7803-2991-0/95 \$4.00 © 1995 IEEE

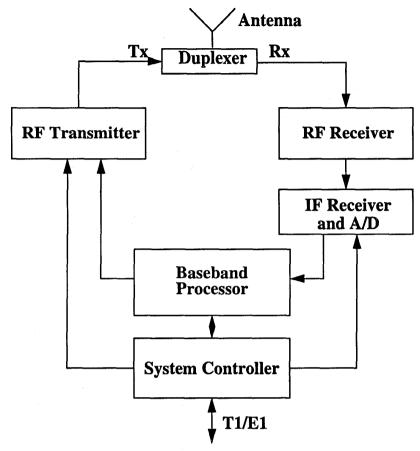


Figure 1: Architecture of a Typical Wireless Microcell

## 2 Microcell Architecture

A wireless microcell is a miniaturized base station used in cellular or Personal Communications Network (PCN) that converts digitized voice and/or data supplied by a network into RF signal for transmission to a remote wireless terminal and also receives RF signals transmitted from a wireless terminal and converts them into digitized voice and/or data for transmission back to the network. A simplified block diagram of the architecture of a typical microcell is shown in Fig. 1. It consists of System Controller and Baseband Processor which form the digital portion of the system, and Transmitter, Duplexer, Antenna, and Receivers which form the RF portion of the system. The details of microcell architecture and application are discussed in several recent papers such as [4, 5]. The high level functionality and the details of the functional blocks that will be impacted by the end-to-end test strategy are discussed below.

The System Controller controls the Baseband Processor and interfaces to the network. It includes a micro-processor and

memory for controlling the system. The Baseband Processor processes audio signals and contains DSPs for this purpose. The Transmitter modulates the audio signals on a RF carrier signal and transmits the signal to Antenna via Duplexer which separates transmit and receive paths. The Receiver amplifies the RF signal from the Antenna, and downconverts it to produce the Intermediate Frequency (IF) signal. The combined IF Receiver and Analog to Digital (A/D) Converter converts IF signal to digitized baseband signal which is then processed by the Baseband Processor. This basic microcell architecture is modified to implement the test strategy as explained in the next section.

## 3 Proposed End-to-End Test Strategy

The end-to-end test strategy for wireless systems is based on two concepts:

- 1. Using Boundary-Scan for digital testing, and
- Using Boundary-Scan to provide a gateway for DSP-based functional testing of RF sub-systems

These concepts are briefly described below.

# 3.1 Boundary-Scan Testing

IEEE Standard 1149.1-1990 defines the basic architecture of Boundary-Scan (B-S) that includes a four-wire (optionally five) serial interface, the test logic on each device, and the protocol for communicating with this logic. It defines a method for controlling/observing each input/output of every device on a board [1]. Boundary-Scan is used for testing interconnects between B-S devices on a board, testing non B-S devices/interconnects using the access provided by B-S, applying static tests to internal device logic via B-S register, etc.

# 3.2 DSP-based RF Testing

In DSP-based RF testing an RF transmission path is tested by measuring the characteristics of a modulation signal instead of the RF carrier. The test data consists of samples of the modulation at the input and/or output of the RF path, and this sampled signal may be analyzed by DSP techniques. This approach enables the recovery of some analog RF performance characteristics from digitally modulated signals for a variety of modulation schemes. The usefulness of this scheme for RF testing is that some of the performance characteristics at radio frequencies are preserved in the modulation signal, independent of the up-conversion and down-conversion of the carrier frequency [6].

## 3.3 Test Methodology

The test strategy uses divide and conquer approach. The digital portion of the system is tested separately from the RF. Boundary-Scan test techniques are used for testing the digital boards and system. After verifying correct operation of the digital portion, the RF sub-system is tested by DSP-based RF test techniques. The DSP-based RF testing is facilitated by a system test architecture (described in section 4) which can download and upload data to the DSPs in the Baseband Processor board for testing and provide the required control operations. No separate instrumentation is required as the test signals and test control are generated within the system for both RF and digital testing thus providing an integrated solution.

The test strategy developed to test the typical wireless microcell architecture is shown in Fig 2. The additional test hardware required for the strategy is shown in shaded blocks in the figure. The test methodology is as follows:

#### 1. Partition Digital and RF

The digital portion of the system containing the System Controller and the Baseband Processor is partitioned from the RF portion.

2. Test System Controller using B-S

In the test strategy, the devices used in the System Controller have B-S architecture [1]. The System Controller includes a Boundary-Scan Master (BSM) device [7,8] which is used with the microprocessor, for the Boundary-Scan testing of the System Controller and the Baseband Processor. The System Controller also includes a commercially available slave interface device such as Addressable Scan Port (ASP) [9,10] manufactured by Texas Instruments or a Scan Bridge device [11,12] from National Semiconductor. The slave interface device distributes the B-S test signals generated by BSM to the digital devices on the System Controller board that are to be B-S tested by the BSM. The System Controller may need extra memory to store test patterns for testing RF Transmitter, RF Receiver, IF Receiver, and A/D Converter. The test patterns may also be stored on disk. In the test strategy, interconnections of the digital devices on the System Controller board (except the microprocessor and the memory) are tested via B-S.

## 3. Test Baseband Processor using B-S

In the test strategy, the DSPs and other devices with B-S architecture are used in the design of the Baseband Processor board so that the interconnects can be tested using B-S techniques. A slave interface device identical to the one in the System Controller is used in the Baseband Processor. It distributes the test signals supplied by the BSM within the Baseband Processor. A five wire backplane system test bus is used for connecting the BSM to the slave interface device. The backplane bus was first described in [13]. Its application to the wireless systems is discussed in section 4.

The DSPs in the Baseband Processor board have B-S architecture and perform additional functions for DSP-based RF testing such as controlling separate testing of the transmit and receive paths and interfacing with the system test bus.

### 4. Test Transmit path using DSP-based RF Testing

In the test strategy, hardware is added to facilitate separate testing of the transmit and receive path. A Coupler is added to the transmit path to couple the transmit signal to an Attenuator. The Attenuator attenuates the RF signal and provides it to a Downconverter where the frequency of the signal is lowered. A/D Converter is then used to convert analog signal to digital signal. The additional hardware for the transmitter test is a partial duplication of the receiver functionality of the system. However, it makes independent testing of the transmit path possible which provides better diagnostic resolution and more accurate measurement. Depending on the desired measurement accuracy and the diagnostics needed in a given system, a trade-off between the transmitter hardware overhead and the overall test effectiveness can be made.

After the correct operation of the System Controller and the

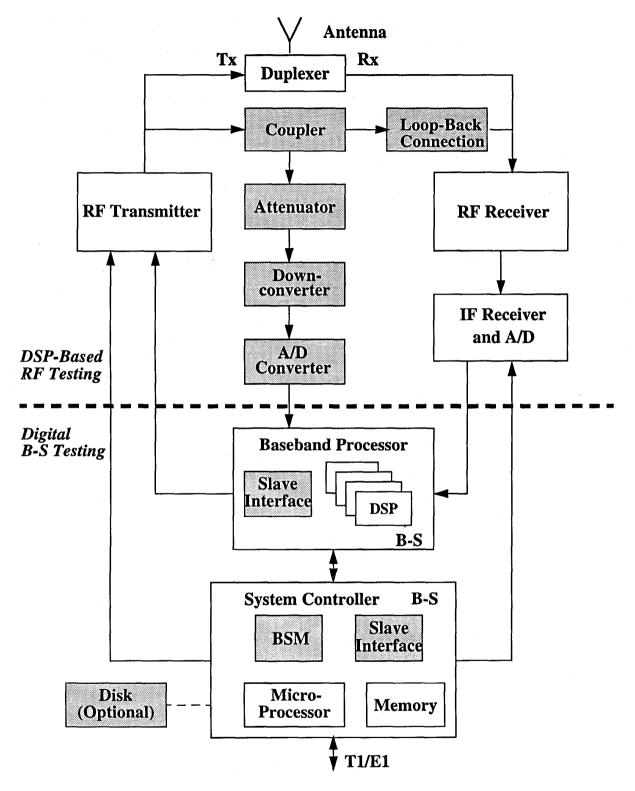


Figure 2: End-to-End Test Strategy for Wireless Microcell

Baseband Processor is verified, the BSM on the System Controller board is used to down load the test patterns to the DSPs in the Baseband Processor. The test signal is sent to the transmit section and the response is observed via the return path provided by the Coupler, Attenuator, Downconverter, and A/D Converter. The complete operation of the transmit path can then be verified by using DSP-Based functional tests.

# 5. Test Receive path using DSP-based RF Testing and Loop-Back

A loop-back connection is used to test the receive path. A loop-back connection is made by using a wide band filter or a cavity filter. Loop-back testing is presently performed in some wireless products, and no modification of the loop-back connection [2] is necessary to implement the end-to-end test strategy. For test purpose, the Coupler is used to feed RF signal to the Loop-Back connection. The Loop-Back connection performs two primary functions. It attenuates the signal and shifts the frequency of the signal to that acceptable by the Receiver. The Loop-back connection may also be made beyond the antenna, for instance with a mobile unit, which would eliminate the hardware overhead in the base station system.

In the test strategy, after the correct operation of the transmit path is verified, the receive path is tested. The test signal generated by the B-S controlled DSPs, after passing through the transmit section is coupled into the receive section via the Loop-Back connection and processed back to the Baseband Processor. The received signal is compared with the expected response to determine the correct operation of the receive path. Finally, other tests required to test the system as given in the system test requirements document can be carried out using the Loop-Back path. The loop-back tests both the transmit and receive paths at the same time. Therefore, if there is a fault, it will not be able to isolate the faulty subsystem between the transmitter and receiver. Hence separate testing of the transmit path prior to loop-back testing is recommended. (In the systems where transmitter and receiver are on the same board, only loop-back testing will be sufficient.)

It can be seen that the end-to-end test strategy does not require external test instrumentation.

# 4 System Test Architecture

In this section, how the end-to-end test strategy for wireless systems is integrated with the system test architecture is discussed. The system test architecture supports a multi-drop configuration using an 1149.1 backplane test bus. Figure 3 depicts this system test architecture. The architecture has the following features:

1. The backplane test bus contains the 5 physical wires with

the familiar 1149.1 signal names (TDI, TDO, TMS, TCK, and optional TRST\*).

- 2. An AT&T Boundary-Scan Master (BSM) device located on the System Controller board controls the communication on the 1149.1 backplane test bus and the 1149.1 testing on the boards in system. The BSM has BIST that can be invoked to verify its operation.
- 3. The slave interface devices provide the board interface to the 1149.1 backplane test bus. They are addressable via a communication protocol and connect a selected board to the bus for testing.
- 4. The microprocessor on the System Controller board controls the operation of the BSM for initiating BIST/B-S tests and reading the test results. Test vectors for the system can be stored locally in on-board memory or external disk.
- 5. In system, the microprocessor, vector storage memory, and the BSM make up the system test controller for B-S testing. So they cannot be tested via B-S in-system. But the rest of the B-S logic on the System Controller board can be B-S tested via the slave interface access.

The system backplane test bus is used to carry out structural tests in the digital portion of the system [13]. If the RF part of the system uses the proposed end-to-end test strategy, then the system test bus can be used for functional testing in addition to the structural testing. For testing the RF portion of the system, the BSM can download test programs/data into the DSPs and up load test responses via the 5-wire system test bus. Therefore, in addition to being used for testing purpose, the system test bus can be used as a gateway to functionally program the DSPs. The system test bus is used for both the structural testing of the digital boards and the functional testing of the RF boards thus providing an integrated test solution. This is a novel and unique feature of the end-to-end test strategy.

# 5 Benefits

The benefits of the end-to-end test strategy are as follows:

- It provides an integrated end-to-end test solution that covers digital, analog, and RF circuits.
- The test signals generated within the system are used for testing thus leading to system self-test.
- The test strategy provides a hierarchical approach that can be used at the various levels in the assembly device, board, system, and in the product life cycle design, manufacturing, field.
- The B-S infrastructure is reused thus increasing the pay back on the initial test investment.
- The test development time is reduced as the same tests are reused.

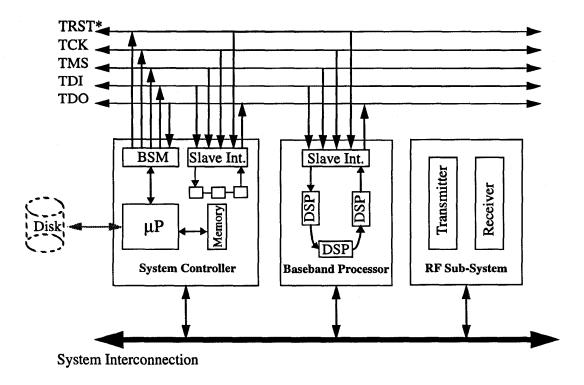


Fig. 3: System Test Architecture

- The test strategy provides diagnostic capability by isolating the faulty sub-system. The Failure Mode Analysis (FMA) on the faulty sub-systems can be used for manufacturing process improvement.
- Remote testing of the system in field may be achieved using this test strategy.
- The self test capability of the system can reduce installation time in the field.
- This end-to-end test strategy can be generalized to other wireless systems.

This is a proposed strategy. No implementation data is available yet about the hardware and software overhead of the scheme and the accuracy of the method. The system test requirements, acceptable overhead in hardware, impact on software development time are some of the factors that need to be considered to determine if the proposed end-to-end test strategy is applicable for a given wireless system.

#### 6 Conclusion

An integrated end-to-end test strategy for wireless systems is proposed. It combines Boundary-Scan and RF loop-back testing into one unique test architecture to achieve system self-test.

## References

- [1] "IEEE Standard Test Access Port and Boundary-Scan Architecture", IEEE Std 1149.1-1990.
- [2] G. Skidmore, "Manufacturing Test of TDMA Cellular Telephones Used in NADC Systems", Hewlett Packard Wireless Communications Symposium, pp. 145-161, 1993.
- [3] M. Mahoney, "DSP-Based Testing of Analog and Mixed-signal Circuits" Computer Society Press of the IEEE, ISBN 0-8186-0785-8.
- [4] C.L. I, L.J. Greenstein, and R.D. Gitlin, "A microcell/macrocell cellular architecture for low and high-mobility wireless users", GLOBECOM'91 Conf. Record, pp. 1006-1011, December 1991.
- [5] L.J. Greenstein, N. Amitay, T.S. Chu, L.J. Cimini, G.J. Foschini, M.J. Gans, C.L. I, A.J. Valenzuela, and G. Vannucci, "Microcells in Personal Communications Systems", IEEE Communications Magazine, pp. 76-88, December 1992, Vol.30, No.12.
- [6] M.S. Heutmaker, et al, "Measurement of the Gain Compression and Phase Distortion of a Radio Frequency Power Amplifier using Digitally-Modulated Signals," In preparation.

Paper T2.2

945

- [7] C.W. Yau and N. Jarwala, "The boundary-scan master: target applications and functional requirements," Proceedings International Test Conference, pp. 311-315, 1990
- [8] AT&T Boundary-Scan Master User Manual, June 1993.
- [9] L. Whetsel, "A Proposed Method of Accessing 1149.1 in a Backplane Environment", Proceedings International Test Conference, pp. 206-216, September 1992.
- [10] Texas Instruments, Boundary-Scan Logic IEEE Std 1149.1 (JTAG) Data Book, 1994.
- [11] J. Andrews, "Roadmap for extending IEEE 1149.1 for hierarchical control of locally-stored, standardized command set, test programs", Proceedings International Test Conference, pp. 300-306, 1994.
- [12] National Semiconductor, SCAN Data Book, 1994.
- [13] D. Bhavsar, "An architecture for extending the IEEE Standard 1149.1 test access port to system backplanes", Proceedings International Test Conference, pp. 768-776, 1991.

o gastori, az Aldráfer