FPGA Implementation of the Real-Time ADTF process using the Intel-Altera DE1 Board for ECG signal Denoising

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***Abstract*— The aim of this paper is to propose an FPGA implementation of the real-time ADTF architecture of the ECG signal denoising based on the DE1 board of Intel-Altera. The results of the proposed implementation as well as the comparative study of this implementation in some different low-cost FPGA architectures show that the proposed FPGA implementation of the real-time ADTF architecture presents an efficient and optimized hardware solution for the real-time ECG signal denoising in different sorts of the low-cost FPGA architectures.**

Keywords- ECG signal; FPGA; VHDL; Real-Time; Intel-Altera

I. INTRODUCTION

Nowadays, there is immense interest in the integration of embedded systems in biomedical applications. The embedded system is a combination of processors, intelligence and memory with great development potential [1]. These systems operate in a wide variety of environments and often provide real-time service for the correct and efficient supervision of patients' health status. One of the embedded architectures widely used in the different fields of biomedical engineering is the FPGA. FPGAs are reconfigurable VLSI components, allowing them to be reprogrammable at will to integrate a wide variety of data analysis and monitoring processes, in our case those of cardiac data. FPGA-based architecture is designed using High-Level Synthesis Tools (HLS) [2] or Hardware Description Language (HDL) such as VHDL [3-5] and Verilog [6].

The ECG signal, as shown in Fig. 1, is an essential factor in the analysis of heart disease. However, this signal is fragile to different kinds of noise, which can reduce the efficiency of the analysis of this signal. ECG signal filtering is an important and obvious tool for solving this problem [7].

The ADTF is a proposed non-linear filter for ECG signal denoising [7-8]. The theoretical bases of this filter were inspired by the median double threshold method [9]. This technique offers an important solution for image filtering. In single-threshold filters, any pixel that has a lower value (Ex: low-pass filter) or higher (Ex: high-pass filter) than the single threshold value is considered a noise. This can increase the possibility of poor noise detection. In the case of the double threshold method, the noisy pixels are identified in a relatively narrow range and can thus reduce the probability of incorrect detection.

This article proposes the hardware implementation of an embedded architecture of the ADTF filter for a real-time process of filtering the ECG signal based on the FPGA-DE1 (Cyclone II) board of the manufacturer Intel-Altera. The proposed architecture is designed to be implementable on different FPGA architectures. We propose a VHDL implementation to optimize and simplify the proposed architecture. This design is based on a structural description of the different functional blocks of the proposed architecture. The overall architecture is designed to accelerate and parallelized the data processing.

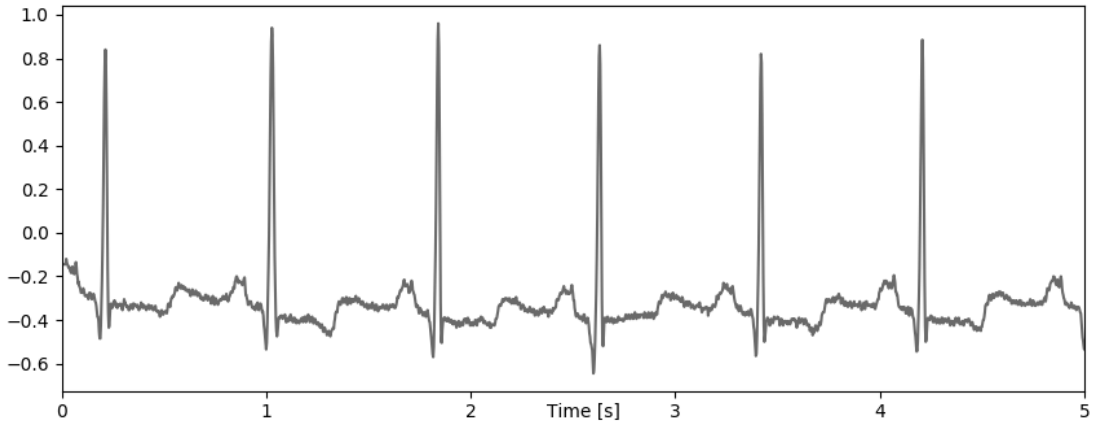

Fig. 1. ECG signal record

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II. ADTF ARCHITECTURE

The architecture of the ADTF is implemented based on the VHDL description language, which can offer the high optimization of the different processing blocks presented in this architecture. The ADTF architecture is based on three modules. The first concerns the loading of cardiac data by providing a real-time processing without occupying a memory space. The second module calculates the elements needed for the ADTF-based treatment. The third module concerns the calculation of the thresholding levels as well as the application of tests on cardiac data and the assignment of data to the output.

A. ADTF Load Module

The principle of the module of the real-time loading (ALM) of ECG signal data is to read the incoming data from the input-signal port of 11 bits (MIT-BIH data encoding) and to prepare them for the modules which follow. This module is based on a shift register with the same processing frequency of the sampling frequency of the ECG signal input. In this case, the MIT-BIH database signals are used with a sampling frequency of 360 Hz.

B. ADTF Features Module

The module of the ADTF features calculation (AFM) makes it possible to prepare the data necessary for processing, namely, the average of the window of the ADTF, the maximum and the minimum of this window. The analyzed data arrives from the output of the first ALM module. The processing frequency of the AFM module is greater than that of the ALM module. This provides real-time ECG signal analysis. We propose a frequency of 3.6 KHz which is 10 times the proposed input signal reading frequency for the ALM module.

C. ADTF Test Module

The principle of the test and the assignment module (ATM) is to calculate the thresholding values for the two levels τ_h and τ_L. The data needed for the calculation come from the output of the MCP module, namely, the average of the window, the maximum and the minimum of this window. The processing frequency of the MTA module is identical to that of the MCP module. Then, this module generates the output signal based on the test results of the two levels τ_h and τ_L.

Fig. 2 shows an overall diagram of the top architecture of the ADTF real-time process. The inputs of this architecture are: the 11-bit input signal (Signal_input), the Reset input, the two clocks “Clk” for reading the input data and “Clk_test” of the MCP and MTA modules. The output of this architecture is the 16-bit corrected signal (Signal_out). All sorts of calculation present the ADTF real-time architecture are proposed in the fixed point form with 11 bits of the integer part and 5 bits of the fractional part in order to optimize the number of the logic elements of the ADTF architecture.

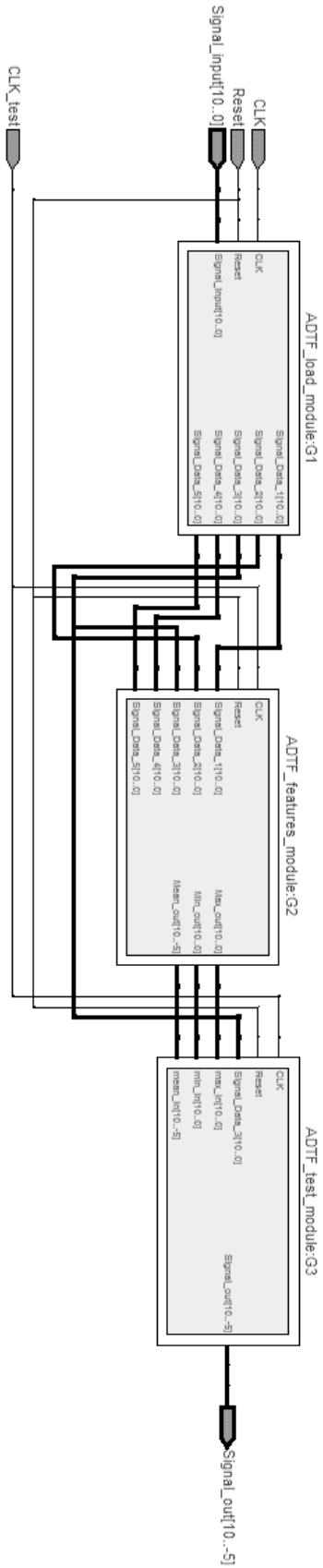

Fig. 2. ADTF top architecture

III. FPGA IMPLEMENTATION USING THE FPGA-DE1 BOARD

The validation of a given architecture in VHDL or others requires a test on FPGA board and the comparison of the results of the hardware test with those proposed by the simulation tool. The purpose of this validation is to check the various features of the proposed architecture and their synchronization with the different elements of the FPGA board.

For the hardware implementation of the real-time architecture of the ADTF, this paper proposes the use of the FPGA-DE1 board based on the Cyclone II of the manufacturer Intel-Altera [15-16]. This board is shown in Fig. 3. The DE1 board has many features that allow the user to implement a wide range of designed circuits, ranging from simple circuits to various more complicated architectures.

The Altera-DE1 board is proposed as a low-cost range of Intel-Altera. The choice of this board is based on the objective of developing an efficient architecture with a constraint of low use of the resources of an FPGA board. This allows the ADTF real-time architecture to be integrated into different FPGA boards of different ranges.

In this paper, we propose the use of Quartus-Altera's "SignalTap II" tool for hardware validation of the proposed ADTF architecture. The embedded SignalTap II logic analyzer is a system-level debugging tool. This tool allows you to analyze the state of the internal signals of the FPGA design under custom user-defined conditions during FPGA board operation without the use of I/O devices. SignalTap II integrates directly into a given design, facilitating functional debugging. In this paper, we propose developing a test level to compare the output signal on the DE1 board with that of the ModelSim-based simulation.

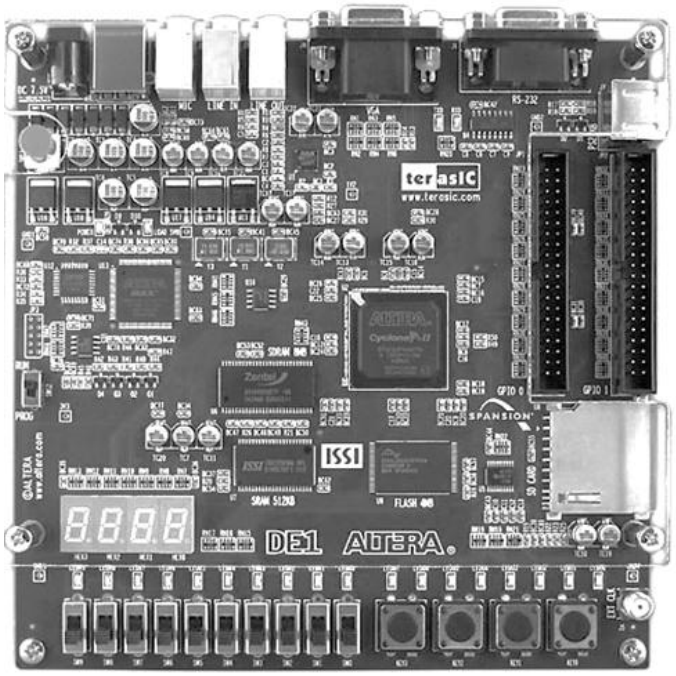

Fig. 3. FPGA-DE1 board of Intel-Altera

IV. RESULTS AND DISCUSSION

Fig. 4 presents an example of the real-time denoising of the ECG signal using the ADTF architecture based on ModelSim which is a simulation software of the embedded architectures [10]. As shown in this figure, the real-time ADTF architecture allows high performances while denoising the ECG signal in real-time condition.

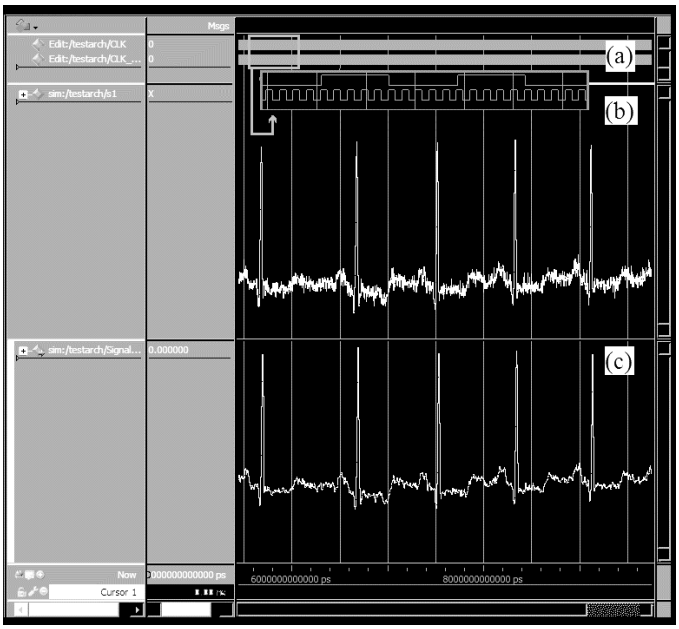

Fig. 4. Real-time denoising of the MIT-BIH signal No. 100 with 20 dB of WGN. (a) CLK and Internal CLK, (b) input signal infected by noises, (c) output signal.

Fig. 5 shows show the results of the SignalTap II comparing to the ModelSim results. For reading the binary word of the output signal in SignalTap II, the reading is from left to right because the binary word starts with the most significant bit to the weakest one in the case of this study. In this case, the binary word of the simulated output signal after its change of state based on Test 1 is identical to the real one proposed by SignalTap II. This reflects the high performance of the hardware implementation of the proposed real-time ADTF architecture. Consequently, this study validates the high efficiency of the real-time ADTF architecture based on VHDL in both cases; the architectural design of the real-time ADTF process and the hardware implementation of this architecture on a low-cost FPGA board.

Table I presents a comparative study of the logic elements used in some of low-cost FPGA architectures of Intel-Altera for the hardware implementation of the real-time ADTF architecture.

As presented in this table, the proposed implementation occupies a modest number of the logic elements presented in the different FPGA architectures proposed in this study. This makes it possible to add other architecture proposals (QRS detection, heart rate, compression, transmission, etc.) to develop a real-time monitoring system for cardiac data and decision support for the cardiologists.

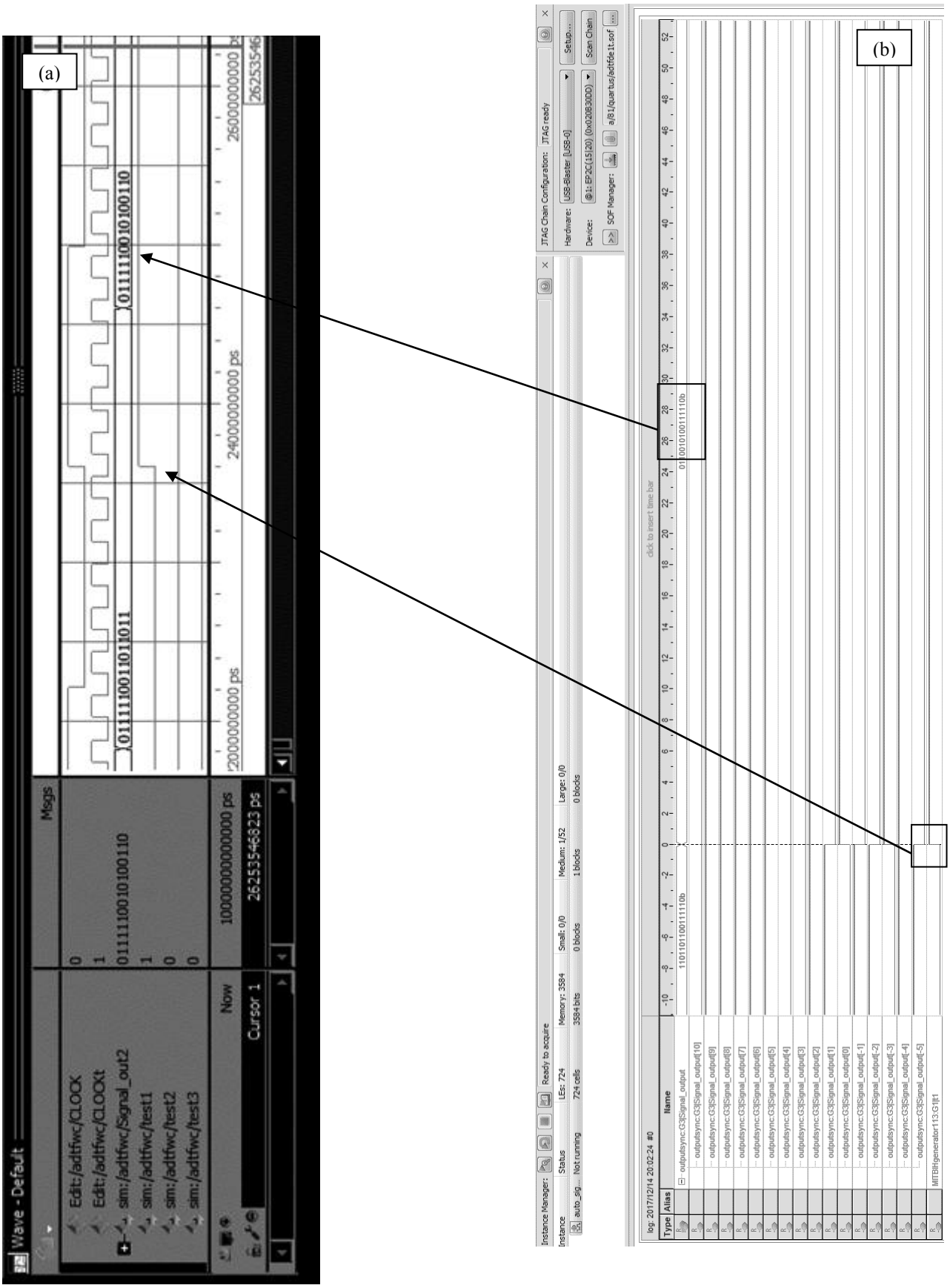

Fig. 5. Signal Tap results comparing to the ModelSim results. (a) ModelSim Result, (b) SignalTap results.

TABLE III
COMPARATIVE STUDY OF THE HARDWARE ELEMENTS USED IN THE FPGA IMPLEMENTATION OF THE ADTF REAL-TIME PROCESS BASED ON SOME OF FPGA ARCHITECTURES OF INTEL-ALTERA

	Cyclone II	Cyclone III	Stratix III
Total logic elements /Logic utilization	23%	4%	4%
Total pins	8%	5%	5%
Total memory bits	0%	0%	0%
9-bit elements block	8%	< 1%	-
18-bit elements block	-	-	1%

V. CONCLUSION

This paper presents an FPGA implementation of the real-time ADTF architecture based ECG signal denoising using the DE1 board of Intel-Altera.

This paper proposes the use of the DE1 board features to test and to validate the efficiency of the ADTF approach in real conditions of utilization using embedded architectures especially the FPGA ones. The results, as proposed by the SignalTap II tool, shows that the proposed FPGA implantation shows identical results to those presented by the simulation tool of ModelSim based on the VHDL conception of the real-time ADTF architecture. The proposed implementation proposes a low occupancy of the different FPGA resources in different low-cost architectures. Accordingly, the proposed FPGA implementation of the real-time ADTF architecture presents an efficient and optimized hardware solution for the real time ECG signal denoising in different sorts of the low-cost FPGA architectures.

VI. REFERENCES

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