An Improved FPGA Parallel Design of Frequency Offset Estimation

Yupeng Wang[1], Liqian Wang[1], Zhiguo Zhang[1], Shanyong Cai[1], Luming Li[2], Jiangxing Chen[2], Xing Liu[2], Ziyang Xiao[2]*

[1]State Key Laboratory of Information Photonics and Optical Communications, Beijing University of Posts and Telecommunications, Beijing, 100876, China
[2]Information and Communications Branch, Jiangxi Electric Power Company, Nanchang, 330096, China
*E-mail : zhangzhiguo@bupt.edu.cn

ABSTRACT

In coherent optical communication QPSK system, an improved FPGA parallel design of frequency offset estimation with low complexity is proposed. The BER simulation results compared with serial scheme verify the feasibility of the parallel design.

Keywords: *coherent optical communication, QPSK, frequency offset estimation, low complexity, FPGA, parallel design.*

1. INTRODUCTION

In recent years, as the demand of communication network for transmission bandwidth continues to increase, the coherent optical communication [1] and digital signal processing (DSP) technology [2] are becoming research hotspots. And with the advent of field programmable gate array (FPGA), the real-time coherent reception [3] and processing technology have attracted a lot of attention.

In the quadrature phase-shift keying (QPSK) system, DSP is used to detect and compensate for various impairments during transmission. For estimating and compensating frequency offset in transmission, many algorithms are proposed. In all classical frequency offset estimation algorithms, removing the modulation phase information of received signals is required before estimating the offset. Two methods currently used are 4th-power operation [4] and training sequence method [5]. Compared with the algorithm based on training sequence, 4th-power algorithm has an obvious advantage in decreasing the complexity of hardware implementation. Nonetheless, in the 4th-power algorithm, the 4th-power operation conducted on the received signal will greatly consume the hardware resources to guarantee the calculation accuracy. Therefore, a simplified method of Mth-power based on absolute value [6] was proposed by Han. However, this method as a serial scheme has low throughput and cannot meet real-time processing requirements. In order to solve these problems, we propose a FPGA parallel design of frequency offset estimation based on an improved absolute value algorithm. This design improves the throughput of the overall system and adopts feed-forward design to guarantee the real-time processing of digital signal. And the comparison of bit error rate (BER) simulation results between serial scheme and parallel scheme verifies the feasibility of parallel design.

2. PRINCIPLE

2.1 The principle of improved absolute value algorithm

Fig. 1(a) shows the principle of the improved algorithm based on absolute value operation. At the receiving end of the QPSK optical transmission system, after the amplitude is normalized, the conjugate multiplication with the adjacent signal is carried out to remove the phase noise caused by the line width of the laser. The signal obtained $S_n^{'}$ can be expressed as follows:

$$S_n^{'} = \exp[j(\theta_n + \varphi_n)] \quad (1)$$

wherein, θ_n is the modulation phase of the received signal, and φ_n stands for the phase change of the frequency offset and phase noise. When $S_n^{'}$ is expressed in the form of plurals, its real part $I_{(n,1)}$ and imaginary part $Q_{(n,1)}$ can be obtained as:

$$I_{(n,1)} = real(S_n^{'}) = \cos(\phi_n) \quad (2)$$

$$Q_{(n,1)} = imag(S_n^{'}) = \sin(\phi_n) \quad (3)$$

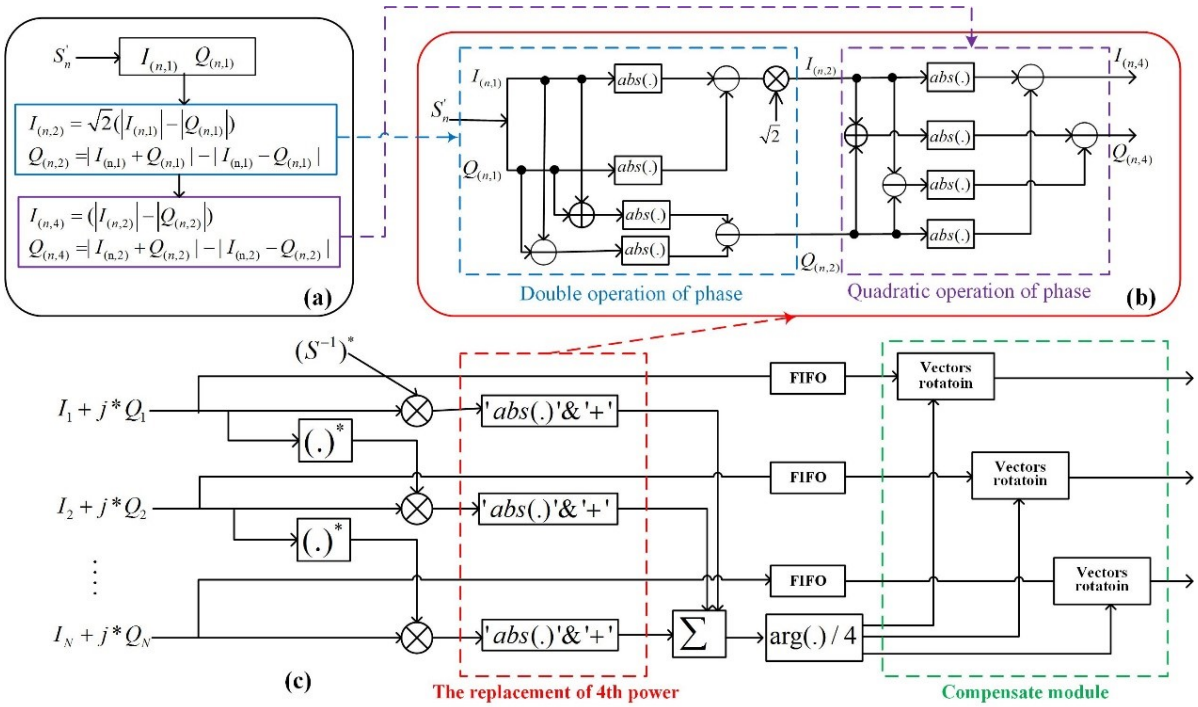

Fig. 1. (a) The principle of improved algorithm. (b) Hardware implementation of the algorithm. (c) The parallel design based on FPGA

where $\phi_n = \theta_n + \varphi_n$. For the QPSK system, I stands for in-phase component and Q is quadrature component.

The quadratic operation of the signal is equivalent to increasing the phase angle by 2 times, so the resulting real part $I_{(n,2)}$ and imaginary part $Q_{(n,2)}$ become:

$$I_{(n,2)} = \cos(2\phi_n) \tag{4}$$

$$Q_{(n,2)} = \sin(2\phi_n) \tag{5}$$

As the results obtained after the quadratic operation of the trigonometric function cosine and sine have the same cycle and approximate variation with the results obtained by taking its absolute value, the above formulas (4) and (5) can be developed using the double angle formula and be further simplified into:

$$\begin{aligned} I_{(n,2)} &= \cos(2\phi_n) \\ &= \cos^2(\phi_n) - \sin^2(\phi_n) \\ &\approx \left|\cos(\phi_n)\right| - \left|\sin(\phi_n)\right| \\ &= \left|I_{(n,1)}\right| - \left|Q_{(n,1)}\right| \end{aligned} \tag{6}$$

$$\begin{aligned} Q_{(n,2)} &= \sin(2\phi_n) \\ &= -\cos(2\phi_n + \frac{\pi}{2}) \\ &\approx |\sin(\phi_n + \frac{\pi}{4})| - |\cos(\phi_n + \frac{\pi}{4})| \\ &= \frac{\sqrt{2}}{2}\left[|I_{(n,1)} + Q_{(n,1)}| - |I_{(n,1)} - Q_{(n,1)}|\right] \end{aligned} \tag{7}$$

Similarly, the results of 4th-power operation can be obtained by further quadratic operation of squared results, and the real part $I_{(n,4)}$ and imaginary part $Q_{(n,4)}$ are:

$$I_{(n,4)} = \left|I_{(n,2)}\right| - \left|Q_{(n,2)}\right| \tag{8}$$

$$Q_{(n,4)} = \left|I_{(n,2)} + Q_{(n,2)}\right| - \left|I_{(n,2)} - Q_{(n,2)}\right| \tag{9}$$

2.2 Parallel design based on FPGA

Fig. 1(c) depicts the parallel processing of the frequency offset estimation and compensation algorithm which is composed of N parallel units. Wherein, N should be equal to B/F in which B is system signal rate and F is FPGA operating frequency. The operation of N signals is processed in each clock cycle. The signal that inputs in every clock cycle performs its own conjugate operation and multiplication operation with the conjugate result of its adjacent symbol. Then the result of the multiplication calculation is sent to the absolute value calculation part. Fig. 1(b) shows the hardware implementation of replacing 4th-power operation with absolute value operation. The calculation results of the N branches are sent together into an accumulator, and the final calculation result of the accumulator is subjected to the angling operation by the coordinate rotation digital computer (CORDIC) module. Then the frequency value is estimated by shifting the obtained angle value to the right by 2 bits and the frequency offset estimation value is used to complete the rotation operation together with the delayed signal on each parallel unit through the CORDIC module. Finally, the real-time compensation operation of the received signal is completed.

978-1-7281-2764-4/19/$31.00 ©2019 IEEE

3. SIMULATION RESULTS AND DISCUSSION

In this section, the simulation system is the 2.5-GBaud polarization multiplexed quadrature phase shift keying (PM-QPSK) coherent optical transmission system, in which the length of the symbol block in the frequency offset part is 512 and the laser linewidth is set to 100 kHz. The number of parallel units N is 16.

The BERs between the classical 4th-power algorithm and the improved absolute value algorithm are compared in simulation system. It can be seen from the Fig. 2 that the algorithm of replacing the 4th-power operation with absolute value has the similar performance in frequency offset estimation with the 4th-power algorithm. In multiple groups of frequency offset values set under the simulation system, the differences between the error rate obtained by the two algorithms are less than 10^{-4}.

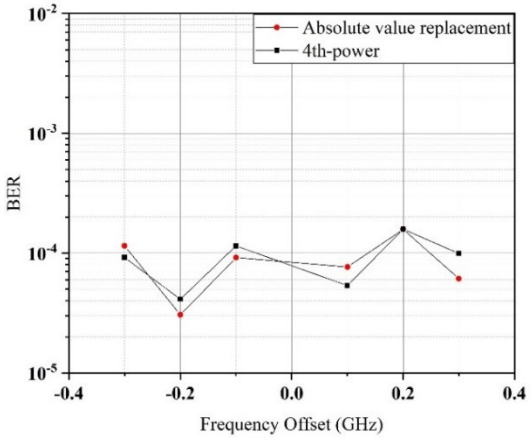

Fig. 2. The performance of frequency offset estimation

Based on the improved algorithm, the relationship between the optical signal noise ratio (OSNR) at the receiving end and the BERs is shown in Fig. 3. It can be seen from Fig. 3 that the parallel design based on the FPGA implementation has almost the same performance with the offline algorithm processing. Their BERs are very close and BERs are decreasing as the OSNR at the receiving end becomes better. Therefore, it can be concluded that the improved frequency offset estimation parallel design based on the FPGA implementation can obtain the similar BERs with the offline algorithm.

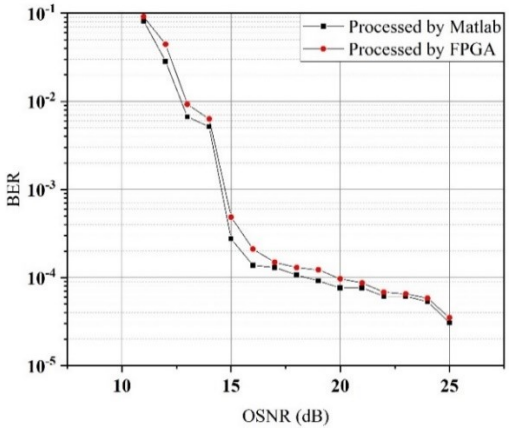

Fig. 3. BER at different OSNR

The resource consumption of the parallel design scheme is shown in Table 1. The complexity of the multiplier is much larger than that of the adder in hardware implementation. In real-time operations, the hardware resources involved in the operation per clock cycle are related to the number of parallel units N. In improved absolute value algorithm, replacing large number of multipliers with adders greatly saves hardware resources.

Table 1. Consumption of resources

Algorithm	Multipliers	Adders
4th-power	8N	4N
Improved	N	8N

4. CONCLUSION

In this paper, a parallel design of frequency offset estimation algorithm based on FPGA implementation is proposed, which is suitable for the coherent optical communication QPSK system, and has the advantages of low complexity and low resource consumption. This design reduces the consumption of hardware resources by replacing the 4th-power operation with absolute value operation, while ensuring the real-time estimation and compensation of frequency offset through the feed-forward design.

5. ACKNOWLEDGMENTS

This study is supported by National Natural Science Foundation of China (No.61671076 and No.61801043).

6. REFERENCES

[1] E. Ip, et al., “Coherent detection in optical fiber systems,” *Opt. Express*, vol. 16, no. 2, pp. 753-791, Jan. 21, 2008

[2] S. Tsukamoto, K. Katoh, K. Kikuchi. “Coherent demodulation of optical multilevel phase shift-keying signals using homodyne detection and digital signal processing,” *IEEE Photon. Technol. Lett.*, vol. 18, no. 10, pp. 1131-1133, 2006.

[3] Z. Zhang, Z. Cao, X. Chen, et al., “Remote pumped EDFA-based 40-Gb/s downstream and 10-Gb/s upstream long-reach WDM PON employing RSOA and FBG equalizer,” *Chin. Opt. Lett*., vol. 11, no.12, Dec. 10, 2013

[4] A. Leven, N. Kaneda, U. V. Koc, and Y. K. Chen, “Frequency estimation in intradyne reception,” *IEEE Photon. Technol. Lett.,* vol. 19, no. 6, pp. 366-368, Mar. 15, 2007

[5] X. Zhou, X. Chen, and K. Long, “Wide-rage frequency offset estimation algorithm for optical coherent systems using training sequence,” *IEEE Photon. Technol. Lett.*, vol. 24, no. 1, pp. 82-84, Jan. 1, 2012

[6] J. Han, W. Li, Z. Yuan, et al., “A simplified implementation method of Mth-power for frequency offset estimation,” *IEEE Photon. Technol. Lett.*, vol. 28, no. 12, pp. 1317-1320, Jun. 15, 2016

978-1-7281-2764-4/19/$31.00 ©2019 IEEE