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Readme\_example0:Here are details of files we need for the design compilation and simulation of example0. These files will be needed for other designs we are going to do. Compilation simulation and loading the design on the evaluation board.

Eample0.scd: **S**ynopsys **D**esign **C**onstrain, for timing analyzing during compilation.

Example0.qsf: For this file we need to add the following line,

set\_global\_assignment -name NUM\_PARALLEL\_PROCESSORS 4

It means the computer will use 4 processors during compilations.

Example0.vso: The file is for simulation, It is created during compilation upon special request

before the compilation.

Example0.cmp: This file is created after simulation by special request from the operator, this

File is important when working with two or more design modules. In our

Project there will be several modules.

Example0 – vhdl list it is required for compilation it is done before compilation.

Now it looks complicate but after the design of exampl0 it will be clear and simple.