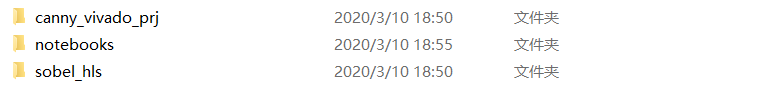
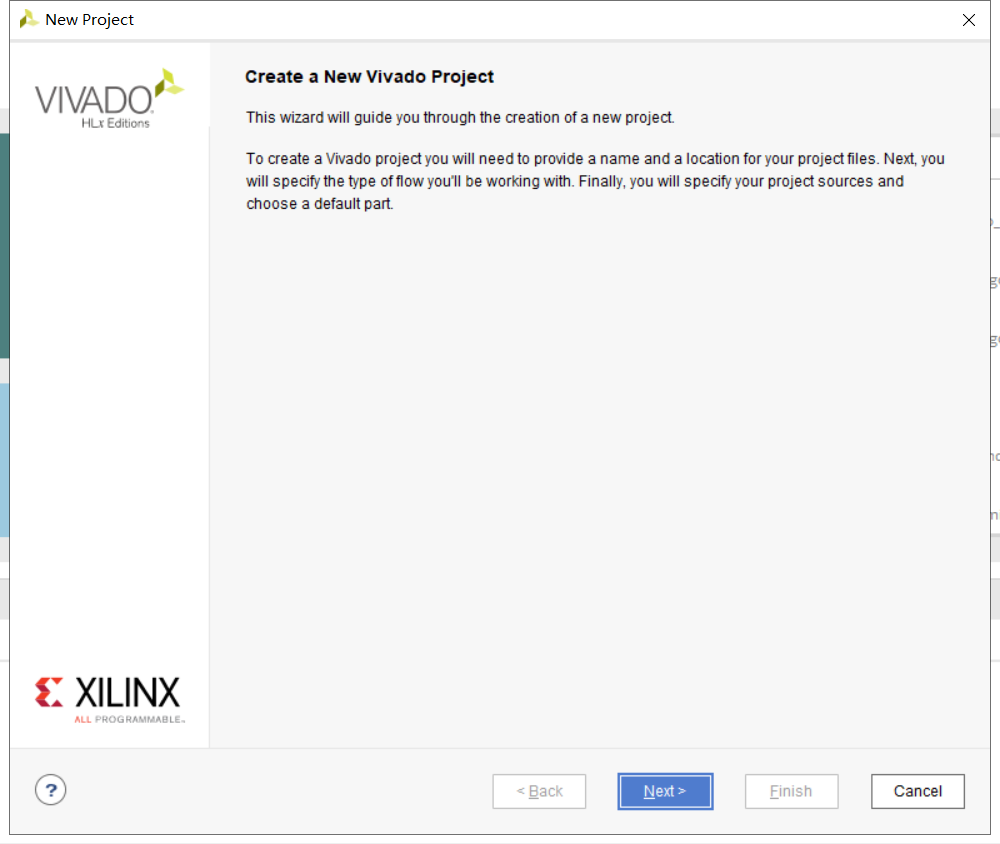
如何移植github 上cv2PYNQ的图像处理项目

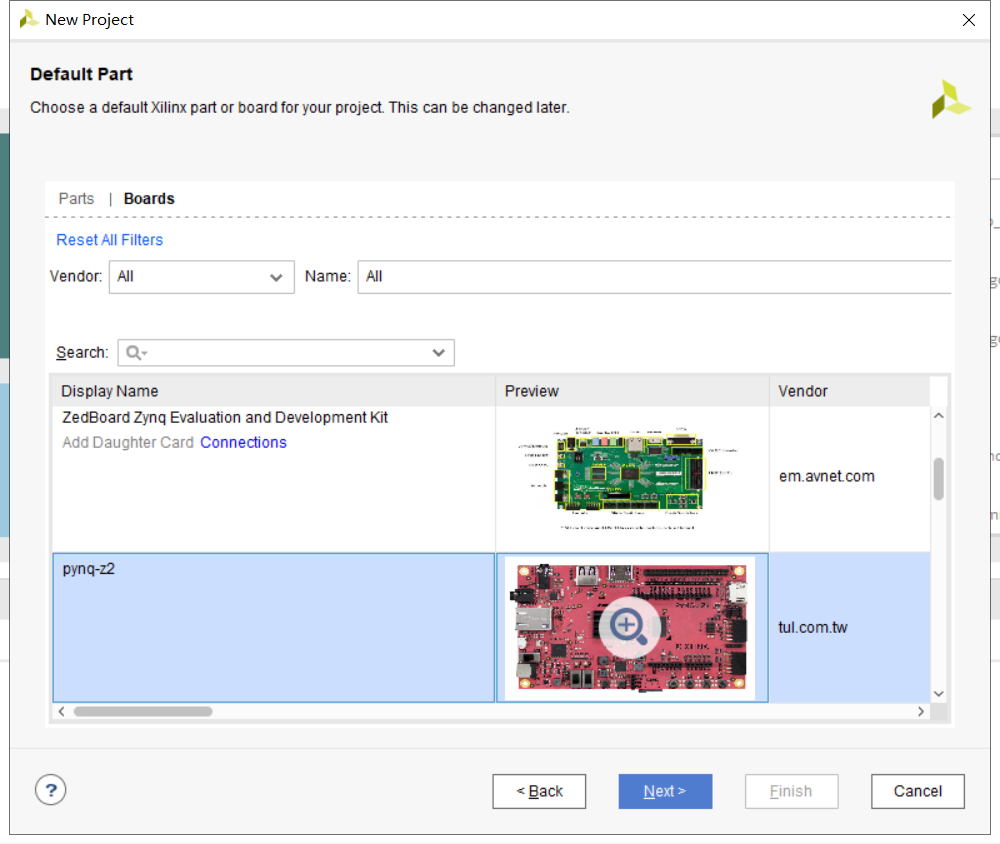
工程目录如下

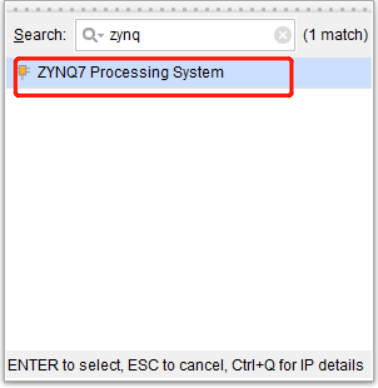
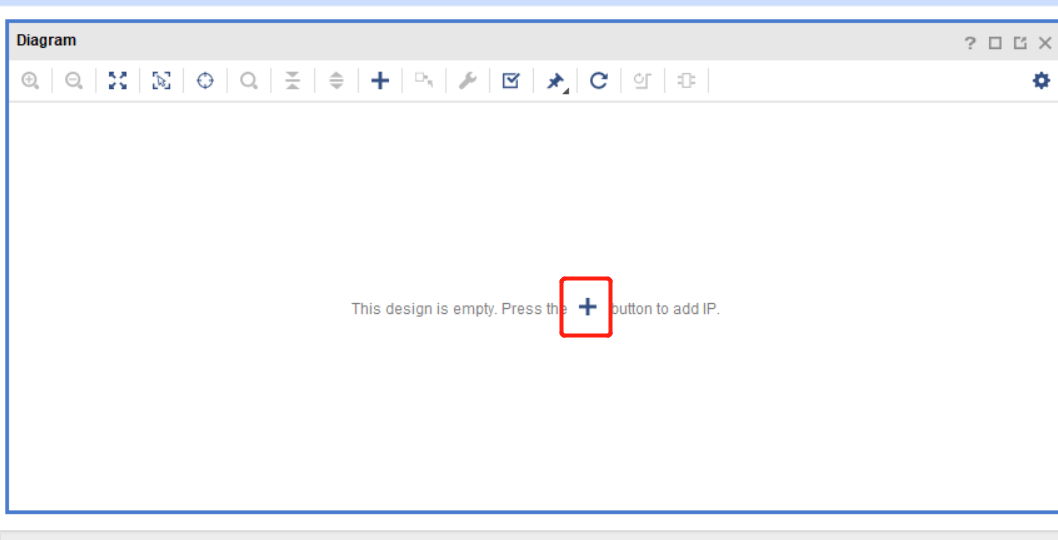
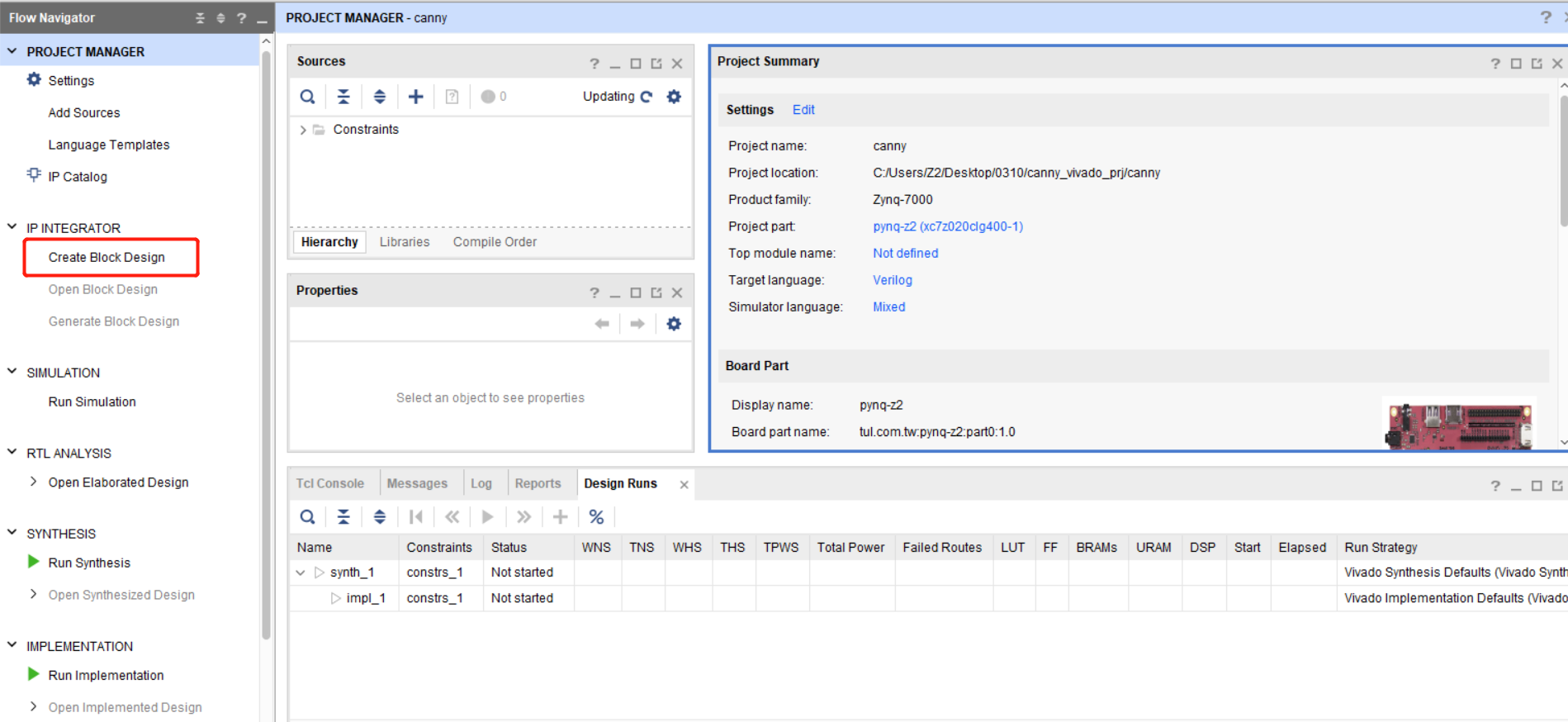


1. 先建立vivado block design

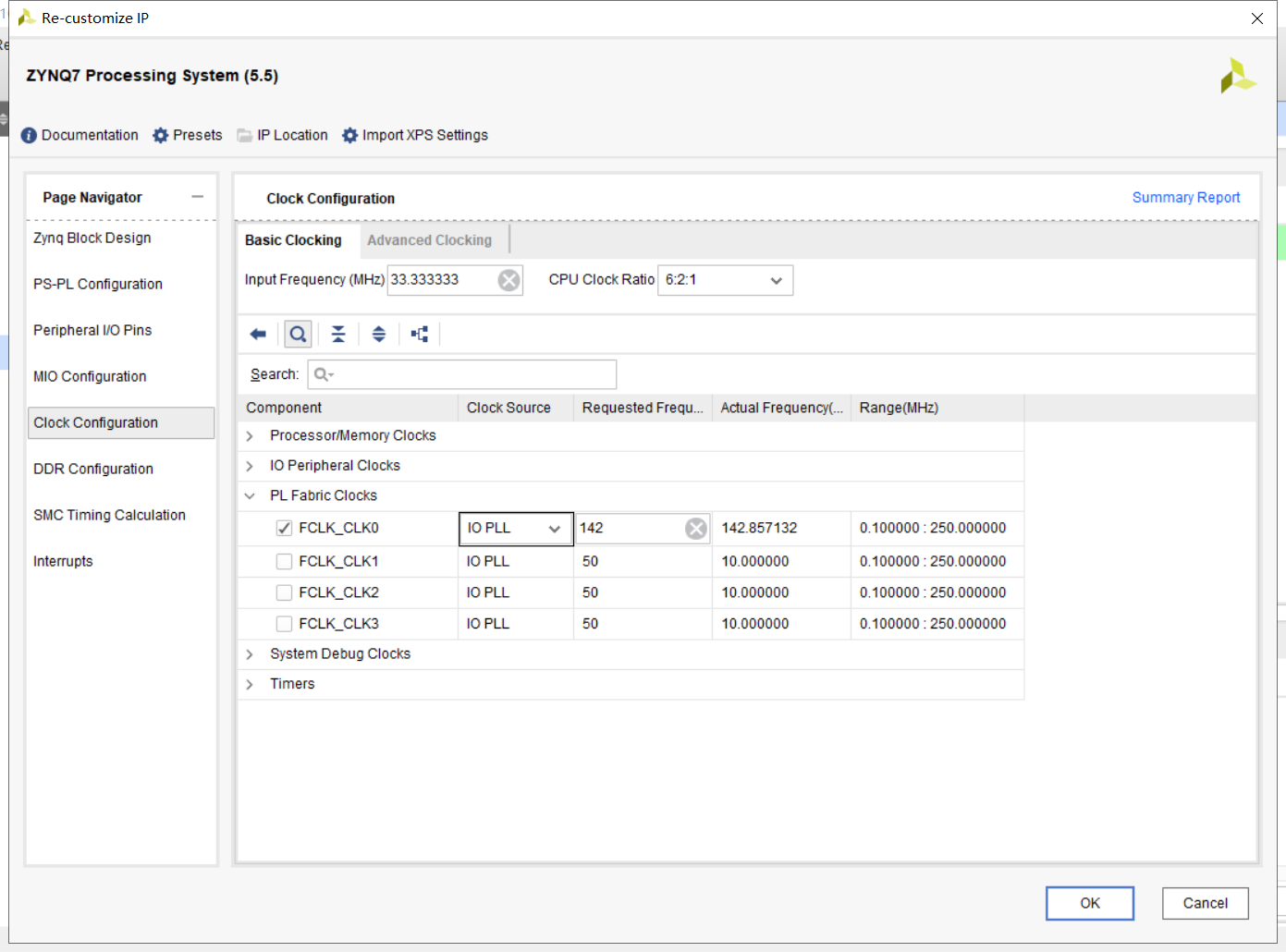
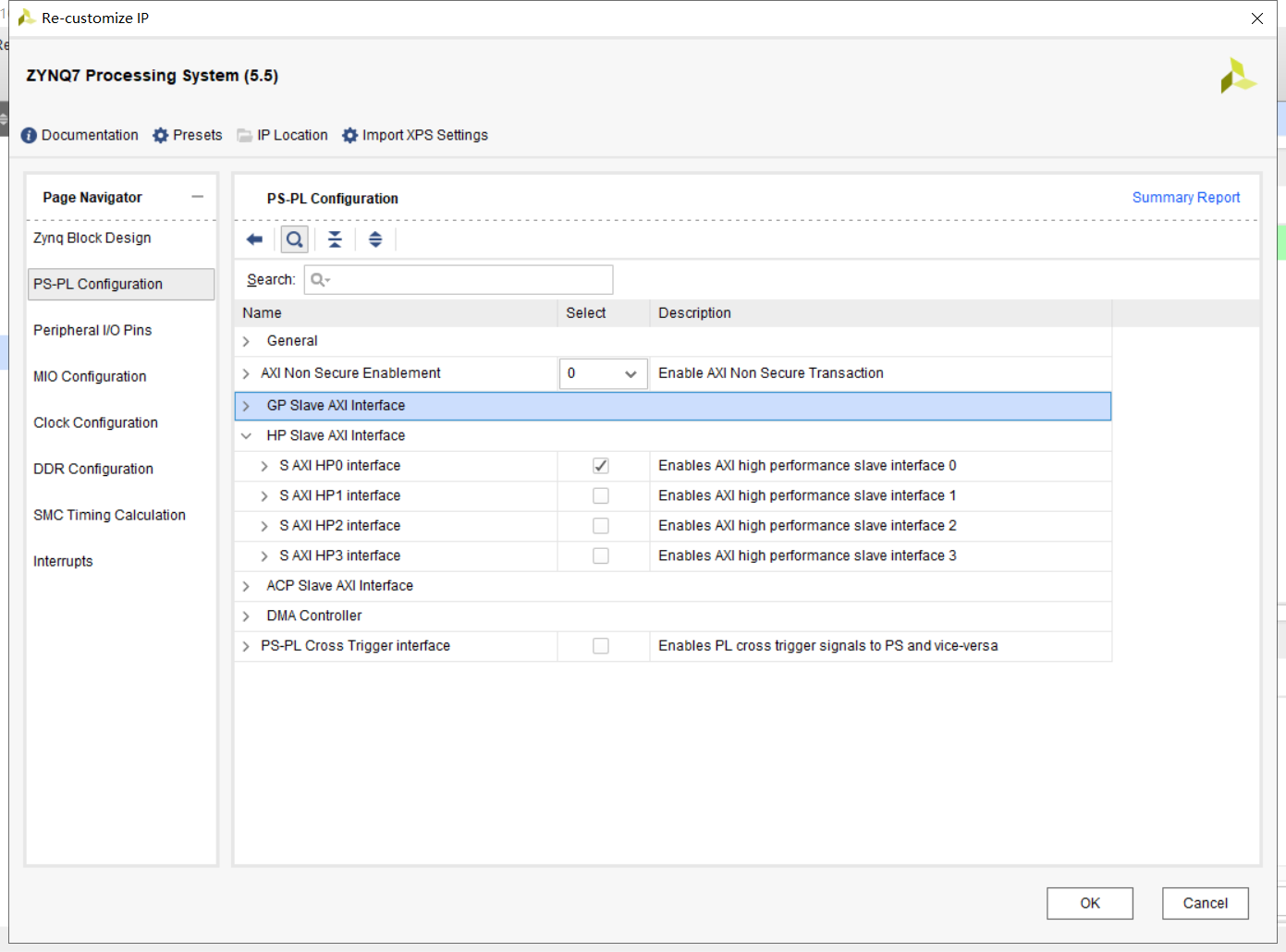
创建新项目：

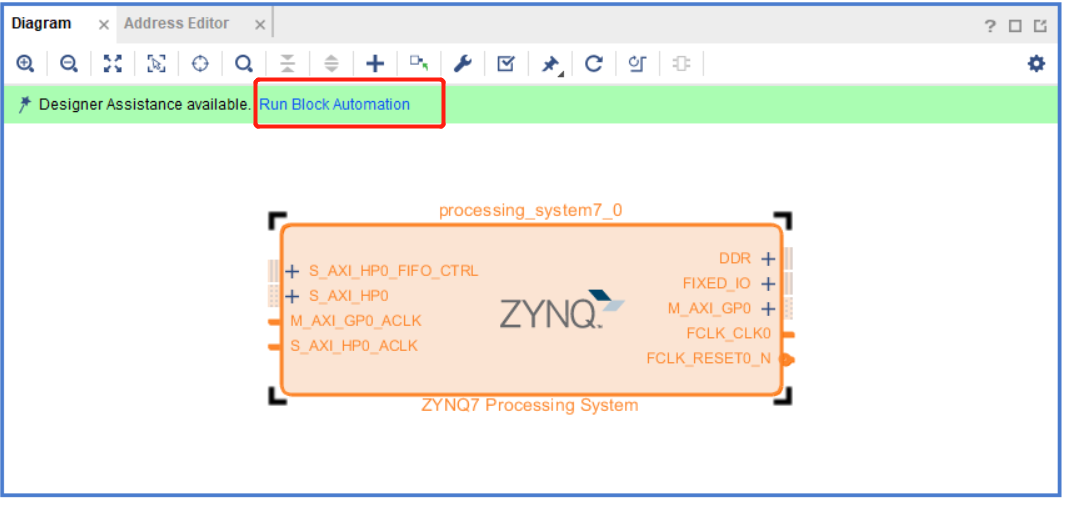




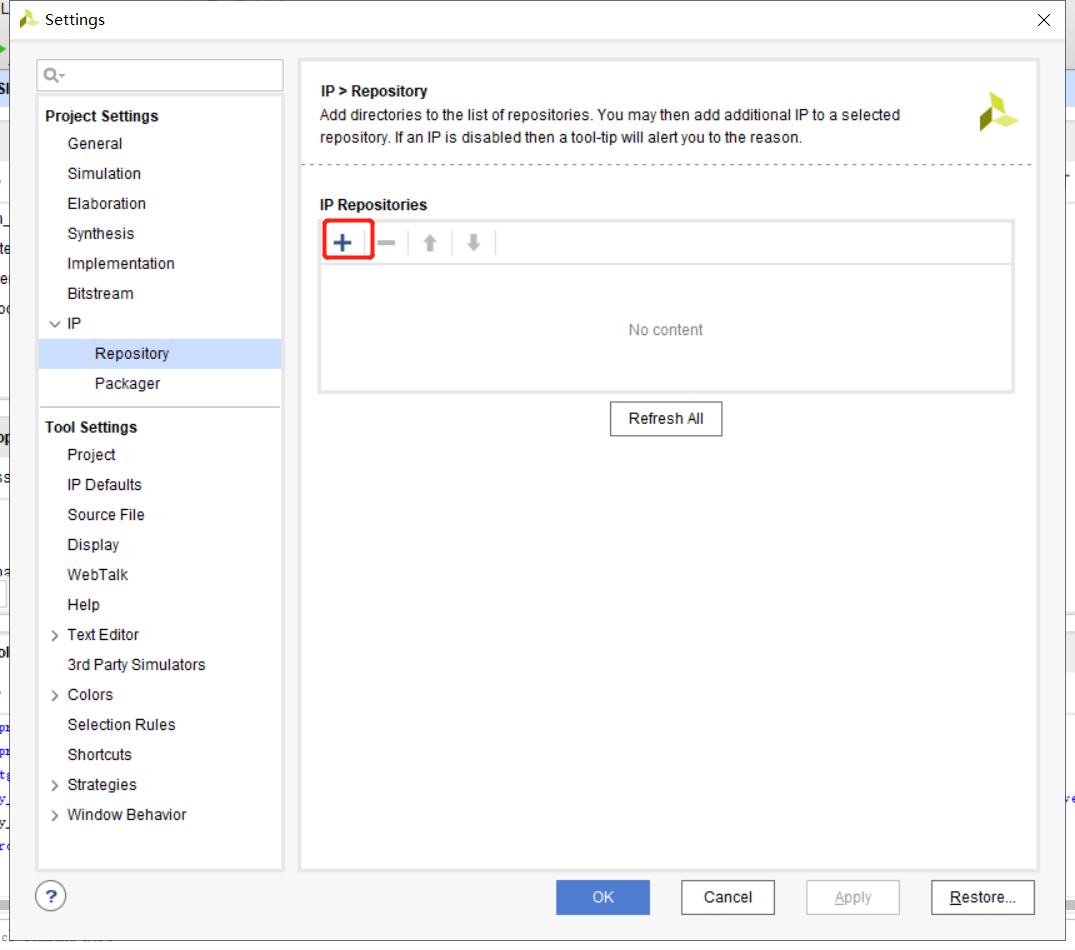
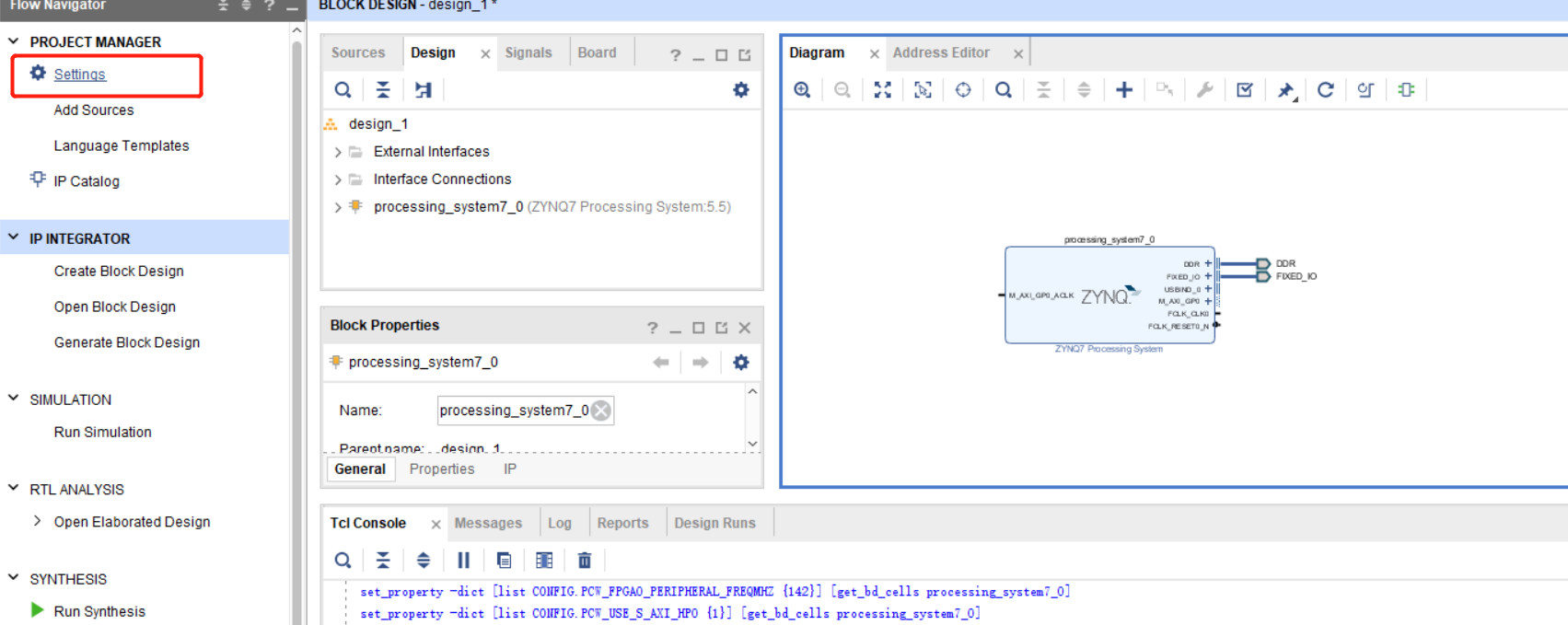


双击生成zynq，打开AXI DMA通路的HP0口并对其时钟进行配置：

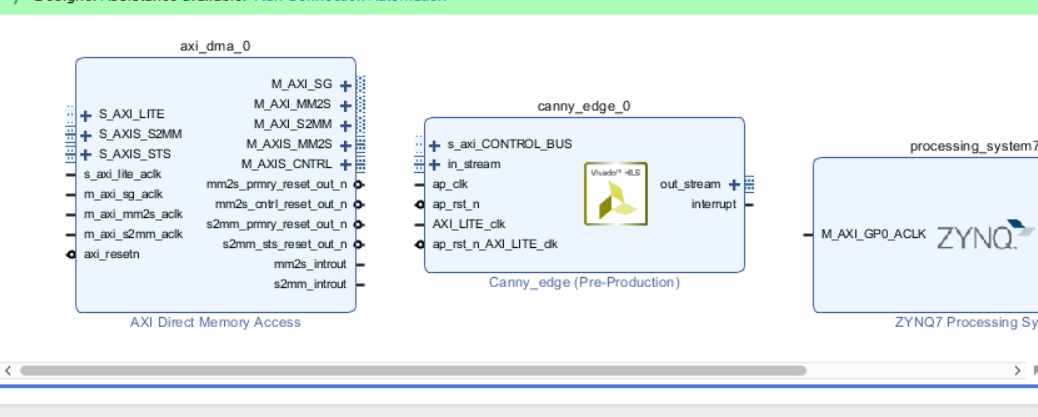




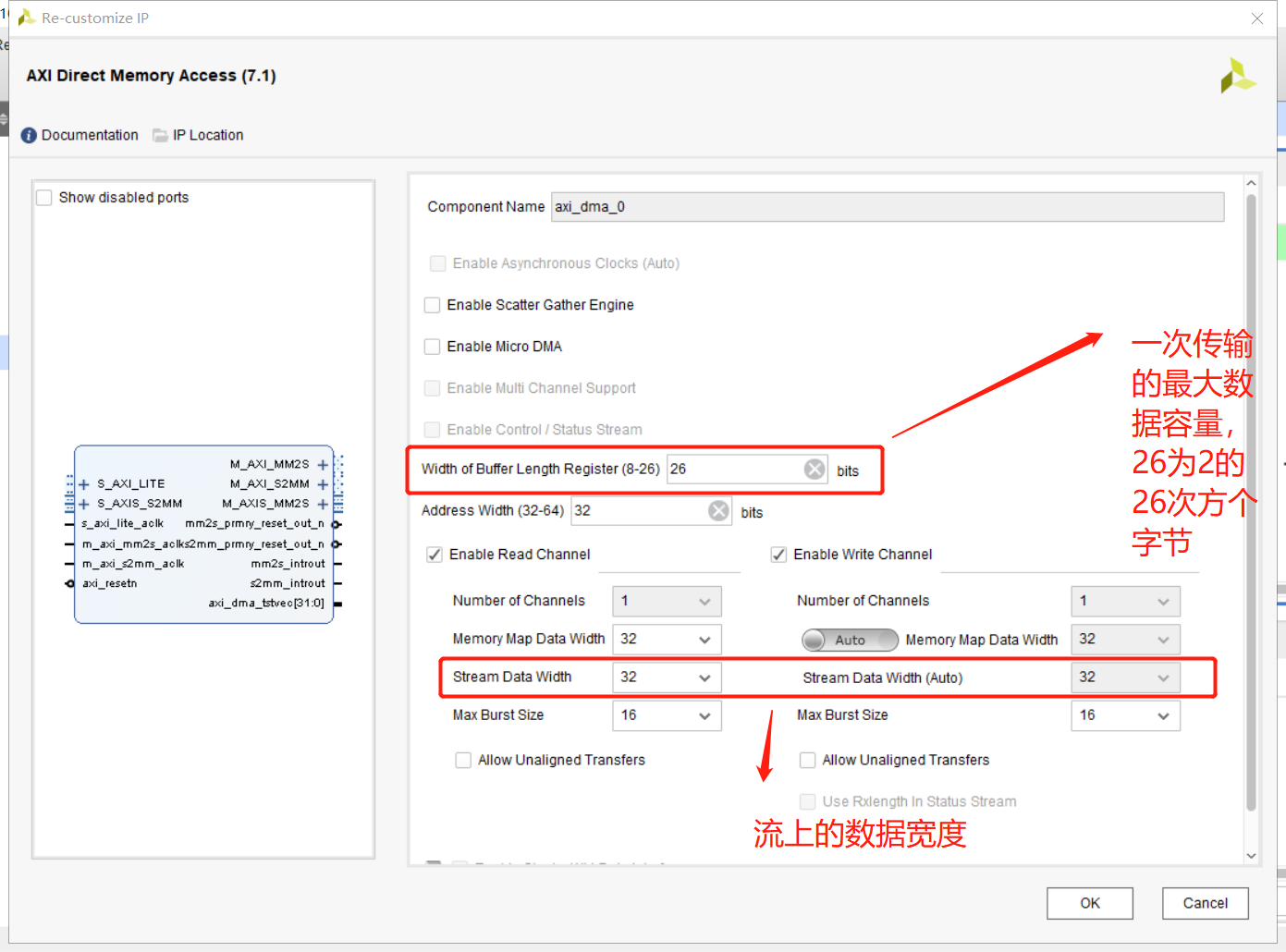
添加canny HLS ip,



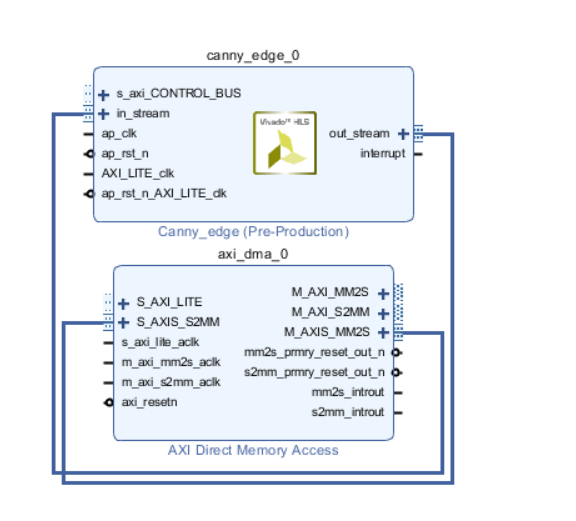
添加canny ip及AXI DMA到block中

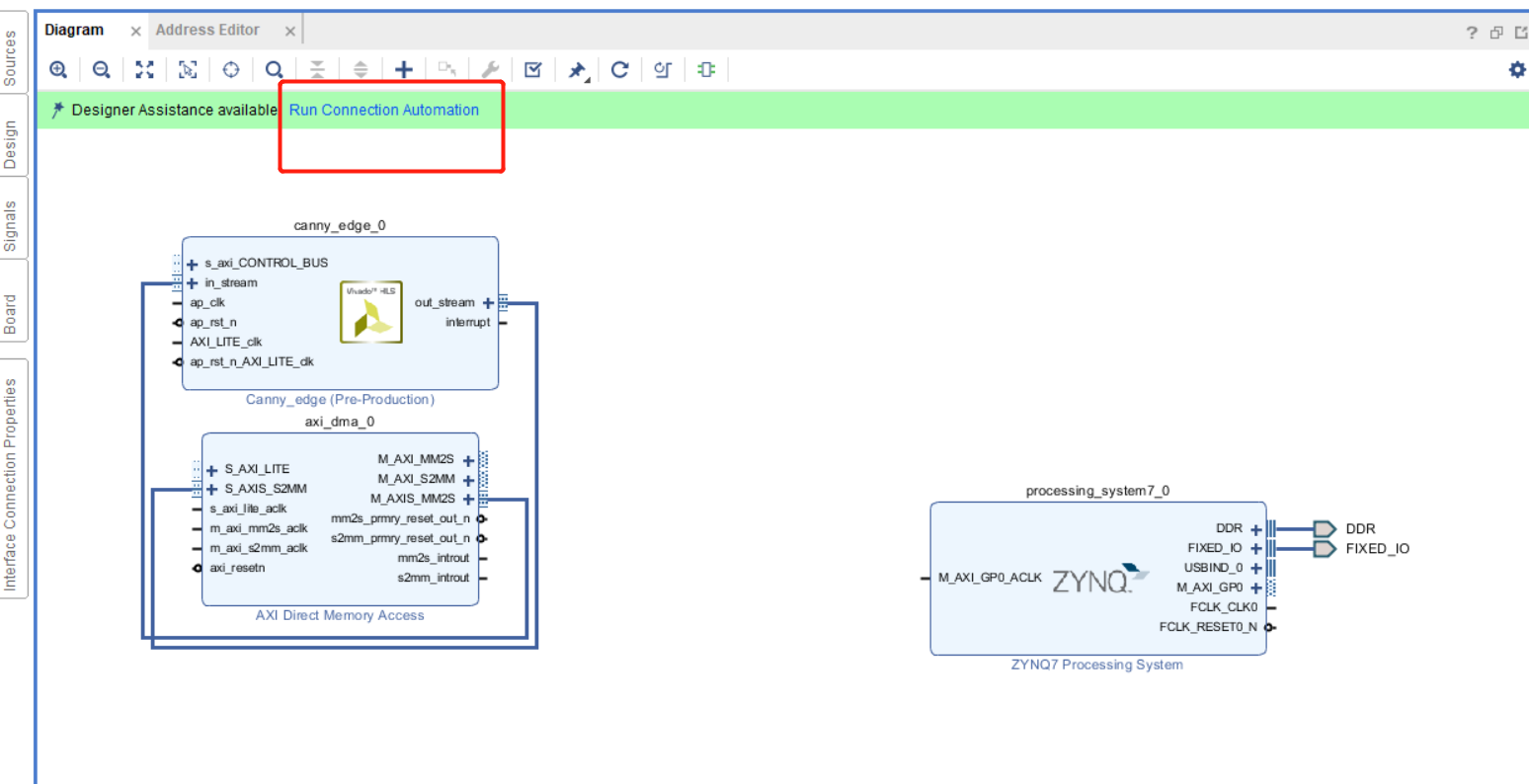


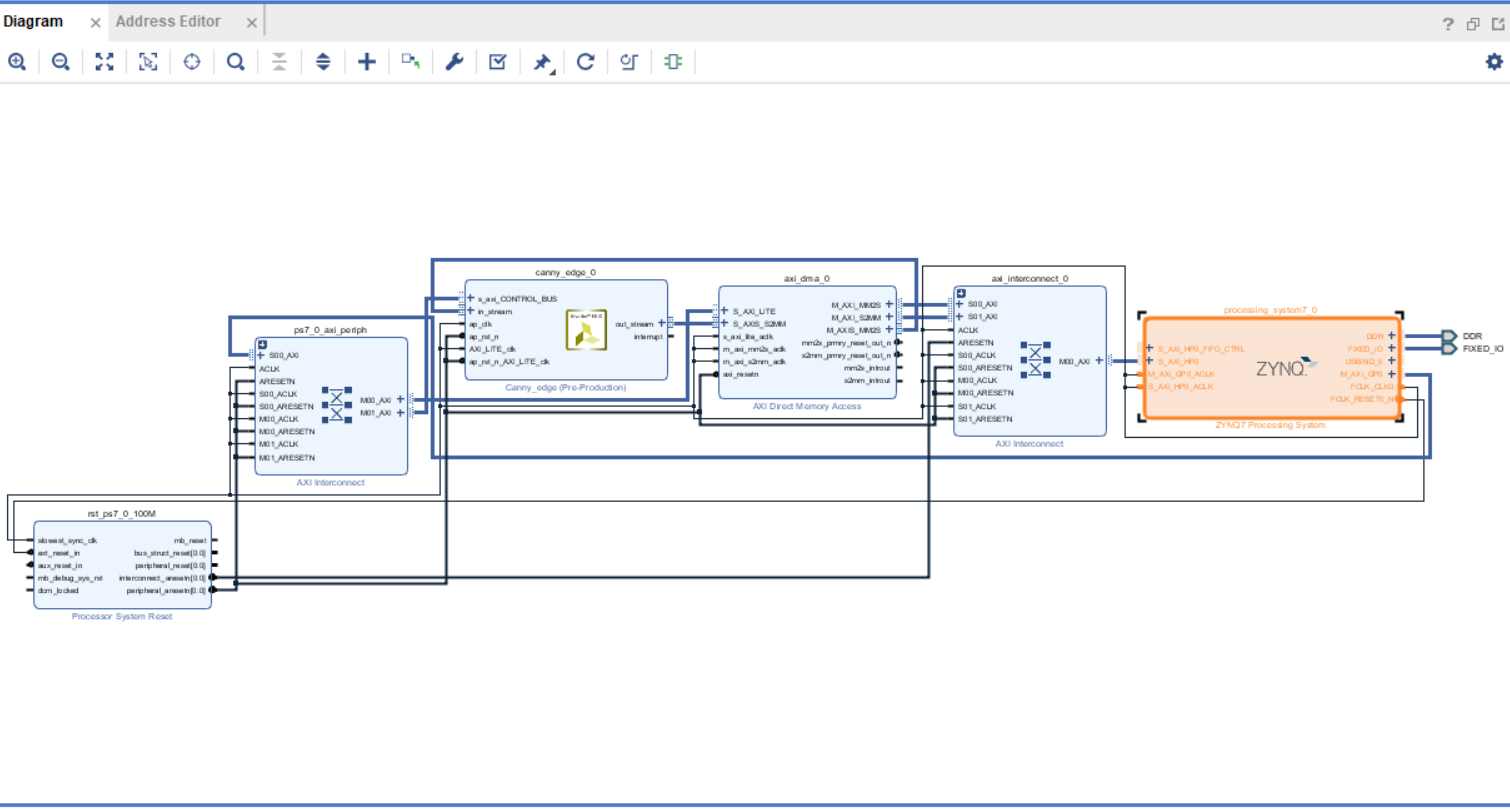
AXI DMA的配置如：



PL中的数据链路连接：

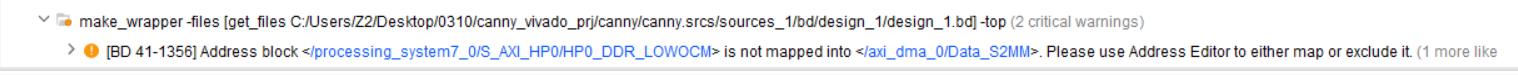




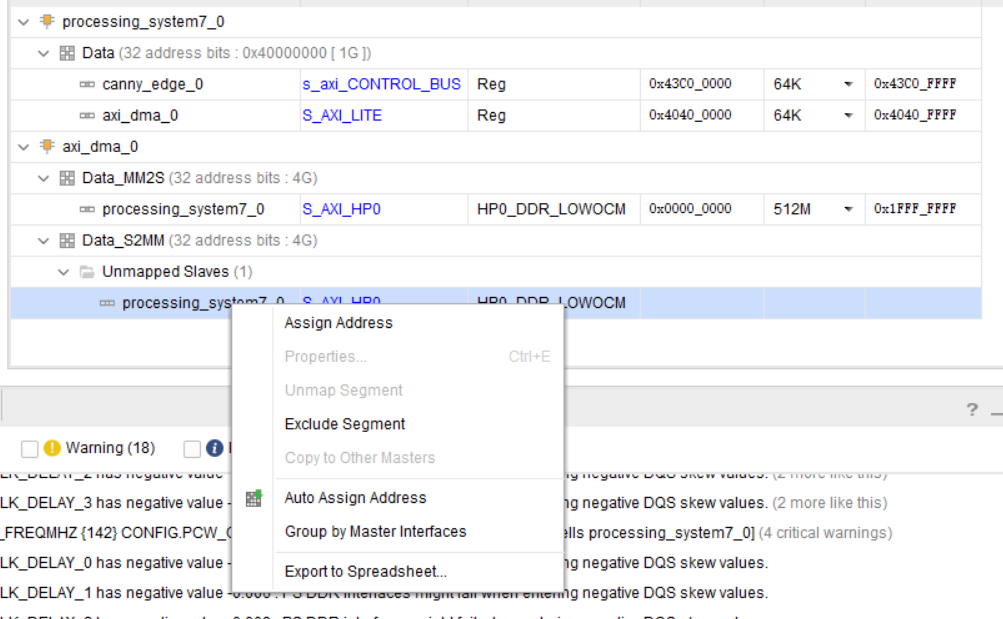


保存block design

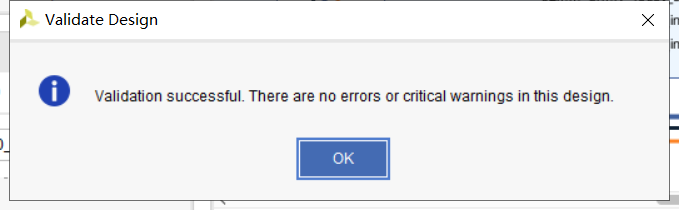
F6检查是否符合要求

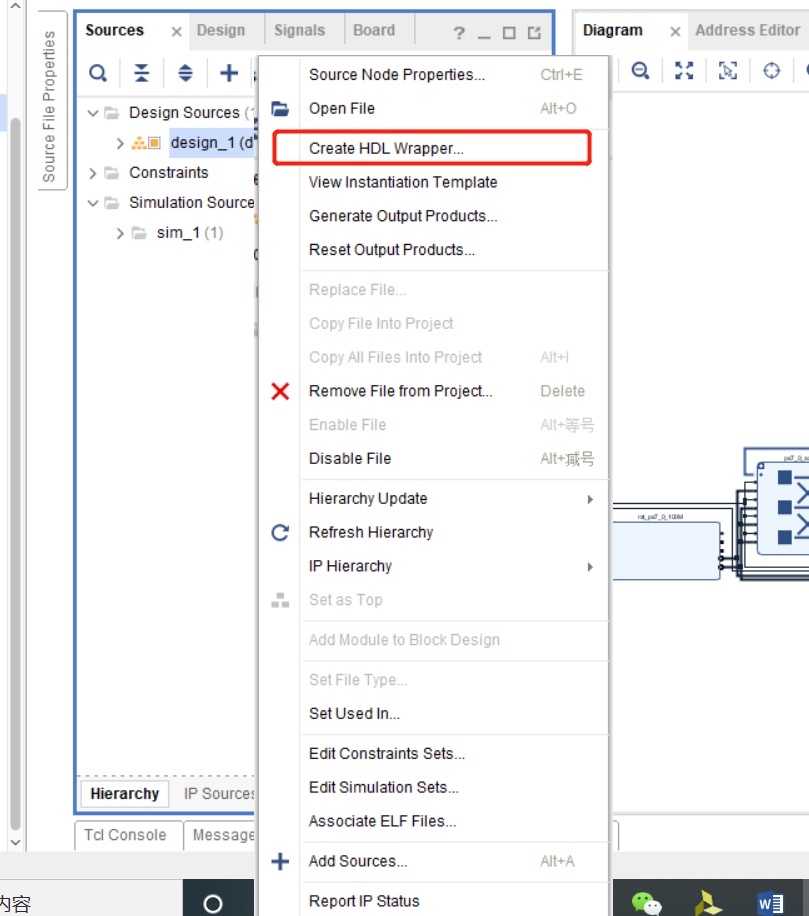


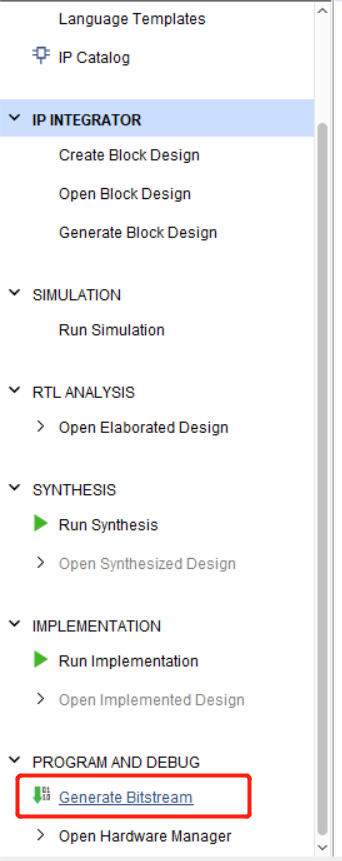
解决：



Assign address.

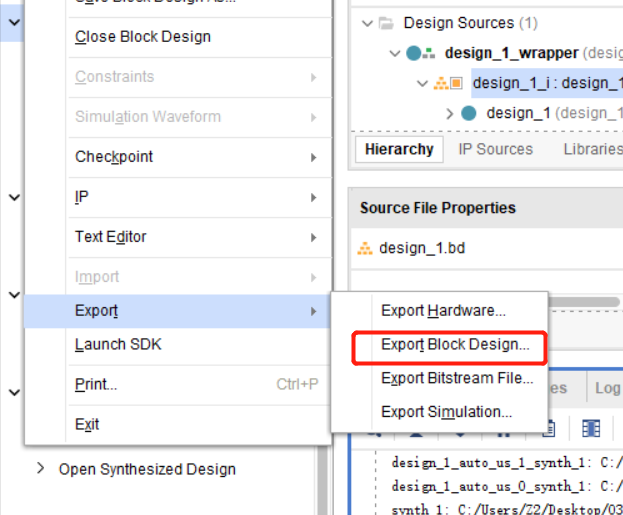




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等候数分钟。生成.bit文件

导出tcl文件：



然后上传至（注意要同名）



然后运行即可

