TENTATIVE Lecture and Lab Schedule for ECE 241F, 2014

Week	Topics covered	Textbook sections	Lab Exercises
1-Sep	Overview of the course: topics covered, mark breakdown (midterm test, labs, final exam), quick overview of digital systems and Moore's law, examples of digital systems, overview of how the lab exercises are organized (students work in groups of two), marks assigned for preparation and lab performance); binary numbers, hex numbers	Chapter 1, 3.1	
8-Sep	Transistors as simple on-off switches; introduction to logic expressions; AND, OR, NOT circuits built using switches; AND, OR, NOT gate symbols; truth tables; simple example of logic circuit with AND, OR, NOT gates	2.1 - 2.4	
	Boolean algebra: duality, axioms, rules, identities; proof of identities using perfect induction (i.e., truth tables); algebraic manipulation of Boolean expressions; timing diagrams; Venn Diagrams and their use to prove some identities	2.5	
	Simple synthesis of logic circuits; sum-of-products (SOP) form; minterms; canonical SOP; product-of-sums form (POS); maxterms; canonical POS; examples of algebraic manipulation;	2.6	
15-Sep	Example logic functions: 2-to-1 multiplexer, XOR gate, full-adder, ripple-carry adder, 7-seg; NAND and NOR logic networks; convert SOP to NAND-NAND, POS to NOR-NOR. Intro to Lab 1	B.5 2.7, 3.2	**Lab 1: Building Simple Logic Functions with 7400-series Chips**
	Verilog introduction, including hierarchy	2.10, Appx A	**Lab tutorial: read on your own time the tutorial: Quartus II Introduction (you must at least do the version that uses Verilog, and can consider also doing the Schematic design version). Download tutorials from the Digital Logic section of http://www.altera.com/education/univ; perform tutorial steps outside of the lab using simulation only**
22-Sep	Introduction to Field Programmable Gate Arrays (FPGAs), lookup tables; Introduction to CAD tools	B.6.5, 2.9	
	Introduction to cost of a logic circuit; terminology: implicant, prime implicant (PI), essential PI, cover, minimum-cost cover; introduction to K-maps (2, 3, 4 variables) More examples of K-maps use, incl as a guide to algebraic manipulation	2.11 - 2.14	**Lab 2: Switches, Lights, and Multiplexers**
29-Sep	5-variable K-maps; don't cares, examples, incl 7-seg with DC		
	Storage elements: introduction, RS latches, timing diagrams, gated RS latch. Gated D latch, D flip-flops, setup and hold times	2.8.3, 5.1 - 5.4	**Lab 3: Combinational Logic and Displays**
6-Oct	Flip-flop reset/preset; registers; shift registers; parallel load Verilog code for synchronous circuits (unblocked assignments) Spare lecture for midterm review	5.5, 5.7, 5.8 5.12	**Lab 4: Latches, Flip-flops, and Registers**
13-Oct	Counters; ripple and synchronous counters; Verilog for counters	5.9, 5.10, 5.13	
	Signed numbers; 2's complement; adders/subtractors Verilog code for arithmetic circuits	3.3	**Midterm week. No lab**
20-Oct	Carry lookahead, multipliers	3.4, 3.6	
	Combinational circuits: implementing logic functions using only multiplexers	4.1 - 4.3	**Lab 5: Counters and Arithmetic**
	Decoders, other combinational circuits; Verilog code	4.4 - 4.6	
27-Oct	Finite state machines intro, one-hot encoding	6.1	
	FSM state assignment, binary encoding Verilog code for FSMs	6.2, 6.4, 6.5	**Lab 6: Finite State Machines**
3-Nov	FSM timing issues (Moore vs Mealy models)		
	RAM and ROM, including FPGA embedded memory Discussion of optional course project, incl VGA and videos	6.3, B.9	**Lab 7: Complex State Machines and VGA Display**
10-Nov	Design example: intro to processors	7.1 – 7.2	
	Timing analysis of circuits: maximum clock frequency, hold time	7.8	**Project 1**
17-Nov	Clock skew, clock synchronization, switch debouncing	7.8 cont.	
	Transistors: S, G, D Building logic gates: NMOS, PMOS, and CMOS	B.1 - B.3	**Project 2**
24-Nov	Timing issues in transistor circuits		
	Synthesis examples: using lookup tables in FPGAs Design examples, miscellaneous topics	B.8, 5.15, B.6.5	**Project 3**
1-Dec	Spare lecture (for review, etc)		
	Spare lecture, for some sections of the course (for review, etc)		