Checklist and Suggested Flow : Layout implications
ECEN 4303 : Digital Integrated Circuit Design, Fall 2018
Oklahoma State University

The following are suggestions that may help those that are having a hard time starting. As always, it is highly recommended that you spend at least one full day using stick diagrams to map things out for your floorplan. Make sure you use the Law of 8 to help you get sizes to help with the pitch matching. Feel free to increase the pitch size to adequately make sure your interconnect can target your intended connections. Making the pitch too large could potentially make your layout ridiculously large for its intended target and possibly miss your delay target. This documents presents a basic overview of the design flow methodology. Remember also to draw the schematics as you plan to lay them out. Do not cheat by creating a schematic of the final design unless you expect to build it this way step-by-step. Again, these steps are meant to give you an approximate vehicle to complete the project; they, in no way, are the only method for completing your work.

Design Flow Methodology

This is your first experience with dealing with a design flow and I hope you see how important it is to know the design flow in and out as well as the importance of floor planning. Based on previous student experiences, we have found it would have been helpful if most of the design flow steps were listed in this document. The steps executed in the following order are summarized below (approximately). These steps are meant to give you an idea of the design methodology to follow to complete the design. Your process may more or less resemble these steps feel free to think outside the box.

Setup

1. Pick a partner, if needed, and organize your directory and create a plan of attack!
2. Copy over project directory to your directory: `cp -r /classes/ecen4303F18/project_F18 .`

Sue

3. Examine Sue schematics
4. Generate `.sim` file from Sue
5. Test project.cmd with IRSIM.

Stick Diagrams

6. Develop a bit-slicing attack!
7. Create your stick Diagrams!
8. Floorplan out your layout and complete datapath

Magic

9. Build the layout of the 1-bit DFF
10. Test with calibre
11. Build the layout of the 1-bit adder
12. Test with calibre
13. Build the layout of the mux21 gate
14. Test with calibre
15. Build the layout of the AND gate
16. Test with calibre
17. Hook complete 1-bit unit (`bit1a.sue`)
18. Test with calibre
19. Hook complete 1-bit unit (`bit1b.sue`) (Note: this floorplan may be different than your other 1-bit unit)
20. Test with calibre
21. Bit-slice custom layout across word-length (might require some zipper lines)
22. LVS with calibre
23. Simulate with IRSIM cmd file from Sue above and see if you get same result (This will almost always work if your LVS on Step 22 is clean).

Verilog

24. See `fsm.sv` for sample FSM
25. Implement the FSM in Verilog and test FSM using the included DO file

HSPICE and Final Items

26. Simulate critical path of custom part in HSPICE.
27. Assemble chip using instructions provided by instructor.
28. Gather statistics of your design, including area, timing, and final pplot.
29. Write your report (estimate 1 week's worth amount of time for final report)!
30. Submit your report, project and final files