

1. Description

1.1. Project

Project Name	Project
Board Name	custom
Generated with:	STM32CubeMX 6.8.0
Date	03/28/2023

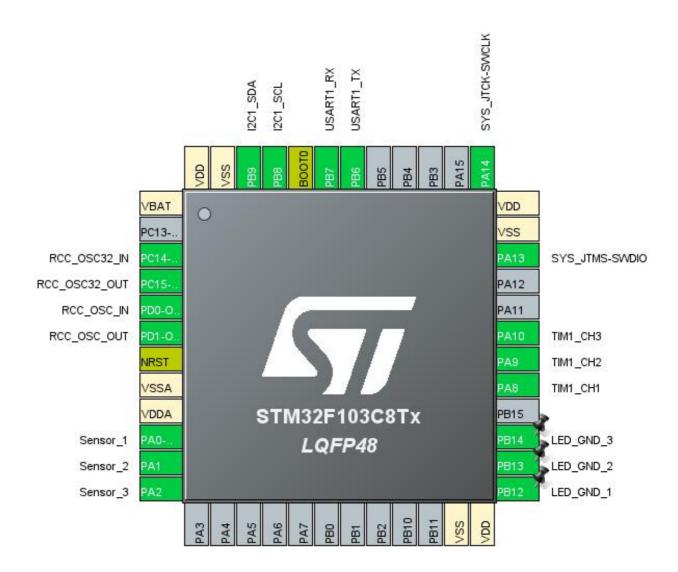
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration

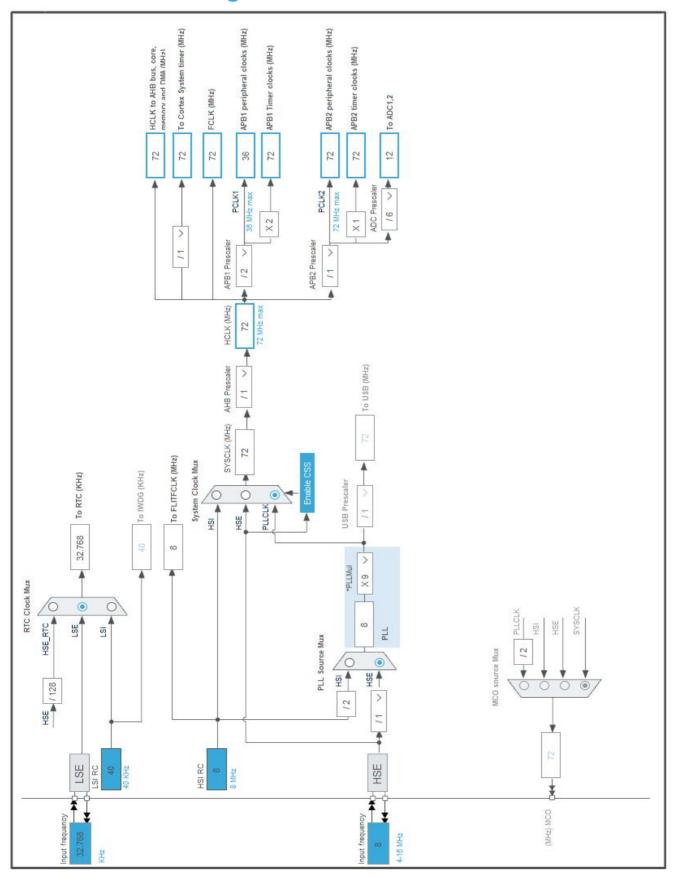


3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	Sensor_1
11	PA1	I/O	ADC1_IN1	Sensor_2
12	PA2	I/O	ADC1_IN2	Sensor_3
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Output	LED_GND_1
26	PB13 *	I/O	GPIO_Output	LED_GND_2
27	PB14 *	I/O	GPIO_Output	LED_GND_3
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	TIM1_CH2	
31	PA10	I/O	TIM1_CH3	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
42	PB6	I/O	USART1_TX	
43	PB7	I/O	USART1_RX	
44	BOOT0	Boot		
45	PB8	I/O	I2C1_SCL	
46	PB9	I/O	I2C1_SDA	
47	VSS	Power		
48	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value	
Project Name	Project	
Project Folder	D:\Documents\GithubProjects\STM32_IntelligentLightingControlSystem\Project	
Toolchain / IDE	MDK-ARM V5.32	
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.4	
Application Structure	Advanced	
Generate Under Root	No	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART1_UART_Init	USART1
5	MX_TIM1_Init	TIM1
6	MX_ADC1_Init	ADC1
7	MX_RTC_Init	RTC
8	MX_I2C1_Init	I2C1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	DS5319_Rev17

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27 mA	14 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.1	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days,	Average DMIPS	61.0 DMIPS
	17 hours		

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1 mode: IN0 mode: IN1 mode: IN2

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Discontinuous Conversion Mode

Right alignment

Enabled

Enabled

Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Number Of Conversion 3 *

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Channel 0
Sampling Time 1.5 Cycles
Rank 2 *

2 ~

Channel 1 *
Sampling Time 1.5 Cycles
Rank 3 *

Channel 2 *
Sampling Time 1.5 Cycles

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

WatchDog:

Enable Analog WatchDog Mode false

7.2. I2C1 I2C: I2C

7.2.1. Parameter Settings:

Master Features:

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) 100000

Slave Features:

Clock No Stretch Mode Disabled

Primary Address Length selection 7-bit

Dual Address Acknowledged Disabled

Primary slave address 0

General Call address detection Disabled

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

7.4. RTC

mode: Activate Clock Source mode: Activate Calendar RTC OUT: No RTC Output 7.4.1. Parameter Settings:

Calendar Time:

Data Format BCD data format

Hours 15 *
Minutes 0
Seconds 0

General:

Auto Predivider Calculation Enabled

Asynchronous Predivider value Automatic Predivider Calculation Enabled

Output No output on the TAMPER pin

Calendar Date:

Week Day

Month

March *

Date

Year

Tuesday *

March *

28 *

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.6. TIM1

Clock Source: Internal Clock
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

71 *

Up

65535

No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection

Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI)

Lock Configuration

Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

7.7. **USART1**

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate 9600 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

* User modified value		
Oser modified value		

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	Sensor_1
	PA1	ADC1_IN1	Analog mode	n/a	n/a	Sensor_2
	PA2	ADC1_IN2	Analog mode	n/a	n/a	Sensor_3
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	n/a	High *	
	PB9	I2C1_SDA	Alternate Function Open Drain	n/a	High *	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PD0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	n/a	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PB7	USART1_RX	Input mode	No pull-up and no pull-down	n/a	
GPIO	PB12	GPIO_Output	Output Push Pull	Pull-down *	High *	LED_GND_1
	PB13	GPIO_Output	Output Push Pull	Pull-down *	High *	LED_GND_2
	PB14	GPIO_Output	Output Push Pull	Pull-down *	High *	LED_GND_3

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte
Memory Data Width: Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
RTC global interrupt	true	0	0	
DMA1 channel4 global interrupt	true	0	0	
DMA1 channel5 global interrupt	true	0	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1 and ADC2 global interrupts	unused			
TIM1 break interrupt	unused			
TIM1 update interrupt	unused			
TIM1 trigger and commutation interrupts	unused			
TIM1 capture compare interrupt	unused			
I2C1 event interrupt	unused			
I2C1 error interrupt	unused			
USART1 global interrupt	unused			

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
RTC global interrupt	false	true	true

Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
DMA1 channel4 global interrupt DMA1 channel5 global interrupt	false	true true	true

^{*} User modified value

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f1_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32ibis.zip

System View https://www.st.com/resource/en/svd/stm32f1_svd.zip

Description

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