

Assignment No : 1

Q.1 Write short note on assembler directives, macros and procedures.

⇒ • Assembler Directives

⇒ These are the statements that directs the assembler to do something. As the name says, it direct the assembler to do a task.

We can divide the assembler directives into various categories.

They are classified into the following categories based on the function performed by them.

- a) Simplified segment directives.
- b) Data allocation directives
- c) Segment directives.
- d) Macros related directives.
- e) Code label directives
- f) Scope directives
- g) Listing control directives.
- h) Miscellaneous directives.

Model	No. of code segments	No. of data segments
Small	One code segment & size $\leq 64\text{ kB}$	One of size $\leq 8\text{ kB}$
Medium	Code segment may be of any no and any size	One of size $\leq 64\text{ kB}$
Compact	One of size $\leq 64\text{ kB}$	Data segment of any no and any size.
Large	Any no, Any size	Any no, Any size

- Macros

⇒ Macros is a set of instruction and the programmer can use it anywhere in the program by using its name. It is mainly used to achieve modular programming. So same set of instructions can be used multiple times whenever required by the help of macro. Whenever macro's identifier is used, it is replaced by the actual defined instructions during compilation thereby no calling and return occurs.

Syntax of Macros

⇒

```
%macro macro-name no-of-parameters
    <macro body>
%endmacro
```

- Procedures

⇒ Procedures are also like macros but they are used for large set of instructions when macro is useful for small set of instructions. It contains a set of instructions which perform a specific task. It contains three main parts i.e. Procedure name to identify the procedure, procedure body which contains set of instruction and RET statements which denote return statements.

Syntax :

```
procedure-name
procedure body
...
RET
```

Q.2

i) Discuss operating mode of 8259.

⇒ 8259 has two operating modes, viz. interrupt driven and polling mode.

- In interrupt driven mode, 8259 interrupts the processor with the INT pin whenever it gets an interrupt

- Polling Mode

⇒ In this mode the INT output is not used.

The microprocessor checks the status of the interrupt request by issuing poll command. The microprocessor reads the content of 8259A after issuing the poll commands.

During the read operation the 8259A provides polled word and set the ISR bit of highest active interrupt request in following format.

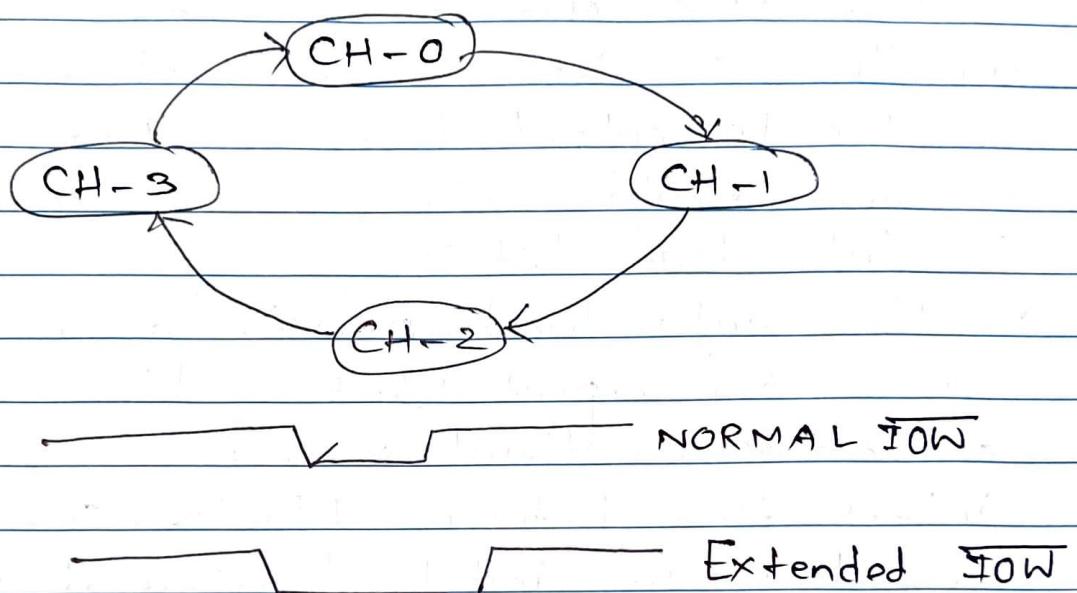
$I = 1$ \downarrow	One or more interrupt requests activated	$I \times \times \times \times W_2 W_1 W_0$ \curvearrowright
		Binary code of highest active priority

$I = 0$	No interrupt request activated	interrupt request
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ii) Explain interfacing of 8259 with 8086, in cascading mode.

- ⇒ • For 8259 can be interfaced with 8086 in following different policies -
- i) 8259 in single mode and 8086 in minimum mode.
 - ii) 8259 in single mode and 8086 in maximum mode.
 - iii) 8259 in cascaded mode and 8086 in minimum mode.
 - iv) 8259 in cascaded mode and 8086 in maximum mode.
- The control signals are provided by 8086 in case of minimum mode, while in maximum mode, bus controller 8288 provides control signals.
- For cascaded 8259, the INT pin of the slaves are connected to the interrupt request pins ($IR_0 - IR_7$) and \overline{INTA} to the \overline{INTA} of master.
- The CAS2- CAS0 lines works as output for the master and input for the slave.

- iii) Explain operating modes of DMAC8257.
- ⇒ i) Rotating Priority Mode
- ⇒ In this case, the DMA channel which is just serviced becomes the lowest priority and next one gets the highest priority. This allows all the channel to get a chance to be serviced.



- ii) Fixed Priority Mode
- ⇒ If the devices connected to the DMAC are of different priority then this mode must be used. In this case the device connected on the channel 0 is given the highest priority and in decreasing order the one connected on channel 3 is given the least priority.
- iii) Extended Write
- ⇒ If EXTENDED Write bit is set, the

duration of both the $\overleftarrow{\text{MEMW}}$ and $\overrightarrow{\text{IOW}}$ signals is extended by activating them earlier in the DMA cycle.

4) TC Stop

⇒ In the TC stop bit is set, a channel is disabled after the Terminal count (TC) output goes true, thus automatically preventing further DMA operation on that channel.

If the TC bit is not set, the occurrence of the TC output has no effect on the channel enable bits.

5) Auto load bit 7

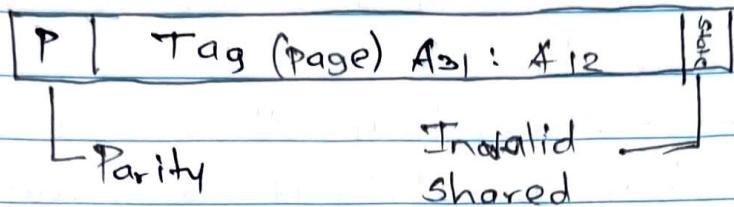
⇒ The auto load permits channel 2 to be used for repeat block or block chaining operations, without immediate software intervention between blocks. Channel 2 registers are initialized as usual for the first data block. Channel 3 registers, however, are used to store the block reinitialization parameters.

Q.3 Write short note on Hyperthreading technology in Pentium 4.

- ⇒ • Hyper-threading is a technology developed by Intel corporation.
- It is used in certain Pentium 4 processors and all Intel Xeon processors.
- Hyper-threading technology, commonly referred to as "HT-Technology", enables the processor to execute two threads, or set of instructions at the same time.
- Since hyper-threading allows two streams to be executed in parallel, it is almost like having two separate processors working together.
- While hyper-threading can improve processing performance, software must support multiple processors to take advantages of the technology.
- Fortunately, recent versions of both Windows and Linux support multiple processors and therefore benefit from hyper-threading.

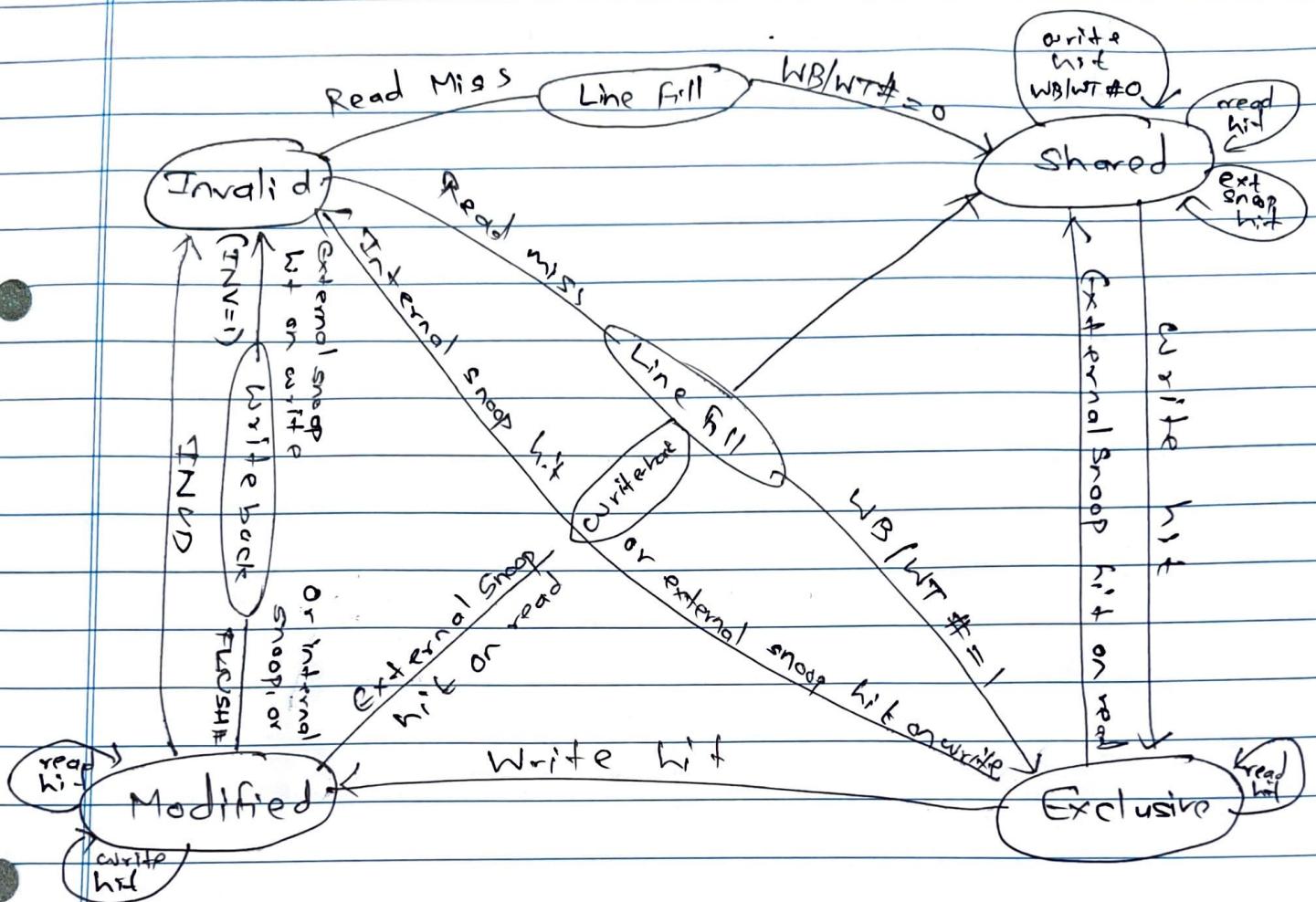
Q. 4

- 1) Explain the cache organization of Pentium processor.
-
- The code cache is 8KB in size, organized as two-way set-associative mapping configuration.
 - The cache ways are referred to as way zero and way one as shown.



- Each cache line is 32 bytes wide and the bus connected from this cache to the prefetcher is also 256 bits, allowing 32 bytes to be delivered to the prefetch queue during a single prefetch.
- Each cache way contains 128 cache lines, with a associated 128 entry directory with each of the cache ways.
- The cache directories are triple ported, to support split line access and snooping.
- The directory entry consists of a 20-bit tag field to identify the pages in the memory; a state bit that indicates whether the line in cache contains valid or invalid information and a parity bit used to detect errors when reading each entry.

v) Draw and explain MESI transitions in data cache of Pentium processor.



- 1) Internal Snoop hits is to be considered in case when the data required by the processor is there in code cache or vice versa. In such cases the modified line is written back to the Main memory and then invalidated , while a non modified line is simply invalidated.
 - 2) Flush# signal indicates the L1 cache to clear the entire cache. WBINVD indicates to clear a particular line in the L1 cache.

3) In case of a INV signal, that simply indicates to invalidate a line without even writing it back for a modified line also, the processor simply invalidate the corresponding line.