

Correctness and Performance Tools for OpenMP



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Correctness Checking

Race Condition



- Data Race: the typical OpenMP programming error, when:
 - → two or more threads access the same memory location, and
 - → at least one of these accesses is a write, and
 - → the accesses are not protected by locks or critical regions, and
 - → the accesses are not synchronized, e.g. by a barrier.
- Non-deterministic occurrence: e.g. the sequence of the execution of parallel loop iterations is non-deterministic and may change from run to run
- In many cases private clauses, barriers or critical regions are missing
- Data races are hard to find using a traditional debugger
 - → Use the Intel Inspector XE

Intel Inspector XE



Detection of

- → Memory Errors
- → Dead Locks
- → Data Races

Support for

- → Linux (32bit and 64bit) and Windows (32bit and 64bit)
- → WIN32-Threads, Posix-Threads, Intel Threading Building Blocks and OpenMP

New Features (compared to Intel Thread Checker)

- → Binary Instrumentation gives full functionality
- → Independent stand-alone GUI for Windows and Linux
- → memory error detection
- → static security analysis (in combination with the Intel 12.X compiler)

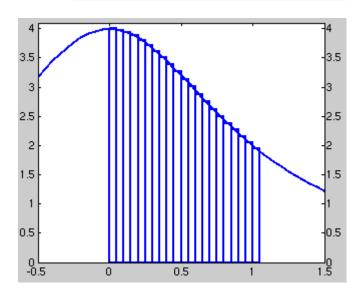
PI Example Code

```
double f(double x)
  return (4.0 / (1.0 + x*x));
double CalcPi (int n)
  const double fH = 1.0 / (double) n;
  double fSum = 0.0;
  double fX;
  int i;
#pragma omp parallel for private(fX,i) reduction(+:fSum)
  for (i = 0; i < n; i++)
    fX = fH * ((double)i + 0.5);
    fSum += f(fX);
  return fH * fSum;
```





$$\pi = \int_{0}^{1} \frac{4}{1 + x^2}$$



PI Example Code



```
double f(double x)
  return (4.0 / (1.0 + x*x));
double CalcPi (int n)
  const double fH = 1.0 / (double) n;
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```

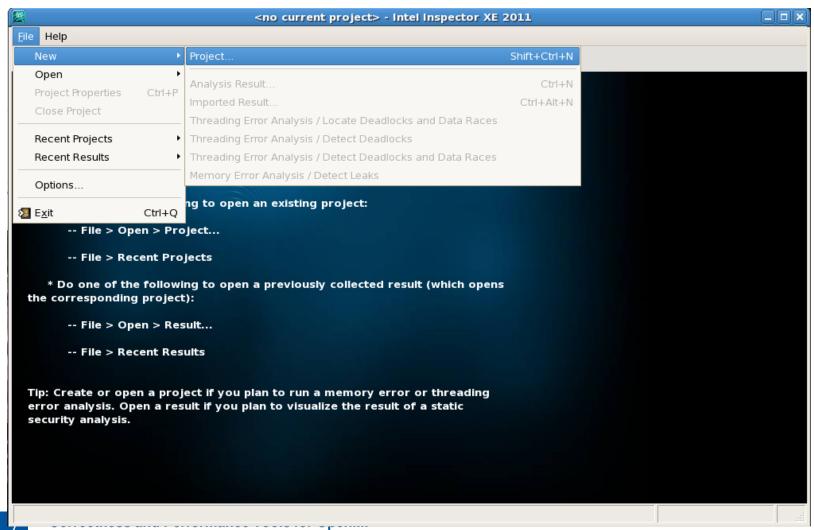
What if we would have forgotten this?

Inspector XE – Create Project





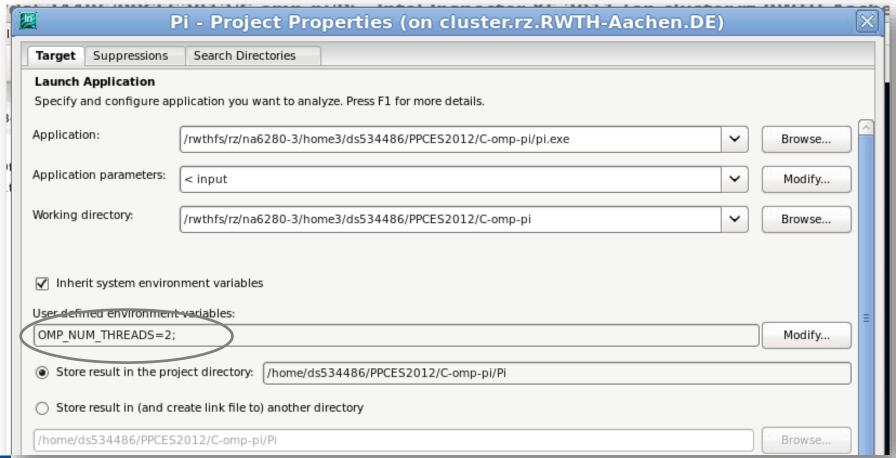
\$ module load intelixe; inspxe-gui



Inspector XE – Create Project



- ensure that multiple threads are used
- choose a real small dataset, execution time can grow 10X 1000X



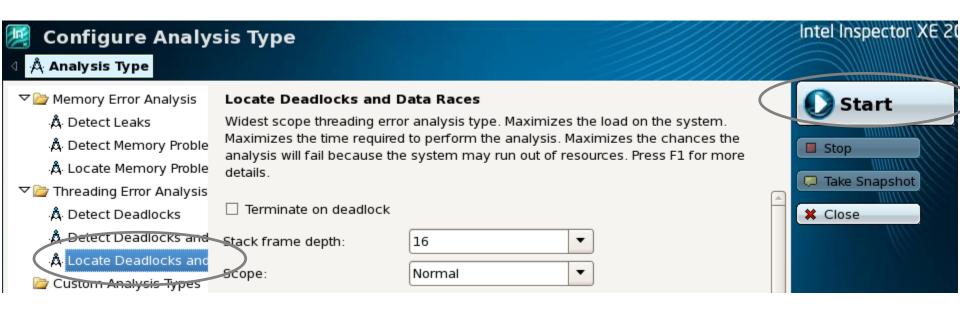
Inspector XE – Configure Analysis



Threading Error Analysis Modes

- Detect Deadlocks
- 2. Detect Deadlocks and Data Races
- 3. Locate Deadlocks and Data Races

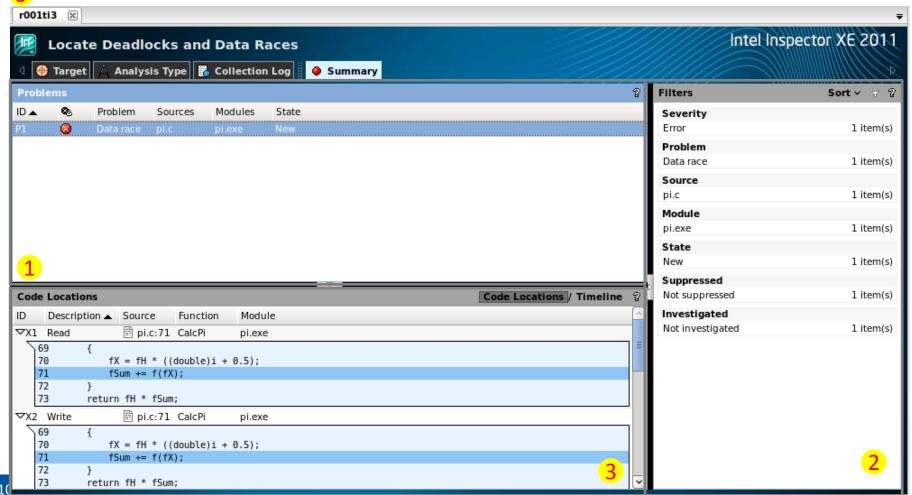
more details, more overhead





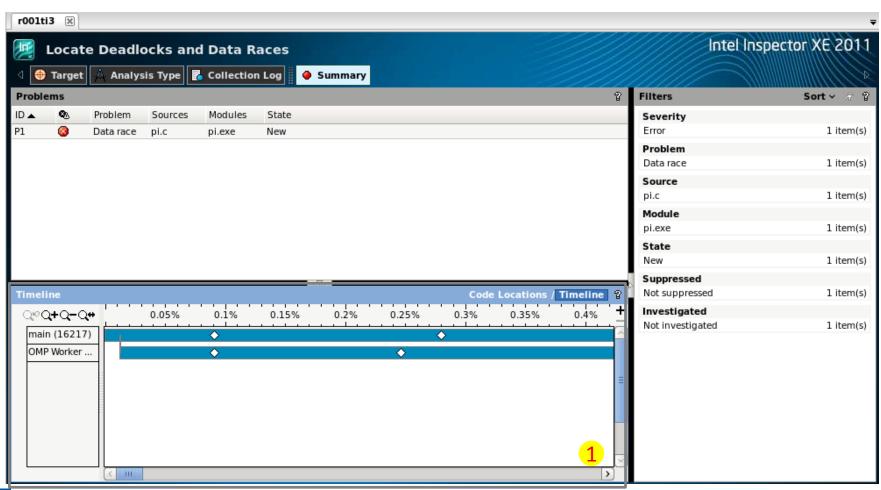


- 1 detected problems
- 2 filters
- 3 code location





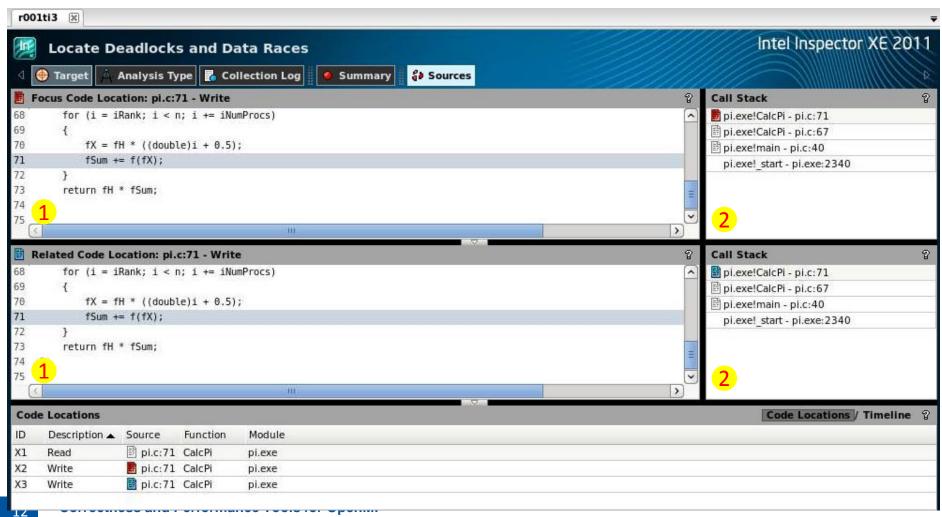
1 Timeline view







- Source Code producing the issue double click opens an editor
- 2 Corresponding Call Stack

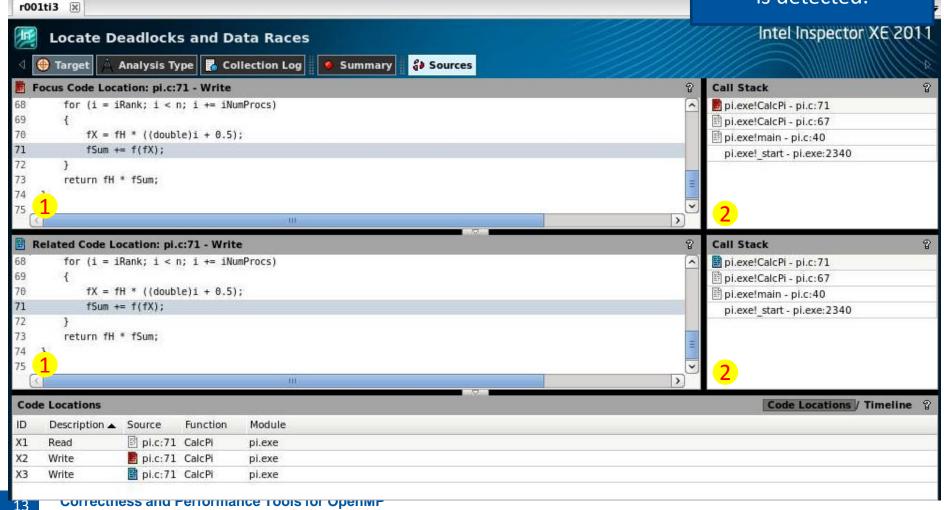






- Source Code producing the issue double click opens an editor
- 2 Corresponding Call Stack

The missing reduction is detected.



PI Example Code



```
double f(double x)
  return (4.0 / (1.0 + x*x));
double CalcPi (int n)
  const double fH = 1.0 / (double) n;
  double fSum = 0.0;
  double fX;
  int i;
#pragma omp parallel for private(fX,i,fSum)
  for (i = 0; i < n; i++)
    fX = fH * ((double)i + 0.5);
    fSum += f(fX);
  return fH * fSum;
```

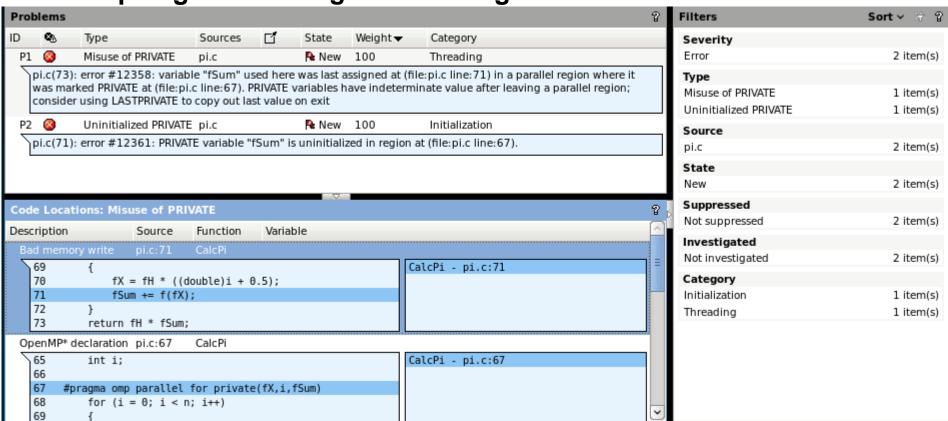
What if we just made the variable private?

Inspector XE – Static Security Analysis





- At runtime no Error is detected!
- Compiling with the argument "-diag-enable sc-full" delivers:



At compile-time this error can be found!

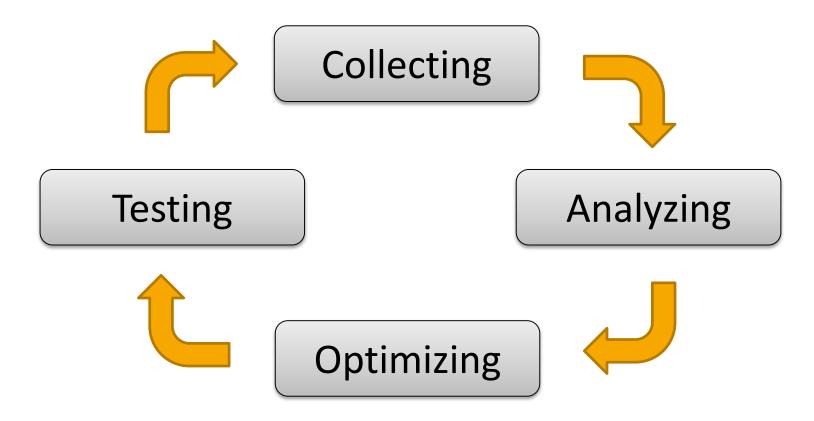


Performance Tuning

Tuning Cycle



Performance Tuning aims to improve the runtime of an existing application.



Hotspots



A Hotspot is a source code region where a significant part of the runtime is spent.

90/10 law

90% of the runtime in a program is spent in 10% of the code.

- Hotspots can indicate where to start with serial optimization or shared memory parallelization.
- Use a tool to identify hotspots. In many cases the results are surprising.



Performance Tools

VTune Amplifier XE



- Performance Analyses for
 - → Serial Applications
 - → Shared Memory Parallel Applications
- Sampling Based measurements
- Features:
 - → Hot Spot Analysis
 - → Concurrency Analysis
 - → Wait
 - → Hardware Performance Counter Support

Stream



- Standard Benchmark to measure memory performance.
- Version is parallelized with OpenMP.

Measures Memory bandwidth for:

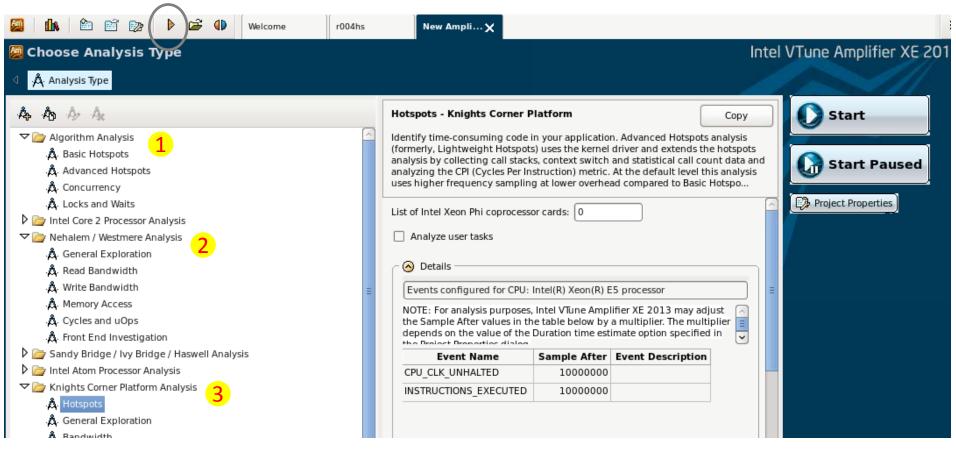
for double vectors x,y,z and scalar double value s

Function	Rate (MB/s)	Avg time	Min time	e Max time
Copy: Scale:	33237.0185	0.0050	0.0048	0.0055
Scale:	33304.6471	0.0049	0.0048	0.0059
Add:	35456.0586	0.0070	0.0068	0.0073
Triad:	36030.9600	0.0069	0.0067	0.0072

Amplifier XE – Measurement Runs



- Basic Analysis Types
- 2 Hardware Counter Analysis Types, choose Nehalem Architecture, on cluster-linux-tuning.
- 3 Analysis for Intel Xeon Phi coprocessors, choose this for OpenMP target programs.



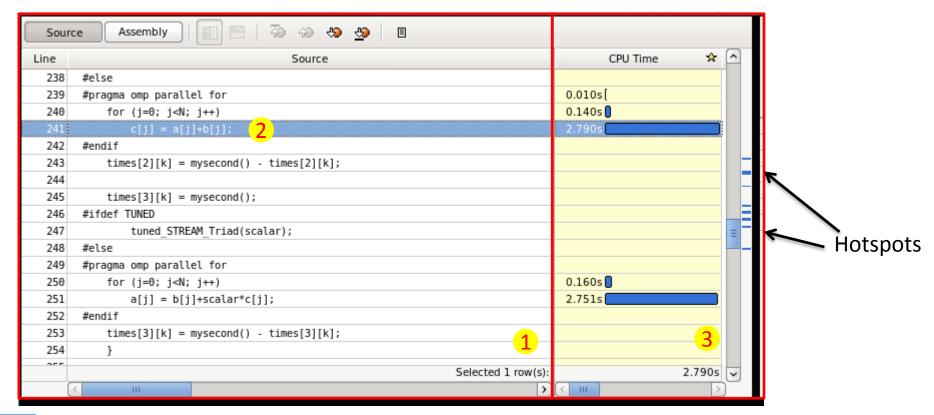
Amplifier XE – Hotspot Analysis





Double clicking on a function opens source code view.

- Source Code View (only if compiled with -g)
- 2 Hotspot: Add Operation of Stream
- 3 Metrics View





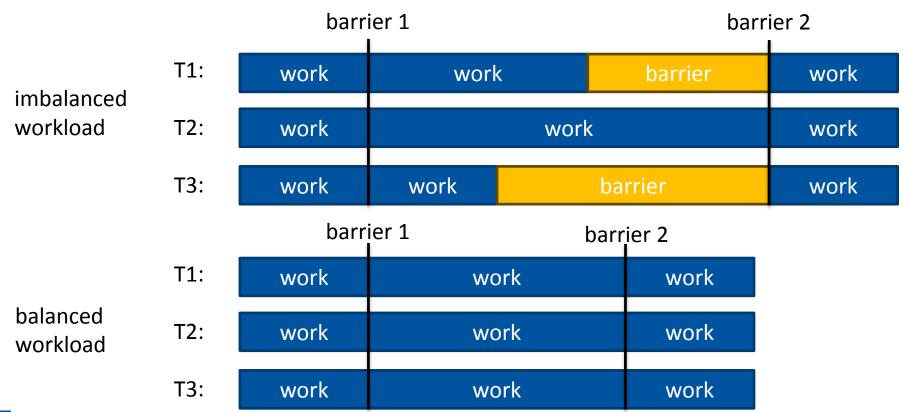
Load Balancing

Load imbalance



Load imbalance occurs in a parallel program

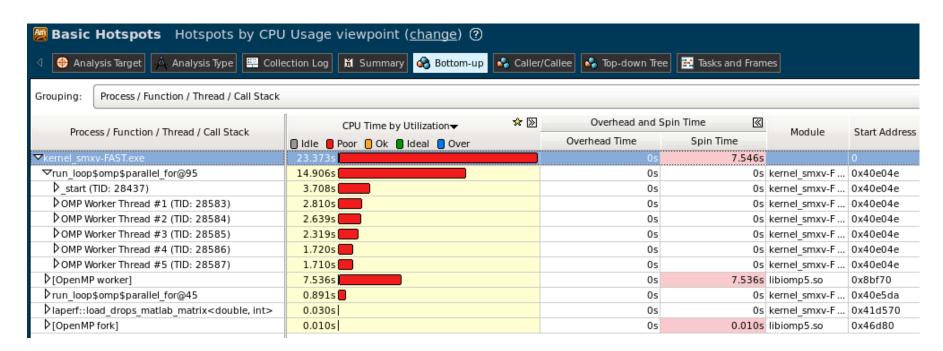
- → when multiple threads synchronize at global synchronization points
- → and these threads need a different amount of time to finish the calculation.



Load Imbalance in VTune



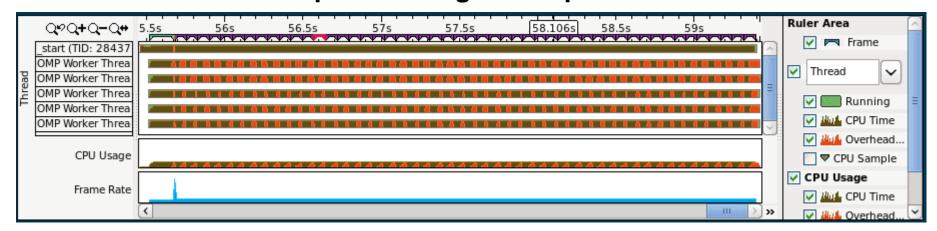
- Grouping execution time of parallel regions by threads helps to detect load imbalance.
- Significant potions of Spin Time also indicate load balance problems.
- Different loop schedules might help to avoid these problems.



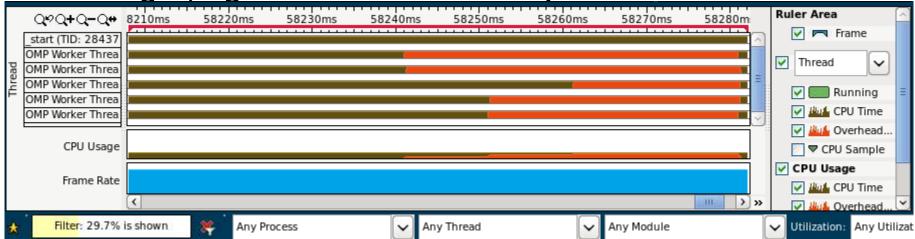
Load Imbalance in VTune



The Timeline can help to investigate the problem further.



Zooming in, e.g. to one iteration is also possible.





Detecting remote accesses



Hardware Counters

Definition: Hardware Performance Counters

In computers, hardware performance counters, or hardware counters are a set of special-purpose registers built into modern microprocessors to store the counts of hardware-related activities within computer systems. Advanced users often rely on those counters to conduct low-level performance analysis or tuning.

(from: http://en.wikipedia.org)

Hardware Performance Counters





Hardware Counters of our Intel Nehalem Processor:

SB DRAIN.ANY, STORE BLOCKS.AT RET, STOR MEM INST RETIRED.LOADS, MEM INST RET MEM_UNCORE_RETIRED.OTHE, MEM_UNCO FP COMP OPS EXE.SSE2 INT. FP COMP OP SIMD_INT_128.UNPACK, SIMD_INT_128.PACK INST QUEUE WRITES, INST DECODED.DECO, L2_RQSTS.IFETCH_HIT, L2_RQSTS.IFETCH_MIS L2 WRITE.RFO.S STATE, L2 WRITE.RFO.M ST

L11.HITS:

Counts all instruction fetches that hit the L1 L2_DATA_RQSTS.DEMAND.M_, L2_DATA_RQS INSTRUCTION cache.

AD MISSES.PDE MIS, DTLB LOAD MISSES.LARGE W, MEM UNCORE RETIRED.L3 D, MP_OPS_EXE.MMX, FP_COMP_OPS_EXE.SSE_FP, NT 128.PACKED SHIFT, SIMD INT 128.PACK, B, LOAD_DISPATCH.ANY, ARITH.CYCLES_DIV_BUSY, HIT, L2 RQSTS.RFO MISS, L2 RQSTS.RFOS, S.DEMAND.S_S, L2_DATA_RQSTS.DEMAND.E_S, A_RQSTS.PREFETCH.M, L2_WRITE.RFO.I_STATE, E, L2 WRITE.LOCK.HIT, L2 WRITE.LOCK.MESI,

L1D_WB_L2.I_STATE, L1D_WB_L2.S_STATE, L1D_WB_L2.E_STATE, L1D_WB_L2.M_STATE, L1D_WB_L2.M_S L1D CACHE LD.M STATE, L1D CACHE LD.MESI, L1D CACHE ST.S STATE, L1D CACHE ST.E STATE, L1D CACHE ST.M STATE, L1D CACHE LOCK.HIT, L1D CACHE LOCK.S STATE, L1D CACHE LOCK.E STATE, L1D CACHE LOCK.M STATE, L1D ALL REF.ANY, L1D_ALL_REF.CACHEABLE, DTLB_MISSES.ANY, DTLB_MISSES.WALK_COMPLET, DTLB_MISSES.STLB_HIT, DTLB_MISSES.PDE_MISS, DTLB_MISSES.LARGE_WALK_C, LOAD_HIT_PRE, L1D_PREFETCH.REQUESTS, L1D_PREFETCH.MISS, L1D_PREFETCH.TRIGGERS, L1D.M_REPL, L1D.M_EVICT, L1D.M_SNOOP_EVICT, L1D_CACHE_PREFETCH_LOCK, L1D_CACHE_LOCK_FB_HIT, CACHE_LOCK_CYCLES.L1D_L2, CACHE_LOCK_CYCLES.L1D, IO_TRANSACTIONS, L11.CYCLES STALLED, LARGE ITLB.HIT, ITLB MISSES.ANY, ITLB MISSES.WALK COMPLET, ILD STALL.LCP, ILD STALL.LCP, ILD STALL.MRU, ILD STALL.RQ FULL, ILD STALL.REGEN, ILD STALL.RAY, BR INST EXEC.COND, BR INST EXEC.DIRECT, BR INST EXEC.INDIRECT NON, BR INST EXEC.NON CALLS, BR INST EXEC.RETURN NEA, BR_INST_EXEC.DIRECT_NEAR, BR_INST_EXEC.INDIRECT_NEA, BR_INST_EXEC.NON_CALLS, BR_INST_EXEC.TAKEN, BR_MISP_EXEC.COND, BR_MISP_EXEC.DIRECT, BR_MISP_EXEC.INDIRECT_NO, BR_MISP_EXEC.NON_CALLS, BR_MISP_EXEC.RETURN_NEA, BR MISP EXEC.DIRECT NEAR, BR MISP EXEC.INDIRECT NEA, BR MISP EXEC.INDIRECT NEA, BR MISP EXEC.INEAR CALLS, RR MISP EXEC.TAKEN, RESOURCE STALLS.ANY, RESOURCE STALLS.LOAD, RESOURCE STALLS.RS FULL, RS FU RESOURCE STALLS.FPCW, RESOURCE STALLS.MXCSR, RESOURCE STALLS.OTHER, MACRO INSTS.FUSIONS DECO, BACLEAR FORCE IQ, ITLB FLUSH, OFFCORE REQUESTS.L1D WR, UOPS EXECUTED.PORT0, UOPS EXECUTED.PORT1, UOPS_EXECUTED.PORT2_COR, UOPS_EXECUTED.PORT3_COR, UOPS_EXECUTED.PORT4_COR, UOPS_EXECUTED.PORT4_COR, UOPS_EXECUTED.PORT5, UOPS_EXECUTED.PORT015, UOPS_EXECUTED.PORT234, OFFCORE_REQUESTS_SQ_FUL, OFF_CORE_RESPONSE_0, SNOOP_RESPONSE.HIT, SNOOP RESPONSE.HITE, SNOOP RESPONSE.HITM, OFF CORE RESPONSE 1, INST RETIRED.ANY P, INST RETIRED.X87, INST RETIRED.MMX, UOPS RETIRED.ANY, UOPS RETIRED.RETIRE SLOTS, UOPS RETIRED.MACRO FUSE, MACHINE CLEARS.CYCLES, MACHINE_CLEARS.MEM_ORDE, MACHINE_CLEARS.SMC, BR_INST_RETIRED.ALL_BRAN, BR_INST_RETIRED.CONDITION, BR_INST_RETIRED.NEAR_CAL, BR_MISP_RETIRED.ALL_BRAN, BR_MISP_RETIRED.NEAR_CAL, SSEX_UOPS_RETIRED.PACKED, SSEX UOPS RETIRED.SCALAR, SSEX UOPS RETIRED.PACKED, SSEX UOPS RETIRED.SCALAR, SSEX UOPS RETIRED.VECTOR, ITLB MISS RETIRED, MEM LOAD RETIRED.11 HIT, MEM LOAD RETIRED.12 HIT, MEM LOAD RETIRED.13 UNS, MEM LOAD RETIRED.OTHER , MEM LOAD RETIRED.L3 MISS, MEM LOAD RETIRED.HIT LFB, MEM LOAD RETIRED.DTLB MI, FP MMX TRANS.TO FP, FP MMX TRANS.TO MMX, FP MMX TRANS.ANY, MACRO INSTS.DECODED, UOPS DECODED.MS, UOPS_DECODED.ESP_FOLDING, UOPS_DECODED.ESP_SYNC, RAT_STALLS.FLAGS, RAT_STALLS.REGISTERS, RAT_STALLS.ROB_READ_POR, RAT_STALLS.SCOREBOARD, RAT_STALLS.ANY, SEG_RENAME_STALLS, ES_REG_RENAMES, UOP_UNFUSION, BR INST DECODED, BPU MISSED CALL RET, BACLEAR.BAD TARGET, BPU CLEARS.EARLY, BPU CLEARS.LATE, L2 TRANSACTIONS.LOAD, L2 TRANSACTIONS.RFO, L2 TRANSACTIONS.FETCH, L2 TRANSACTIONS.PFEFETCH, L2 TRANSACTIONS 12_TRANSACTIONS.FILL, 12_TRANSACTIONS.WB, L2_TRANSACTIONS.ANY, 12_LINES_IN.S_STATE, L2_LINES_IN.E_STATE, L2_LINES_IN.ANY, L2_LINES_OUT.DEMAND_CLEA, L2_LINES_OUT.DEMAND_DIRT, L2_LINES_OUT.PREFETCH_CLE, L2 LINES OUT.PREFETCH DIR, L2 LINES OUT.ANY, SQ MISC.SPLIT LOCK, SQ FULL STALL CYCLES, FP ASSIST.ALL, FP ASSIST.OUTPUT, FP ASSIST.INPUT, SIMD INT 64.PACKED MPY, SIMD INT 64.PACKED SHIFT, SIMD INT 64.PACK, SIMD INT 64.UNPACK, SIMD INT 64.PACKED LOGICA, CPUID, SIMD INT 64.PACKED ARITH, SIMD INT 64.SHUFFLE MOVE, UNC GQ CYCLES FULL.READ , UNC GQ CYCLES FULL.WRITE, UNC GQ CYCLES FULL.PEER , UNC GQ CYCLES NOT EMPTY, UNC_GQ_CYCLES_NOT_EMPTY, UNC_GQ_CYCLES_NOT_EMPTY, UNC_GQ_ALLOC.READ_TRACK, UNC_GQ_ALLOC.RT_L3_MISS, UNC_GQ_ALLOC.RT_TO_L3_RE, UNC_GQ_ALLOC.RT_TO_RTID_, UNC_GQ_ALLOC.WT_TO_RTID_, UNC_GQ_ALLOC.WT.TO_RTID_, UNC_GQ_ALLOC.WT.TO_RTI UNC GQ ALLOC.PEER PROBE, UNC GQ DATA.FROM QPI, UNC GQ DATA.FROM QMC, UNC GQ DATA.FROM L3, UNC GQ DATA.FROM CORES , UNC GQ DATA.FROM CORES , UNC GQ DATA.FOOM CORES , UNC GQ DATA.FOOM CORES , UNC GQ DATA.FROM CORES , UNC GQ

UNC_GQ_DATA.TO_CORES, UNC_SNP_RESP_ UNC SNP RESP TO REMOTE, UNC SNP RES UNC L3 HITS.ANY, UNC L3 MISS.READ, UNC UNC_L3_LINES_OUT.M_STATE, UNC_L3_LINE UNC QHL REQUESTS.REMOTE, UNC QHL RE UNC_QHL_CYCLES_NOT_EMPT, UNC_QHL_CY UNC QHL CONFLICT CYCLES., UNC QHL CO UNC QMC NORMAL FULL.WRI, UNC QMC UNC_QMC_BUSY.READ.CH1, UNC_QMC_BUS' UNC QMC ISSOC OCCUPANCY., UNC QMC UNC_QMC_NORMAL_READS.A, UNC_QMC_H UNC QMC CRITICAL PRIORIT, UNC QMC W UNC_QHL_FRC_ACK_CNFLTS.L, UNC_QPI_TX_ UNC QPI TX STALLED SINGL, UNC QPI TX

BR MISP EXEC.COND:

Counts the number of mispredicted conditional near branch instructions executed, but not UNC_QMC_CRITICAL_PRIORIT, UNC_QMC_W UNC_QMC_CANCEL.CHO, UNC_QMC_CANCEL NECESSARILY retired.

_RESP_TO_LOCAL_H, UNC_SNP_RESP_TO_REMOTE, HITS.READ, UNC L3 HITS.WRITE, UNC L3 HITS.PROBE, NC L3 LINES IN.F STATE, UNC L3 LINES IN.ANY, UESTS.IOH_RE, UNC_QHL_REQUESTS.IOH_WR, L CYCLES FULL.LOCA, UNC QHL CYCLES NOT EMPT, _QHL_ADDRESS_CONFLIC, UNC_QHL_CONFLICT_CYCLES.I, MC NORMAL FULL.WRI, UNC QMC NORMAL FULL.WRI, UNC QMC ISOC FULL.WRITE.C, UNC QMC BUSY.READ.CHO, CUPANCY.CH1, UNC_QMC_OCCUPANCY.CH2, , UNC QMC NORMAL READS.C, INC_QMC_CRITICAL_PRIORIT, UNC_QMC_CRITICAL_PRIORIT, MC WRITES.PARTIAL.C, UNC QMC WRITES.PARTIAL.C, TE, UNC QMC PRIORITY UPDATE,

I_TX_STALLED_SINGL, UNC_QPI_TX_STALLED_SINGL, QPI TX STALLED MULTI, UNC QPI TX STALLED MULTI,

UNC_QP_TX_HEADER.BUSY.LI, UNC_QP_TX_HEADER.B UNC DRAM PAGE CLOSE.CH1, UNC DRAM PAGE CLOSE.CH2, UNC DRAM PAGE MISS.CH0, UNC DRAM PAGE MISS.CH1, UNC DRAM PAGE MISS.CH2, UNC DRAM READ CAS.CH1, UNC DRAM READ C UNC DRAM READ CAS.AUTO, UNC DRAM READ CAS.CH2, UNC DRAM READ CAS.AUTO, UNC DRAM_WRITE_CAS.CH2, UNC DRA UNC DRAM WRITE CAS.AUTO, UNC DRAM REFRESH.CHO

Hardware Performance Counters



Derived Metrics

- Clock cycles per Instructions (CPI)
 - → CPI indicates if the application is utilizing the CPU or not
 - → Take care: Doing "something" does not always mean doing "something useful".
- Floating Point Operations per second (FLOPS)
 - → How many arithmetic operations are done per second?
 - → Floating Point operations are normally really computing and for some algorithms the number of floating point operations needed can be determined.

Hardware Performance Counters



1 CPI rate (Clock cycles per instruction): In theory modern processors can finish 4 instructions in 1 cycle, so a CPI rate of 0.25 is possible. A value between 0.25 and 1 is often considered as good for HPC applications.

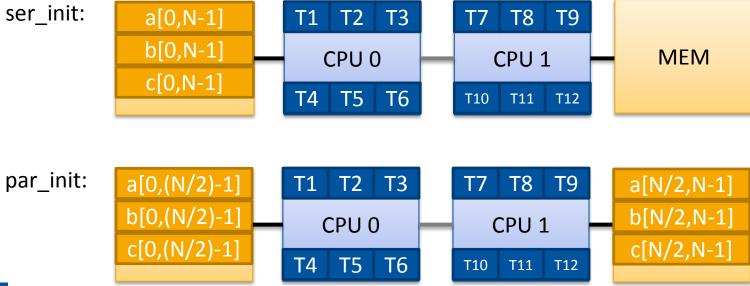
	Elapsed Time: 1.872s				
5355	Hardware Event Count:	125,574,000,000			
	CPU_CLK_UNHALTED.THREAD:	6.3462e+10			
	INST_RETIRED.ANY:	6.2112e+10			
1	CPI Rate:	1.022			
	The CPI may be too high. This could be caused instructions. Explore the other hardware-relate	이 사람이 가득하다 이 경우에 다른 이렇게 되었다면 하게 되었다면 하지만 하지만 하지만 되었다면 되었다. 그렇게 되었다면 하지만			
	Retire Stalls:	0.570s			
	A high number of retire stalls is detected. This issues. Use this metric to find where you have				
	LLC Miss:	0.013s			
	LLC Load Misses Serviced By Remote DRAM:	0.001s			
	Instruction Starvation:	0.098s			
	Branch Mispredict:	0.001s			
	Execution Stalls:	0.288s			
	Demontors and Destaurance Testa for Occutto				

Counters for Remote Traffic



- Stream example $(\vec{a} = \vec{b} + s * \vec{c})$ with and without parallel initialization.
 - → 2 socket sytem with Xeon X5675 processors, 12 OpenMP threads

	сору	scale	add	triad
ser_init	18.8 GB/s	18.5 GB/s	18.1 GB/s	18.2 GB/s
par_init	41.3 GB/s	39.3 GB/s	40.3 GB/s	40.4 GB/s



Counters for Remote Traffic

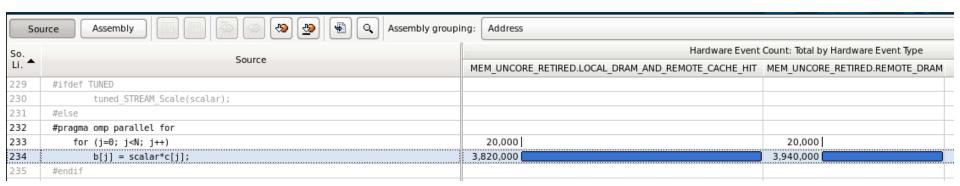


- Hardware counters can measure local and remote memory accesses.
 - → MEM_UNCORE_RETIRED.LOCAL_DRAM_AND_REMOTE_CACHE_HIT accesses to local memory
 - → MEM_UNCORE_RETIRED.REMOTE_DRAM accesses to remote memory
- Absolute values are hard to interpret, but the ratio between both is useful.

Counters for Remote Traffic



Detecting bad memory accesses for the stream benchmark.



Ratio of remote memory accesses:

	сору	scale	add	triad
ser_init	52%	50%	50%	51%
par_init	0.5%	1.7%	0.6%	0.2%

Percentage of remote accesses for ser init and par init stream benchmark.



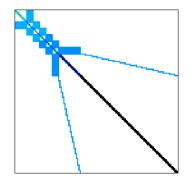
CG Solver

Case Study: CG



Sparse Linear Algebra

- → Sparse Linear Equation Systems occur in many scientific disciplines.
- → Sparse matrix-vector multiplications (SpMxV) are the dominant part in many iterative solvers (like the CG) for such systems.
- → number of non-zeros << n*n



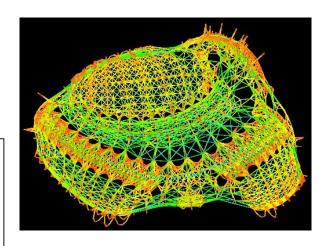
Beijing Botanical Garden

Oben Rechts: Orginal Gebäude

Unten Rechts: Modell Unten Links: Matrix

(Quelle: Beijing Botanical Garden and University of Florida, Sparse Matrix Collection)









Hotspot analysis of the serial code:

Call Stack	CPU Time: Total by Utilization		
	📗 Idle 📕 Poor 📙 Ok 📗 Ideal 📙 Over		
▽¹i cg	46.7%		
Þ	40.8% 1.		
Þ ⊴ xpay	1.4% 2.		
⊳ы axpy	1.4% 2.		
	1.2% 3.		
Þ ⊴ axpy	1.1% 2.		
	0.6% 3.		

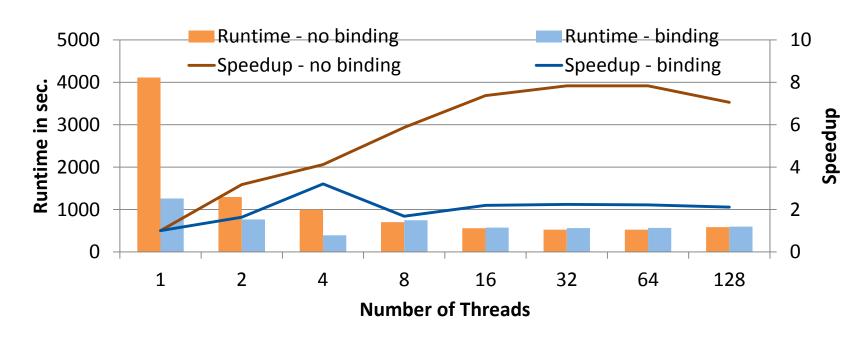
Hotspots are:

- 1. matrix-vector multiplication
- scaled vector additions
- 3. dot product



Tuning:

- parallelize all hotspots with a parallel for construct
- use a reduction for the dot-product
- activate thread binding







Hotspot analysis of naive parallel version:

Event Name		
MEM_UNCORE_RETIRED.LOCAL_DRAM_AND_REMOTE_CACHE_HIT		
MEM_UNCORE_RETIRED.REMOTE_DRAM		

A lot of remote accesses occur in nearly all places.

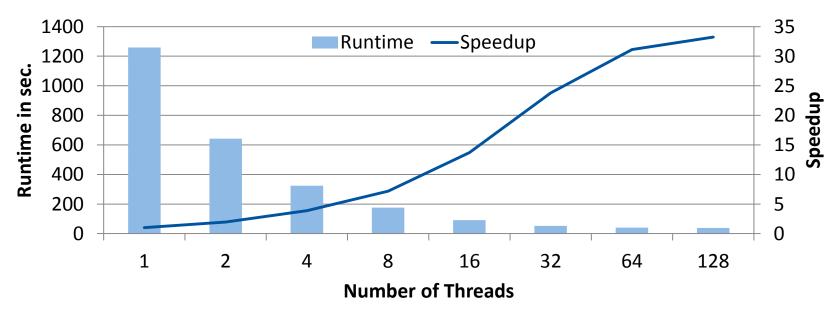
	MEM_UNCORE_RETIRED.LOCAL	MEM_UNCORE_RETIRED.REMOTE
void matvec(const int n, const int		
int i,j;		
<pre>#pragma omp parallel for private(j)</pre>	20,000	0
for(i=0; i <n; i++){<="" td=""><td>0</td><td>0</td></n;>	0	0
y[i]=0;	0	0
for(j=ptr[i]; j <ptr[i+1]; j<="" td=""><td>6,740,000</td><td>3,720,000</td></ptr[i+1];>	6,740,000	3,720,000
y[i]+=value[j]*x[index[17,580,000	6,680,000
}		
}		





Tuning:

- Initialize the data in parallel
- Add parallel for constructs to all initialization loops



Scalability improved a lot by this tuning on the large machine.



Analyzing load imbalance in the concurrency view:

So Line	Source	CPU Time: Total by Didle Poor Ok III	
49	void matvec(const int n, const int nnz,		
50	int i,j;		
51	<pre>#pragma omp parallel for private(j)</pre>	22.462s	10.612s
52	for(i=0; i <n; i++){<="" td=""><td>0.050s</td><td>0s</td></n;>	0.050s	0s
53	y[i]=0;	0.060s	0s
54	for(j=ptr[i]; j <ptr[i+1]; j++){<="" td=""><td>1.741s</td><td>0s</td></ptr[i+1];>	1.741s	0s
55	y[i]+=value[j]*x[index[j]];	9.998s	0s

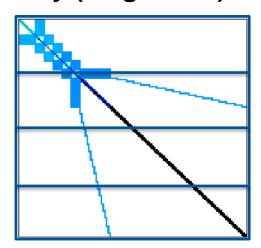
- 10 seconds out of ~35 seconds are overhead time
- other parallel regions which are called the same amount of time only produce 1 second of overhead

Case Study: CG

$$A = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 2 & 2 & 0 & 0 \\ 0 & 0 & 3 & 0 \\ 4 & 0 & 4 & 4 \end{pmatrix}$$

- Format: compressed row storage
- store all values and columns in arrays (length nnz)
- store beginning of a new row in a third array (length n+1)

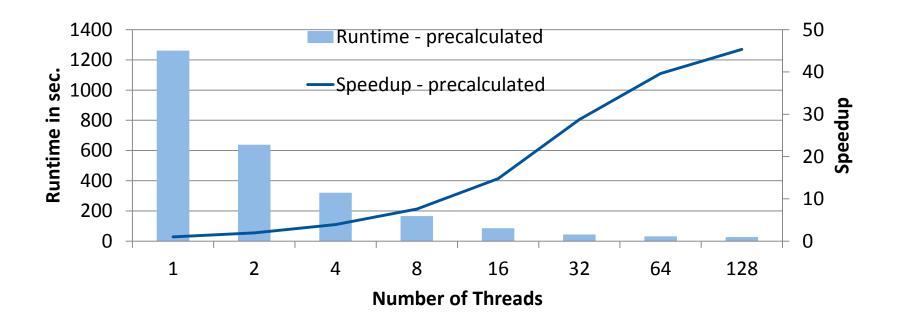
row:	1	1	2	7	7		
index:	0	0	1	2	0	2	3
value:	1	2	2	3	4	4	4





Tuning:

→ pre-calculate a schedule for the matrix-vector multiplication, so that the non-zeros are distributed evenly instead of the rows





The Roofline Model

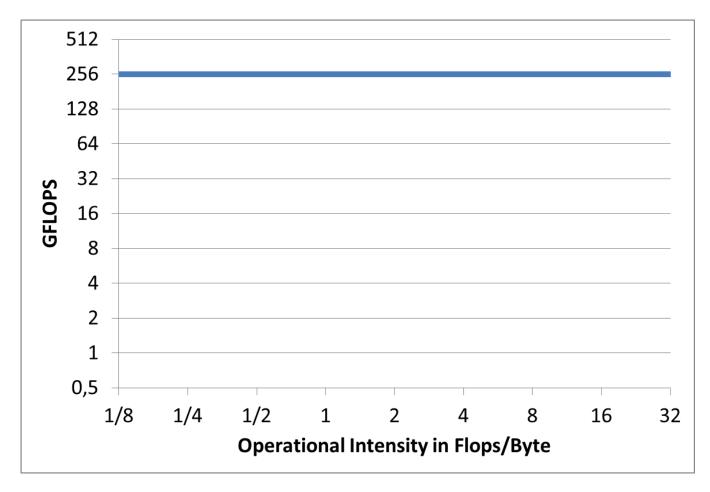
When to stop tuning?



- Depends on many different factors:
 - → How often is the code program used?
 - → What are the runtime requirements?
 - → Which performance can I expect?
- Investigating kernels may help to understand larger applications.

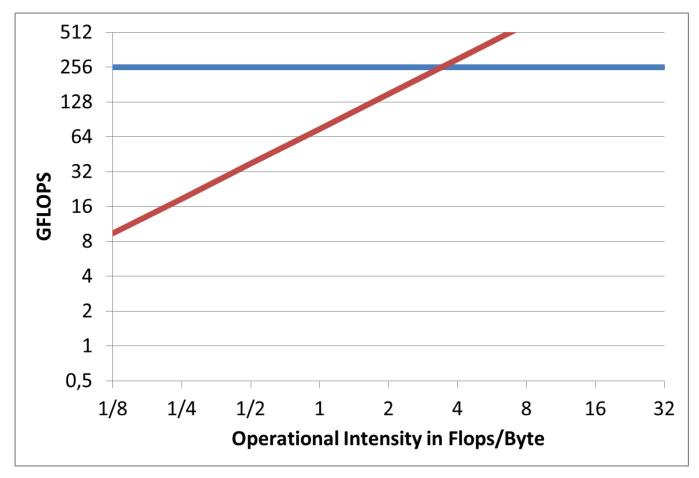


Peak performance of a 4 socket Nehalem Server is 256 GFLOPS.



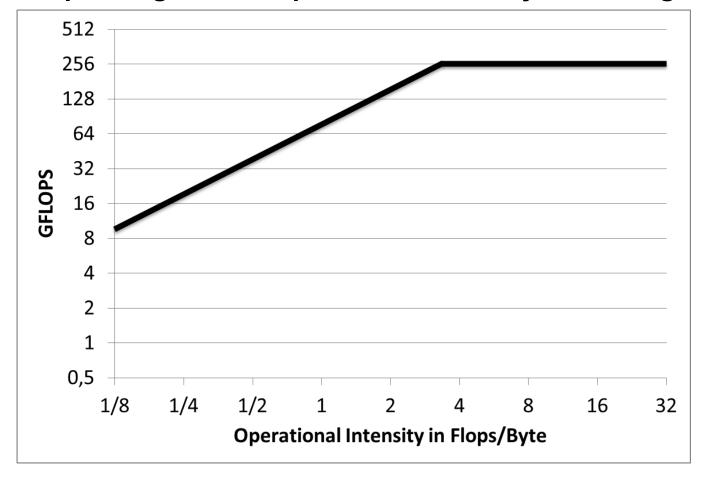


Memory bandwidth measured with Stream benchmark is about 75 GB/s.





The "Roofline" describes the peak performance the system can reach depending on the "operational intensity" of the algorithm.



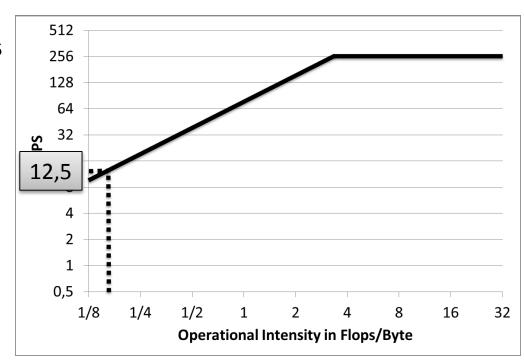




Example: Sparse Matrix Vector Multiplication y=Ax

Given:

- x and y are in the cache
- A is too large for the cache
- measured performance was12 GFLOPS
- 1 ADD and 1 MULT per element
- load of value (double) and index (int) per element
- -> 2 Flops / 12 Byte = 1/6 Flops/Byte





Task-Analysis with Performance Tools

Intel VTune Amplifier XE



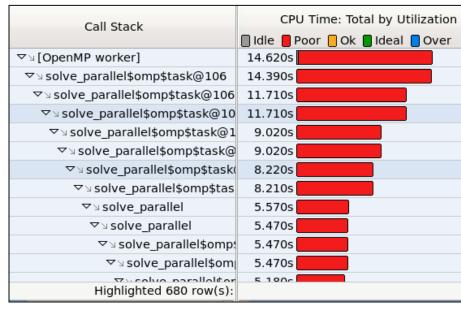
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Top Hotspots 🕒	
This section lists the most active overall application performance.	
Function	CPU Time
solve_parallel\$omp\$task@106	9.090s
CSudokuBoard::checkHorizontal	5.730s
CSudokuBoard::check	1.910s
CSudokuBoard::checkBox	1.620s
CSudokuBoard::CSudokuBoard	1.370s

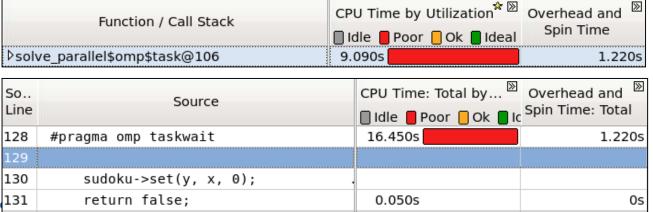
The Task-region is our main Hotspot.

Overhead and Spin time is found for the task region ...

... and even for individual source code lines.



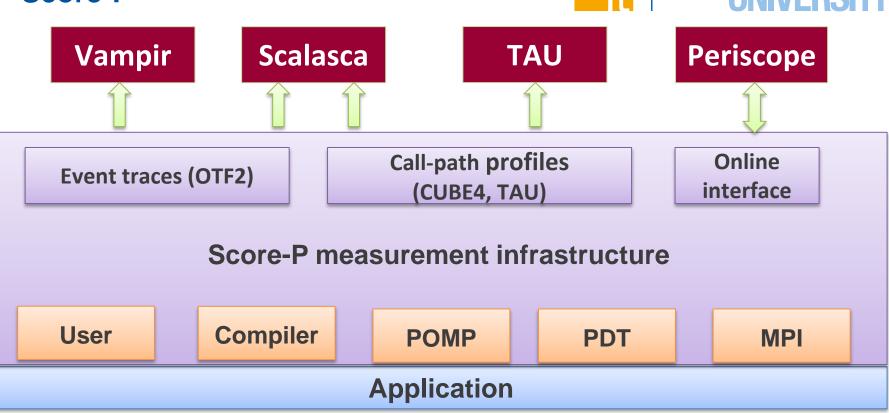
There is a long recursive call stack and the amount of work per level declines.



Performance Measurements with Score-P





















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Score-P Usage



Compiling and Linking:

- → gcc -> scorep gcc
- → g++ -> scorep g++
- → gfortran -> scorep gfortran

2. Run your application:

- → SCOREP_ENABLE_PROFILING=true/false to enable/disable profiling
- → SCOREP_ENABLE_TRACING=true/false to enable/disable tracing

Profiling	Tracing
Accumulated events are recorded. e.g. total time spend in foo()	Every event is recorded with a timestamp. e.g. start and end time for every call of foo()
less accurate	all information stored
reduced storage requirements (44 KB for Sudoku)	might need a lot of storage (1.2 GB for Sudoku)
Visualized e.g. in Cube Browser	Visualized e.g. in Vampir

Score-P (Profiling)/ Cube

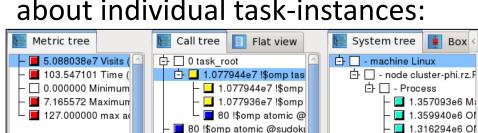


1.289513e6 Of

1.318732e6 Of

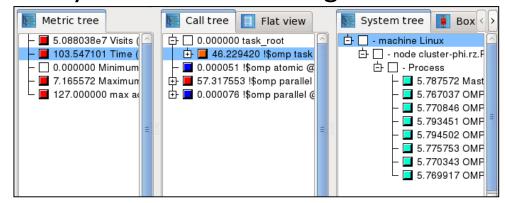
■ 1.384539e6 OI ■ 1.384849e6 OI ■ 1.368480e6 OI

Profiling also gives more details about individual task-instances:



1.854197e7 !\$omp paralle

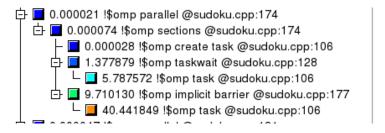
Every thread is executing ~1.3m tasks...



- ... in ~5.7 seconds.
- => average duration of a task is $^4.4 \mu s$

Profiled Code with:

- OpenMP constructs enabled
- Function instrumentation disabled



The Task-region is identified as hotspot.

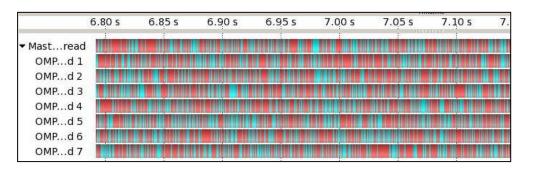
No mapping to source code possible.

Score-P (Tracing)/ Vampir

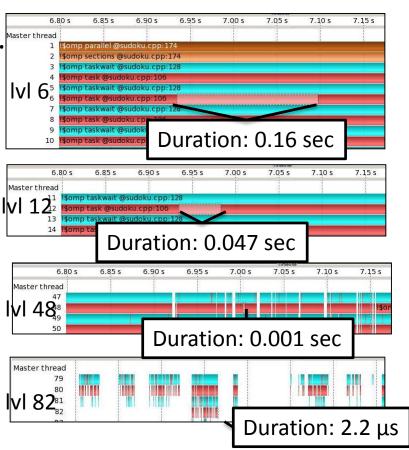




Tracing gives a detailed timeline view...



... but also more detailed information on the call stack and the task durations can be shown.



Tasks get much smaller down the call stack.



Questions?