**Adaptive Write-Update and Write-Invalidate Cache Coherence Protocols**

**for Producer-Consumer Sharing**

**Group Members:**

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**Project Web Page**

<https://lihao98722.github.io/15740>

**Project Description**

Briefly describe the goal of your project (i.e., what research question(s) are you trying to answer and what metrics will be used to evaluate its success?). Include a 100% goal (if all goes as expected), a 75% goal (what you can still accomplish of things go more slowly than expected), and a 125% goal (what you might accomplish if things go faster than expected).

**Logistics**

Please address each of the following issues regarding how you will carry out your project:

Plan of Attack and Schedule: How will you go about completing your project? Please include a week-by-week schedule of exactly who in your group will be doing what. We will not strictly hold you to this schedule (other than meeting your milestone, as described below), but it is important that you have a concrete and realistic plan. Identify what you expect to be the critical path in your schedule. Indicate how the work will be divided among your group members.

**Milestone**

Indicate what your group plans to accomplish by Tuesday, April 11th (i.e., after four weeks). On that date, you will submit a brief report describing your progress up to that point. Your ability to set a reasonable milestone and to meet this goal will be factored into your final project grade.

**Literature Search**

[1] Cheng, Liqun, John B. Carter, and Donglai Dai. "An adaptive cache coherence protocol optimized for producer-consumer sharing." *High Performance Computer Architecture, 2007. HPCA 2007. IEEE 13th International Symposium on*. IEEE, 2007.

[2] Qureshi, Moinuddin K., et al. "Adaptive insertion policies for high performance caching." *ACM SIGARCH Computer Architecture News*. Vol. 35. No. 2. ACM, 2007.

[3] Danny. "The Disruptor - Lock-free Publishing." Codeaholics.org. http://blog.codeaholics.org/2011/the-disruptor-lock-free-publishing/, 28 June 2011. Web. 10 Mar. 2017.

**Resources Needed**

* Pin: <https://software.intel.com/en-us/articles/pin-a-dynamic-binary-instrumentation-tool>
* Murphi: <http://seclab.stanford.edu/pcl/mc/mc.html>
* Stack trace: implement a stack trace tool which dynamically traces the sequences of multithread calls.

**Getting Started**

We have read multiple papers and articles on the joint research field of cache coherence and producer-consumer sharing pattern in multicore systems, and had two meetings with Prof. Beckmann discussing about the feasibility of research approach. We now have a clear idea of the current direction we should dig into: dynamically adapting write-update and write-invalidate cache coherence protocols according to sharing patterns. However, we don’t have a very good estimation of the project complexity and it is possible that the project scheme may be adjusted in the future due to unexpected difficulty. We will get started by researching on the sequential consistency criterions of alternating two protocols.