Assigment 3

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Question 1

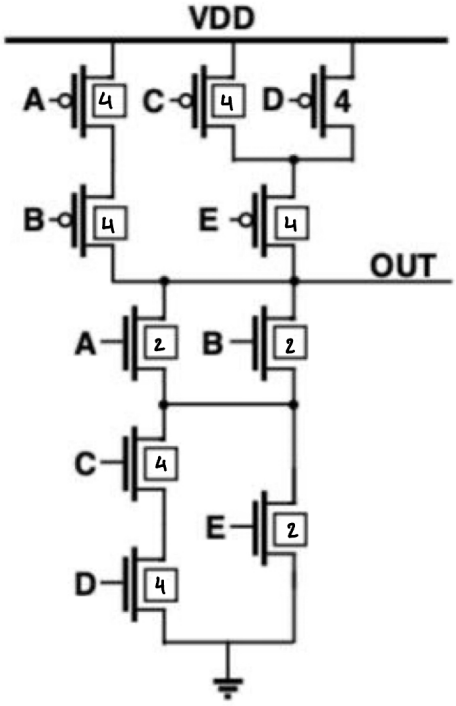
Part a

Based on the lecture notes, the boolean expression can be calculated to be the following:

$$O\bar{U}T = (A + B) \cdot (C \cdot D + E) \tag{1}$$

Part b

The appropriate transistor sizing is the following:



Part c

As discussed in the lecture, the output is low and R_{out} is at its lowest when all the inputs are high That is:

$$A = 1, B = 1, C = 1, D = 1, E = 1, \tag{2}$$

This resistance value is equal to:

$$R_{out} = \frac{\frac{12k}{2}}{\frac{12k}{2}} + \frac{\frac{12k}{4} + \frac{12k}{4}}{\frac{12k}{2}} = 6k\Omega \tag{3}$$

Part d

Similarly, when the output is high, R_{out} is lowest when all the inputs are low. That is:

$$A = 0, B = 0, C = 0, D = 0, E = 0 \tag{4}$$

And the output resistance can be caculated to be:

$$R_{out} = \frac{\frac{12k}{2} + \frac{12k}{2}}{\frac{\frac{12k}{2}}{\frac{12k}{2}} + \frac{12k}{2}} = 5.14K\Omega \tag{5}$$

Part e

As seen in the lecture, this can be calcuated in the following manner

$$t_{pLH,best} = 0.69 * 5.14k * 100f = 355ps \tag{6}$$

$$t_{pHL,best} = 0.69 * 6k * 100f = 414ps \tag{7}$$

Question 2

Part a

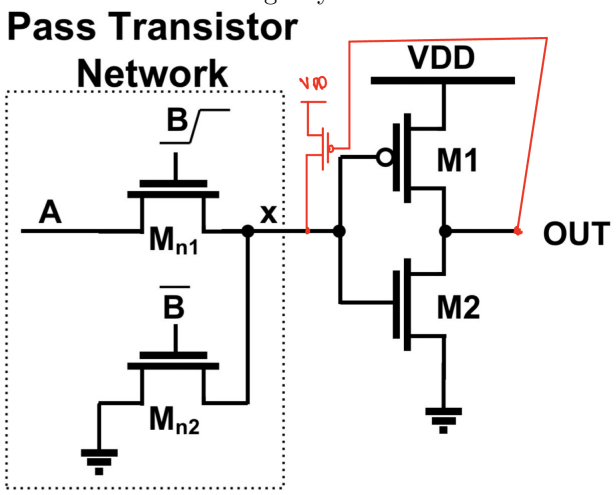
This circuit performs the function of a NAND gate. The PASS transistor network performs AND then an inverter by M1 and M2.

Part b

When A=B=1, the pass transistor would pass up to VDD - $V_{th(NMOS)}$ to the X^{nth} node. This results in M1 not completely turning off which leads to static power dissipation as both M1 and M2 are on.

Part c

This can be done in the following way:



One should note that the transistor should be small enough to pull the node X to GND when B is 0

Part d

This can be done in the following way: