Assigment 4

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Question 1

Based on the figure, we can observe that the worst case delay occurs when the carry is generated from then LSB, that is $C_{o,0}$. This ends up rippeling all the way up until when $C_{o,k}$ is generated.

Assume that $C_{i,0}$ is 0

The initial value of S_{N-1} would be 0 and A_0 and B_0 must be 1. This would mean that all other stages are in propogate mode and at any point either A_i or B_i would be 1. Setting A_{N-1} and B_{N-1} to 0 can yield a high sum bit.

Assume that $C_{i,0}$ is 1

This would mean that either A_0 and B_0 would need to be 1.

Question 2

Part a

We know that the delay of an N-bit adder with M-bits per stage is:

$$t_{add} = t_{setup} + M * t_{carry} + \frac{N}{M} * t_{mux} + t_{sum} \tag{1}$$

This means that:

$$t_{add} = 2 + M + \frac{16}{M} + 2 = 4 + M + \frac{16}{M} \tag{2}$$

We know that the delay for an N-bit ripple carry adder is:

$$t_{add,ripple-carry} = (N-1)t_{carry} + t_{sum} = 17 \tag{3}$$

Based on equations (2) and (3) we can claim that if M $\geq$ 2, the carry select adder has less propagation delay than the ripple-carry adder.

Part b

Based on the equations (1) and (3) we can claim:

$$T_{add,select-carry} = 2 + 4 * 1 + \frac{N}{4} * 1 + 2 = \frac{N}{4} + 8 \tag{4}$$

$$T_{add,ripple-carry} = (N - 1) * 1 + 2 = N + 1 \tag{5}$$

We assumed that $T_{add,select-carry} < T_{add,ripple-carry}$, that is

$$\frac{N}{4} + 8 \leq N + 1 \tag{6}$$

$$N + 32 \leq 4N + 4 \tag{7}$$

$$28 \leq 3N \tag{8}$$

That is N $\geq$ 9.33. Hence if N $\geq$ 10 then the carry select adder has lesser propagation delay.